Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date: 18-03-2023

Name: NAGAVENI L G	SRN: PES2UG21CS315	Section F

Week#____8_____ Number:_____1___

Consider a direct mapped cache of size 16 bytes with block size 4 bytes. The size of main memory is 256 bytes.

a) Find Number of bits in tag, index and offset.

b) The processor generates requests as following requests.

1,4,8,5,14,11,13,38,9,B,4,2B,5,6,9,11.

Find hit rate and miss rate.

i)Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Instruction Breakdown

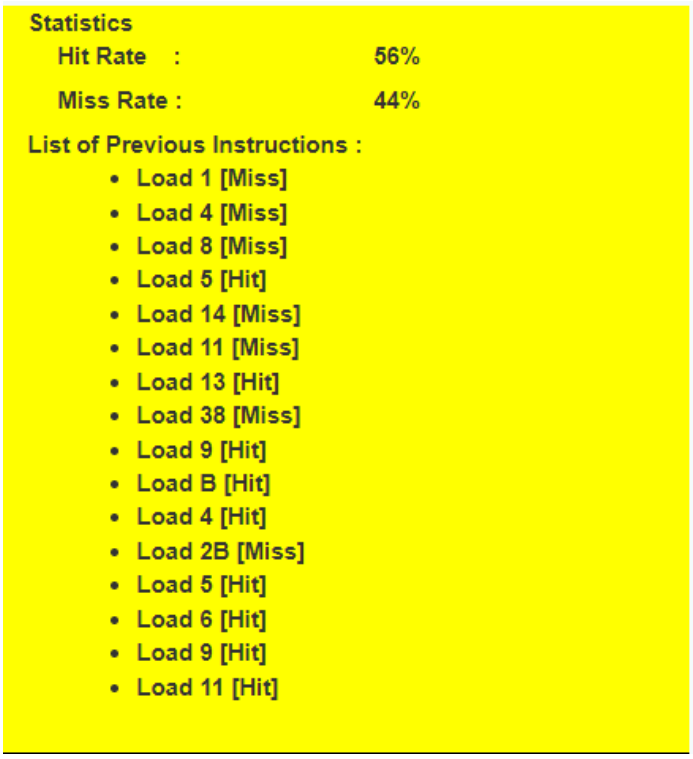
TAG	INDEX	OFFSET
3 bit	12 bit	2 bit

ii) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	000	BLOCK 0 WORD 0 - 3	0
1	1	000	BLOCK 1 WORD 0 - 3	0
2	1	000	BLOCK 2 WORD 0 - 3	0
3	0	-	0	0
4	1	000	BLOCK 4 WORD 0 - 3	0
5	1	000	BLOCK 5 WORD 0 - 3	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	1	000	BLOCK A WORD 0 - 3	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	1	000	BLOCK E WORD 0 - 3	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0

iii) Screenshot showing hit and miss rates



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4th Semester, Academic Year 2020-21

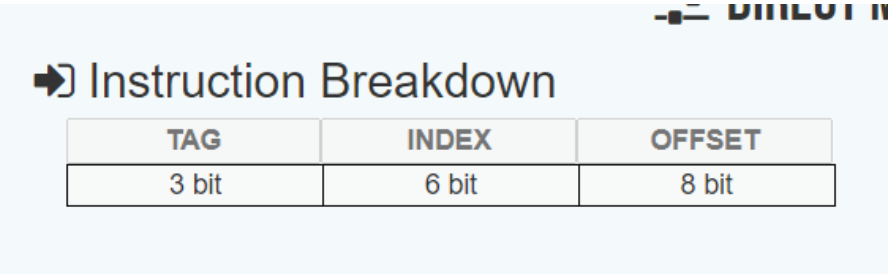
Date:

Name: NAGAVENI L G	SRN: PES2UG21CS315	Section F

Week#____8_____ Number:_____2___

Consider a direct mapped cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

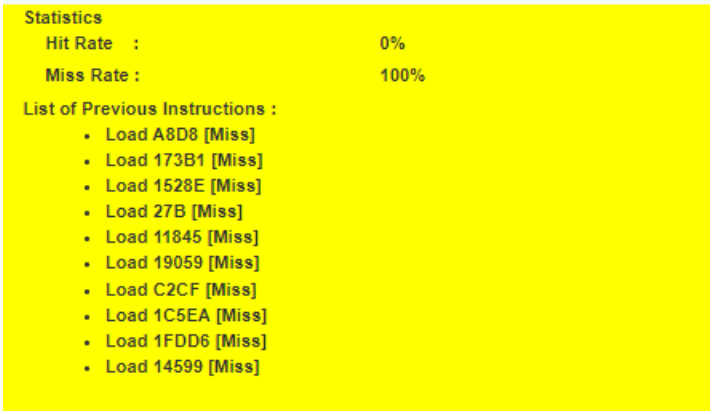


b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	1	011	BLOCK C2 WORD 0 - 255	0
3	0	-	0	0
4	0	-	0	0
5	1	101	BLOCK 145 WORD 0 - 255	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	1	110	BLOCK 190 WORD 0 - 255	0
17	0	-	0	0
18	1	101	BLOCK 152 WORD 0 - 255	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	1	100	BLOCK 118 WORD 0 - 255	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0
32	0	-	0	0
33	0	-	0	0
34	0	-	0	0
35	0	-	0	0
36	0	-	0	0
37	0	-	0	0
38	0	-	0	0
39	0	-	0	0
40	1	010	BLOCK A8 WORD 0 - 255	0
41	0	-	0	0
42	0	-	0	0
43	0	-	0	0
44	0	-	0	0
45	0	-	0	0
46	0	-	0	0
47	0	-	0	0
48	0	-	0	0
49	0	-	0	0
50	0	-	0	0
51	1	101	BLOCK 173 WORD 0 - 255	0
52	0	-	0	0
53	0	-	0	0
54	0	-	0	0
55	0	-	0	0
56	0	-	0	0
57	0	-	0	0
58	0	-	0	0
59	0	-	0	0
60	0	-	0	0
61	1	111	BLOCK 1FD WORD 0 - 255	0
62	0	-	0	0
63	0	-	0	0

c) Screenshot showing hit and miss rates



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4th Semester, Academic Year 2020-21

Date:

Name: NAGAVENI L G	SRN: PES2UG21CS315	Section F

Week#____8_____ Number:_____3___

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte.
a) Calculate the number of bits in each of the Tag, Block, and Word fields of the memory address.
(b) When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176
All the above addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, indicate whether the cache access will result in a hit or a miss.

a)Cache Address Table showing the splitup of the address fields for the requests generated by the processor

Instruction Breakdown

TAG	INDEX	OFFSET
5 bit	5 bit	6 bit

c)Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	1	00000	BLOCK 4 WORD 0 - 63	0
5	1	00100	BLOCK 85 WORD 0 - 63	0
6	1	00100	BLOCK 86 WORD 0 - 63	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics

Hit Rate : 33%

Miss Rate : 67%

List of Previous Instructions :

- Load 128 [Miss]
- Load 144 [Miss]
- Load 2176 [Miss]
- Load 2180 [Miss]
- Load 128 [Hit]
- Load 2176 [Hit]

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

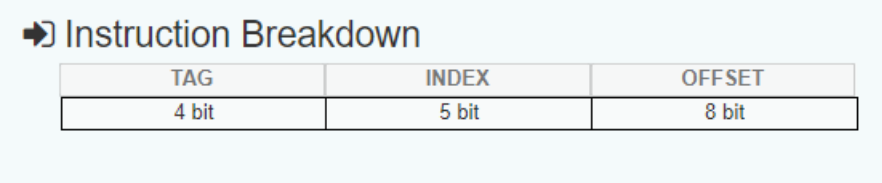
Date:

Name: NAGAVENI L G	SRN: PES2UG21CS315	Section F

Week#____8_____ Number:____4___

Consider a 2-way set associative cache of size 16 KB with block size 256 bytes. The size of main memory is 128 KB. Find Number of bits in tag. Randomly generate 10 addresses and find hit rate and miss rate.

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor



b) Screenshot showing the Cache Table

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	1	f	B. F1 W. 0 - 255	0
2	1	a	B. A2 W. 0 - 255	0
3	1	5	B. 53 W. 0 - 255	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	1	1	B. 17 W. 0 - 255	0
8	1	b	B. B8 W. 0 - 255	0
9	1	9	B. 99 W. 0 - 255	0
10	1	a	B. AA W. 0 - 255	0
11	1	3	B. 3B W. 0 - 255	0
12	1	c	B. CC W. 0 - 255	0
13	0	-	0	0
14	1	8	B. 8E W. 0 - 255	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	0	-	0	0
2	0	-	0	0
3	0	-	0	0
4	0	-	0	0
5	0	-	0	0
6	0	-	0	0
7	0	-	0	0
8	0	-	0	0
9	0	-	0	0
10	0	-	0	0
11	0	-	0	0
12	0	-	0	0
13	0	-	0	0
14	0	-	0	0
15	0	-	0	0
16	0	-	0	0
17	0	-	0	0
18	0	-	0	0
19	0	-	0	0
20	0	-	0	0
21	0	-	0	0
22	0	-	0	0
23	0	-	0	0
24	0	-	0	0
25	0	-	0	0
26	0	-	0	0
27	0	-	0	0
28	0	-	0	0
29	0	-	0	0
30	0	-	0	0
31	0	-	0	0

c) Screenshot showing hit and miss rates

Statistics

Hit Rate : 0%

Miss Rate : 100%

List of Previous Instructions :

- Load 144FF [Miss]
- Load 198AA [Miss]
- Load 13271 [Miss]
- Load A7E4 [Miss]
- Load 11C18 [Miss]
- Load 1E2CB [Miss]
- Load 7792 [Miss]
- Load 2F41 [Miss]
- Load 1547D [Miss]
- Load 171DF [Miss]

Microprocessor and Computer Architecture Laboratory

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4th Semester, Academic Year 2020-21

Date:

Name: NAGAVENI L G	SRN: PES2UG21CS315	Section F

Week#____8_____ Number:____5___

Consider a main memory having 64 byte capacity and cache memory of 8 bytes initially empty .The following addresses are generated by the CPU. All values in hexadecimal. Clearly label data that is replaced in cache lines

Show the cache memory table and filled data in the cache lines of block size 1 byte. LRU Policy is used.

The cache is mapped as

a) Direct Mapped
b) Two way set Associative
c) Four Way Set associative
d) Fully Associative

a) Cache Address Table showing the splitup of the address fields for the requests generated by the processor

DIRECT MAPPED

Instruction Breakdown

TAG	INDEX	OFFSET
3 bit	3 bit	0 bit

2-way SA

Instruction Breakdown

TAG	INDEX	OFFSET
4 bit	2 bit	0 bit

4-way SA

Instruction Breakdown

TAG	INDEX	OFFSET
5 bit	1 bit	0 bit

Fully associative

Instruction Breakdown

BLOCK	OFFSET
6 bit	0 bit

b) Screenshot showing the Cache Table

Direct mapped

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	0	-	0	0
1	1	000	BLOCK 1 WORD 0 - 0	0
2	1	110	BLOCK 32 WORD 0 - 0	0
3	0	-	0	0
4	1	000	BLOCK 4 WORD 0 - 0	0
5	1	100	BLOCK 25 WORD 0 - 0	0
6	1	000	BLOCK 6 WORD 0 - 0	0
7	0	-	0	0

2-way SA

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	7	B. 1C W. 0 - 0	0
1	1	d	BLOCK 35 WORD 0 - 0	0
2	1	3	B. E W. 0 - 0	0
3	1	3	B. F W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	8	BLOCK 20 WORD 0 - 0	0
1	1	9	BLOCK 25 WORD 0 - 0	0
2	1	b	BLOCK 2E WORD 0 - 0	0
3	1	c	BLOCK 33 WORD 0 - 0	0

4-way SA

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1d	B. 3A W. 0 - 0	0
1	1	7	B. F W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	d	B. 1A W. 0 - 0	0
1	1	1d	B. 3B W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	1f	B. 3E W. 0 - 0	0
1	1	19	B. 33 W. 0 - 0	0

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	5	B. A W. 0 - 0	0
1	0	-	0	0

Fully associative

Cache Table

Index	Valid	Tag	Data (Hex)	Dirty Bit
0	1	011111	BLOCK 1F WORD 0 - 0	0
1	1	101111	BLOCK 2F WORD 0 - 0	0
2	1	100111	BLOCK 27 WORD 0 - 0	0
3	1	101010	BLOCK 2A WORD 0 - 0	0
4	1	000001	BLOCK 1 WORD 0 - 0	0
5	1	110100	BLOCK 34 WORD 0 - 0	0
6	1	111100	BLOCK 3C WORD 0 - 0	0
7	1	000101	BLOCK 5 WORD 0 - 0	0

c) Screenshot showing hit and miss rates

direct mapped

Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load 12 [Miss]
- Load 35 [Miss]
- Load 12 [Hit]
- Load 1A [Miss]
- Load 4 [Miss]
- Load 6 [Miss]
- Load 21 [Miss]
- Load 32 [Miss]
- Load 1 [Miss]
- Load 25 [Miss]

2-way SA

Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load 11 [Miss]
- Load E [Miss]
- Load 1C [Miss]
- Load F [Miss]
- Load 20 [Miss]
- Load 33 [Miss]
- Load 11 [Hit]
- Load 25 [Miss]
- Load 2E [Miss]
- Load 35 [Miss]

4-way SA

Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load 22 [Miss]
- Load F [Miss]
- Load 30 [Miss]
- Load 3E [Miss]
- Load A [Miss]
- Load 3B [Miss]
- Load 3A [Miss]
- Load 33 [Miss]
- Load 1A [Miss]
- Load F [Hit]

Fully associative

Statistics

Hit Rate : 10%

Miss Rate : 90%

List of Previous Instructions :

- Load 17 [Miss]
- Load 2F [Miss]
- Load 27 [Miss]
- Load 2A [Miss]
- Load 1 [Miss]
- Load 34 [Miss]
- Load 3C [Miss]
- Load 5 [Miss]
- Load 1F [Miss]
- Load 2A [Hit]

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- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:
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Date: 18-03-2023