# Microprocessor and Computer Architecture

## UE21CS251B

## 4th Semester, Academic Year 2022-23

Date: 20/01/2023

| | | |
|---|---|---|
| Name: Nagaveni L G | SRN: PES2UG21CS315 | Section: F |

Week#____1_______ Program Number:____1___

Title of the Program

**Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0**

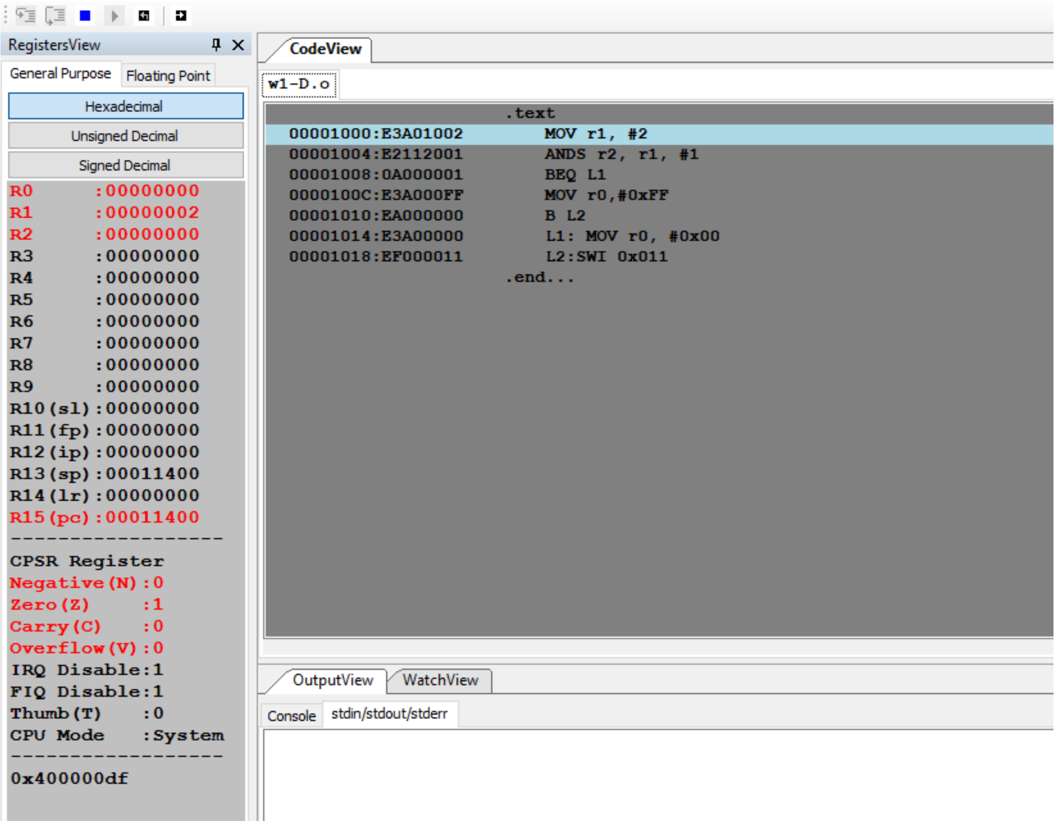
## I. ARM Assembly Code

```
.text
    MOV r1,  #3
    ANDS r2, r1, #1
    BEQ L1
    MOV r0,#0xFF
    B L2
    L1: MOV r0, #0x00
    L2:SWI 0x011
.end
```

## II. Output Screen Shot (Two)

The output should be verified for both even and odd numbers.

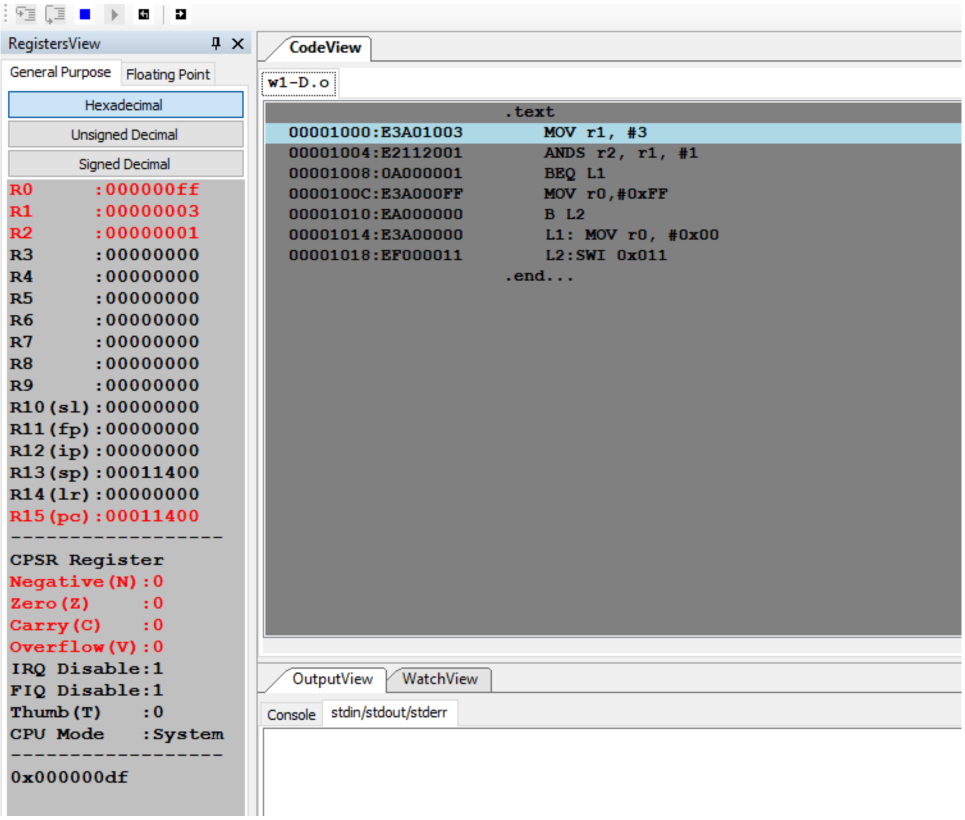
Even:



```
R0        :00000000
R1        :00000002
R2        :00000000
R3        :00000000
R4        :00000000
R5        :00000000
R6        :00000000
R7        :00000000
R8        :00000000
R9        :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00011400
R14(lr):00000000
R15(pc):00011400
------------------
CPSR Register
Negative(N):0
Zero(Z)     :1
Carry(C)    :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)    :0
CPU Mode    :System
------------------
0x400000df
```

```
                       .text
  00001000:E3A01002        MOV r1, #2
  00001004:E2112001        ANDS r2, r1, #1
  00001008:0A000001        BEQ L1
  0000100C:E3A000FF        MOV r0,#0xFF
  00001010:EA000000        B L2
  00001014:E3A00000        L1: MOV r0, #0x00
  00001018:EF000011        L2:SWI 0x011
                       .end...
```

Odd:



```
R0       :000000ff
R1       :00000003
R2       :00000001
R3       :00000000
R4       :00000000
R5       :00000000
R6       :00000000
R7       :00000000
R8       :00000000
R9       :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00011400
R14(lr):00000000
R15(pc):00011400
------------------
CPSR Register
Negative(N):0
Zero(Z)     :0
Carry(C)    :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)    :0
CPU Mode    :System
------------------
0x000000df
```

```
                    .text
00001000:E3A01003       MOV r1, #3
00001004:E2112001       ANDS r2, r1, #1
00001008:0A000001       BEQ L1
0000100C:E3A000FF       MOV r0,#0xFF
00001010:EA000000       B L2
00001014:E3A00000       L1: MOV r0, #0x00
00001018:EF000011       L2:SWI 0x011
                    .end...
```

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Week#____1_______        Program Number:_____2___

Title of the Program

**Write an ALP to compare the value of R0 and R1, add if R0 = R1, else subtract**

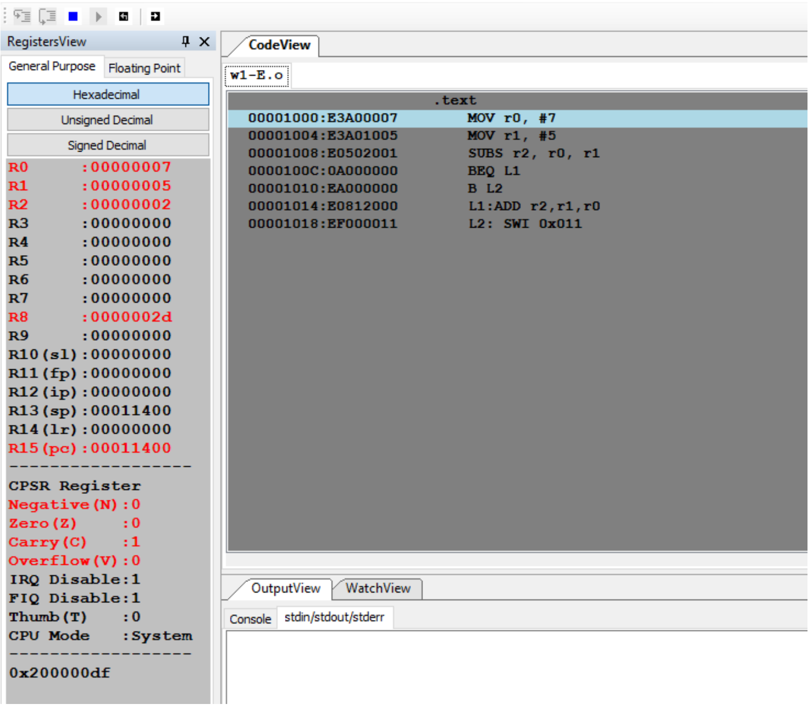
## I.ARM Assembly Code

```
.text
    MOV r0, #5
    MOV r1,  #5
    SUBS r2, r0, r1
    BEQ L1
    B L2
    L1:ADD r2,r1,r0
    L2: SWI 0x011
```

## II. Output Screen Shot (Two)

The output should be verified for both equal and nor equal values

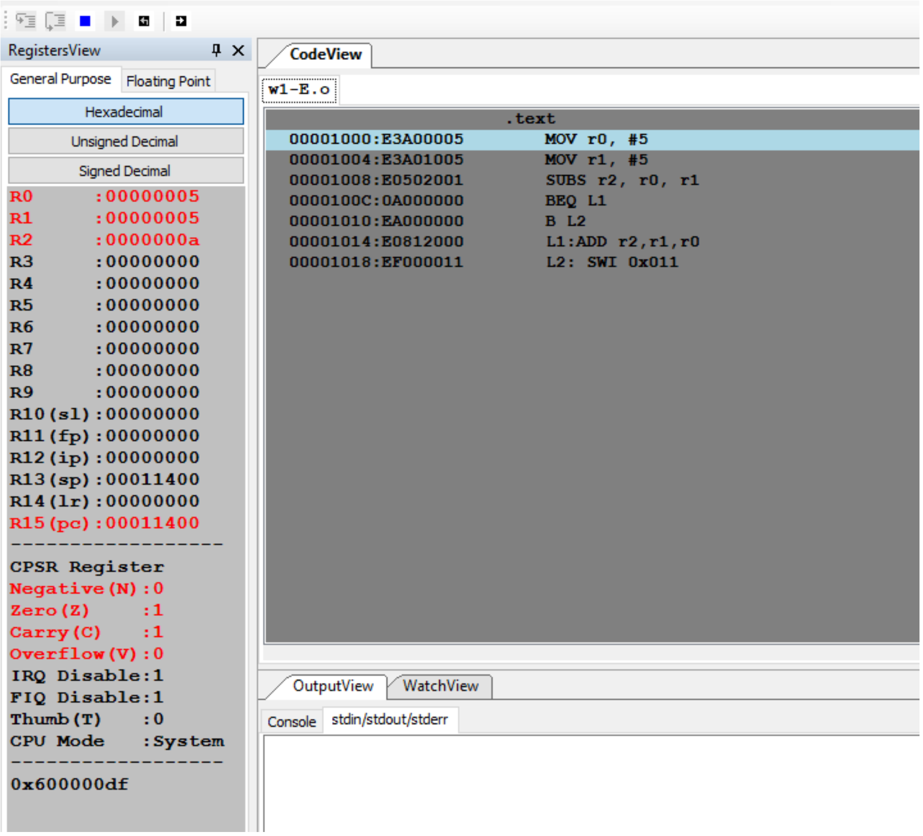
Not equal:



```
R0       :00000007
R1       :00000005
R2       :00000002
R3       :00000000
R4       :00000000
R5       :00000000
R6       :00000000
R7       :00000000
R8       :0000002d
R9       :00000000
R10(sl)  :00000000
R11(fp)  :00000000
R12(ip)  :00000000
R13(sp)  :00011400
R14(lr)  :00000000
R15(pc)  :00011400
------------------
CPSR Register
Negative(N):0
Zero(Z)    :0
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
------------------
0x200000df
```

```
                        .text
00001000:E3A00007        MOV r0, #7
00001004:E3A01005        MOV r1, #5
00001008:E0502001        SUBS r2, r0, r1
0000100C:0A000000        BEQ L1
00001010:EA000000        B L2
00001014:E0812000        L1:ADD r2,r1,r0
00001018:EF000011        L2: SWI 0x011
```

## Equal:



```
R0       :00000005
R1       :00000005
R2       :0000000a
R3       :00000000
R4       :00000000
R5       :00000000
R6       :00000000
R7       :00000000
R8       :00000000
R9       :00000000
R10(sl)  :00000000
R11(fp)  :00000000
R12(ip)  :00000000
R13(sp)  :00011400
R14(lr)  :00000000
R15(pc)  :00011400
------------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
------------------
0x600000df
```

```
                        .text
00001000:E3A00005        MOV r0, #5
00001004:E3A01005        MOV r1, #5
00001008:E0502001        SUBS r2, r0, r1
0000100C:0A000000        BEQ L1
00001010:EA000000        B L2
00001014:E0812000        L1:ADD r2,r1,r0
00001018:EF000011        L2: SWI 0x011
```

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Week#____1_______ Program Number:_____3____

Title of the Program

**Based on the value of the number in R0, Write an ALP to store 1 in R1 if R0 is zero, Store 2 in R1 if R0 is positive, Store 3 in R1 if R0 is negative. (Program shown in class)**

I.ARM Assembly Code

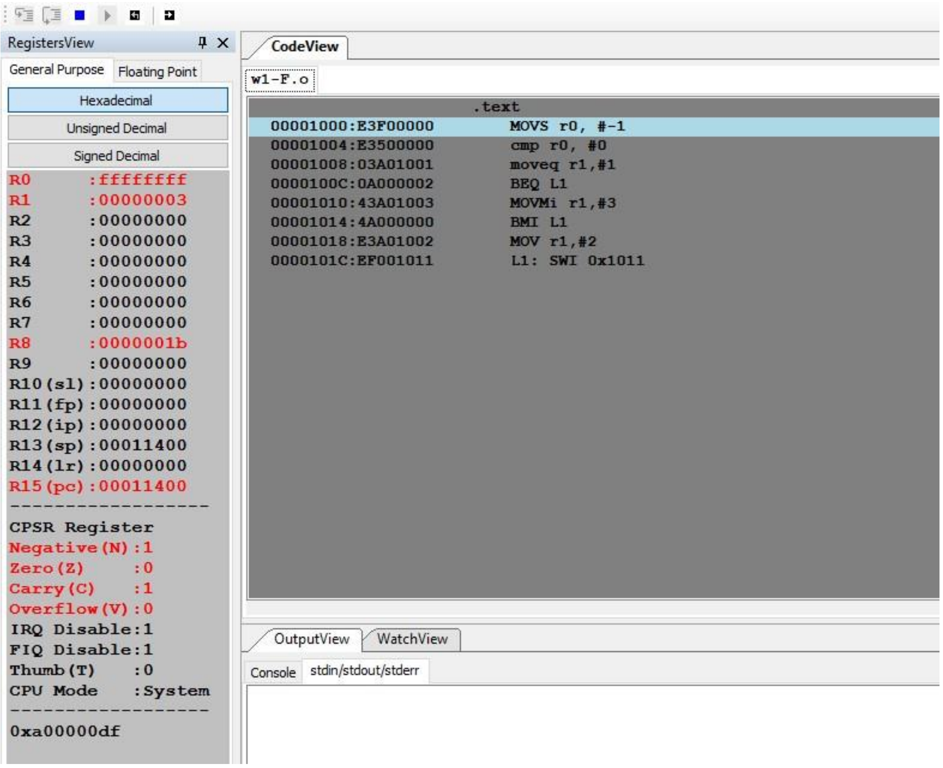
```
.text
    MOVS r0, #0
    cmp r0, #0
    moveq r1,#1
    BEQ L1
    MOVMi r1,#3
    BMI L1
```

```
MOV r1,#2
L1: SWI 0x1011
```

## II. Output Screen Shot (Three)

The output should be verified for zero, positive and negative cases.

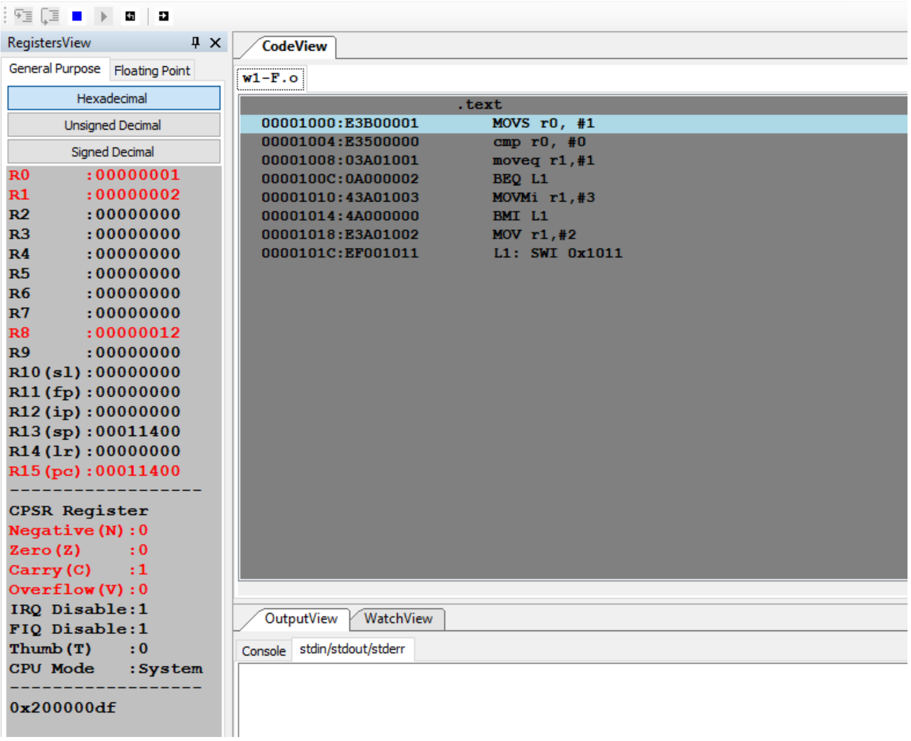
Negative:



```
R0       :ffffffff
R1       :00000003
R2       :00000000
R3       :00000000
R4       :00000000
R5       :00000000
R6       :00000000
R7       :00000000
R8       :0000001b
R9       :00000000
R10(sl)  :00000000
R11(fp)  :00000000
R12(ip)  :00000000
R13(sp)  :00011400
R14(lr)  :00000000
R15(pc)  :00011400
------------------
CPSR Register
Negative(N):1
Zero(Z)    :0
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
------------------
0xa00000df
```

```
                         .text
00001000:E3F00000        MOVS r0, #-1
00001004:E3500000        cmp r0, #0
00001008:03A01001        moveq r1,#1
0000100C:0A000002        BEQ L1
00001010:43A01003        MOVMi r1,#3
00001014:4A000000        BMI L1
00001018:E3A01002        MOV r1,#2
0000101C:EF001011        L1: SWI 0x1011
```

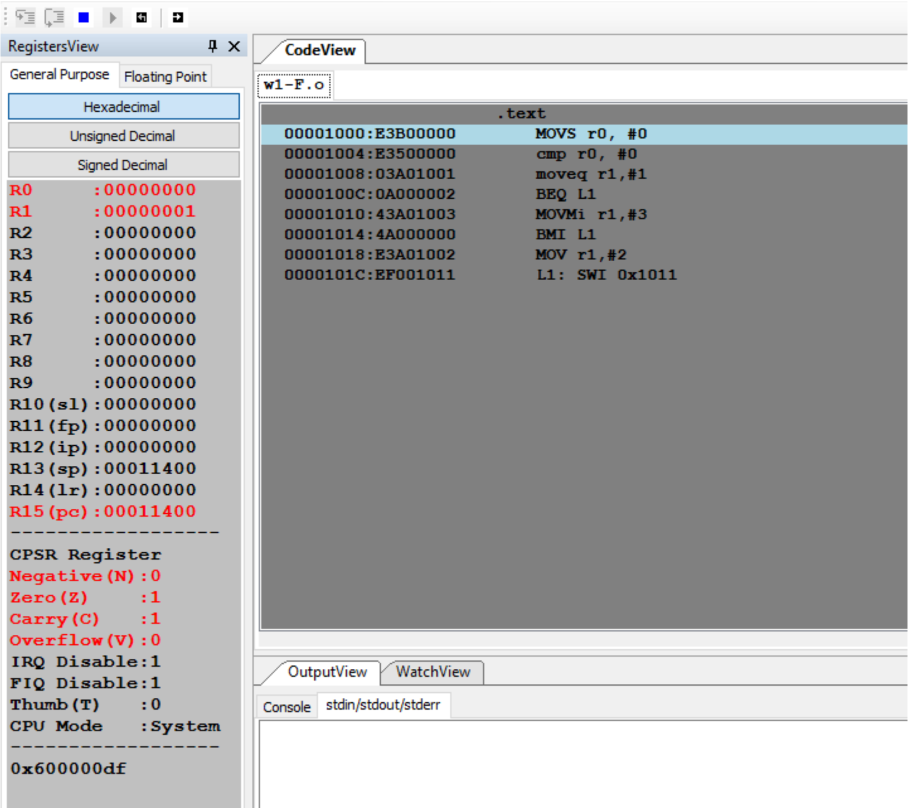
Positive:



```
R0      :00000001
R1      :00000002
R2      :00000000
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000012
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00011400
R14(lr):00000000
R15(pc):00011400
-----------------
CPSR Register
Negative(N):0
Zero(Z)    :0
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
-----------------
0x200000df
```

```
                    .text
00001000:E3B00001        MOVS r0, #1
00001004:E3500000        cmp r0, #0
00001008:03A01001        moveq r1,#1
0000100C:0A000002        BEQ L1
00001010:43A01003        MOVMi r1,#3
00001014:4A000000        BMI L1
00001018:E3A01002        MOV r1,#2
0000101C:EF001011        L1: SWI 0x1011
```

# Zero:



```
R0      :00000000
R1      :00000001
R2      :00000000
R3      :00000000
R4      :00000000
R5      :00000000
R6      :00000000
R7      :00000000
R8      :00000000
R9      :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00011400
R14(lr):00000000
R15(pc):00011400
-----------------
CPSR Register
Negative(N):0
Zero(Z)    :1
Carry(C)   :1
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T)   :0
CPU Mode   :System
-----------------
0x600000df
```

```
                    .text
00001000:E3B00000        MOVS r0, #0
00001004:E3500000        cmp r0, #0
00001008:03A01001        moveq r1,#1
0000100C:0A000002        BEQ L1
00001010:43A01003        MOVMi r1,#3
00001014:4A000000        BMI L1
00001018:E3A01002        MOV r1,#2
0000101C:EF001011        L1: SWI 0x1011
```

## Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature:
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Section: F
Date: 20/01/2023