MPCA - Theory Assignment-2

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1) Concides the following sequence of instructions in MIPS architecture

LDR R_1, [R_2 #40]
ADD R_2, R_3, R_3
ADD R_1, R_1, R_2
STR R_1, [R_2, #20]

a) find all dependencies in this instruction sequence.
b) find all hazards in this instruction sequence for a five-stage pipeline with & without data forwarding
c) find whether NOPs are required to be introduced inspite of data forwarding in this instruction sequence

Solution:

a) RAW dependency (R_1 at 4th, R_2 at 3rd Instruction)
WAW dependency (R_1 at 4th instruction)

b) **With data forwarding**

IF1 ID1 EX1 M1 WB1
IF2 ID2 EX2 M2 WB2
IF3 ID3 EX3 M3 WB3
IF4 ID4 EX4 M4 WB4

There is a hazard at 3rd & 4th instr. caused by R_1

Without data forwarding

IF1 ID1 EX1 M1 WB1
IF2 ID2 EX2 M2 WB2
IF3 ID3 EX3 M3 WB3
IF4 ID4 EX4 M4 WB4

hazard at 3rd & 4th instruction caused by R_1 & R_2

c) NOP's should be introduced after 3rd instructions

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2) consider following sequence of instructions in MIPS architecture

```
LDR R1, [R6, #40]
BEQ R2, R3, LABEL2
ADD R1, R6, R4
LABEL2: BEQ R1, R2, LABEL1
        STR R2, [R4, #20]
        AND R1, R1, R4
```

a) Draw the pipeline execution diagram for this code, assuming there are no delay slots & that branches execute in EX stage

b) Repeat the exercise mentioned in and draw pipeline execution diagram for this code assuming that delay slots are used by writing a "SAFE INSTRUCTION" in delay slot.

a)

```
IF ID EX M WB
   IF ID EX M WB
      IF ID X X X
         IF ID EX M WB
            IF ID EX M WB
               IF ID EX M WB
```

b)

```
IF ID EX M WB
   IF ID EX M WB   (Branch)
      IF ID EX M WB  (delay slot instr)
         IF ID EX M WB (delay slot instr)
            IF ID EX M WB
               IF ID EX M WB
               IF ID EX M WB
               IF ID EX M WB
               IF ID EX M WB
               IF ID EX M WB
```

delay slot instr ⟶

delay slot instr ⟶

delay slot instr could be Nop