Register map description of the XENSIV™ PAS CO2

About this document

Scope and purpose

This application note provides a detailed description of the register map of XENSIV™ PAS CO2.

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1 Register map access method

The registers that can be accessed by the user's application via the communication interfaces are covered here. Registers need to be addressed byte-wise.

Table 1 Bit access terminology

Mode	Symbol	Description
Read/Write	rw	This bit or bitfield can be written or read.
Read	r	This bit or bitfield is read-only.
Write	w	This bit or bitfield is write-only (read as 0_H).
Read/Write hardware or firmware affected	rwh	As rw, but bit or bitfield can also be modified by hardware or firmware.
Read hardware or firmware affected	rh	As r, but bit or bitfield can also be modified by hardware or firmware.
Sticky	s	Bits with this attribute are "sticky" in one direction. If their reset value is overwritten once they can be switched again into their reset state only by a reset operation. Software and internal logic (except reset-like functions) cannot switch this type of bit into its reset state by writing directly to the register. The sticky attribute can be combined with other functions (e.g. "rh").
Reserved/Not implemented	0	Bitfields named "0" indicate functions not implemented. They have the following behavior: • Reading these bitfields returns 0H. • Writing these bitfields has no effect. These bitfields are reserved. When writing, software should always set such bitfields to 0_H to preserve compatibility with future products.
Reserved/Not defined	Res	Certain bitfields or bit combinations in a bitfield can be marked as "Reserved", indicating that the behavior of the device is undefined for that combination of bits. Setting the register to such an undefined value may lead to unpredictable results. When writing, the software must always set such bitfields to legal values.

2 Register map

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
PROD_ID	0x00	PROD r				REV r				0x4F
SENS_STS	0x01	SEN_RDY rh	PWM_DIS_ST rh	ORTMP rhs	ORVS rhs	ICCER rhs	ORTMP_CLR w	ORVS_CLR w	ICCER_CLR w	0xC0
MEAS_RATE_H	0x02	VAL rwh								0x00
MEAS_RATE_L	0x03	VAL rwh								0x3C
MEAS_CFG	0x04	0 rw		PWM_OUTEN rw	PWM_MODE rw	BOC_CFG rwh		OP_MODE rwh		0x24
CO2PPM_H	0x05	VAL r								0x00
CO2PPM_L	0x06	VAL r								0x00
MEAS_STS	0x07	0 rw		Res rh	DRDY rhs	INT_STS rhs	ALARM rhs	INT_STS_CLR w	ALARM_CLR w	0x00
INT_CFG	0x08	0 rw			INT_TYP rw	INT_FUNC rw			ALARM_TYP rw	0x11
ALARM_TH_H	0x09	VAL rw								0x00
ALARM_TH_L	0x0A	VAL rw								0x00
PRESS_REF_H	0x0B	VAL rwh								0x03
PRESS_REF_L	0x0C	VAL rwh								0xF7
CALIB_REF_H	0x0D	VAL rwh								0x01
CALIB_REF_L	0x0E	VAL rwh								0x90
SCRATCH_PAD	0x0F	VAL rw								0x00
SENS_RST	0x10	SRTRG w								0x00
Reserved	0x11 ... 0x14	Reserved registers Read & Write access to those registers generate a communication error								
Reserved	0x15 ... 0xFF	Reserved registers Read & Write access to those registers generate a non-acknowledge condition.								

3 Description of different registers

3.1 Product and revision ID register (PROD_ID)

This register displays the device's product and version ID. Write accesses to this register are ignored.

Register name: **PROD_ID** **Address**: 0x00

Reset value: 0x4F

Field	Bits	Type	Description
PROD	7:5	r	**Product ID** This bitfield indicates the product type. 001_b: Revision 1.
REV	4:0	r	**Revision ID** This bitfield indicates the product and firmware revision. 0001_b: Revision 1.

3.2 Sensor status register (SENS_STS)

This register displays and controls the status of the sensor. Write accesses to the read-only bits of this register are ignored.

Register name: SENS_STS **Address**: 0x01

Reset value: 0xC0

Field	Bits	Type	Description
SEN_RDY	7	rh	**Sensor ready bit** This bit indicates if the initialization of the sensor after power-on reset has been performed correctly. 0_b: The sensor has not been initialized correctly. 1_b: The sensor has been initialized correctly.
PWM_DIS_ST	6	rh	**PWM_DIS pin status** This bit indicates the level read at pin **PWM_DIS**. 0_b: A low level is read at pin **PWM_DIS**. 1_b: A high level is read at pin **PWM_DIS**. Note: This bit is updated at every transition at pin **PWM_DIS**.
ORTMP	5	rhs	**Out-of-range temperature error bit (sticky bit)** This bit indicates if a condition where the temperature has been outside the specified valid range has been detected. 0_b: No error has occurred. 1_b: An error has occurred. This bit is cleared by setting **SENS_STS.ORTMP_CLR**.
ORVS	4	rhs	**Out-of-range VDD12V error bit (sticky bit)** This bit indicates if a condition where VDD12V has been outside the specified valid range has been detected. 0_b: No error has occurred. 1_b: An error has occurred. This bit is cleared by setting bit **SENS_STS.ORVS_CLR**.

Description of different registers

ICCER	3	rhs	**Communication error notification bit (sticky bit)** This bit indicates if a non-valid command has been received by the serial communication interface. 0_b: No invalid command received. 1_b: An invalid command has been received. This bit is cleared by setting **SENS_STS.ICCER_CLR**.
ORTMP_CLR	2	w	**Out-of-range temperature error clear bit** Writing this bit with 1_b clears the sticky bit **SENS_STS.ORTMP**. This bit is read back as 0_b.
ORVS_CLR	1	w	**Out-of-range VDD12V error clear bit** Writing this bit with 1_b clears the sticky bit **SENS_STS.ORVS**. This bit is read back as 0_b.
ICCER_CLR	0	w	**Communication error clear bit** Writing this bit with 1_b clears the sticky bit **SENS_STS.ICCER**. This bit is read back as 0_b.

3.3 Measurement period configuration registers (MEAS_RATE_H and MEAS_RATE_L)

Registers **MEAS_RATE_H** and **MEAS_RATE_L** define the measurement period used in continuous mode. The concatenation of **MEAS_RATE_H** (MSB) and **MEAS_RATE_L** (LSB) define the period. The concatenated value is coded as a two's complement signed short integer (1 bit = 1 s).

Values above $0FFF_H$ are treated as being equal to FFF_H (4095 s). Values below 0005_H are treated as being equal to 0005_H (5 s).

Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set).

Note: When writing to MEAS_RATE_H and MEAS_RATE_L, the new value is not immediately considered by the device. It is internally latched at the next transition from idle to continuous mode.

Register name: **MEAS_RATE_H** **Address**: 0x02

Reset value: 0x00

Field	Bits	Type	Description
0	7:4	rw	**Reserved** This bitfield shall be written with 0_H.
VAL	3:0	rwh	**MSB of the measurement period in continuous mode** The concatenation of this value with bitfield **MEAS_RATE_L** defines the measurement period in continuous mode. Note: Values above $0F_H$ reserved. Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set) and sets the bitfield to $0F_H$.

Register name: **MEAS_RATE_L** **Address**: 0x03

Reset value: 0x3C

Field	Bits	Type	Description
VAL	7:0	rwh	**LSB of the measurement period in continuous mode** The concatenation of this value with bitfield **MEAS_RATE_H.VAL** defines the measurement period in continuous mode.

			Note: Values 00_H to 04_H are reserved. Writing a non-valid value to this field generates a communication error (bit **SENS_STS**.**ICCER** set) and sets the bitfield to 05_H.

3.4 Measurement mode configuration register (MEAS_CFG)

This register defines the operation settings of the device.

Register name: **MEAS_CFG** **Address**: 0x04

Reset value: 0x24

Field	Bits	Type	Description
Res	7:6	rwh	**Reserved** This bitfield shall be written with 00_b.
PWM_OUTEN	5	rwh	**PWM output software enable bit** 0_b: **PWM** output is disabled by software. 1_b: **PWM** output is enabled by software. Note 1: The actual state of pin **PWM** depends on both **MEAS_CFG.PWM_OUTEN** and pin **PWM_DIS**. Note 2: This bit is automatically set at a high to low transition at pin **PWM_DIS**.
PWM_MODE	4	rw	**PWM mode configuration** 0_b: PWM single-pulse mode. 1_b: PWM pulse-train mode.
BOC_CFG	3:2	rwh	**Baseline offset compensation configuration** 00_b: Automatic baseline offset compensation (ABOC) disabled. No offset compensation occurs. 01_b: ABOC enabled. The offset is periodically updated at each BOC computation. Note: In single-shot mode, ABOC correction factor is applied but the ABOC scheme is not active and not updated. 10_b: Forced compensation. Note: After the forced compensation is done, device automatically reconfigures itself into ABOC (**MEAS_CFG.BOC_CFG** = 01_b). 11_b: Reserved.

Description of different registers

OP_MODE	1:0	rwh	**Sensor operating mode** 00_b: Idle mode. 01_b: Single-shot mode enabled. Writing 01_b to this field triggers a single measurement sequence. This field is reset by firmware automatically. 10_b: Continuous mode enabled. 11_b: Reserved (as 00_b).

3.5 CO_2 concentration result register (CO2PPM_H and CO2PPM_L)

Registers **CO2PPM_H** and **CO2PPM_L** are used to display the result of the last CO_2 concentration measurement. The concatenation of **CO2PPM_H** (MSB) and **CO2PPM_L** (LSB) define the CO_2 concentration value. The concatenated CO_2 concentration value is coded as a two's complement signed short integer (1 bit = 1 ppm). This field is updated at the end of each measurement sequence.

Reading register **CO2PPM_L** clears bit **MEAS_STS.DRDY**.

When reading the CO_2 concentration value, the user shall first read registers **CO2PPM_H** and then **CO2PPM_L**.

Register name: **CO2PPM_H** **Address**: 0x05

Reset value: 0x00

Field	Bits	Type	Description
VAL	7:0	rh	**MSB of the CO_2 concentration value** The concatenation of this value with bitfield **CO2PPM_L.VAL** gives the CO_2 concentration value.

Register name: **CO2PPM_L** **Address**: 0x06

Reset value: 0x00

Field	Bits	Type	Description
VAL	7:0	rh	**LSB of the CO_2 concentration value** The concatenation of this value with bitfield **CO2PPM_H.VAL** gives the CO_2 concentration value. Reading this bitfield clears bit **MEAS_STS.DRDY**.

3.6 Measurement status register (MEAS_STS)

This register displays the status information of the sensor. Write accesses to the read-only bits of this register are ignored.

Register name: **MEAS_STS** **Address**: 0x07

Reset value: 0x00

Field	Bits	Type	Description
0	7:6	rw	**Reserved** This bitfield is read as 00_b.
Res	5	rh	**Reserved** This bit is reserved.
DRDY	4	rhs	**Data ready bit (sticky bit)** This bit indicates if new data are available in register **CO2PPM_H** and **CO2PPM_L**. 0_b: No new data are available. 1_b: Unread data are available. This bit is set at the end of every measurement sequence. This bit is cleared by reading **CO2PPM_L**.
INT_STS	3	rhs	**INT pin status bit** This bit indicates if pin **INT** has been latched to active state (in case of alarm or data ready). 0_b: Pin **INT** has not been latched to active state. 1_b: Pin **INT** has been latched to active state. This bit is set at the end of every measurement sequence in case of a latching condition. This bit is cleared by setting bit **MEAS_STS.INT_STS_CLR**.

Description of different registers

ALARM	2	rhs	**Alarm notification (sticky bit)** This bit indicates if a threshold violation occurred. 0_b: No violation occurred. 1_b: Violation occurred. This bit is set at the end of every measurement sequence in case of violation. This bit is cleared by setting bit **MEAS_STS.ALARM_CLR**.
INT_STS_CLR	1	w	**INT pin status clear bit** Writing this bit with 1_b clears the sticky bit **MEAS_STS.INT_STS** and forces pin **INT** to inactive level. This bit is read back as 0_b.
ALARM_CLR	0	w	**Alarm notification clear bit** Writing this bit with 1_b clears the sticky bit **MEAS_STS.ALARM**. This bit is read back as 0_b.

3.7 Interrupt pin configuration register (INT_CFG)

This register defines the configuration of pin **INT**.

Register name: **INT_CFG** **Address**: 0x08

Reset value: 0x11

Field	Bits	Type	Description
0	7:5	rw	**Reserved** This bitfield shall be written with 00_b.
INT_TYP	4	rw	**Pin INT electrical configuration** 0_b: Pin **INT** is configured as push-pull and low active. 1_b: Pin **INT** is configured as push-pull and high active. *Note:* Writing this bitfield forces pin **INT** to inactive state.
INT_FUNC	3:1	rw	**Pin INT function configuration** 000_b: Pin **INT** is inactive. 001_b: Pin **INT** is configured as alarm threshold violation notification pin. 010_b: Pin **INT** is configured as data ready notification pin. 011_b: Pin **INT** is configured as sensor busy notification pin. 100_b: Pin **INT** is configured as early measurement start notification pin (this function only is available in continuous mode with **MEAS_CFG.OP_MODE** = 10_b, otherwise the pin is inactive). 101_b: Reserved … 111_b: Reserved

Description of different registers

ALARM_TYP	0	rw	**Alarm type configuration bit** This bitfield defines if an alarm is issued in case of lower or higher threshold violation. 0_b: Crossing down – the concatenated value of register **ALARM_TH_H** and **ALARM_TH_L** is defined as a lower threshold register. 1_b: Crossing up – the concatenated value of register **ALARM_TH_H** and **ALARM_TH_L** is defined as a higher threshold register.

3.8 Alarm threshold register (ALARM_TH_H and ALARM_TH_L)

Registers **ALARM_TH_H** and **ALARM_TH_L** define the value used as a threshold for the alarm violation. The concatenation of **ALARM_TH_H** (MSB) and **ALARM_TH_L** (LSB) define the threshold value that shall be considered by the device. The concatenated alarm threshold value is coded as a 2's complement signed short integer (1 bit = 1 ppm).

Register name: **ALARM_TH_H** **Address**: 0x09

Reset value: 0x00

Field	Bits	Type	Description
VAL	7:0	rw	**MSB of the alarm threshold** The concatenation of this value with bitfield **ALARM_TH_L.VAL** defines the threshold value.

Register name: **ALARM_TH_L** **Address**: 0x0A

Reset value: 0x00

Field	Bits	Type	Description
VAL	7:0	rw	**LSB of the alarm threshold** The concatenation of this value with bitfield **ALARM_TH_H.VAL** defines the threshold value.

3.9 Pressure compensation registers (PRES_REF_H and PRES_REF_L)

Registers **PRES_REF_L** and **PRES_REF_H** are used to capture the atmospheric pressure to be compensated. The concatenation of **PRES_REF_H** (MSB) and **PRES_REF_L** (LSB) define the pressure value that shall be considered by the device. The concatenated pressure value is coded as an unsigned short integer (1 bit = 1 hPa). Since even small variations of the external pressure may lead to significant changes in the output provided by the sensor, it must be ensured that a coherent value is available for the sensor. For that purpose, **PRES_REF_H** and **PRES_REF_L** are associated with two internal shadow registers from which the device reads the pressure value to be used by the internal firmware. When writing to **PRES_REF_L**, the complete 16-bit pressure value is loaded into the shadow registers. When writing to **PRES_REF_H**, the shadow registers are not updated. Therefore, to update the pressure value, the user has to write first **PRES_REF_H** and then **PRES_REF_L**.

Pressure compensation is de facto deactivated if the default value is not updated.

For correct operation, the user shall ensure that pressure value programmed is within the specified pressure operating range of the device. The valid range of operation is 750 hPa to 1150 hPa.

Values below 750 hPa will be treated as 750 hPa (register automatically updated). Similarly, values above 1150 hPa will be treated at 1150 hPa (register automatically updated). If a value outside this range is written, bit **SENS_STS**.**ICCER** is set.

Register name: **PRES_REF_H** **Address**: 0x0B

Reset value: 0x03

Field	Bits	Type	Description
VAL	7:0	rwh	**MSB of the pressure compensation value** The concatenation of this value with bitfield **PRESS_REF_L**.**VAL** gives the pressure compensation value.

Register name: **PRES_REF_L** **Address**: 0x0C

Reset value: 0xF7

Field	Bits	Type	Description
VAL	7:0	rwh	**LSB of the pressure compensation value** The concatenation of this value with bitfield **PRESS_REF_H**.**VAL** gives the pressure compensation value.

3.10 Automatic baseline offset compensation reference

Registers **CALIB_REF_H** and **CALIB_REF_L** define the reference value used for the ABOC and the force calibration. The concatenation of **CALIB_REF_H** (MSB) and **CALIB_REF_L** (LSB) define the reference value. The concatenated offset value is coded as a two's complement signed short integer (1 bit = 1 ppm).

Values must be comprised between 350 ppm and 900 ppm. Values below 350 ppm will be treated as 350 ppm (register automatically updated). Similarly, values above 900 ppm will be treated at 900 ppm (register automatically updated). If a value outside this range is written, bit **SENS_STS**.**ICCER** is set.

Register name: **CALIB_REF_H** **Address**: 0x0D

Reset value: 0x01

Field	Bits	Type	Description
VAL	7:0	rwh	**MSB of the ABOC** The concatenation of this value with bitfield **CALIB_REF_L**.**VAL** gives the currently used reference value.

Register name: **CALIB_REF_L** **Address**: 0x0E

Reset value: 0x90

Field	Bits	Type	Description
VAL	7:0	rwh	**LSB of the ABOC** The concatenation of this value with bitfield **CALIB_REF_H**.**VAL** gives the currently used reference value.

3.11 Scratch pad register (SCRATCH_PAD)

This register provides a readable and writable address space for data integrity test during runtime. This register is not associated with a specific hardware functionality.

Register name: **SCRATCH_PAD** **Address**: 0x0F

Reset value: 0x00

Field	Bits	Type	Description
VAL	7:0	rw	**Read/Write value** This bit field is “don’t care” for the device.

3.12 Soft reset register (SENS_RST)

This register is used to trigger a soft reset.

In case an invalid command is received, bit **SENS_STS.ICCER** is set.

Register name: **SENS_RST** **Address**: 0x10

Reset value: 0x00

Field	Bits	Type	Description
SRTRG	7:0	w	**Soft reset trigger** Writing $A3_H$ to this field triggers a soft reset event. Writing BC_H to this field resets the ABOC context. Writing CF_H to this field saves the force calibration offset immediately in the internal non-volatile memory. Writing DF_H to this field disables the Stepwise Reactive IIR Filter. Writing FC_H to this field resets the forced calibration correction factor. Writing FE_H to this field enables the Stepwise Reactive IIR Filter (by default enabled). Other values are reserved. Writing a non-valid value to this field generates a communication error (bit **SENS_STS.ICCER** set). This bit is read back as 00_H.

Revision history

Document version	Date of release	Description of changes
V 1.0	04.11.2020	Creation
V 2.0	01.07.2021	Filter implemented, added filter settings
V 2.1	01.07.2022	Updated product ID and notes

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