ACADEMIC YEAR: 2023-2024

YEAR: III SEMESTER: I

FACULTY NAME: ABDUL AZEEM

SUBJECT: DIGITAL LOGIC DESIGN **REGULATION**: R20

MID-I QUESTION BANK

UNIT-1

Q.No	Question	Marks	Cognitive level
1	a) Represent +65 and -65 in sign magnitude, sign 1's complement and sign 2's Complement representation.	5M	L2
	b) Convert $(97.75)_{10}$ to base 2 and Convert $(2468)_{10}$ to $(\)_{16}$	5M	L2
2	Given the 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single error.	10M	L2
3	Perform the following addition using excess-3 code. i) 386+756 ii) 738 + 444	10M	L2
4	Perform the subtraction with the following unsigned binary numbers by taking the 2'scomplement of the subtrahend. i) $11010-10010$ ii) $11011-1101$ iii) $100-110000$ iv) $1010100-1010100$	10M	L2
5	Describe different types of numeric codes? Explain them with suitable exam	10M	L1
6	a) Perform the following: (i) $(1523)_{16} = ()_{12}$ (ii) $(1101.11)_2 = ()_{10}$ b) Discuss how the binary codes are obtained in weighted form? Encode decimal digits in 2 4 2 1, 7 3 2 -1 and 8 4 - 2 -1	10M 10M	L2 L1
7	a) Using 9's complement perform the following decimal arithmetic. Also justifyanswersWith10'scomplement i) 3765 – 4249 ii) – 255 – 106 b) What is meant by BCD? Obtain binary codes for decimal digits in BCD and 2421 codes?	5M	L2
		5M	L1
8	Implement the following functions using NAND gates. a) $F1= A (B+C D) + (B C)$ b) $F2=w x+ x^{-}y^{-}(z+w)$	10M	L2
9	What are universal gates realize AND,OR,NOT,EX-OR using NAND	10M	L2

10	The message below coded in 7-bit hamming code is transmitted	10M	L3
	through a noisy channel. Decode the message assuming that at most		
	a single error occurred in the code word. Code word= 1001001		

UNIT-2

Q.No	Question	Marks	Cognitive level
1	For the given Boolean function	10M	L2
	F = x y' z + x' y' z + w' x y + w x' y + w x y		
	Simplify the function to minimal literals using Boolean algebra		
2	a)Convert the given expression in standard SOP form	5M	L2
	f(A,B,C) = AC + BA + BC	5 N /	1.2
	b) Convert the given expression in standard POS form	5M	L2
	y = A.(A + B + C)		
3	Show that the dual of the exclusive-OR is equal to its complement.	10M	L2
4	Simplify and draw the AND/OR implementations for the following	10M	L2
	switching functions?		
	i) (A' + B) (B' + C)+ (AB + C)		
	ii) (A + B) (ABC)+ (A'C)		
5	Minimize the following function using K-map and also verify	10M	L2
	through tabulation method.		
	$F(A, B, C, D) = \sum m(1,4,5,7,8,9,12,14) + d(0,3,6,10).$		
6	a) Convert each of the following expressions to extended sum of	5M	L2
	products (SOP) form		
	i) (a + b')(a + b' + c)		
	ii) (b' c + d') a + a' b' (c'+ d)	5M	L2
	b) Implement the following functions with NAND and NOR gates		
	i) f (a, b, c, d) = a + b' (c + a' d)		
	ii) $f(a, b, c, d) = ab' c' d + a'(bcd' + b'c')$	403.6	7.0
7	Reduce the expression $f=\sum m(0,2,4,6,7,8,10,12,13,15)$ using k-	10M	L3
0	maps and implement the real minimal expression in universal logic.	10 3/	T 2
8	Reduce the expression $f=\sum m(0,2,6,8,10,13,14,15)$ using k-maps	10 M	L3
9	and implement the real minimal expression in universal logic.	101/	L2
9	Simplify using k-map	10M	L2
	i) (ABC)' + B'CD' + A'BD + ABCD + AC'D + A'BC'D'		
10	ii) (AB)' + A'C + BC + AB + AC' + (ABC)' + ABC	101/	1.2
10	Express the Boolean functions	10M	L2
	i) F = AB + AC		

ii) $F = x + y'z$	
in a POS,SOP form	

UNIT-3

Q.No	Question	Marks	Cognitive level
1	Implement the following logic functions using 4-to-16-line decoder and 16×1 De multiplexer ?	10M	L2
	i) $f1 = \sum m(0, 1, 4, 7, 12, 14, 15)$ ii) $f2 = \sum m(1, 3, 6, 9, 12)$		
2	How full adder carries are calculated ahead? Discuss the design of carry look ahead adder	10M	L2
3	Realize the following logic functions with decoder i) F1 (W ,X ,Y ,Z) = \sum m(0,2,3,4,5,6,11,12,13,14,15) ii) F2 (W ,X ,Y ,) = \sum m(1,2,3,5,7,9)	10M	L2
4	Design a circuit to convert Excess-3 code to BCD code using discrete Logic gates	10M	L2
5	Implement Full adder using half adder, full sub tractor using half sub tractor	10M	L2
6	Discuss how four bit excess – 3 adder circuit is designed. Explain its operation	10M	L2
7	Design 4 bit Binary adder/sub tractor and explain circuit operation with an example?	10M	L2
8	Implement the Boolean function given below using 8×1 multiplexer $f(A,B,C,D)=\sum m(0,2,3,5,8,11,12,14,15)$	10M	L2
9	Design BCD adder circuit using 4-bit parallel binary adder and logic gates.	10M	L2
10	Implement full adder using half adder and derive output equations	10M	L2