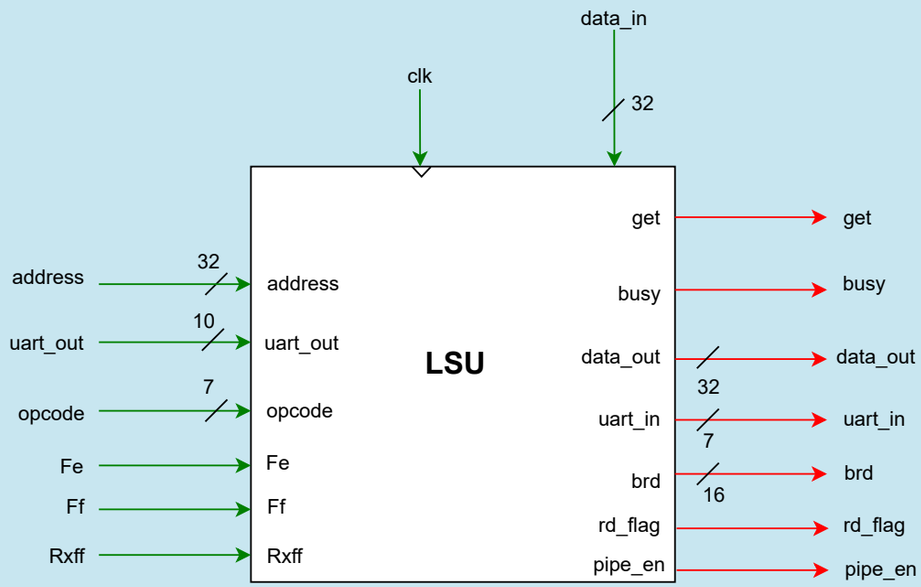
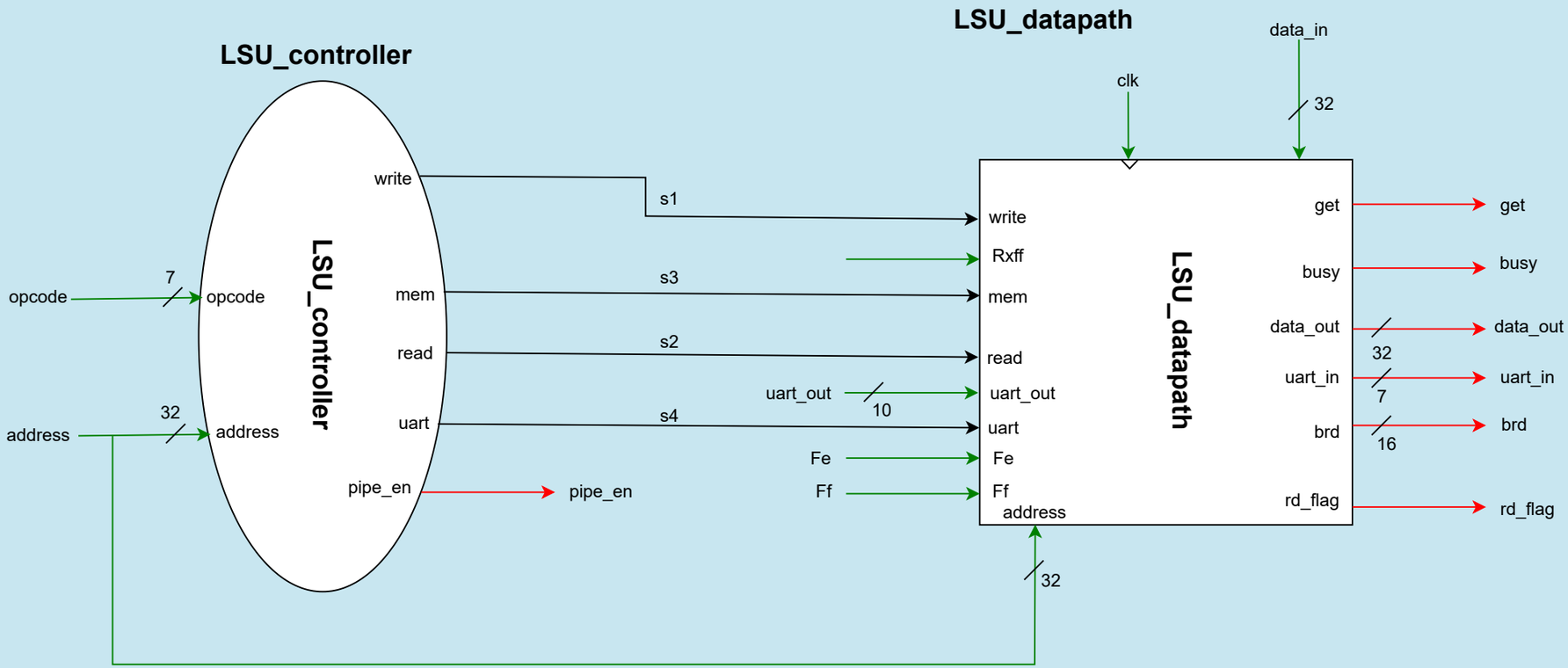
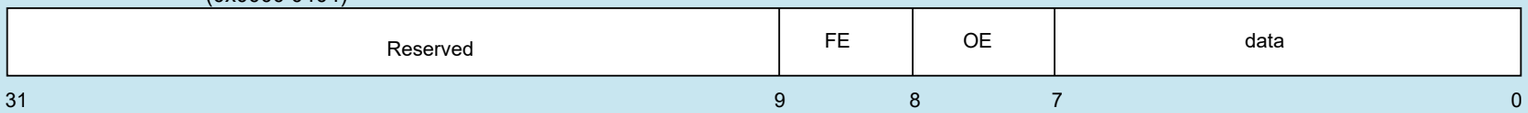

data_in
clk
32
address
32
address
uart_out
10
uart_out
LSU
opcode
7
opcode
Fe
Fe
Ff
Ff
Rxff
Rxff
get
busy
data_out
32
uart_in
7
brd
16
rd_flag
pipe_en
get
busy
data_out
uart_in
brd
rd_flag
pipe_en


LSU_controller
LSU_datapath
opcode
7
address
32
opcode
address
write
mem
read
uart
pipe_en
s1
s3
s2
s4
pipe_en
uart_out
10
Fe
Ff
clk
data_in
32
write
Rxff
mem
read
uart_out
uart
Fe
Ff
address
32
get
busy
data_out
32
uart_in
7
brd
16
rd_flag
get
busy
data_out
uart_in
brd
rd_flag

# Uart_reg

uart_tx_reg (0x0000 0400)


uart_rx_reg (0x0000 0404)




uart_ctrl_reg (0x0000 0408)


uart_baud_reg (0x0000 040C)


BRD = sysclk/(16*baud rate)

## LSU_controller table

| opcode | address | write | read | mem | uart |
|---|---|---|---|---|---|
| 0100 011 | [11: 8] != 4'd4 | 1 | 0 | 1 | 0 |
| 0100 011 | [11: 8] = 4'd4 | 1 | 0 | 0 | 1 |
| 0000 011 | [11: 8] != 4'd4 | 0 | 1 | 1 | 0 |
| 0000 011 | [11: 8] = 4'd4 | 0 | 1 | 0 | 1 |