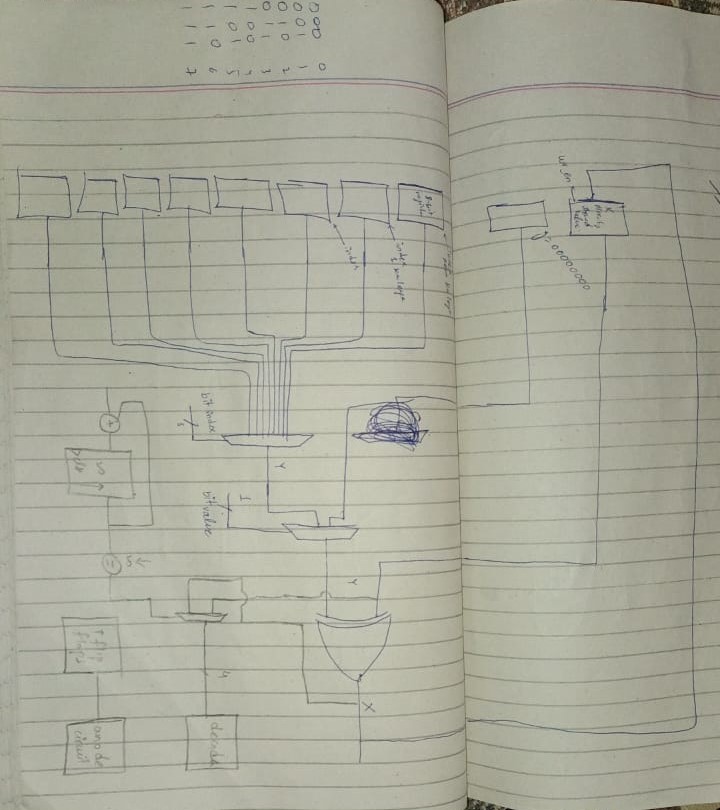
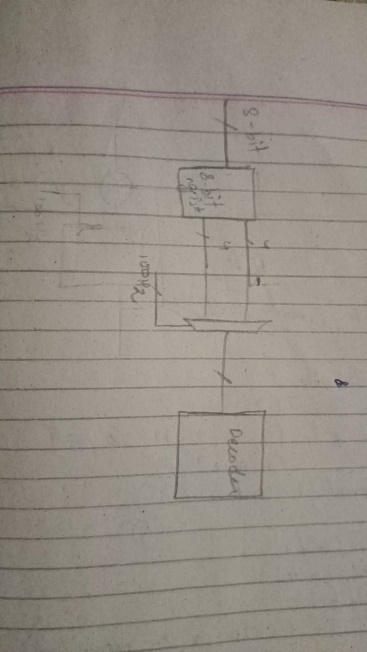
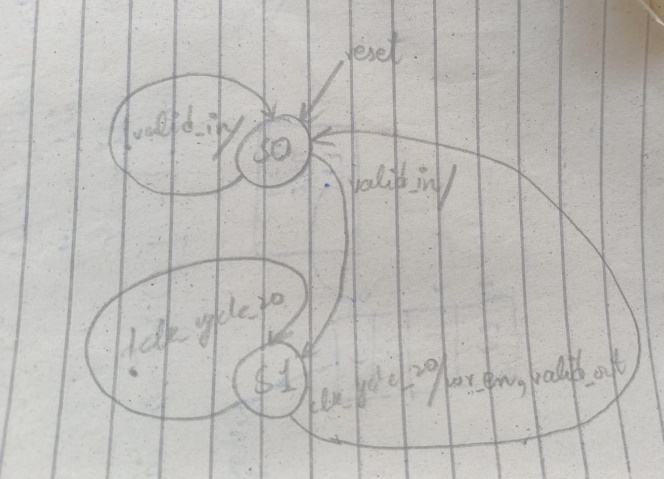
**Name: NAQI-UL-HASSAN REPORT LAB # 9 ROLL# 2022-EE-164**

Hand-made design:

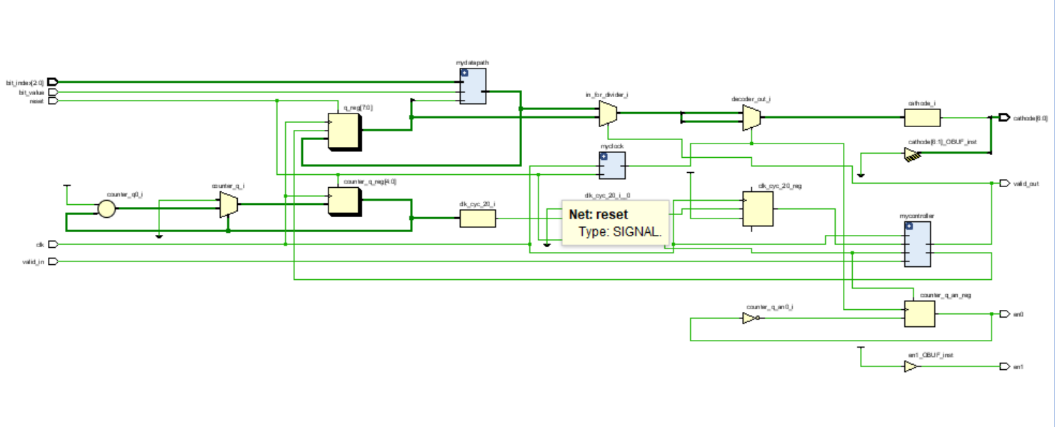




There is also the stg diagram:

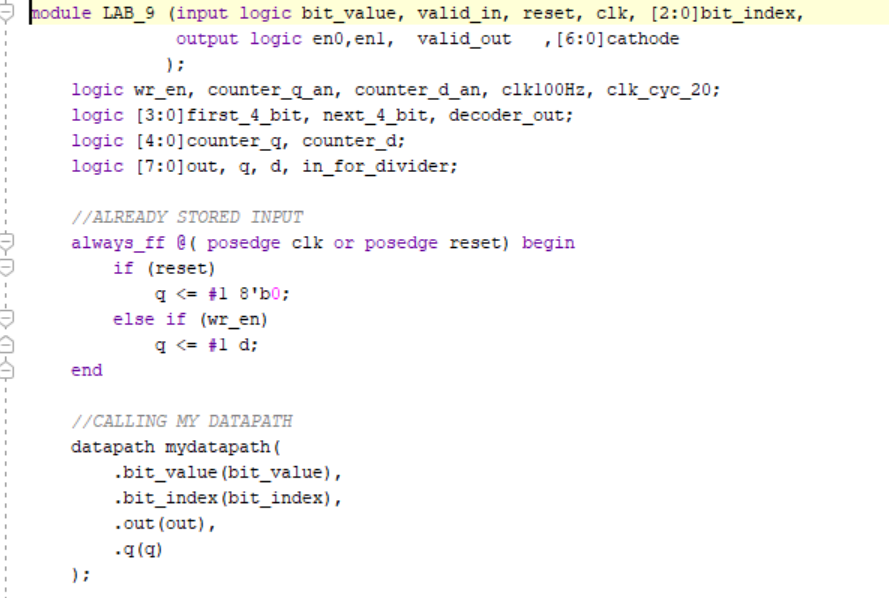


Circuit Diagram:

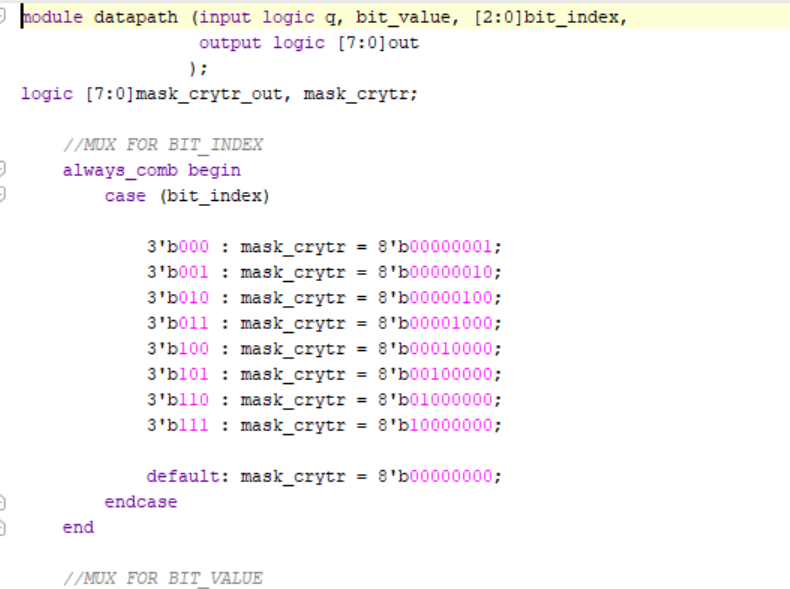


Coding:

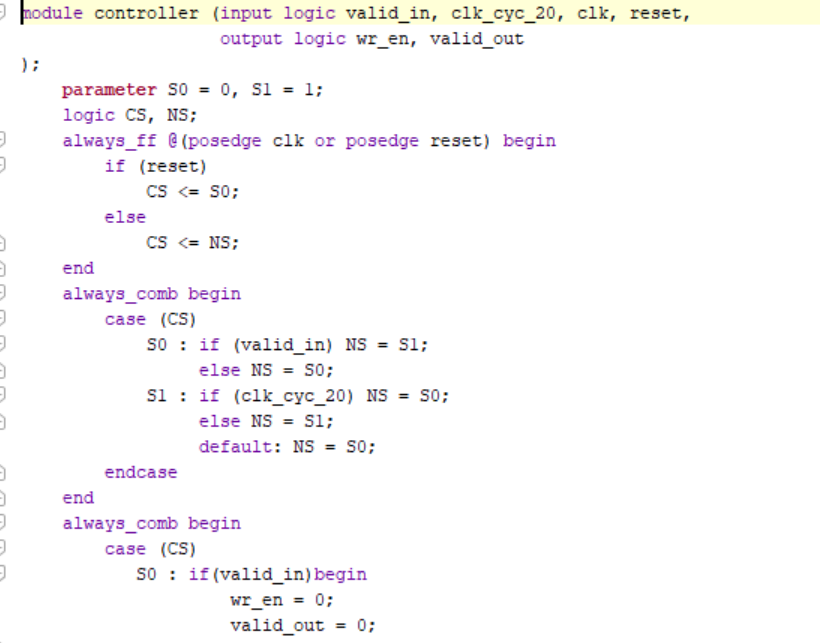
Combined module:

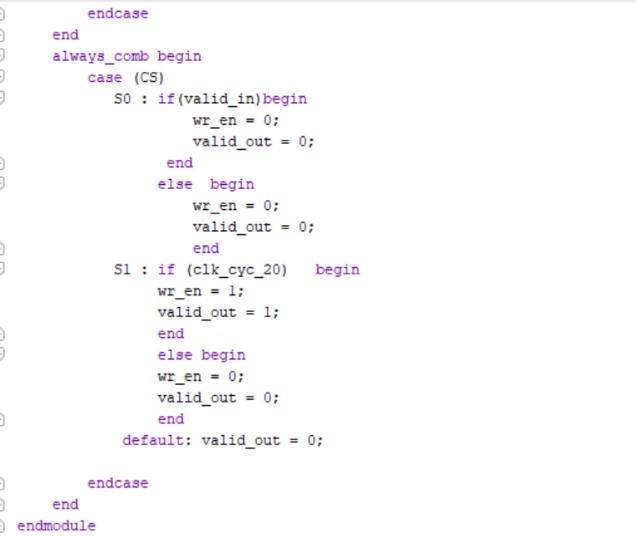


Datapath:

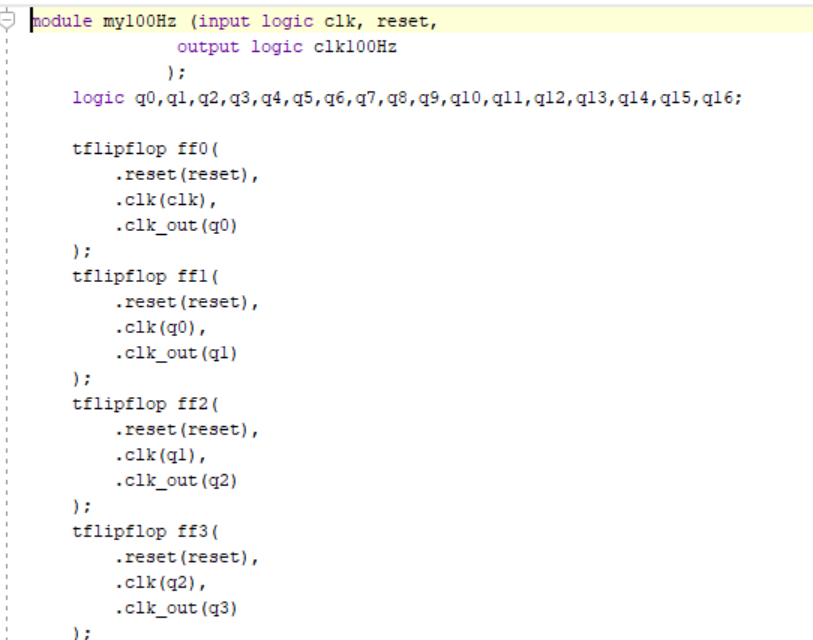


Controller:

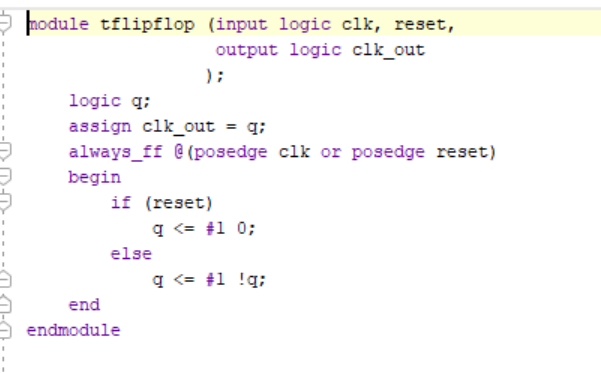




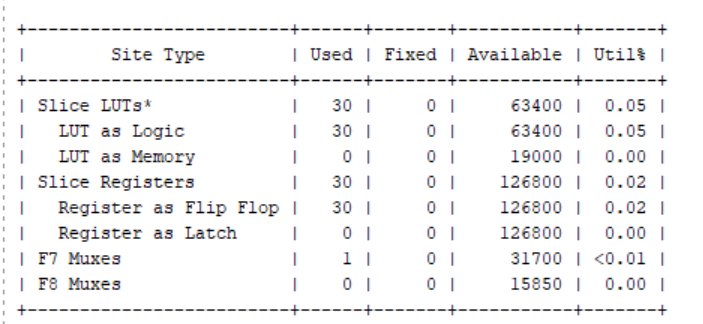
100Hz clock:

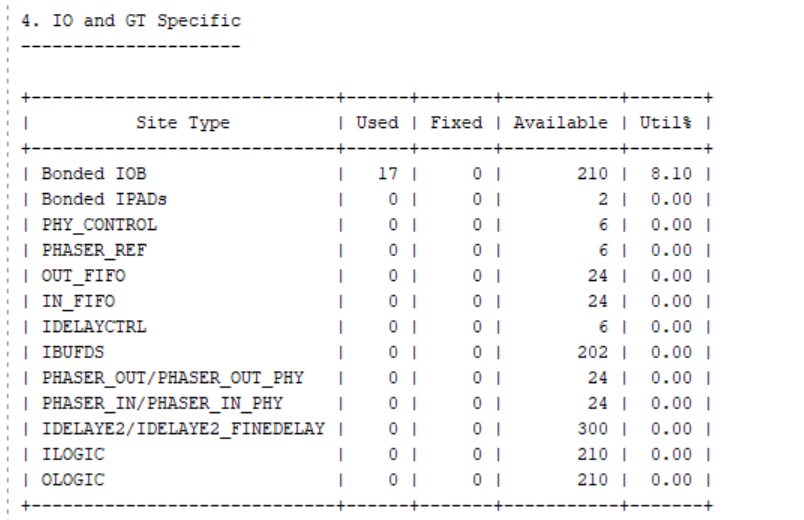


T flipflop:

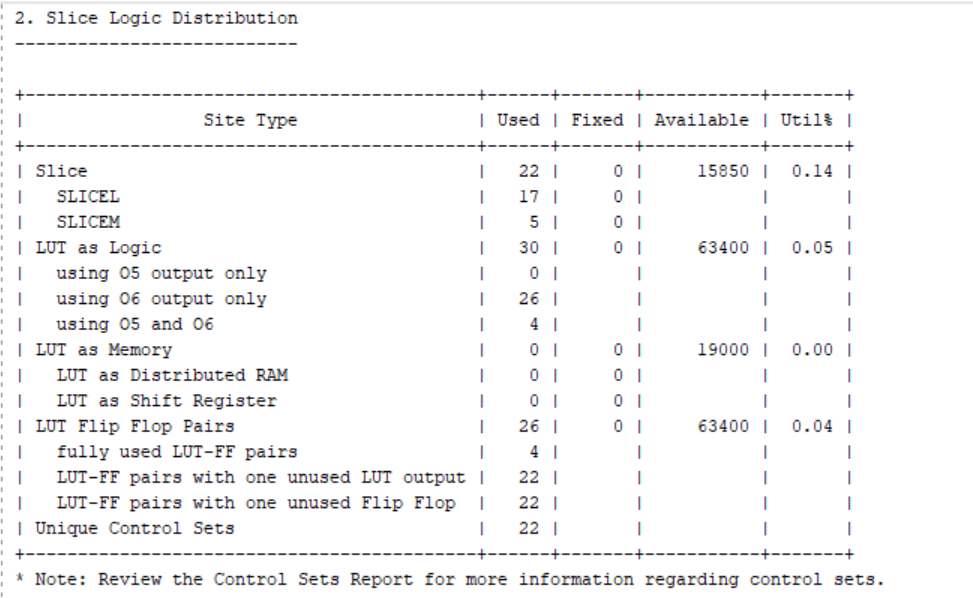


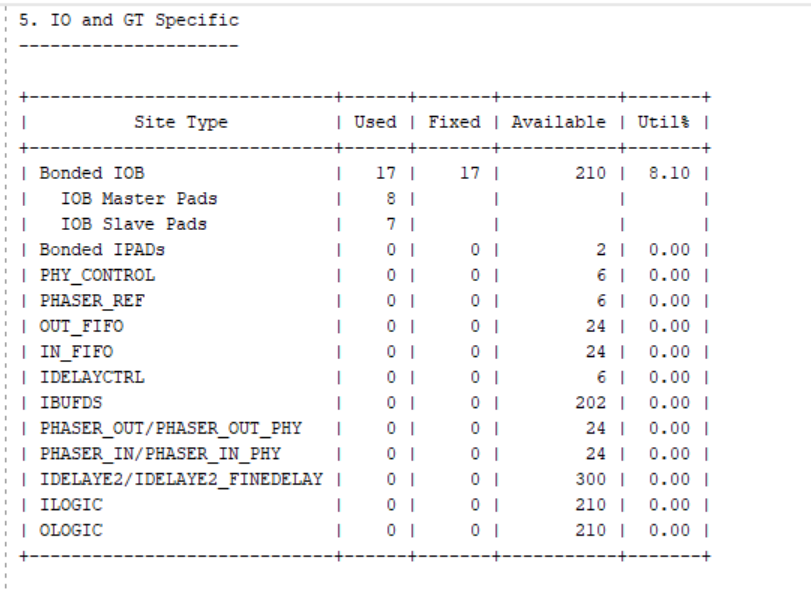
Synthesis report:

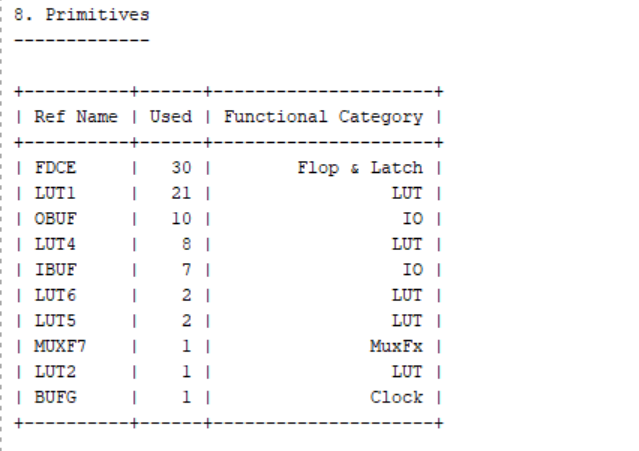


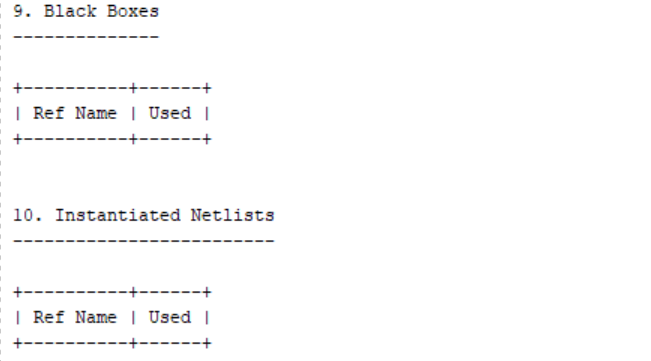


Implementation report:

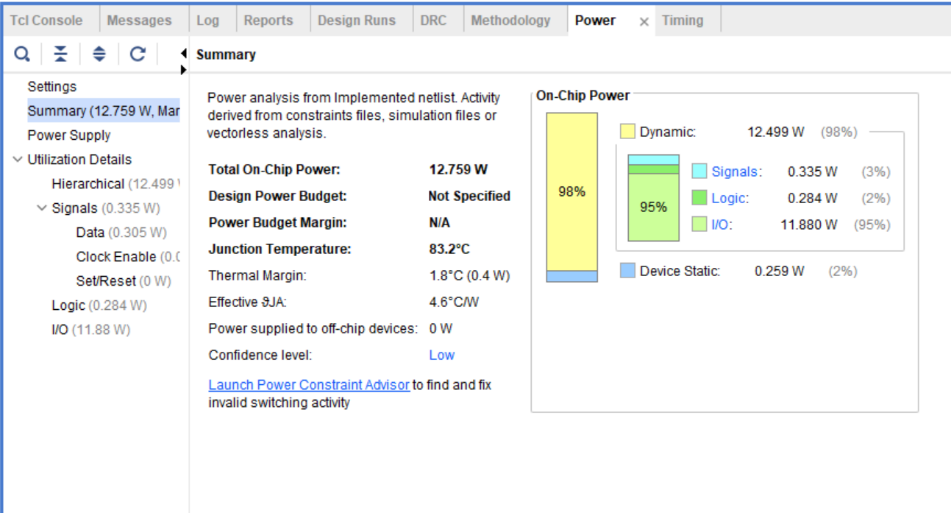








Power generation:



Combinational delays:

