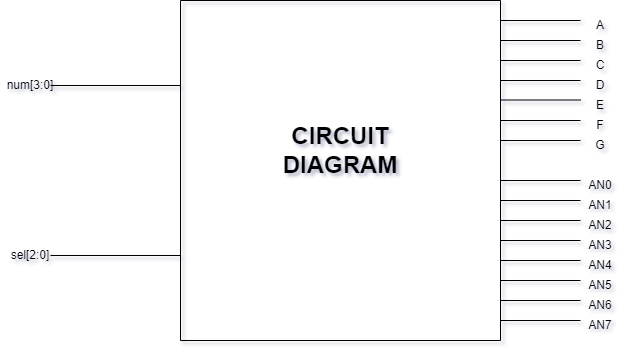
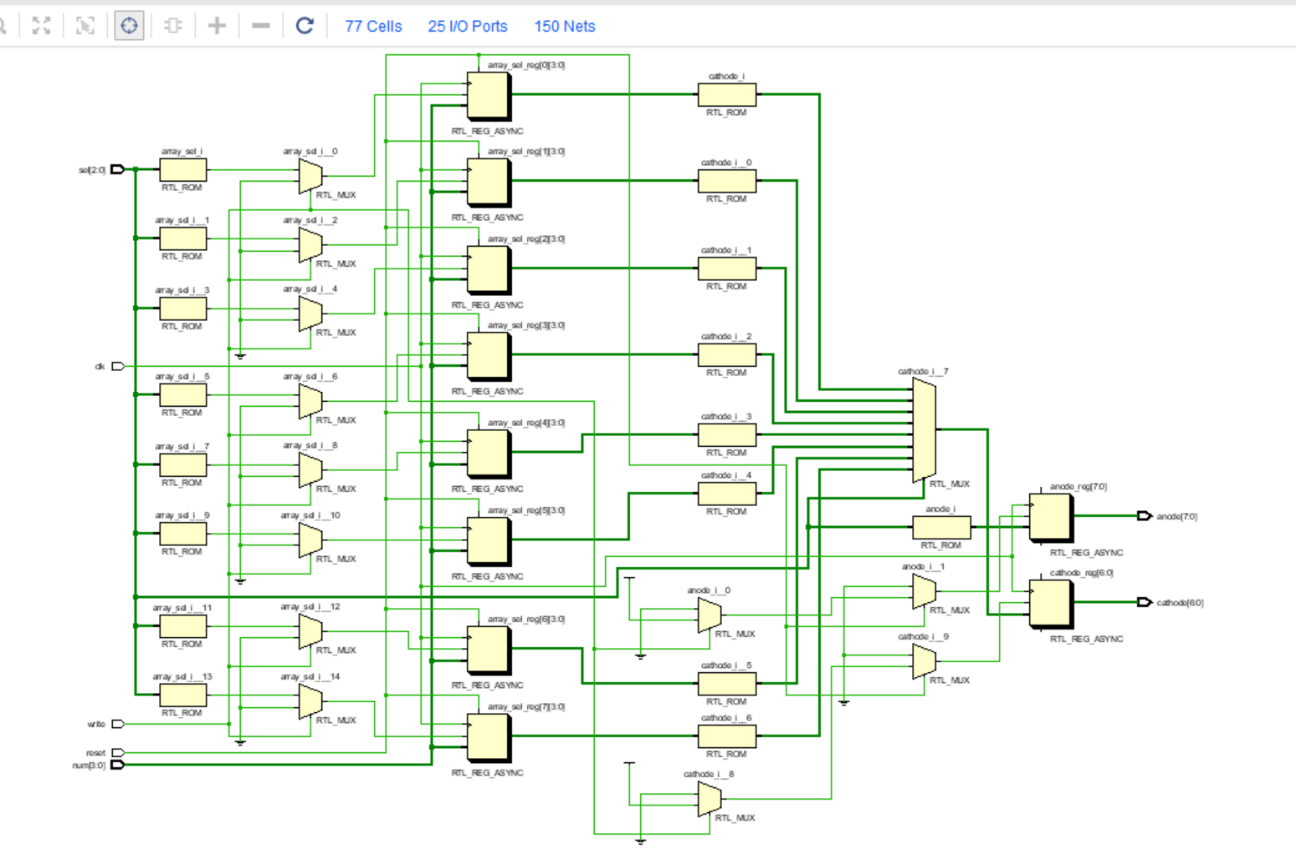
Name: NAQI UL HASSAN LAB (Report # 6) ROLL # 2022-EE-164

No. of I/O ports:

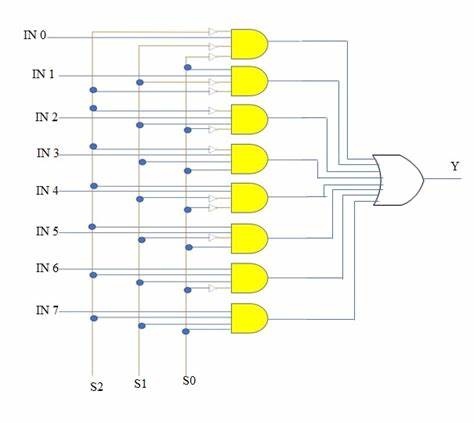


Circuit Diagram:

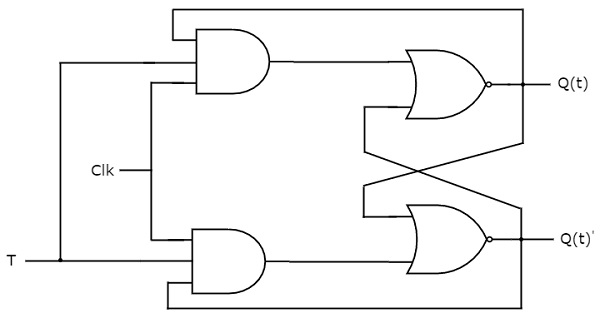


Here, I have used 8 D flip flops each of 4-bit, 2 decoders, one 8x1 MUX, and some RTL ROMS.

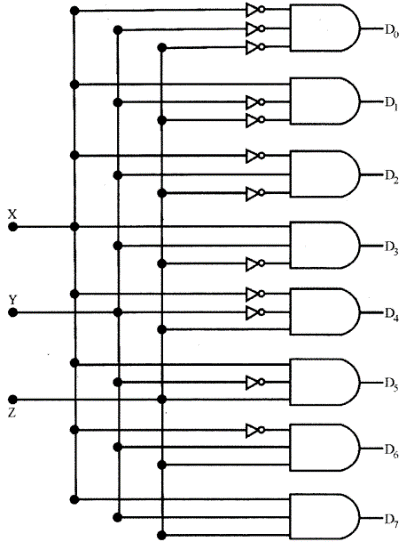
Circuit diagram of 8x1 MUX:



Circuit diagram of D Flip Flop:



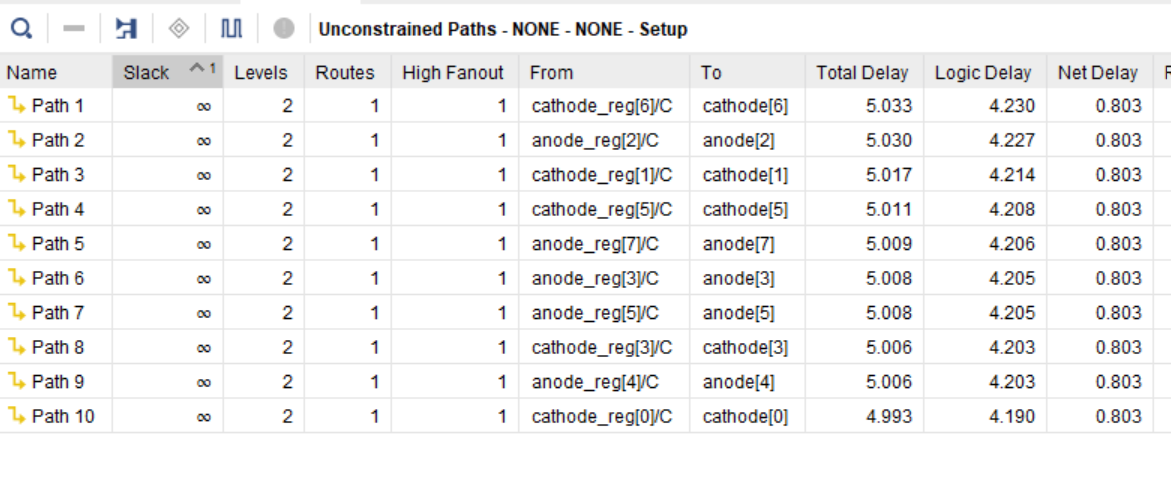
Circuit diagram of 3x8 decoder:



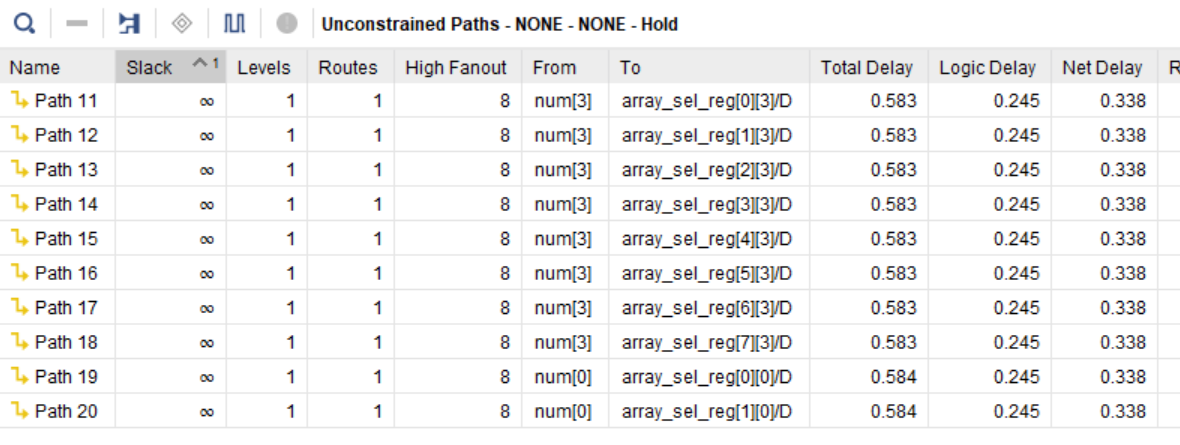
These are all gate level diagrams of the used logics and structures.

Synthesis report (Maximum combinational delays):

Following is the setup time report for synthesis report:

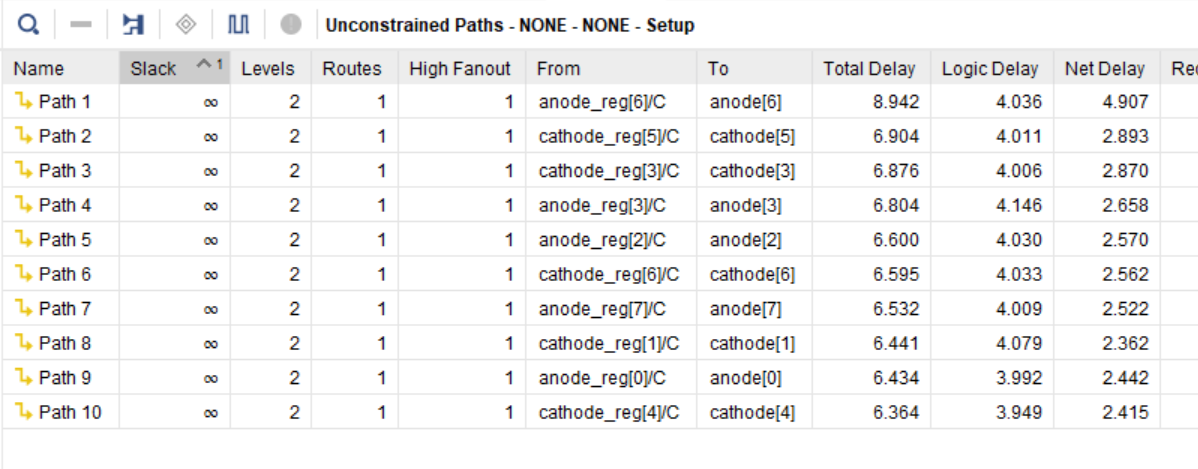


Following is the hold time report for synthesis report:

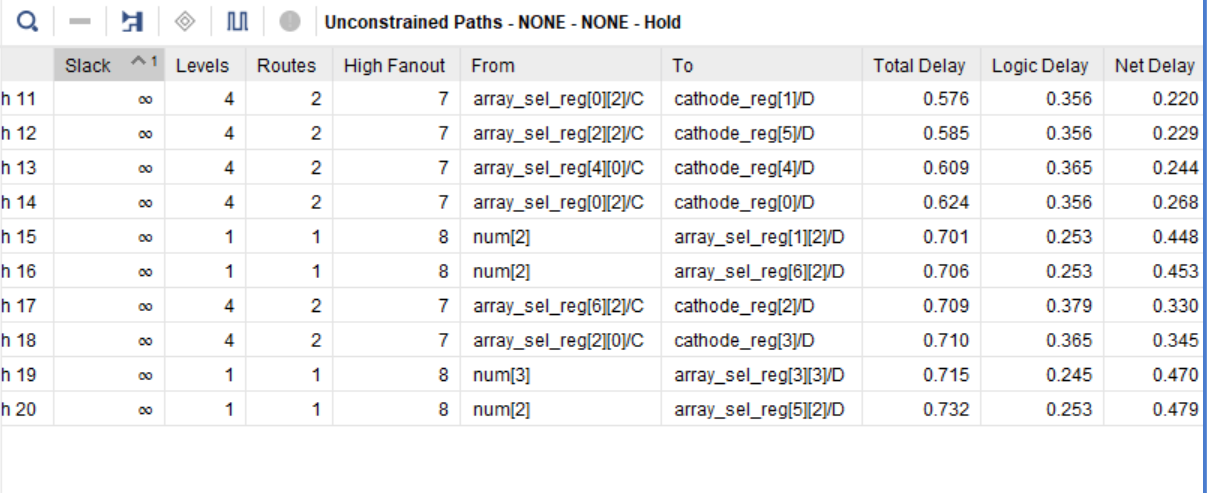


Implementation report (Maximum combinational delays):

Following is the setup time report for implementation report:

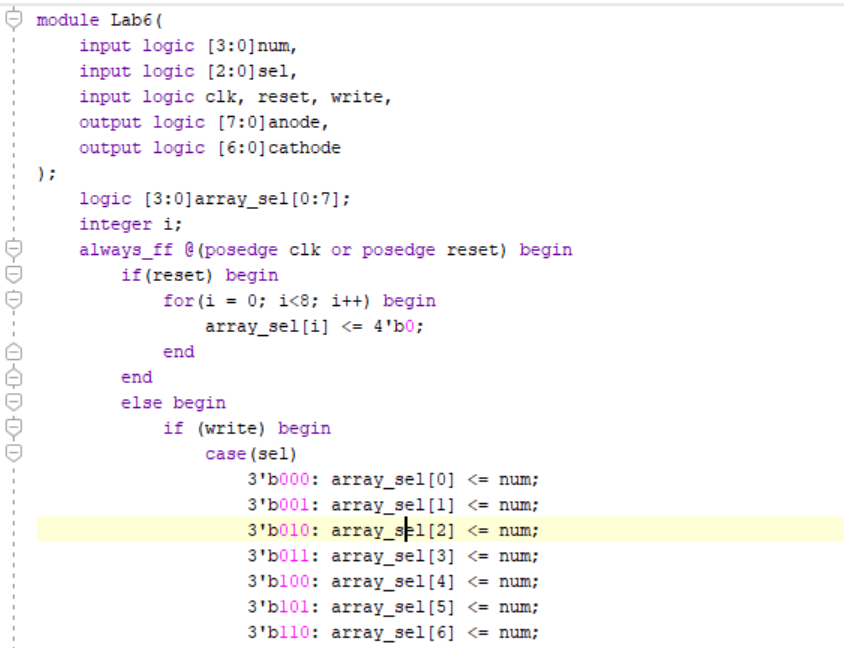


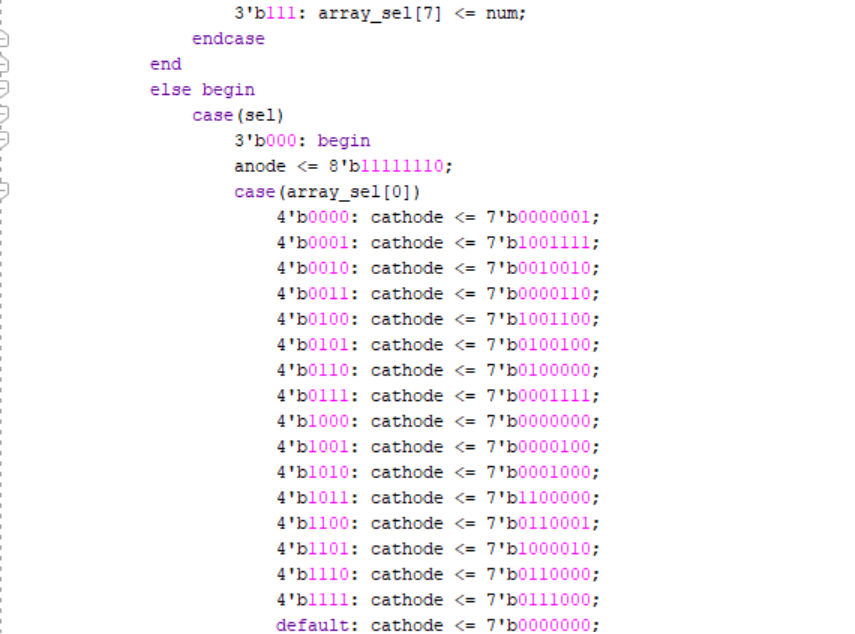
Following is the hold time report for implementation report:

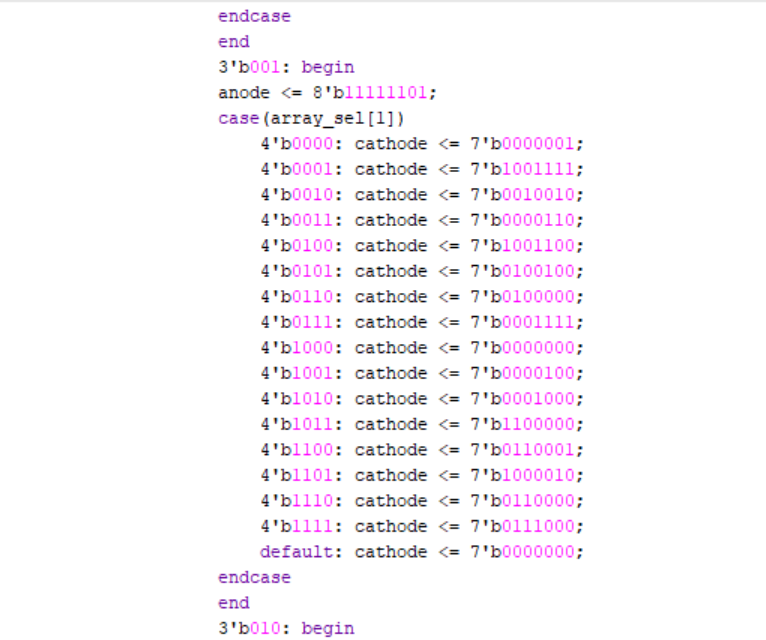


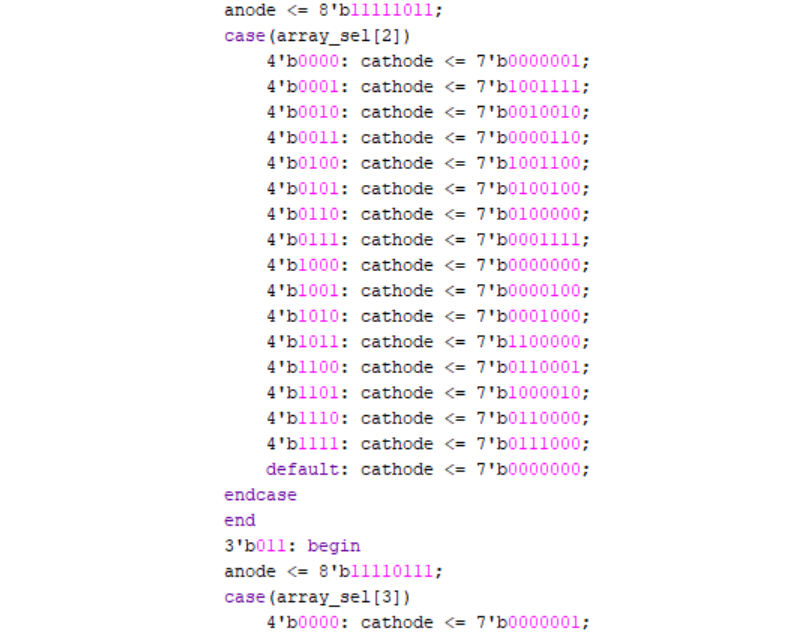
Codes for the LAB:

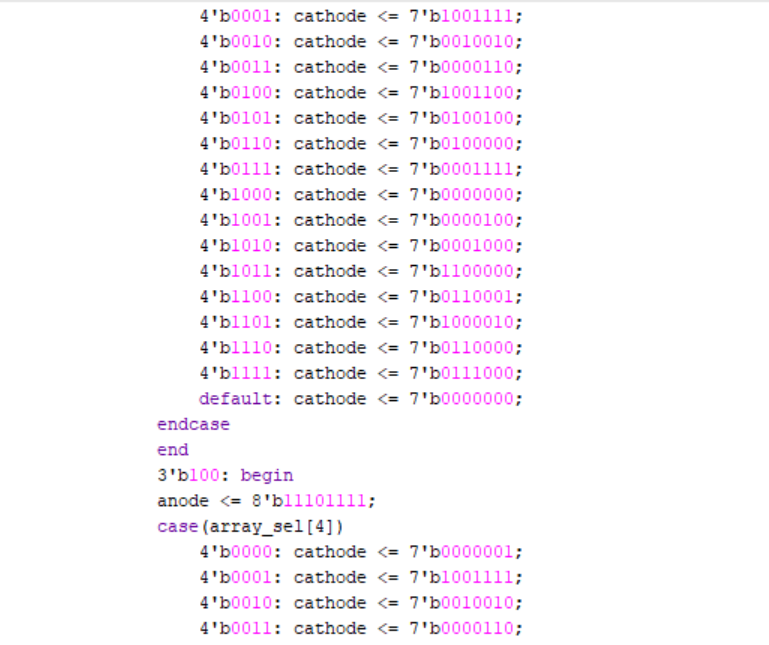
Following is the source code:

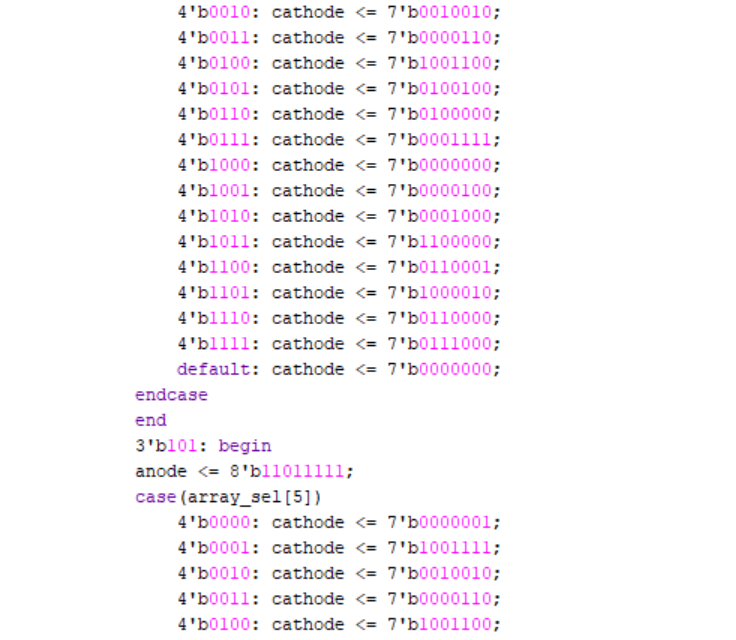


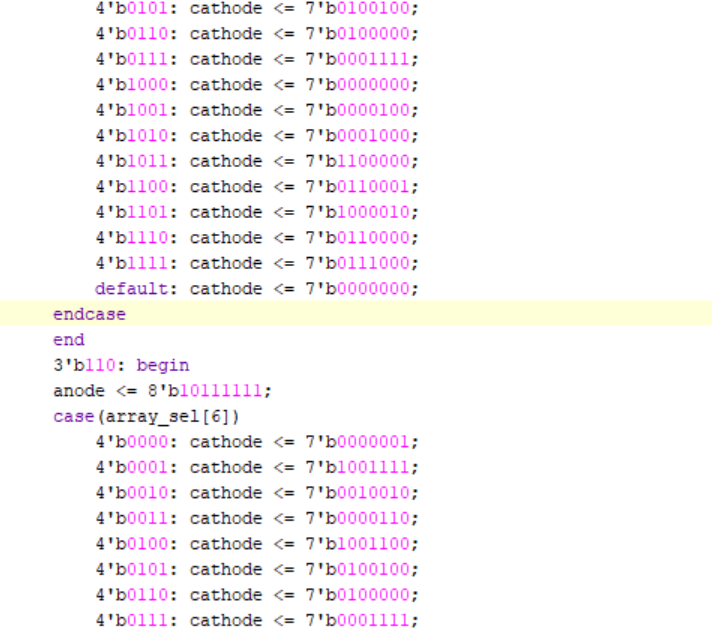


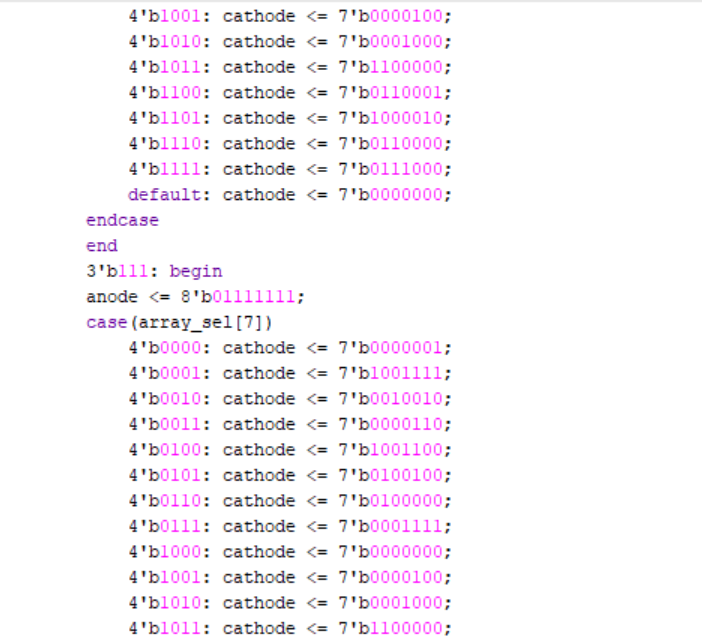


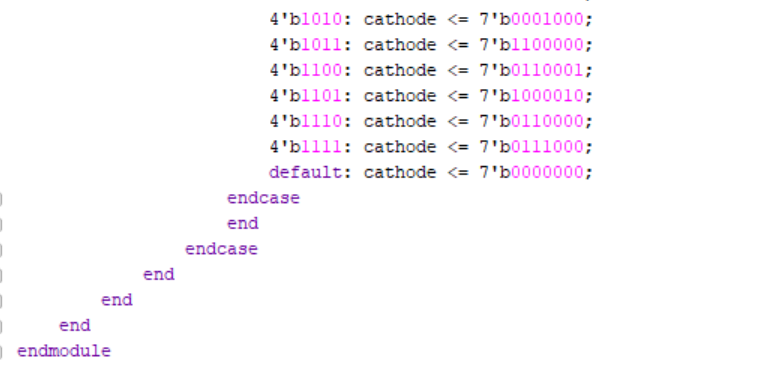




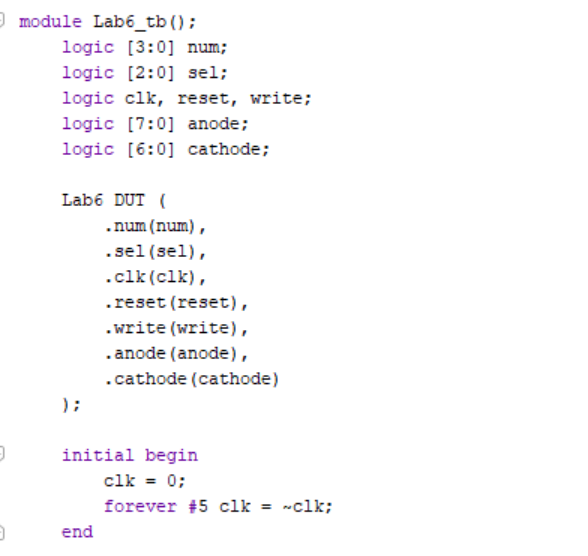


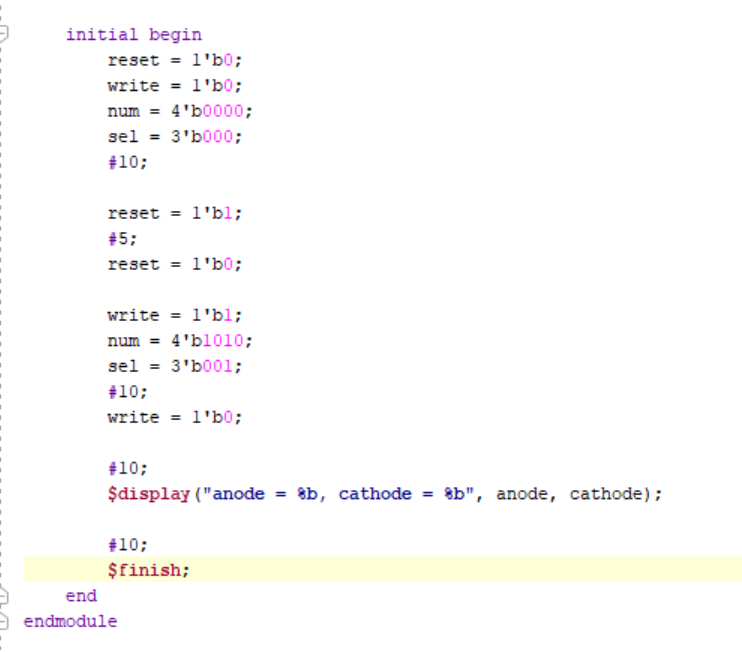






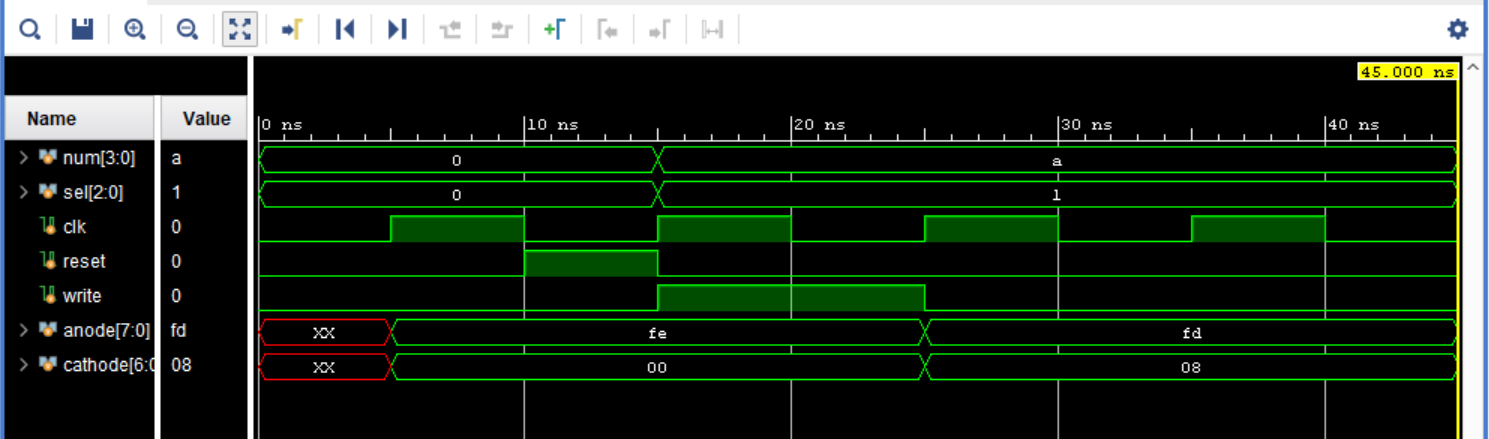
Following is the test bench code:





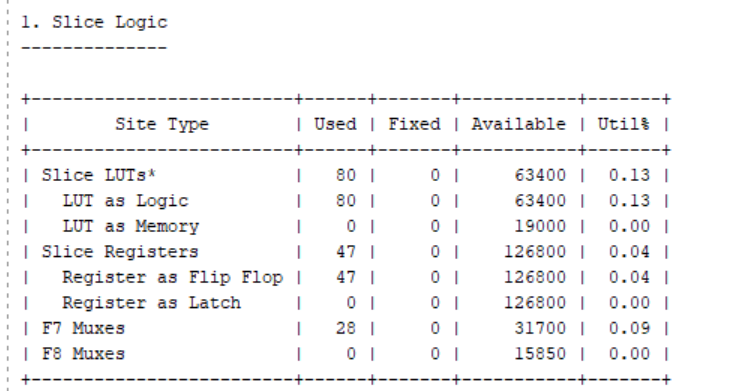
Simulation results:

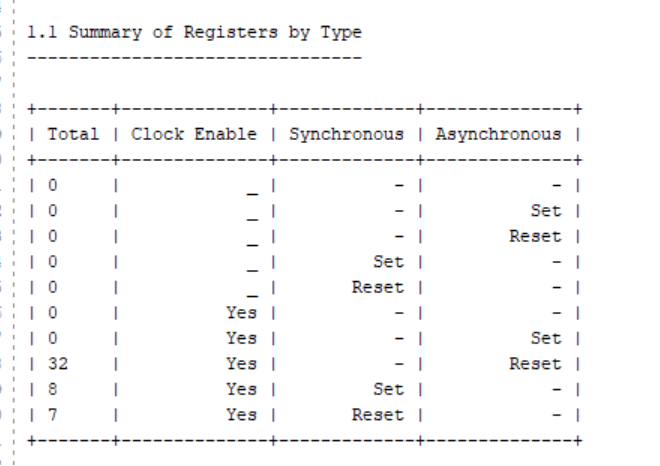
Following are the simulation results:

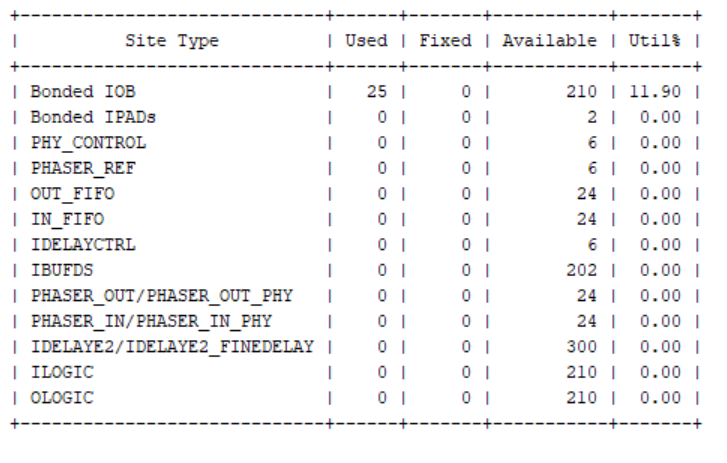


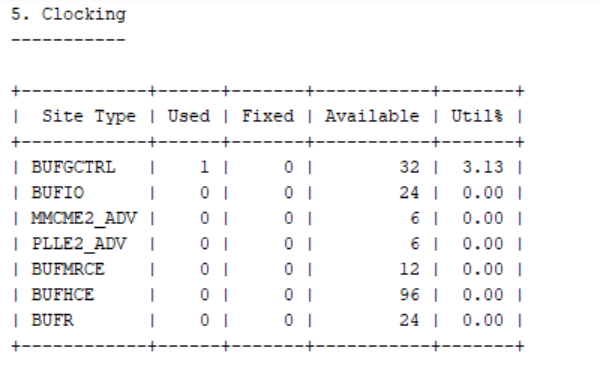
Resources utilization:

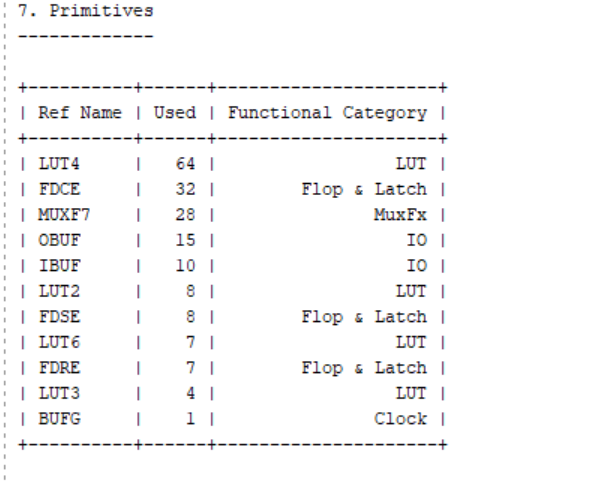
Following are the resource utilization:

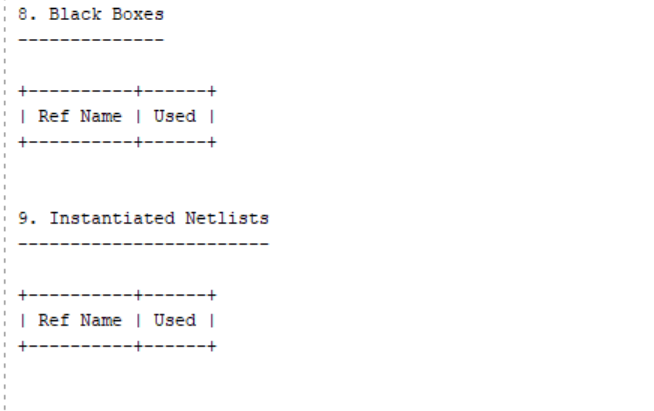












Power summary:

Following is the power summary:

