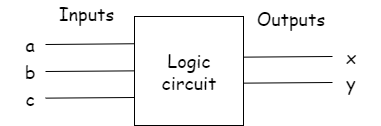
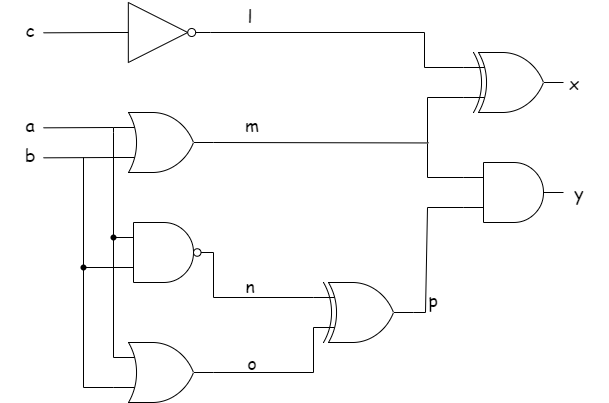
Structural diagram:



Logic circuit:



Circuit equations:

Truth table:

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | |  | | | | | **Outputs** | |
| **a** | **b** | **c** | **l** | **m** | **n** | **o** | **p** | **x** | **y** |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

Errors found in code (Task 2):

Listing 4 errors:

1. In line no. 6, there was a “,” after “carry”.
2. The given code didn’t had “assign” before sum in line no 8.
3. And there should be an & sign in line#10 after “c”.

Listing 5 errors:

1. There should be a “logic carry1” in line#6.
2. In line#7, there should be a DUT name.
3. Line#18 should have a1, b1, c1.
4. Line#20 should have c1 instead of c.
5. Also, there should be an increase in the time in the previous value of time so that time limit increases.
6. Line#24 should have b1 instead of b.
7. Line#30 should have a1 instead of a
8. In line before the “endmodule”, we have to write “end” so that we can end the execution.