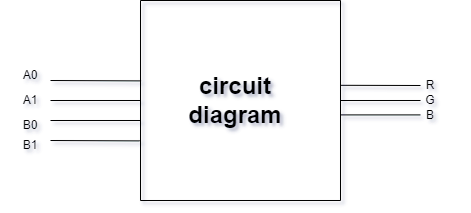
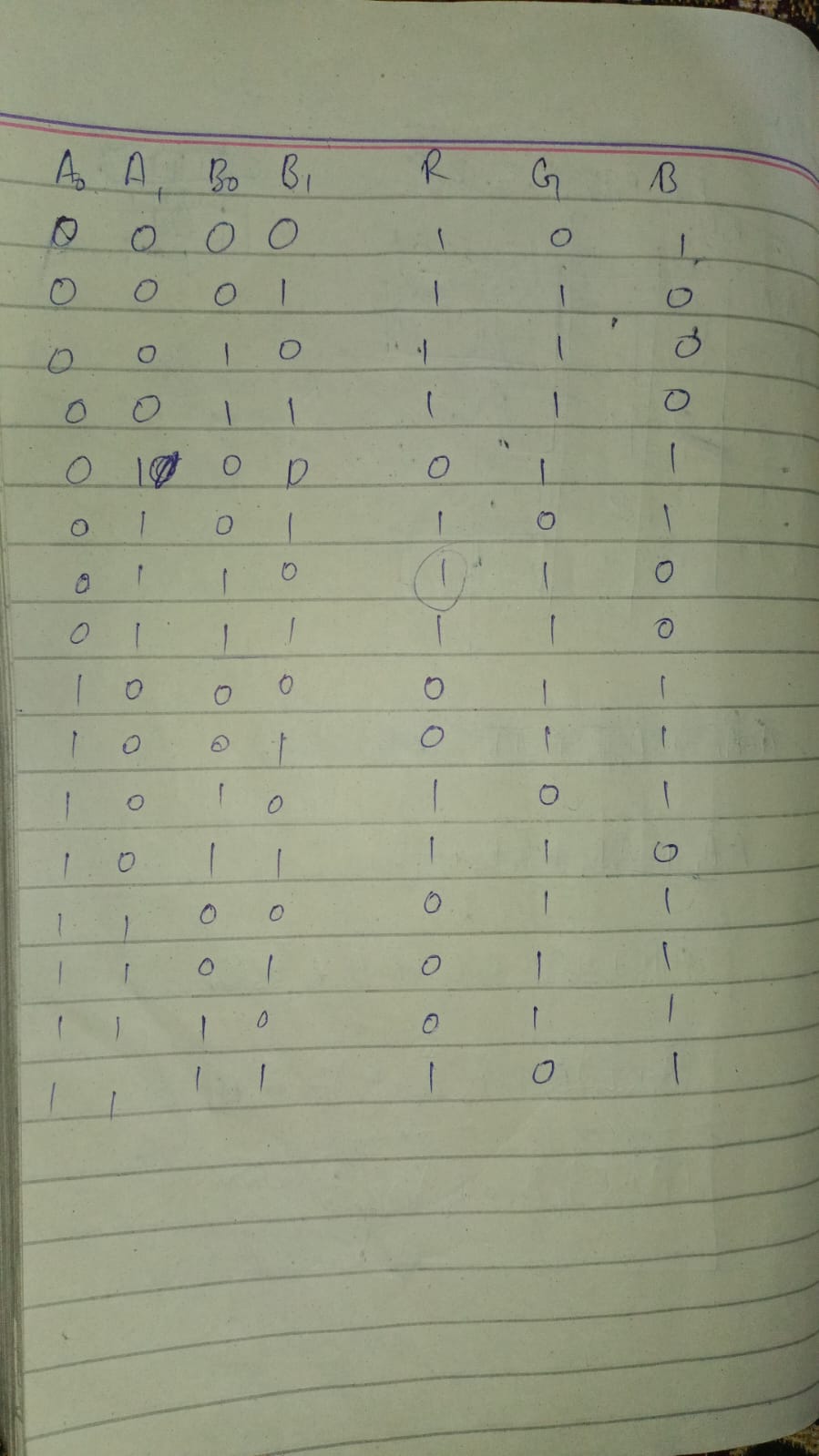
LAB # 4(Report)

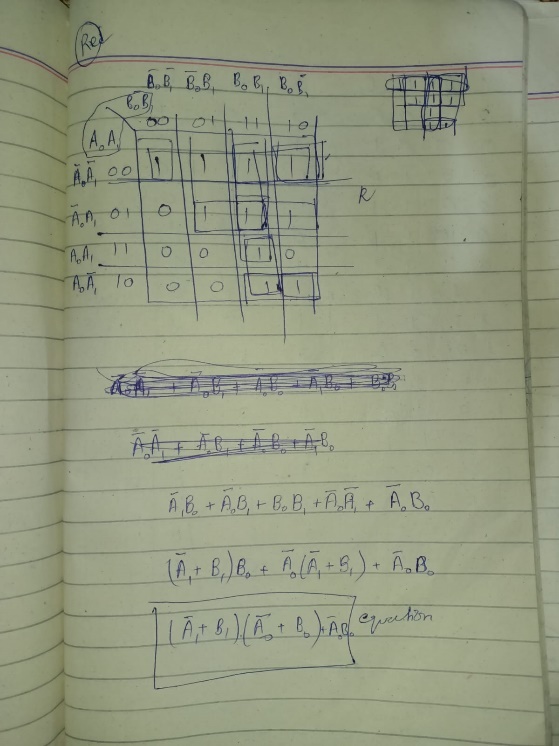
Circuit I/O:

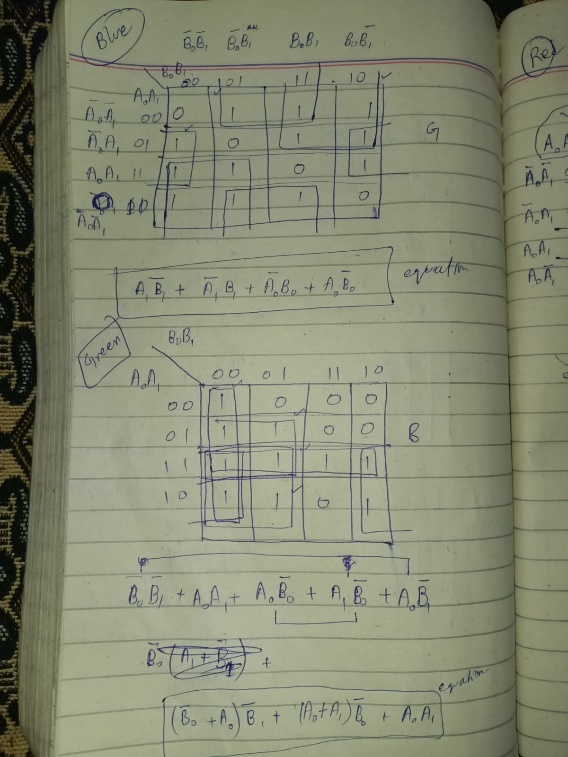


Truth Table:



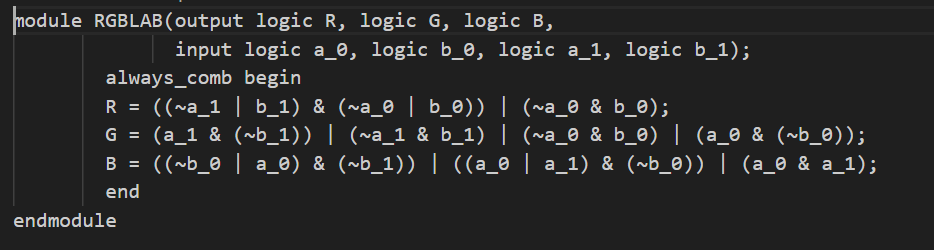
K-Maps:



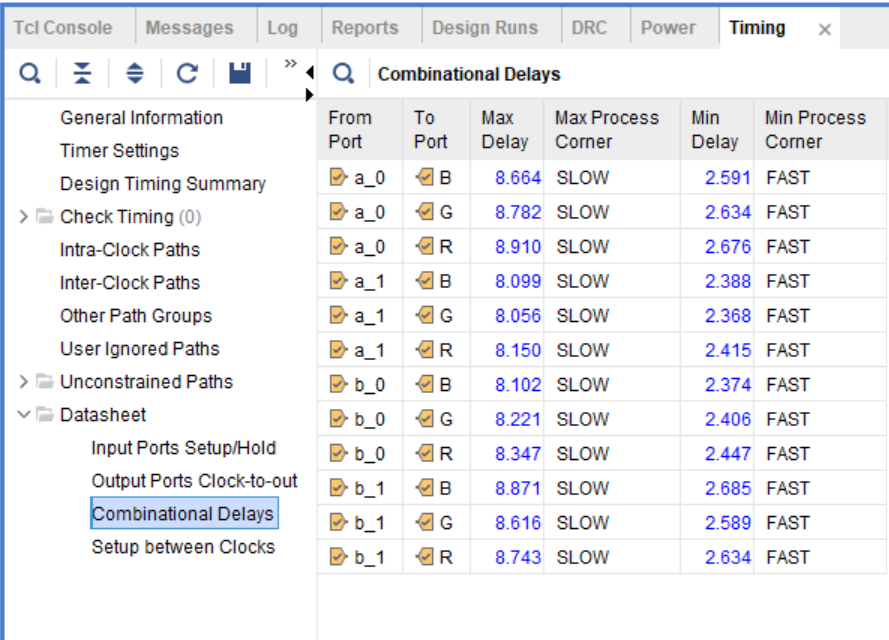


So, these are the three K-maps and their equations.

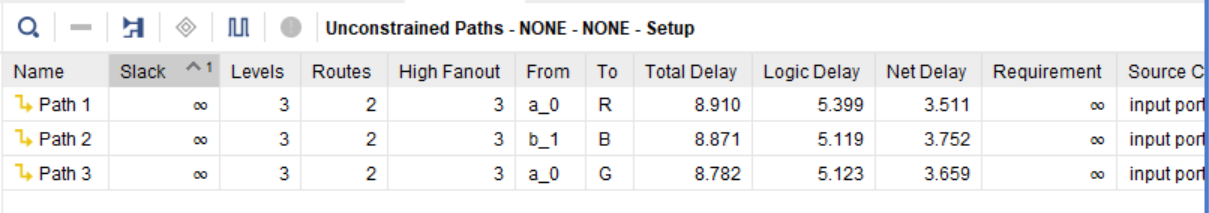
Structural Modeling (.sv file):

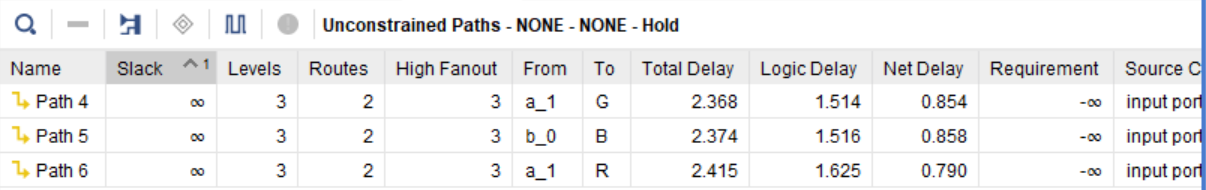


Combinational delays:



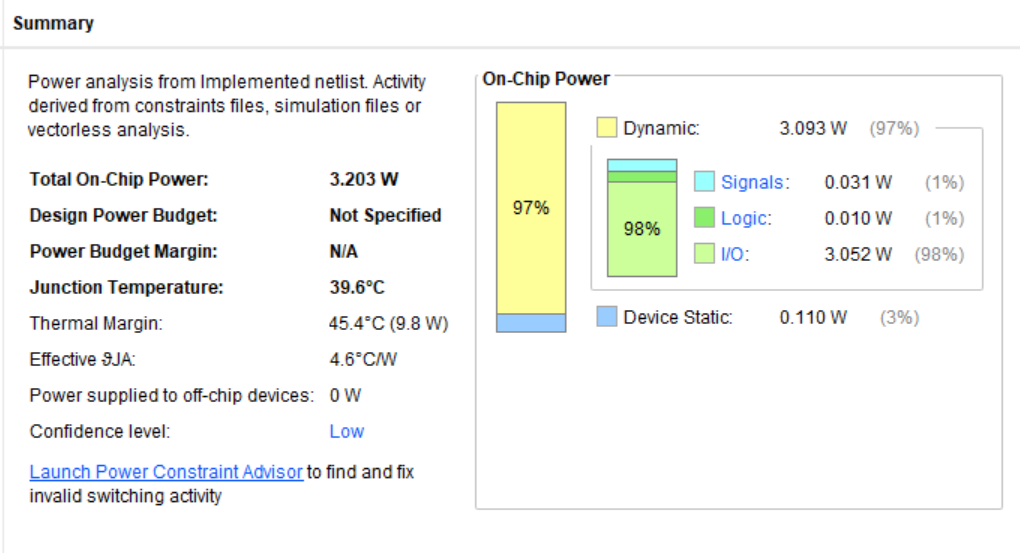
Propagational delay is 8.910ns from a\_0 to R and Conteminational delay is 2.685ns from b\_1 to B.



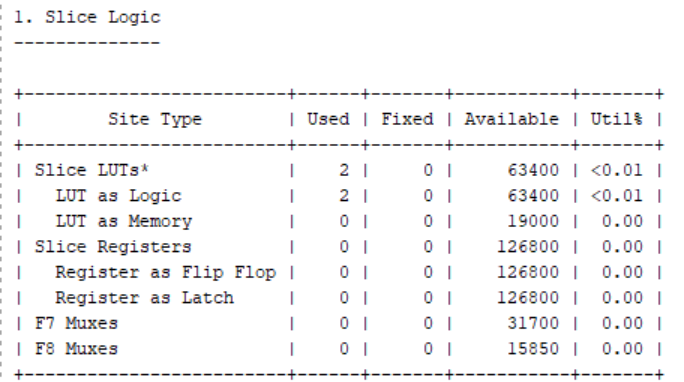


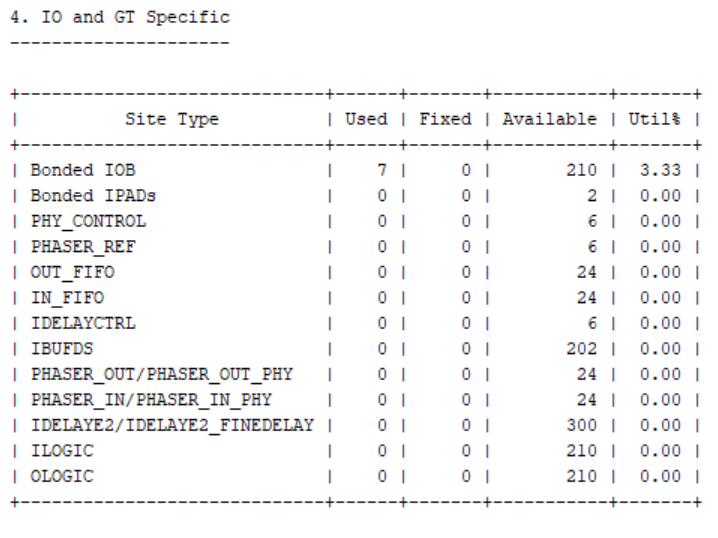
Power consumption:

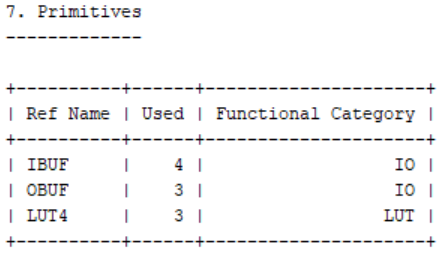
Here is some power consumption summary:

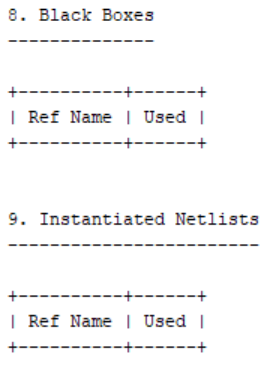


Resource utilization:



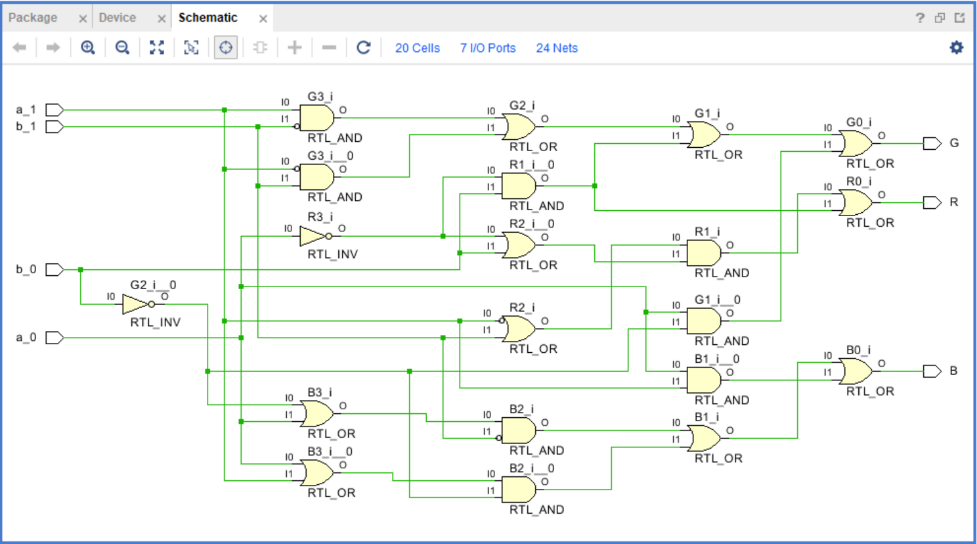






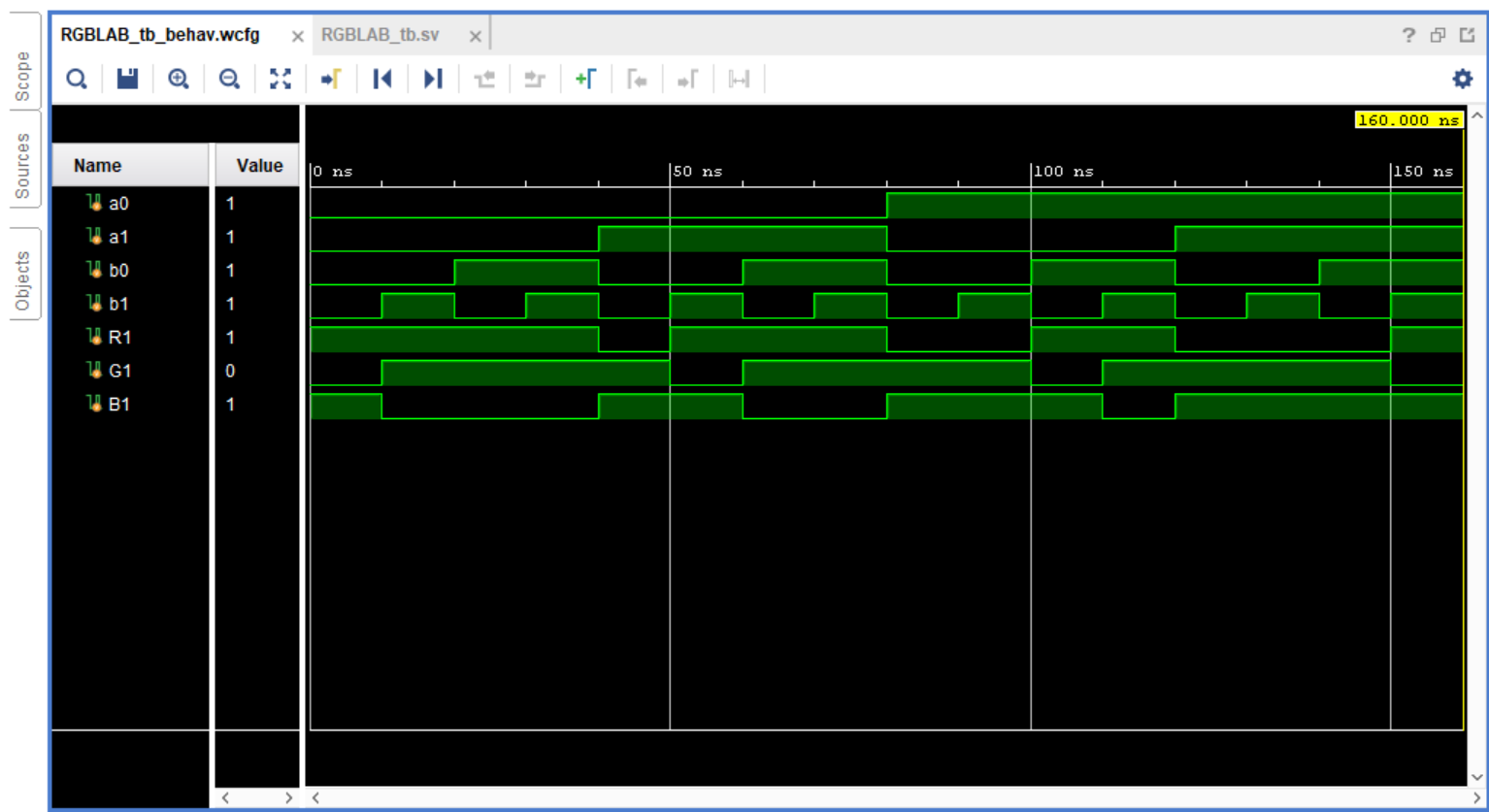
Here, two LUT slice logics, 7 Bonded IOB, 4 IBUF, 3 OBUF, 3 LUT4… have been used.

Circuit Diagram:



So, this is the circuit diagram.

Simulation Results:



Here is our simulation result.