SRAM Project Report

Digital VLSI Design

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OBJECTIVE

Design and Simulation of 8×8 SRAM Array Using 6T Cell in Cadence.

ANALYSIS

6T SRAM Cell Design

The 6T SRAM cell is composed of: two pull-up PMOS transistors (P1, P2), two pull-down NMOS transistors (N1, N2) and two access NMOS transistors (N3, N4) connected to the wordline (WL)

The pull-up and pull-down transistors form two cross-coupled inverters, creating a bistable storage element. The access transistors connect the internal storage nodes (Q and $\overline{Q}$) to the differential bitlines (BL and BLB) when the wordline (WL) is asserted.

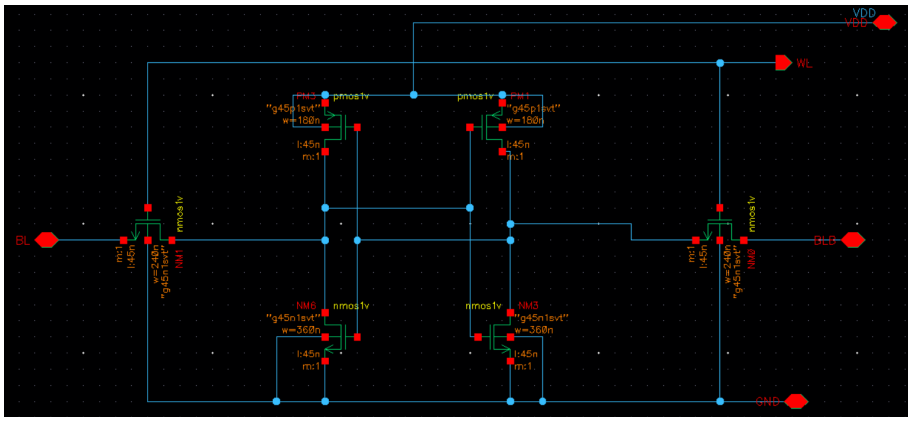
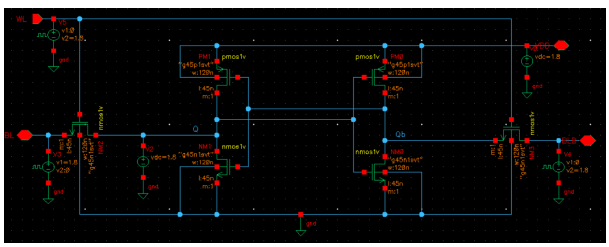


Figure 1: 6T SRAM Cell

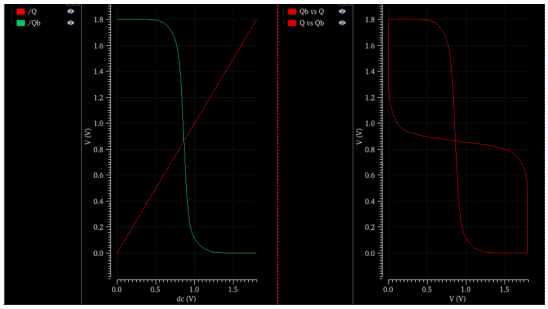
Butterfly Curve

The stability of a 6T SRAM cell is evaluated using the **butterfly curve**, which graphically represents the voltage transfer characteristics (VTC) of the two cross-coupled inverters inside the cell.

The butterfly curve is generated by plotting the VTC of one inverter against the mirrored VTC of the other inverter.



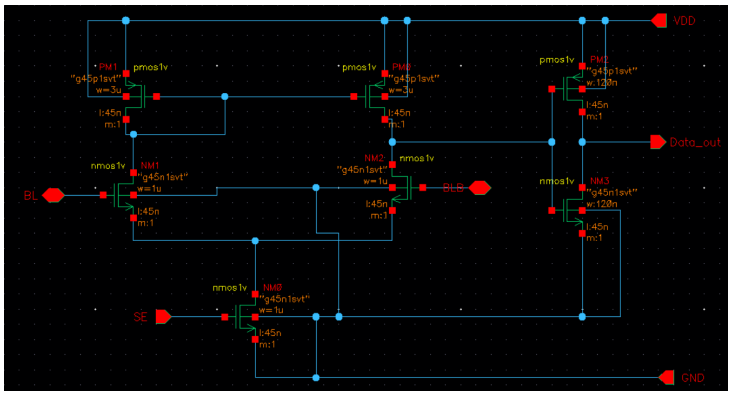
(a) Fig 2a: 6T SRAM Test



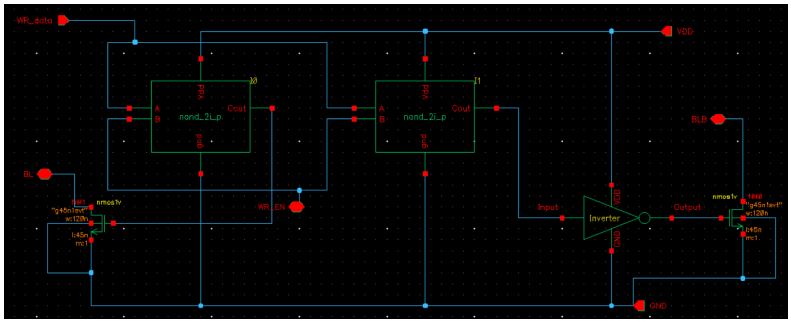
(b) Fig 2b: Butterfly Curve

Sense Amplifier and Write circuit

The sense amplifier is used to detect the small voltage difference that develops on the differential bitlines (BL and BLB) during a read operation.
The write driver circuit forces the bitlines to the desired logic levels during a write operation.



(a) Fig 3a:Sense Amplifier



(b) Fig 3b:Write Operation Circuit

Precharge Circuit

Before every read operation, the bitlines (BL and BLB) must be precharged to a known voltage level, typically V_{DD}.

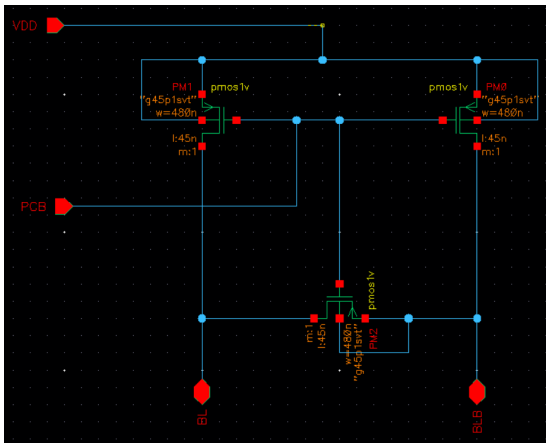


Figure 4: Precharge Circuit

3x8 Decoder

Row and column 3×8 decoders are used to uniquely select one wordline and one bitline pair from the 8×8 memory array, enabling efficient addressing using only three address bits for each dimension.

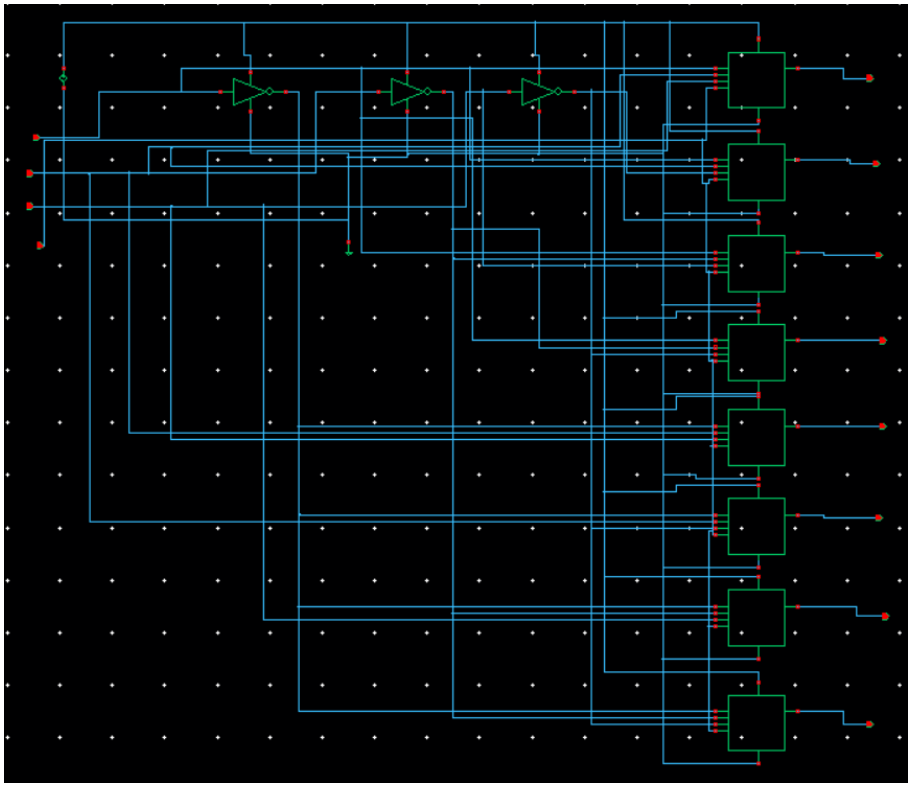


Figure 5: 3x8 Decoder Circuit

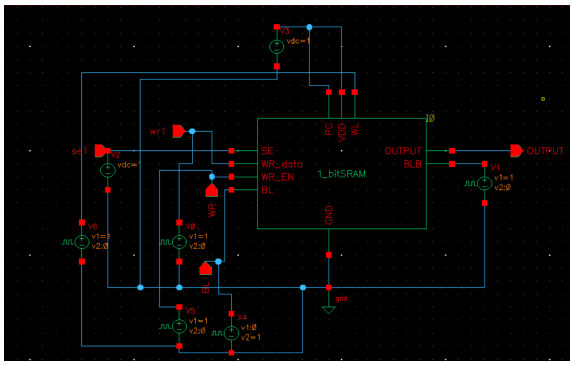
Transistor Sizing

Circuit	Cell	Width
SRAM	N(cell)	360nm
	P(cell)	180nm
	N(access)	240nm
Sense amplifier	pmos	3um
	nmos	1um
Precharge	pmos	480nm
Write Operation	nmos	120nm
	pmos	120nm
Decoder 3x8	nmos	120nm
	pmos	120nm

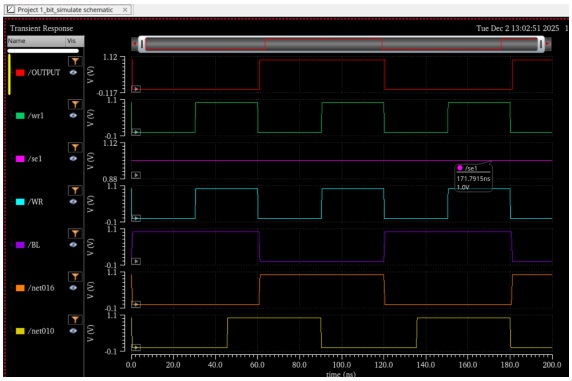
Table 1: Transistor Sizing

SIMULATION

1 Bit SRAM Cell



(a) Fig 6a:1 Bit SRAM Cell



(b) Fig 6b:1 Bit SRAM output

8x8 SRAM Cell

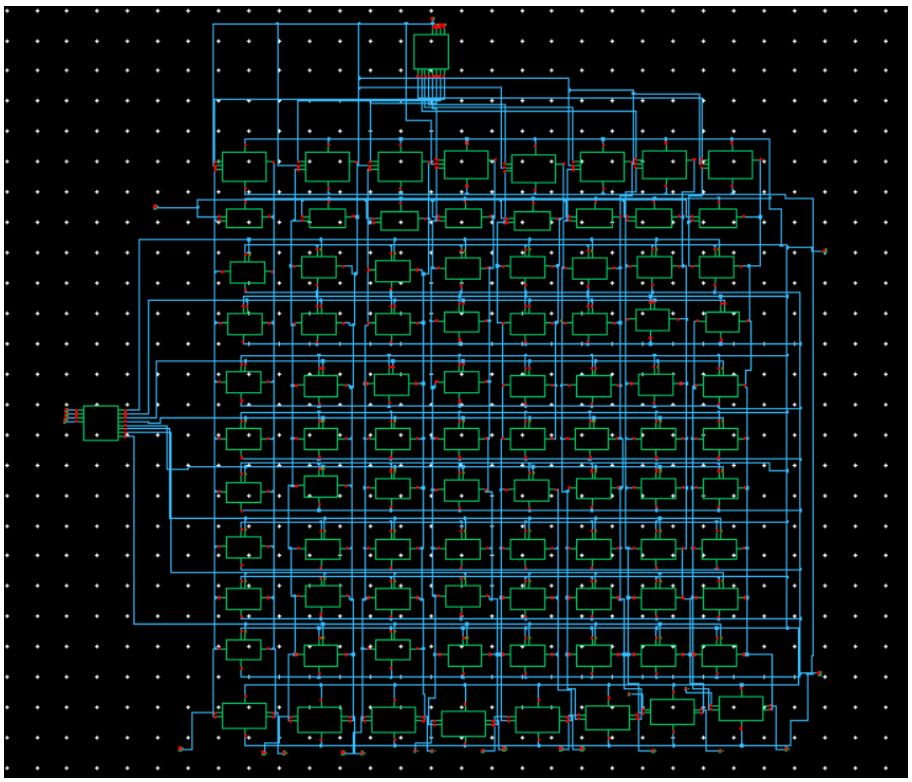


Figure 7: 8x8 SRAM Design

8x8 SRAM Cell OUTPUT

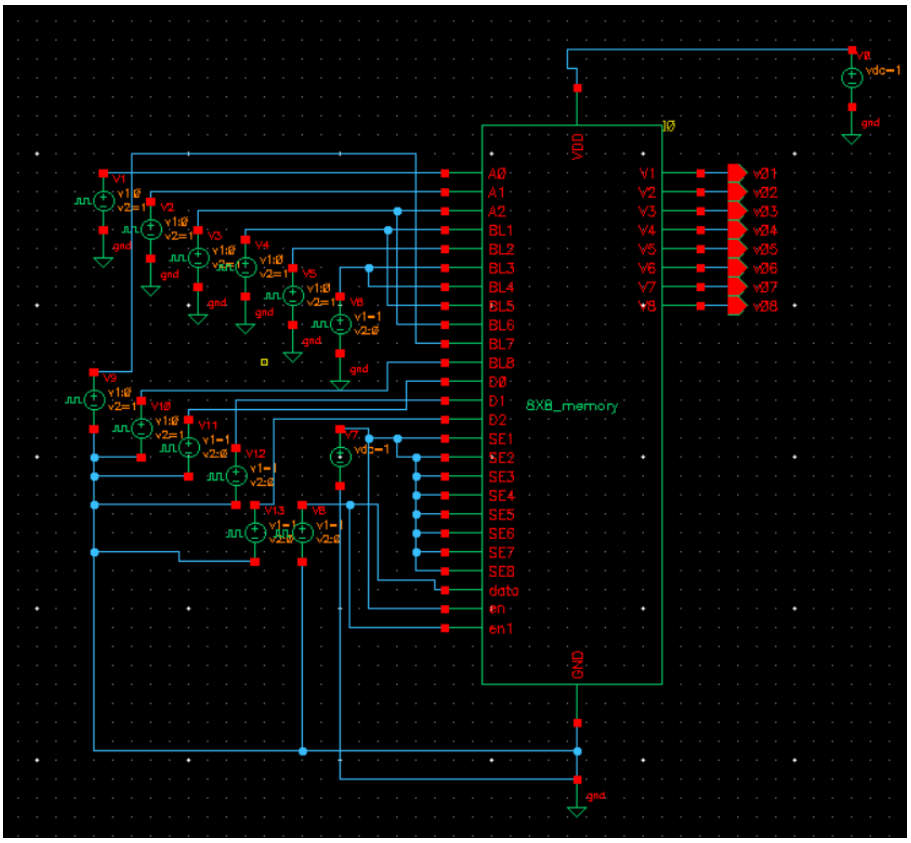


Figure 8: 8x8 SRAM Cellview

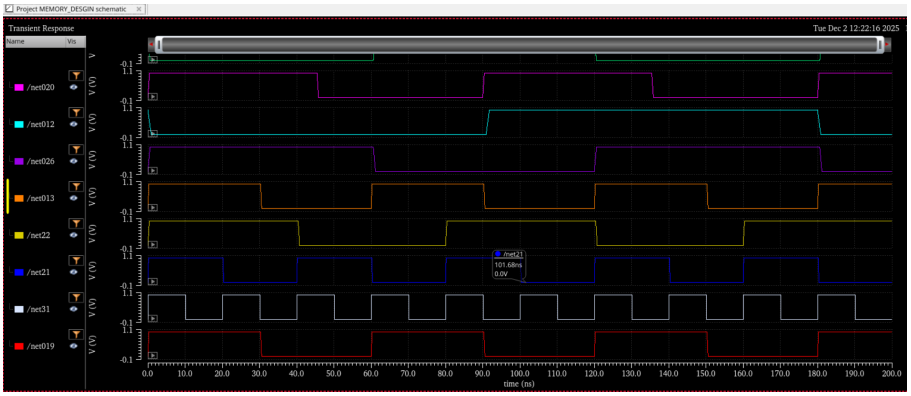


Figure 9: 8x8 SRAM Input Signal

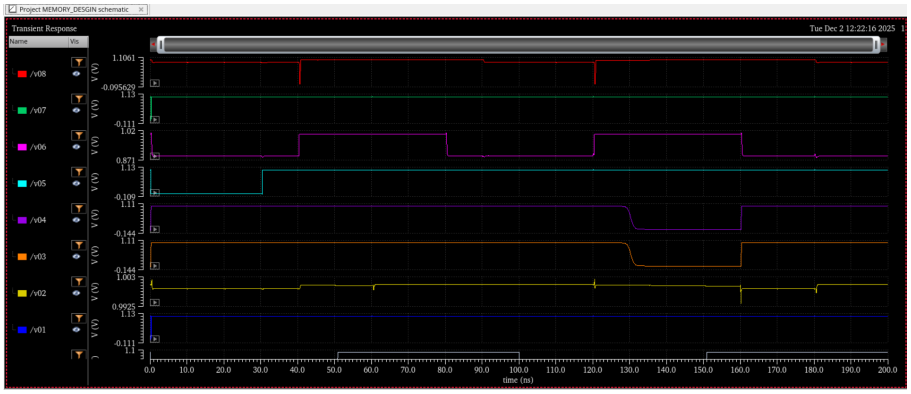


Figure 10: 8x8 SRAM OUTPUT

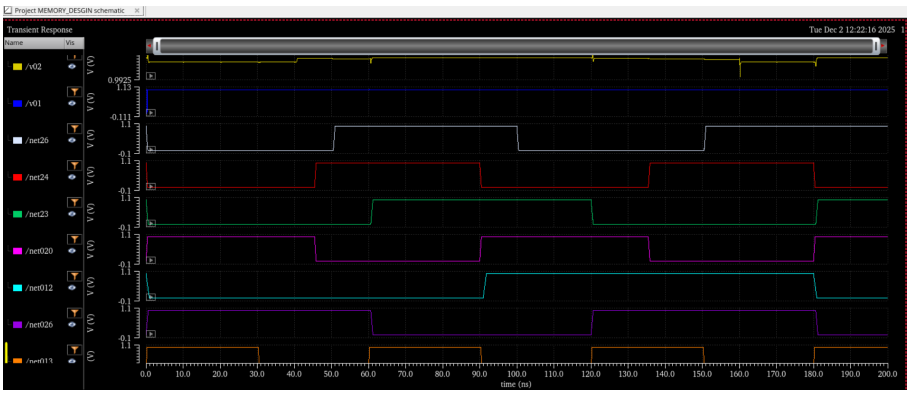


Figure 11: 8x8 SRAM OUTPUT

RESULTS

Read and Write Timing Analysis

- . During the **write operation**, the write driver forces the BL and BLB lines to the required logic levels, and when the wordline (WL) is asserted high, the access transistors turn on, allowing the internal node voltages to switch to the new stored value. The waveform shows that the cell successfully overwrites its previous state within the specified access time

- For the **read operation**, both BL and BLB are first precharged to V_{DD}. When the WL goes high, the cell is connected to the bitlines, causing a small differential voltage to develop depending on the stored data. The sense amplifier quickly amplifies it to a full logic level. The waveforms confirm that the sense amplifier triggers only after the bitline differential is established, ensuring a stable and accurate read.

- The internal storage nodes remain unchanged during the read operation, indicating that the design does not suffer from read disturbance.

CONCLUSION

- SRAM memory with an operating voltage of 1.8 V and an access time of less than 2.5 ns is designed.
- The standard 1-bit 6T SRAM cell consists of six transistors, including a pair of cross-coupled CMOS inverters and two NMOS access transistors (M5, M6). The NMOS transistors (M2, M4) act as the driver transistors, while the PMOS transistors (M1, M3) function as the pull-up devices.
- The area of the memory can be optimized by reducing the number of cells or by replacing multiple functional cells with a single, multifunctional cell.
- Based on the results, the proposed design can be used for a low-leakage SRAM cell with improved stability, while incurring only a slight area overhead. This area increase is acceptable in applications that require tight stability constraints and extended battery life.