Design and Simulation of a 4-Input Comparator using Cadence Virtuoso

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August 6, 2025

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Abstract

This project presents the complete design, verification, and simulation flow of a 4-input comparator using the Cadence Virtuoso platform. The design process began with schematic creation and initial functional verification through transient simulations. Once validated, the corresponding layout was implemented following design best practices. Design Rule Check (DRC) was performed to ensure layout compliance with foundry rules, followed by Layout Versus Schematic (LVS) checks to verify structural consistency between the schematic and layout. Parasitic extraction was then carried out using Assura RCX to generate an average extracted view of the layout, which was subsequently used for post-layout simulation. Finally, proper input and output pad connections were integrated to prepare the design for practical interfacing and characterization. The successful completion of all stages confirms the functional correctness, reliability, and readiness of the comparator design for further integration.

Keywords

Comparator,symbol, Schematic, Layout,DRC, LVS,RCX

Introduction

Magnitude comparator is a type of Combinational circuit, It Basically compares two binary numbers and determines their relative magnitude. It gives output whether one number is greater than the other, or less than or equal. These comparators are used in digital systems, such as for sorting networks, and decision-making circuits to handle numerical comparisons perfectly without any error.

4-Bit Magnitude Comparator

A comparator used to compare two binary numbers each of four bits is called a 4-bit magnitude comparator. It consists of eight inputs each for two four-bit numbers and three outputs to generate less than, equal to, and greater than between two binary numbers.

Table 1: Representative Truth Table of a 4-bit Comparator

A (Decimal)	**B (Decimal)**	$A = B$	$A > B$	$A < B$
0	0	1	0	0
3	5	0	0	1
7	2	0	1	0
9	9	1	0	0
12	15	0	0	1
15	12	0	1	0
8	8	1	0	0
1	14	0	0	1
14	1	0	1	0

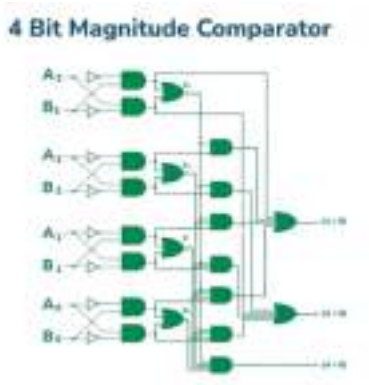


Figure 1: Circuit diagram of the 4-input comparator

Methodology

The methodology of this project followed a bottom-up design approach using the Cadence Virtuoso environment. To implement a 4-input comparator, the process began by designing the fundamental building blocks individually. These included basic logic gates such as an inverter, 2-input AND gate, 3-input AND gate, 4-input AND gate, 2-input OR gate, and 4-input OR gate. Each of these components was first constructed at the schematic level to ensure functional correctness.

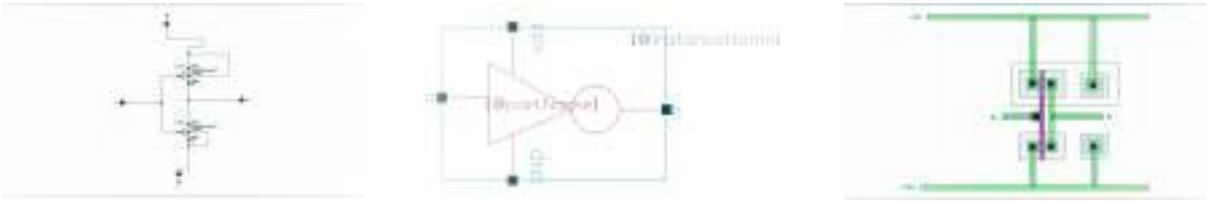
For every schematic created, a corresponding symbol was generated. This modular approach enabled easier hierarchical design when integrating the blocks into the full comparator circuit. After symbol creation, layouts were designed for each individual gate. Layout design followed best practices to match the schematic using appropriate design rules, and each layout was verified against its schematic using Layout Versus Schematic (LVS) checks.

Once all the basic components were completed and verified, they were integrated to form the full comparator. At the schematic level, the comparator was constructed by combining the previously created symbols, effectively representing the logic of a 4-input comparator. Similarly, the layout of the full comparator was assembled by placing and connecting the layouts of the individual components.

After the final schematic and layout were completed, several verification steps were carried out. Design Rule Check (DRC) ensured that the layout adhered to the fabrication constraints. LVS verified that the layout structurally matched the schematic. Parasitic extraction using Assura RCX was performed to generate an average extracted view of the design, capturing realistic resistance and capacitance effects. Finally, post-layout simulations were conducted using the extracted view to validate the circuit's behavior, and input-output pads were added to prepare the design for practical interfacing.

Schematic and Layout Design

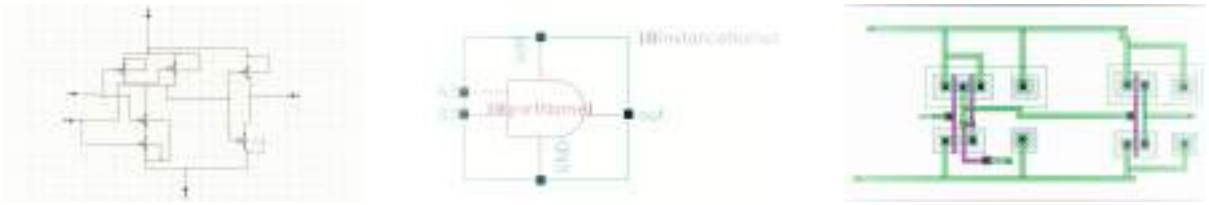
Inverter



(a) Inverter Schematic (b) Inverter Symbol (c) Inverter Layout

Figure 2: Inverter Design Steps

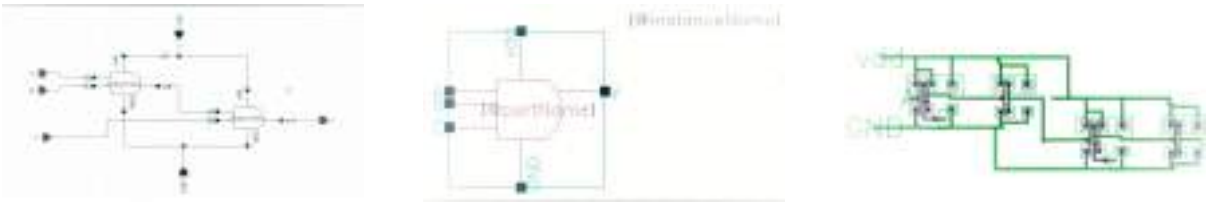
2-input AND Gate



(a) 2-input AND Schematic (b) 2-input AND Symbol (c) 2-input AND Layout

Figure 3: 2-input AND Gate Design

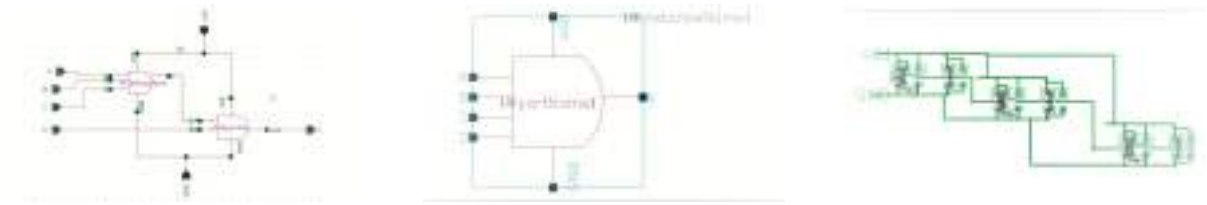
3-input AND Gate



(a) 3-input AND Schematic (b) 3-input AND Symbol (c) 3-input AND Layout

Figure 4: 3-input AND Gate Design

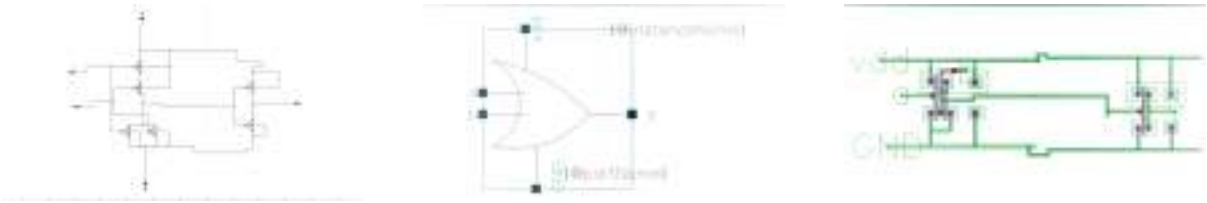
4-input AND Gate



(a) 4-input AND Schematic (b) 4-input AND Symbol (c) 4-input AND Layout

Figure 5: 4-input AND Gate Design

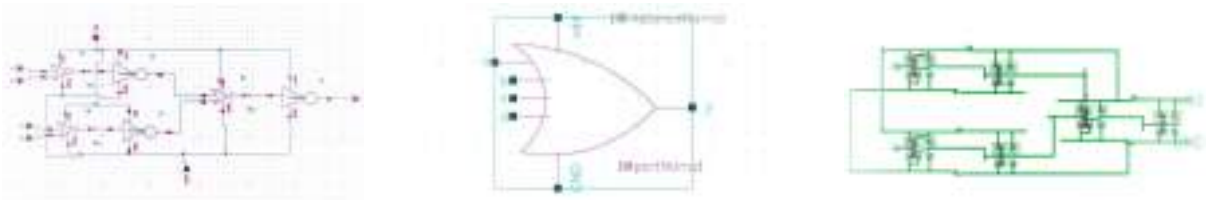
2-input OR Gate



(a) 2-input OR Schematic (b) 2-input OR Symbol (c) 2-input OR Layout

Figure 6: 2-input OR Gate Design

4-input OR Gate



(a) 4-input OR Schematic (b) 4-input OR Symbol (c) 4-input OR Layout

Figure 7: 4-input OR Gate Design

Final 4 Bit Comperator

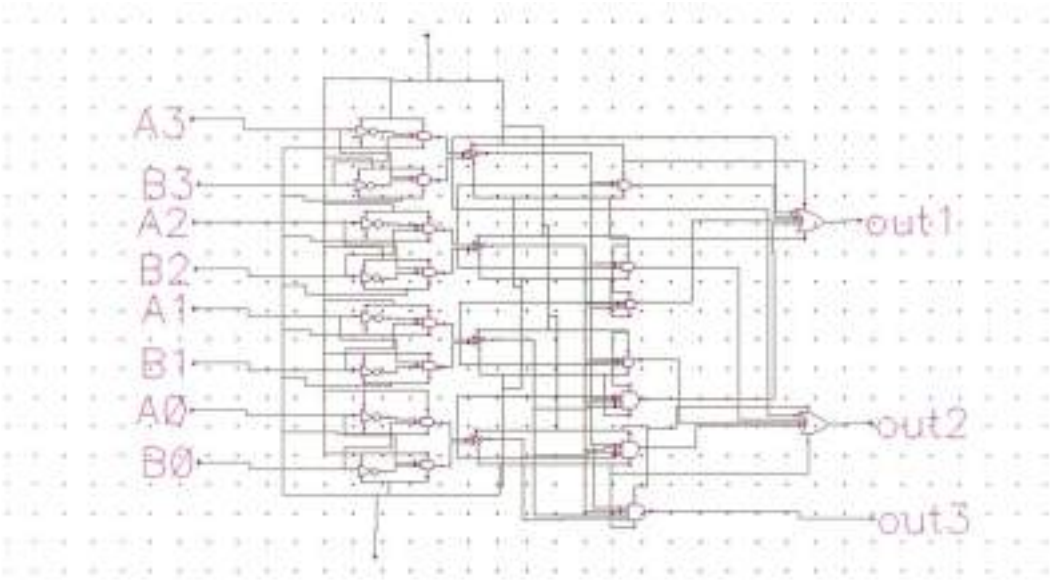


Figure 8: 4-bit Comparator Schematic

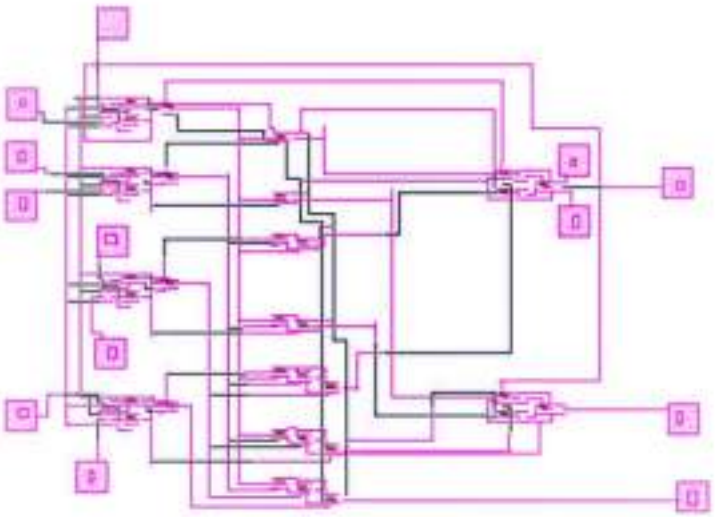


Figure 9: 4-bit Comparator Layout After Padding

Simulations & Results

This section presents the simulation results obtained from Cadence Virtuoso for the 4-bit comparator design. The input signal waveforms, output waveform, and ADE L environment are shown to validate the functionality of the circuit.

Figure 10: Input signal parameters for A0, A1, A2, and A3. These waveforms were applied during the schematic-level simulation.

Figure 11: Input signal parameters for B0, B1, B2, and B3. These signals were used to represent the 4-bit binary input B.

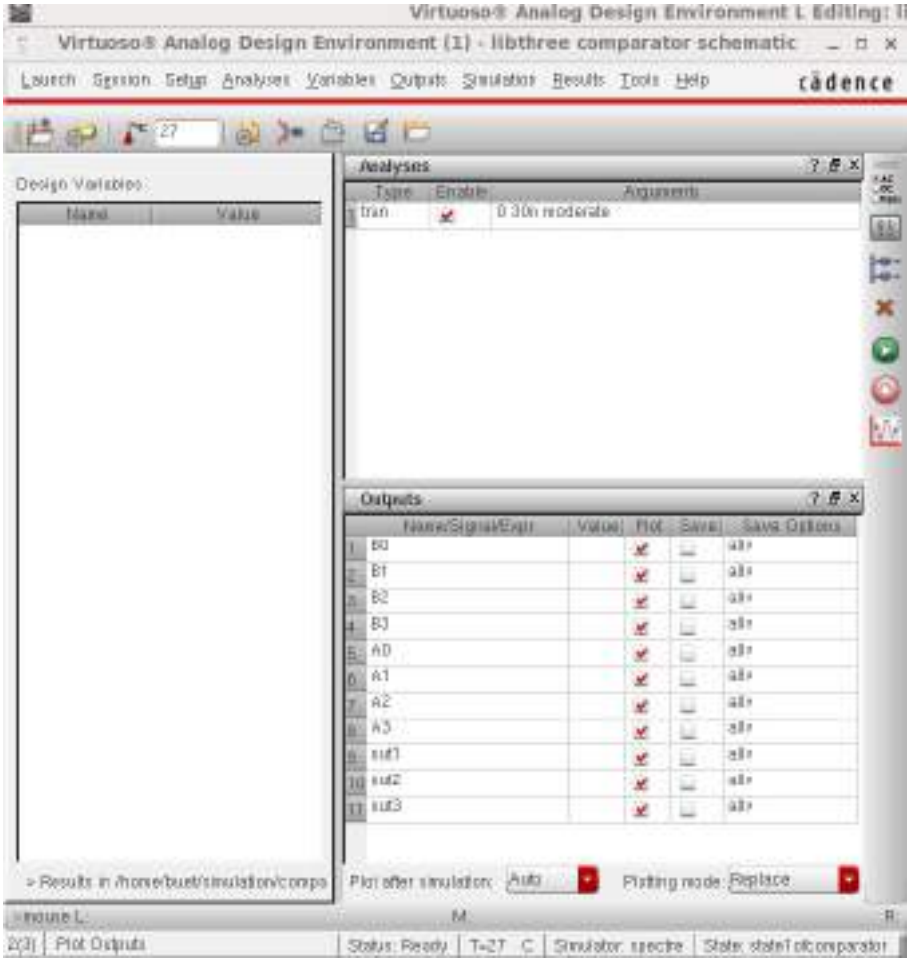


Figure 12: ADE L simulation setup used for schematic-level testing of the 4-input comparator in Cadence Virtuoso.

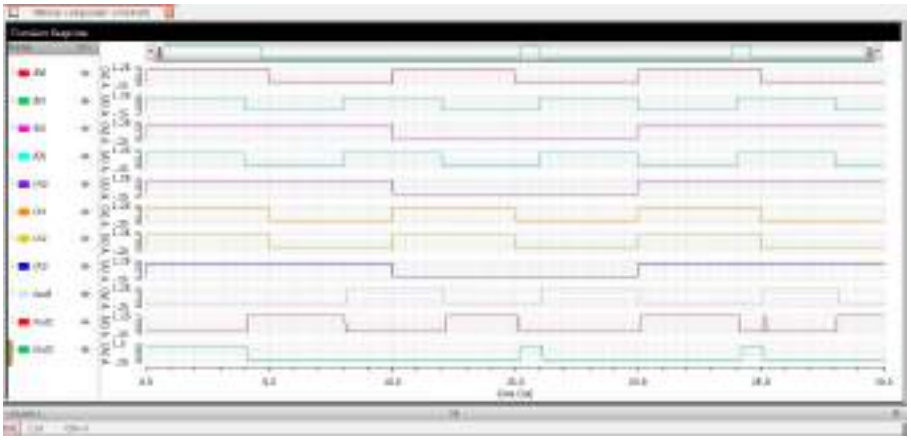


Figure 13: Output waveform of the 4-bit comparator schematic showing the comparison results

Post-Layout Results and Verification

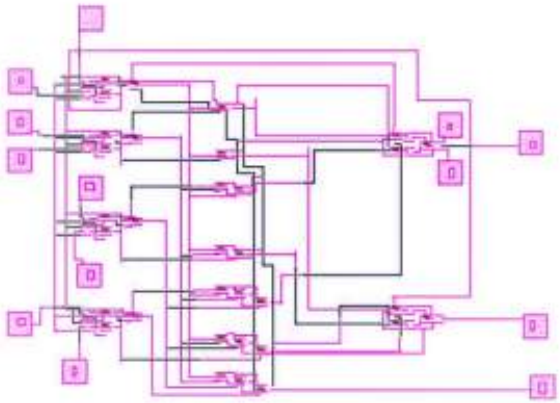


Figure 14: Final layout of the 4-bit comparator after layout padding, ready for physical verification.

DRC Test

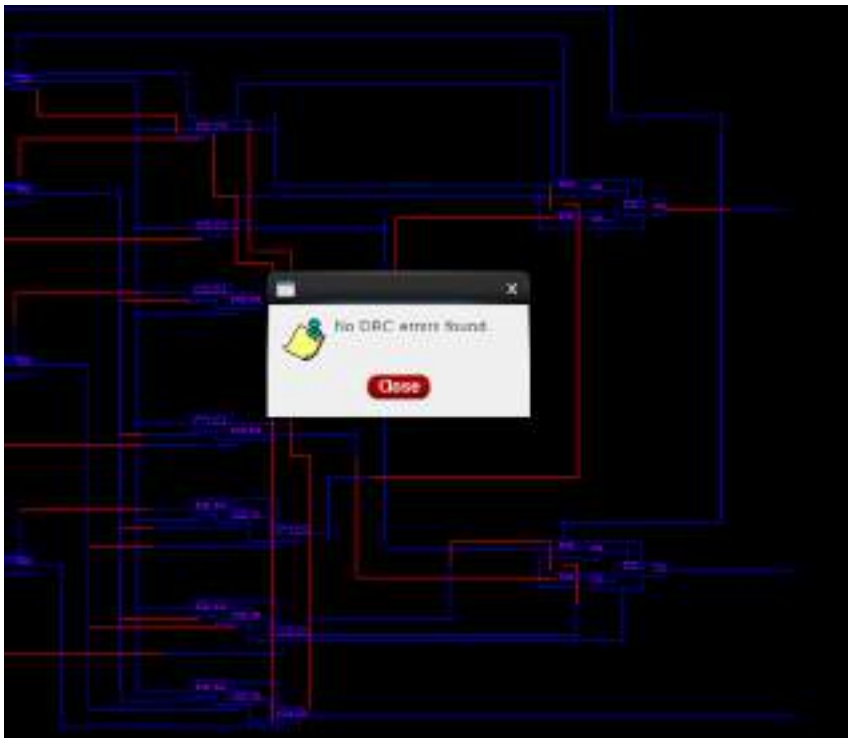


Figure 15: DRC check passed successfully with zero errors, ensuring design rule compliance.

LVS Test

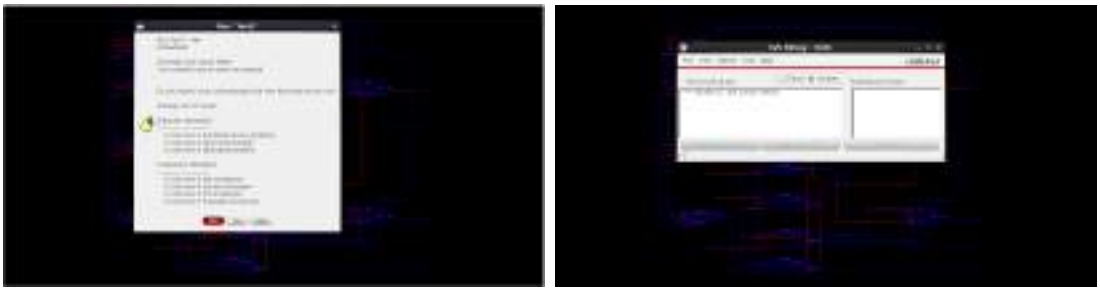


Figure 16: LVS report showing a successful match between the layout and schematic netlist.

RCX Test

Figure 17: RCX Interface in Cadence Virtuoso

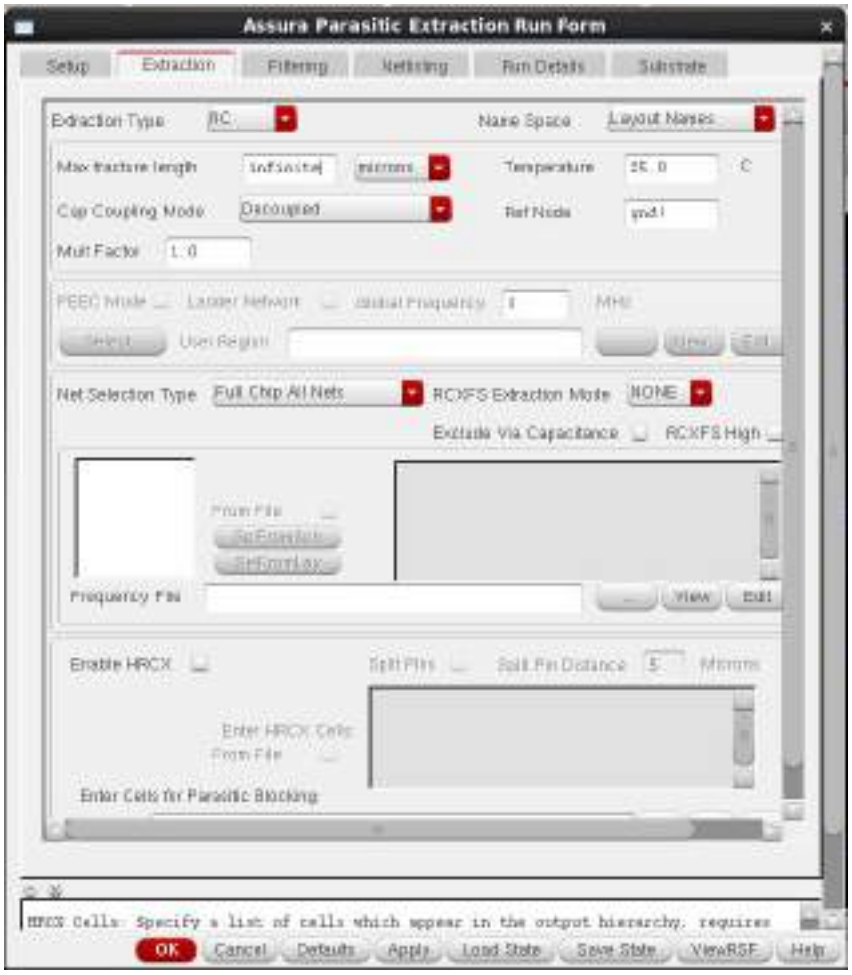


Figure 18: Assura RCX Parasitic Extraction Run Form

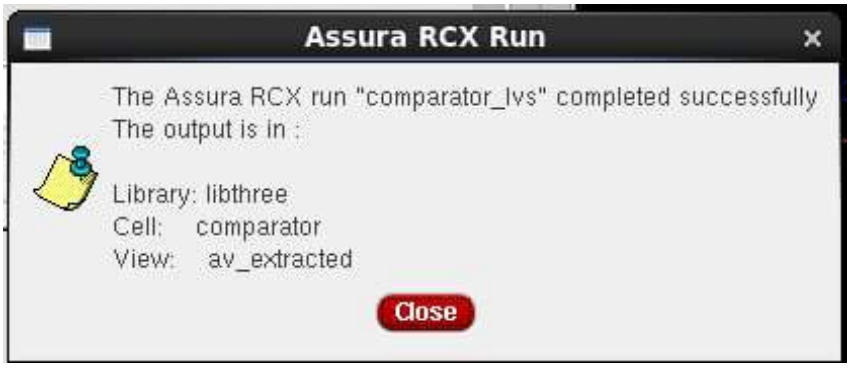


Figure 19: RCX Result Showing Successful Extraction

Average Extracted View

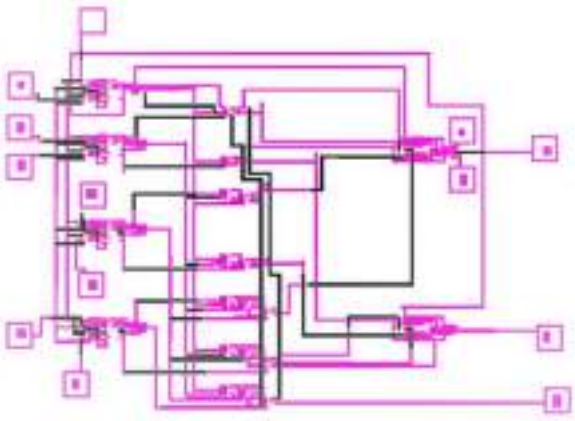


Figure 20: Average extracted view generated after RCX for post-layout simulation.

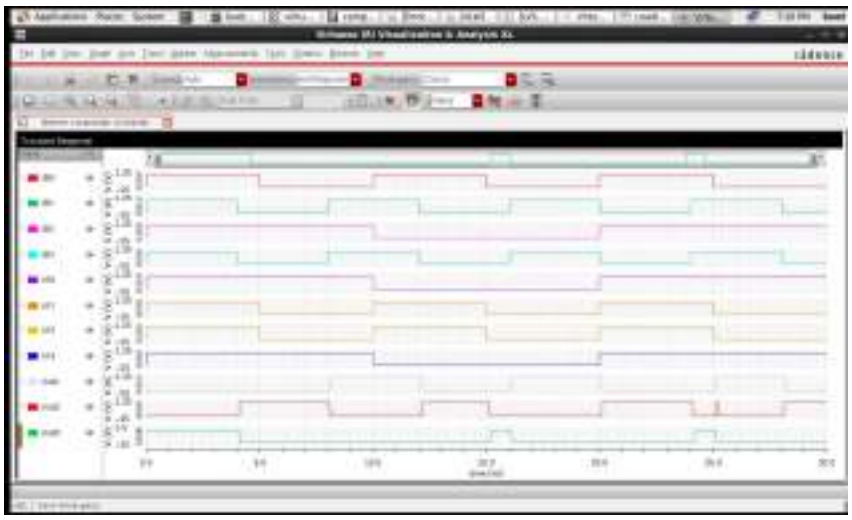


Figure 21: Post-layout simulation output showing accurate functionality with parasitic effects.

Conclusion

In this project, we successfully designed and implemented a 4-input comparator using Cadence Virtuoso. The design process involved schematic creation, symbol generation, and layout design, followed by functional verification through simulation. We analyzed the output waveforms, calculated propagation delay, and measured rise and fall times, all of which confirmed the correct functionality of the comparator.

Furthermore, we performed parasitic extraction using Assura RCX and verified the layout's integrity against the schematic. This step ensured that the post-layout netlist accurately reflected real-world parasitic effects, improving the reliability and performance estimation of the circuit.

Through this project, we gained valuable hands-on experience in full-custom VLSI design and verification workflows. The integration of schematic, layout, simulation, and

parasitic analysis helped us understand the practical challenges in analog and digital circuit design, as well as the importance of physical verification in modern VLSI systems.

References

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3. Lab Sheet 3: RCX Parasitic Extraction and LVS Verification. Available at: https://classroom.google.com/c/NzgyMjExMDIxMTA0/m/NzgyMjExMjI0MzQz/details