Contents

Abstract

This project focuses on designing the schematic of a 2-input AND gate, creating its symbol, and verifying its operation through simulation. The output waveforms confirm the correct logical behavior, where the output is high only when both inputs are high.The schematic accurately represents the logic operation of the AND gate, ensuring that the output is high only when both inputs are high.Simulation results are obtained to validate the expected logical behavior of the gate. The output waveforms clearly demonstrate the correct operation of the AND gate, showing precise transitions corresponding to the input conditions.

Keywords

Cadence Virtuoso, CMOS NAND Gate, 2-input NAND Gate, Schematic Design, Circuit Simulation, Universal Gate, nMOS Transistor, pMOS Transistor, Digital Logic.

Objective

1. To login in to the Cadence Server shell and start the Cadence virtuoso software
2. To create a working library
3. To draw the schematic of a 2-input NAND gate in Cadence Virtuoso Schematic Editor
4. To create a symbol view of the NAND gate from the schematic
5. To simulate the NAND gate using MMSIM Spectre
6. To determine the delay of the output waveforms.
7.To determine the total power of the output waveform.
8. To determine the Risen time and Fall time of output waveform

Introduction

In this experiment, the design of a 2-input CMOS NAND gate is demonstrated using Cadence Virtuoso software. The process includes creating a new library, drawing the schematic, and performing circuit simulation. The NAND gate, known as a universal gate, is essential in digital logic design as it can replicate the functions of other basic gates like AND, OR, and NOT.

Simulation

In this section, the schematic of the designed 2-input NAND gate is simulated using Cadence Virtuoso. The following figure shows the schematic used in the simulation.

The simulation verifies the logical operation of the NAND gate and ensures the correct functionality according to the design parameters.

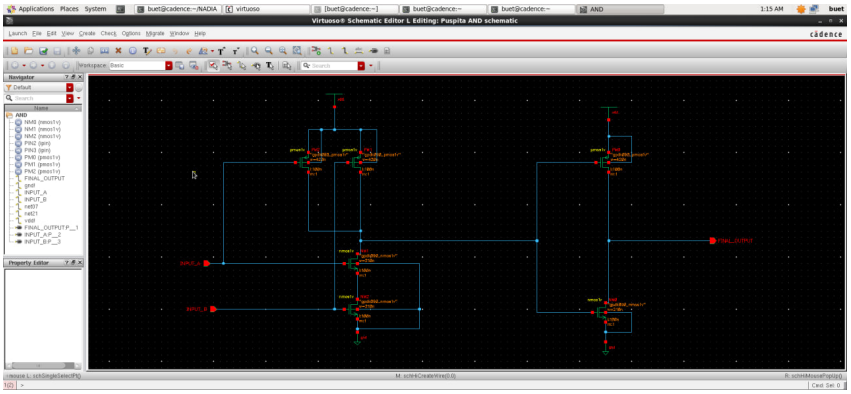

Figure 1: Schematic Drawing for Pmos = 4200 nm, Nmos = 210 nm.

Parameters

In this section, the parameters used for input A, input B, and the global source are shown side by side.

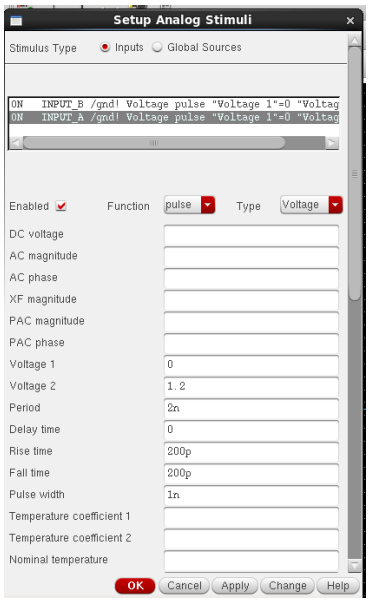

Figure 2: Parameter for Input A

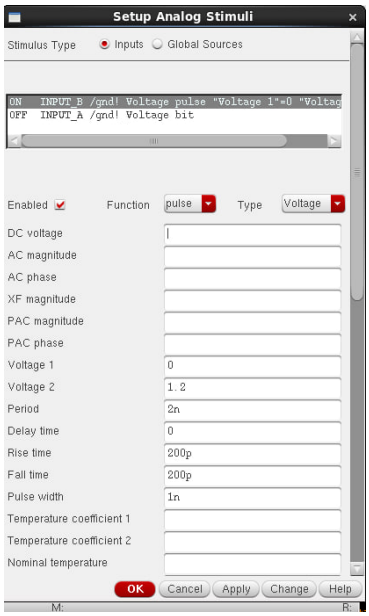

Figure 3: Parameter for Input B

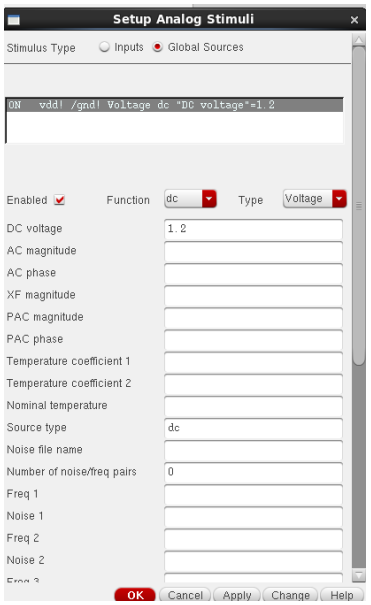

Figure 4: Parameter for Global Source

Simulation Result

The simulation results for the designed 2-input AND gate are presented below.

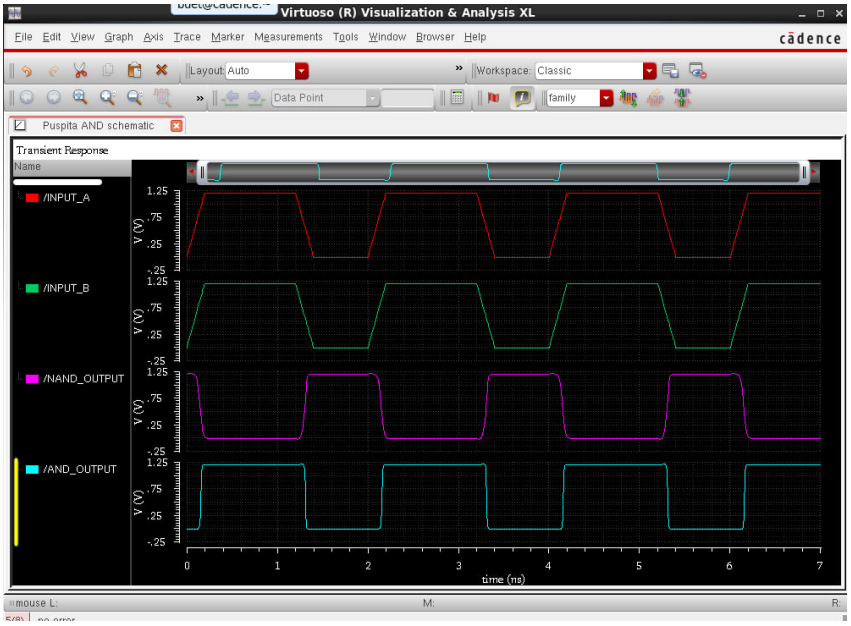

Figure 5: FinalL Output Waveform for AND Gate

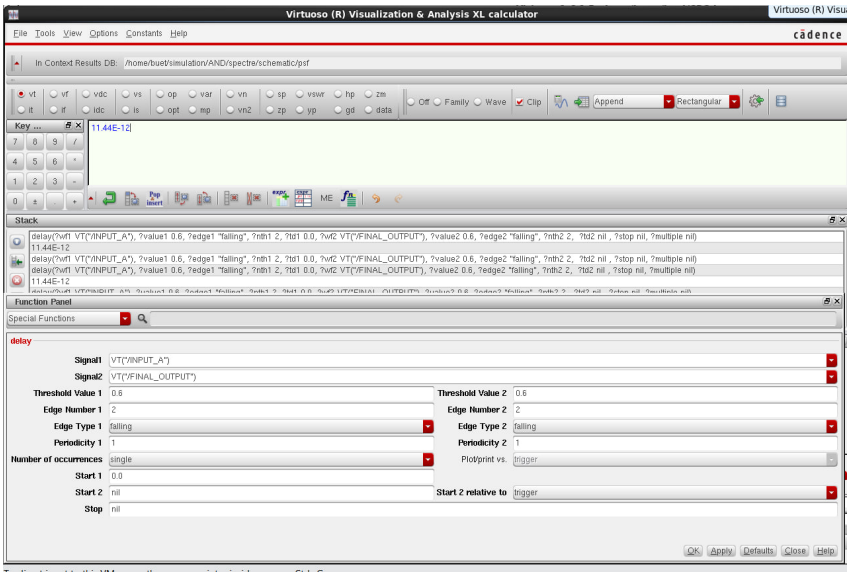

Figure 6: Delay Calculation with Respect to Input A

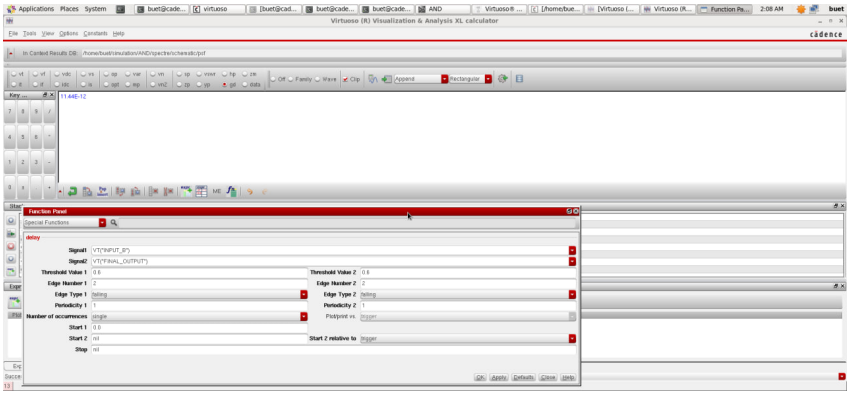

Figure 7: Delay Calculation with Respect to Input B

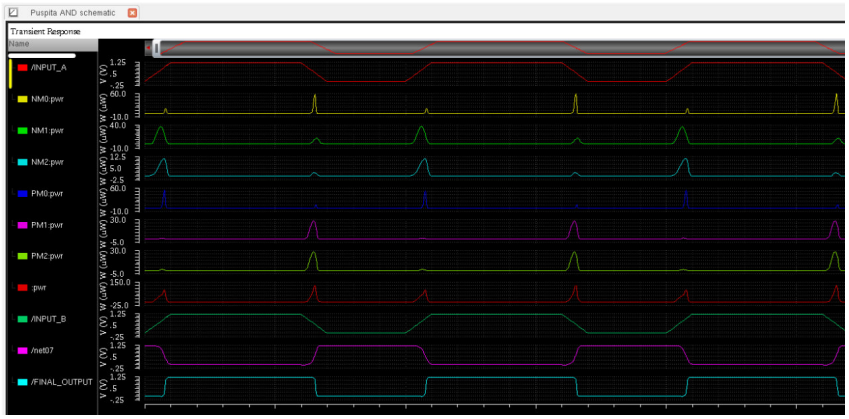

Figure 8: Output Power Waveform of All the pMOS and nMOS Transistors

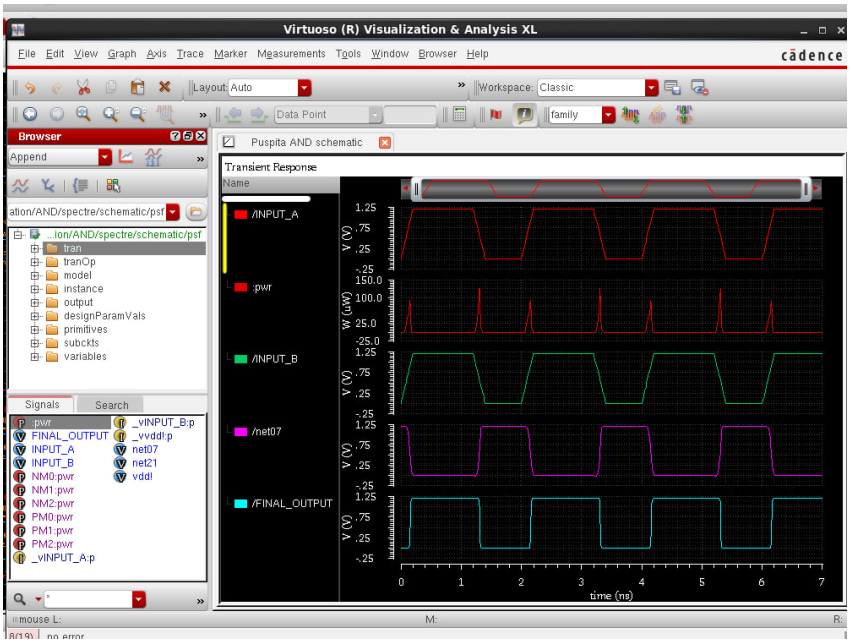

Figure 9: Final Output Power Waveform

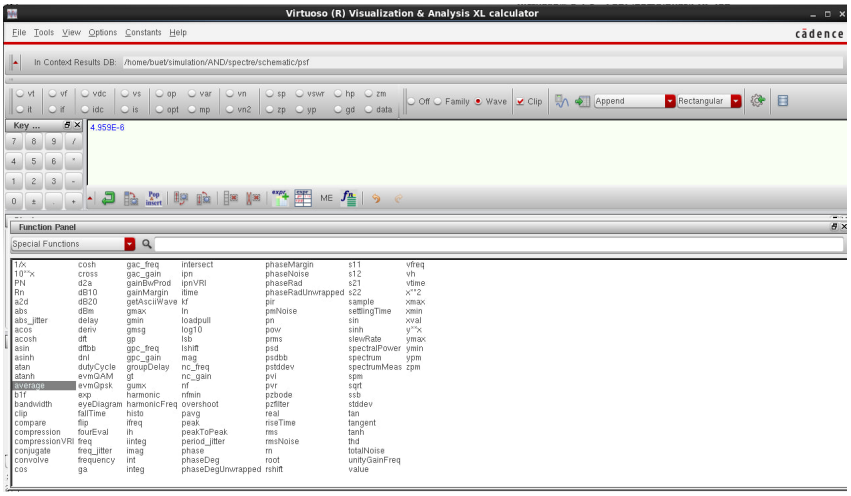

Figure 10: Output Calculation

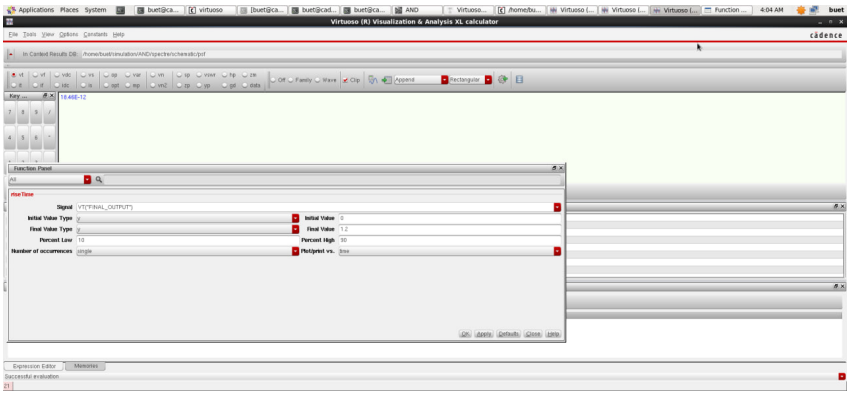

Figure 11: Rise Time Calculation

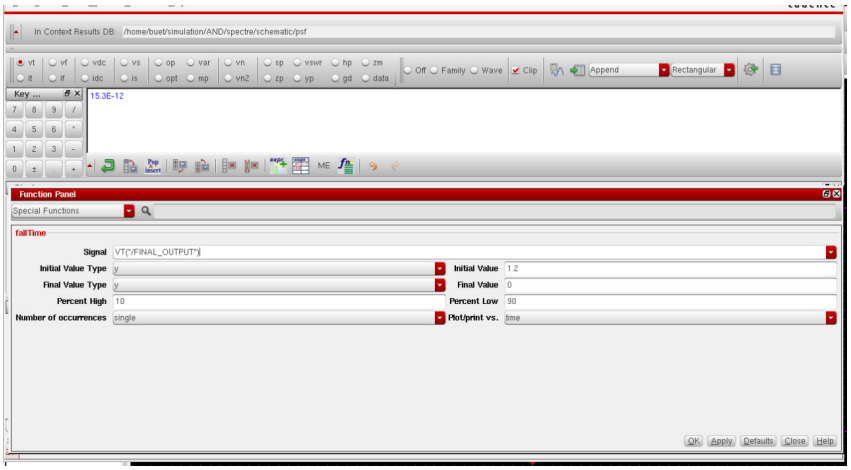

Figure 12: Fall Time Calculation

Tools Used

1. Cadence Virtuoso.
2. Virtual Box.
3.LaTeX

Conclusion

This project successfully demonstrated the design, schematic creation, and simulation of a 2-input AND gate using Cadence Virtuoso. The simulated output waveforms confirmed the correct logical operation of the gate, where the output is high only when both inputs are high. The propagation delay and power waveforms were analyzed to evaluate the performance and efficiency of the circuit. Overall, the experiment provided practical insights into CMOS digital circuit design and verification, reinforcing key concepts in digital logic and circuit simulation

References

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