Experiment 04

DC Analysis and Symbol Creation of Inverter and AND Gate

Abstract

This report focuses on the DC analysis and symbol creation of CMOS logic gates, specifically the inverter and AND gate, using Cadence Virtuoso and ADE L. The aim is to understand the transfer characteristics of an inverter by varying the width of PMOS and NMOS transistors and to learn how to construct reusable hierarchical symbols for complex circuit design.

Keywords

CMOS Inverter, AND Gate, Symbol Creation, Parametric Analysis, Transfer Characteristics Curve (TCC)

Objective

- To analyze the DC sweep and parametric simulation in ADE L for an inverter.
- To observe the effect of NMOS width variation on TCC.
- To learn symbol creation in Cadence for reusable hierarchical design.
- To design and simulate a 2-input AND gate and understand logic behavior through waveform analysis.

Introduction

Logic gates are the fundamental building blocks of digital circuits. In this experiment, we explore the behavior of a CMOS inverter and AND gate through DC analysis using Cadence Virtuoso. We perform parametric sweeps to observe how changes in transistor sizing affect circuit behavior. The experiment also introduces symbol creation which allows hierarchical schematic design and modularity in VLSI design environments.

A1: the effect of changing NMOS width on the TCC of an inverter.

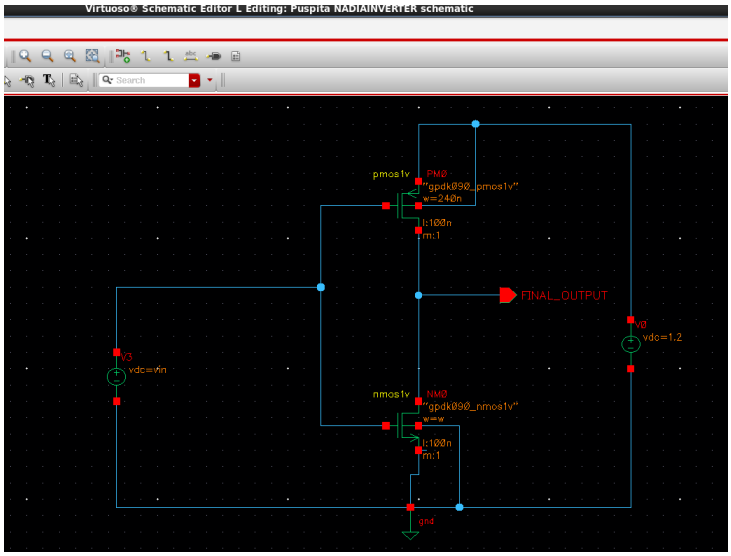
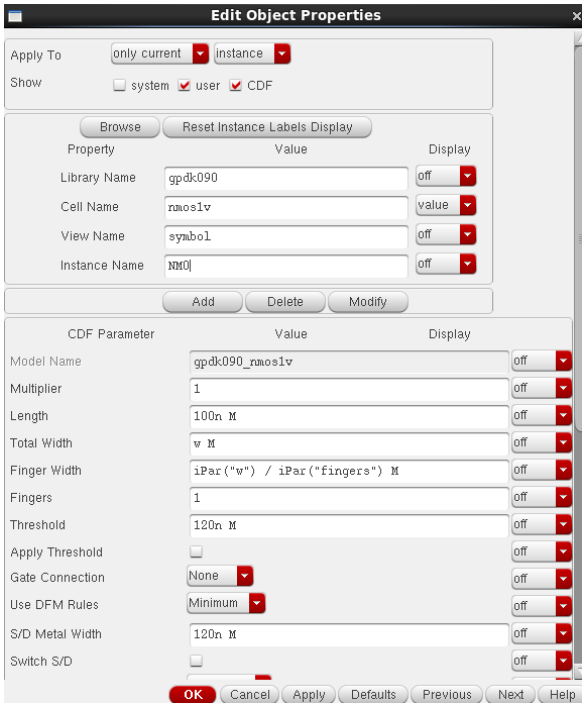
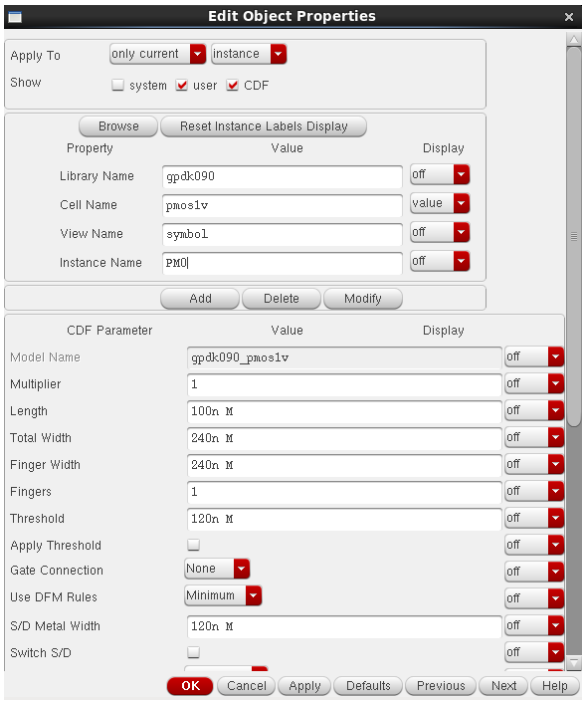


Figure 1: Schematic of the inverter used for NMOS width variation analysis.



(a) Simulation parameter setup for NMOS



(b) Simulation parameter setup for NMOS.

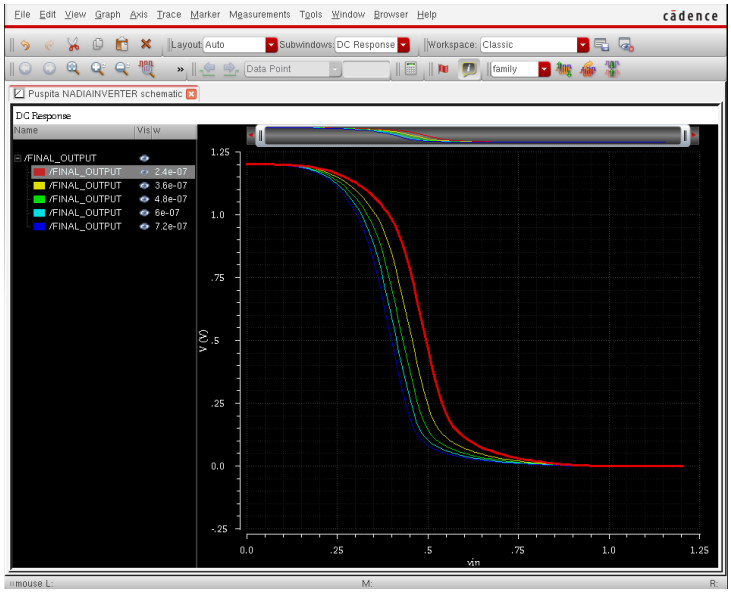


Figure 3: Transfer characteristics curve (TCC) showing the impact of NMOS width variation.

A2: A 2-input OR gate along with its symbol.

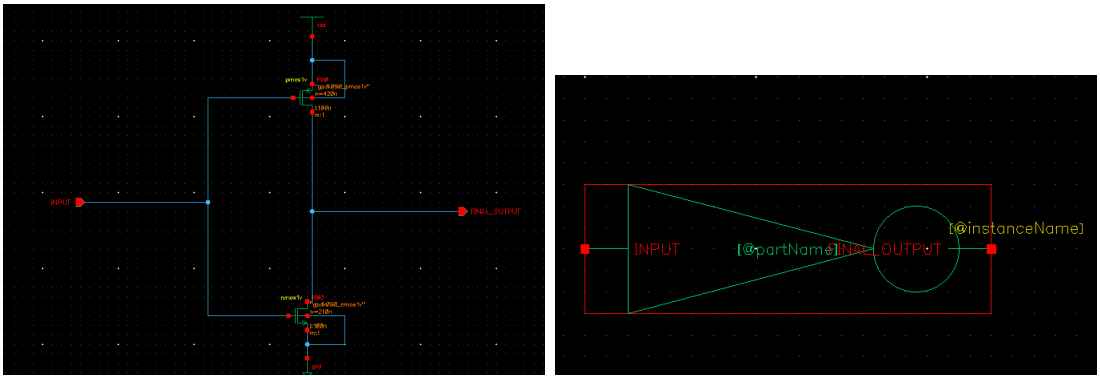


Figure 4: Left: Inverter schematic. Right: Symbol of the inverter.

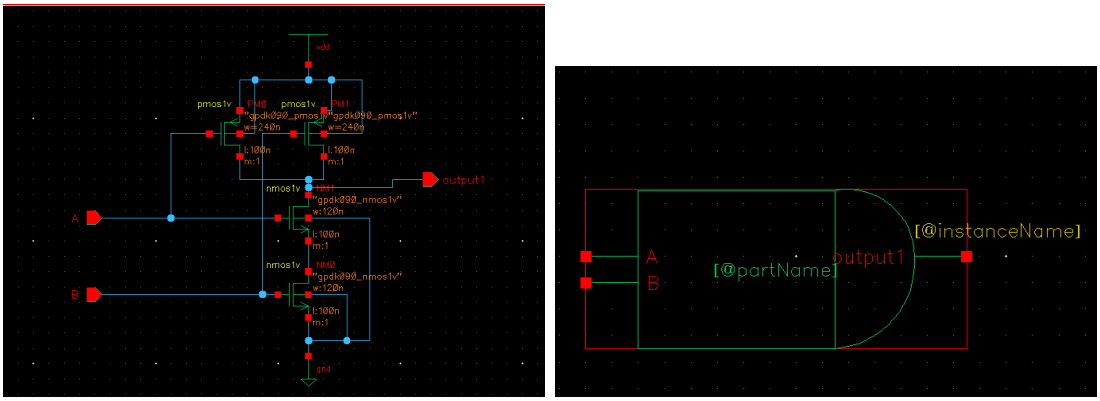


Figure 5: Left: Schematic of the 2-input AND gate. Right: Output waveform showing logic transitions.

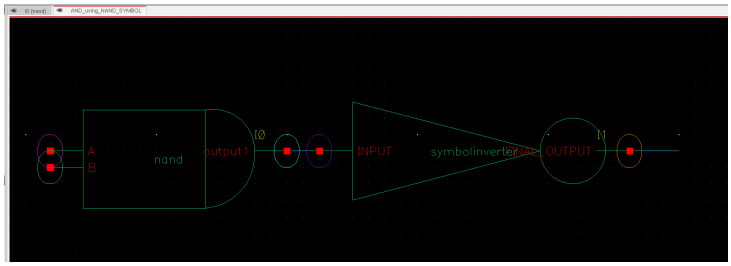


Figure 6: Final hierarchical symbol representation of the complete AND gate.

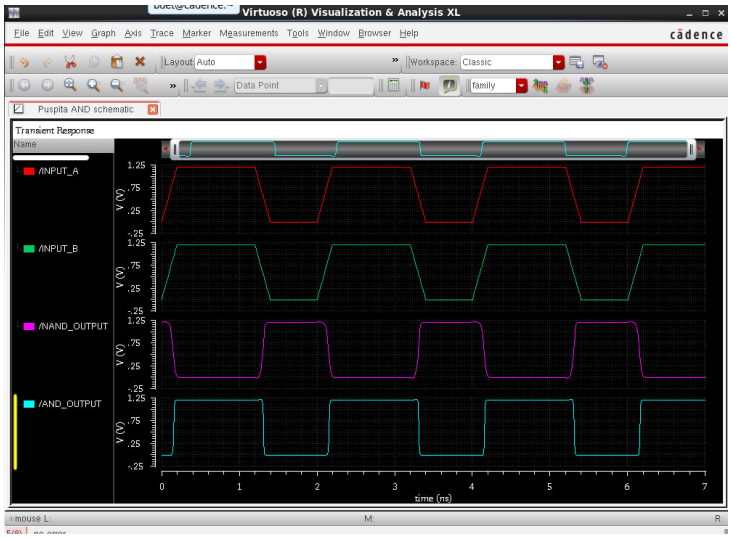


Figure 7: FinalL Output Waveform for AND Gate.

Discussion

In this experiment, we analyzed the behavior of a CMOS inverter through DC simulation using Cadence Virtuoso and ADE L. By varying the NMOS transistor width, we observed the changes in the inverter's transfer characteristics curve (TCC), helping us understand how transistor sizing affects the switching threshold and output response.

We also learned how to perform parametric sweeps using design variables and plotted the simulation results to visualize their impact. Additionally, we created a custom symbol for the inverter, allowing us to reuse it in hierarchical designs.

Building on the inverter, we designed a 2-input AND gate and ran logic simulations using pulse inputs. The output waveform confirmed the correct logical behavior of the AND gate. Finally, we created a symbol for the AND gate to support future modular circuit designs. This experiment helped us strengthen our understanding of DC analysis, parametric simulation, and symbol creation in a VLSI design environment.