

# Datapath-Controller Design of a Radix – 2 Booth Multiplier

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**Abstract** — This paper presents the Datapath-Controller design of the Radix – 2 Booth's Algorithm. It takes two numbers and finds their product.

**Keywords**—booth's algorithm, radix-2, shift and add

## I. DESCRIPTION

Conventional Shift and Add Multiplication involves N additions and N Shift Operations. Either zero or the Multiplicand is added to the 2N-bit partial product according the current bit of the Multiplier. In Booth's Algorithm, we skip the addition process whenever there are consecutive zeros or ones in the Multiplier.

The basic idea is that we continuously check the 0<sup>th</sup> bit of the Multiplier and its shifted out value,  $Q_{-1}$ .

$Q_0$	$Q_{-1}$	Operation
0	0	Shift Right {A, Q}
0	1	A + M Shift Right {A, Q}
1	0	A – M Shift Right {A, Q}
1	1	Shift Right {A, Q}

A is a N-bit register, M is the N-bit Multiplicand, Q is N-bit Multiplier,  $Q_{-1}$  is the shifted out value of Q.

## II. STATE DIAGRAM

We start from the S0 state where the design is initialized. Then S1 state, we load the value of the Multiplicand, M and count is initialized to N.

In state S2, Multiplier Q is loaded. Now we check the bits  $Q_0$  and  $Q_{-1}$ . If it is 01, we go to state S3. Else if it is

10 we go to state S4. If it is 00 or 01 state is S5. After S3, S4, or S5

count is checked. If it is non-zero, again, the two bits of the Q are checked and the process is repeated. If it is zero, we reach S6, at which the result is final.

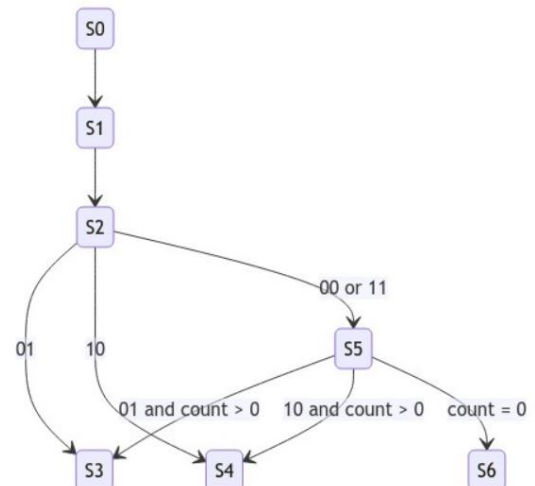
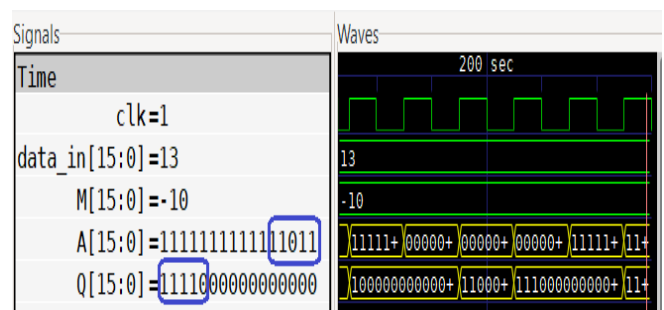


Figure 1: State Diagram for the Booth's Algorithm

## III. WAVEFORM



## REFERENCES

- [1] Indranil Sengupta, "Hardware Modelling using Verilog", NPTEL