North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	5
Experiment Title:	Design of an ALU
Course Code:	**CSE332L**
Course Name:	**Computer Organization & Architecture Lab**
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Date of Experiment:	21/4/2021
Date of Submission:	23/4/2021

★ Objectives:
- Designing a 16-bit ALU
- Implementing AND, OR, ADD, SUB operations in 1-bit ALU
- Designing a 16-bit ALU using 1-bit ALUs

★ Equipment:
- Logisim tools

★ Block diagram:

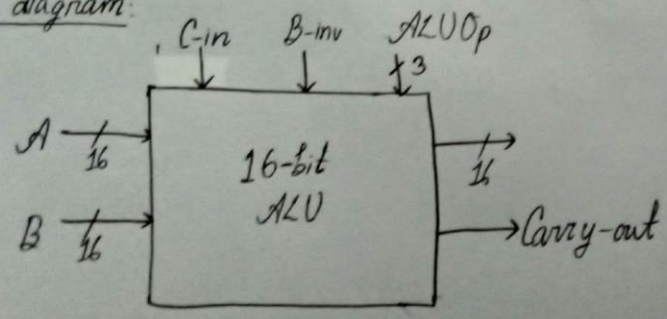


Figure 1 Block diagram for 16-bit ALU

★ Control table:

ALUOp	Function
000	AND
001	OR
010	ADD
011	SUB

Table 1: Control selections for execution of instructions in 16-bit ALU.

Circuit diagram:

Figure 2: Circuit diagram of 1-bit ALU

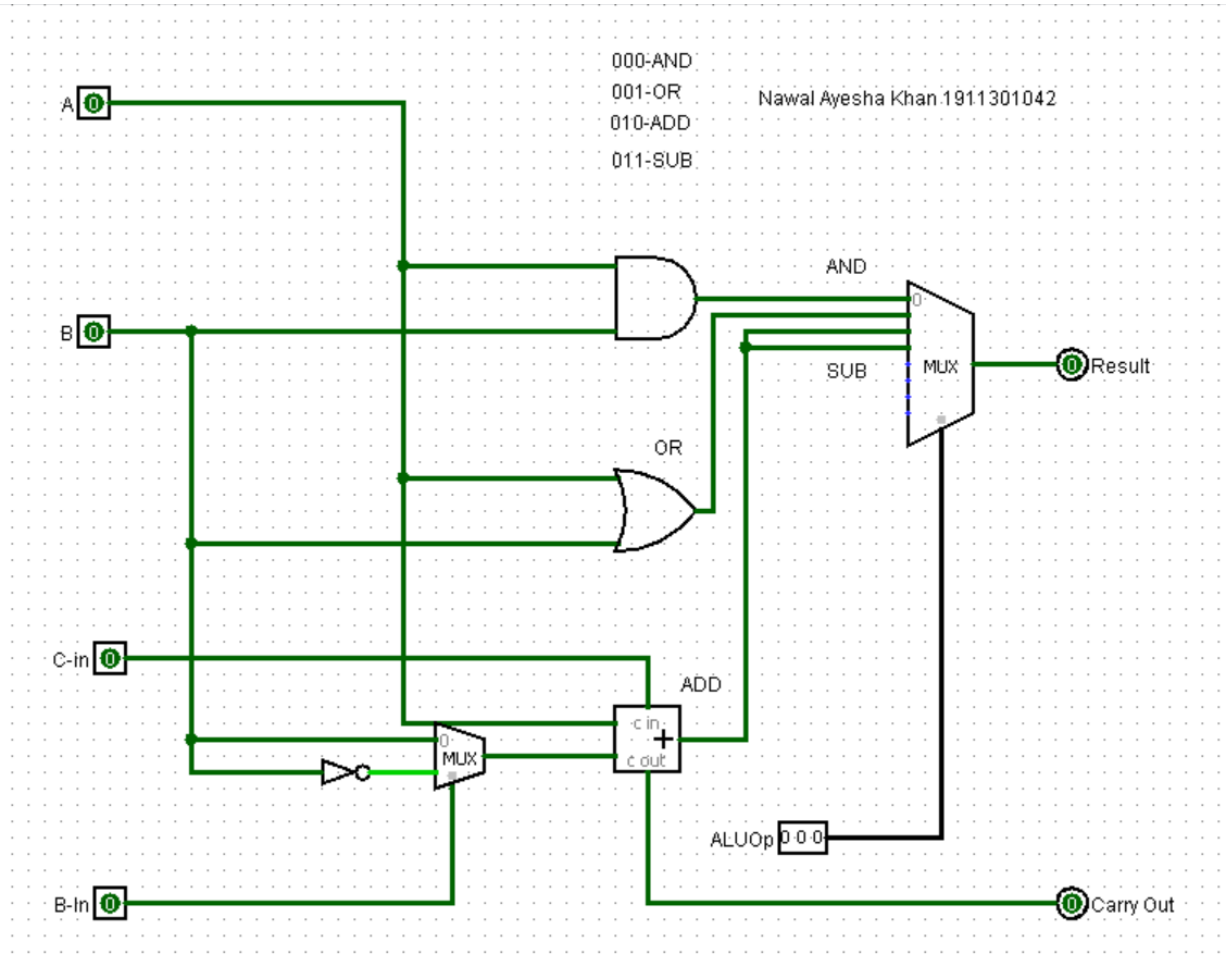
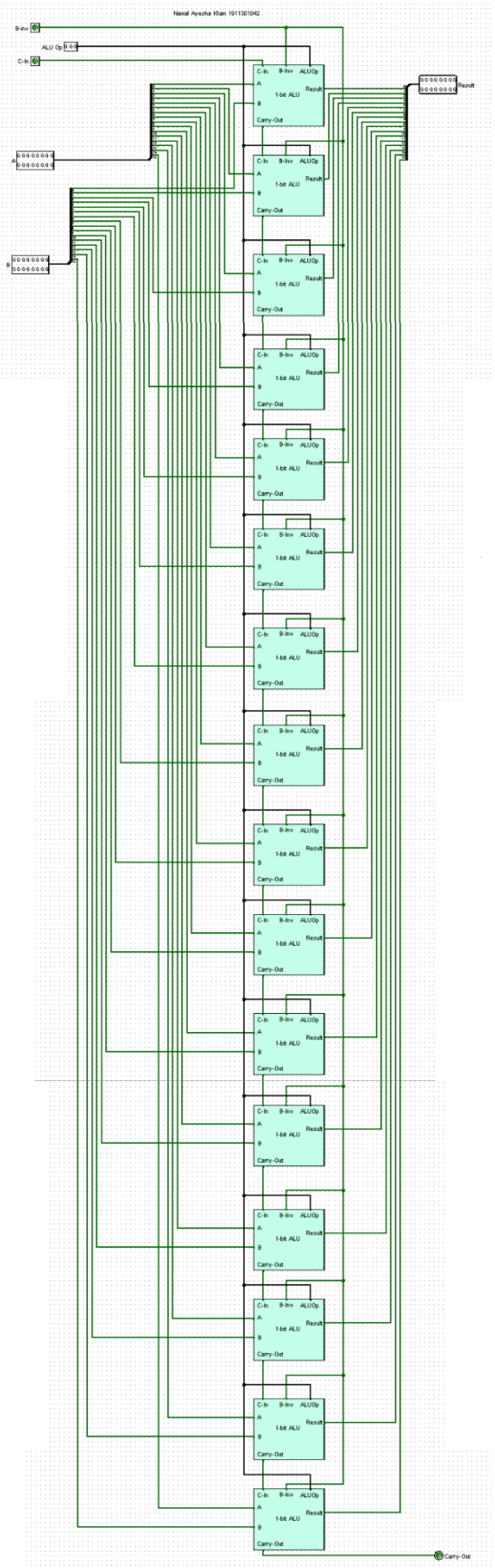


Figure 3: Circuit diagram of 16-bit ALU


Nawal Ayesha Khan 191301042
B-inv
ALU Op
C-In
A
B
Result
C-In B-Inv ALUOp
A
1-bit ALU
B
Result
Carry-Out
Carry-Out

★ Discussion: In this experiment, we learned about designing a 16-bit ALU, using 16 1-bit ALUs. The experiment was simulated on Logisim using multiplexers, full-adder, and basic logic gates. Multiplexer inputs for ALUOp are chosen based on which operation has to be carried out. We test the circuit using various input values and observed the corresponding outputs. There are no difference between theoretical and experimental values as it was done as a simulation. Since the outputs match theoretical ones and the 16-bit ALU works as designed, we can conclude experiment was successful.