North South University

Department of Electrical & Computer Engineering

Lab Report

Experiment No:	6
Experiment Title:	Build a single cycle datapath
Course Code:	**CSE332L**
Course Name:	**Computer Organization & Architecture Lab**
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Date of Experiment:	28/4/2021
Date of Submission:	29/4/2021

★ Objectives: * Design an Instruction fetch Unit of datapath
* Design an R-format and Load/Store datapath

★ Equipment: * Logisim tools

★ Block diagram:

*Figure 1: Block diagram for Instruction Fetch and ~~R-format~~ datapath

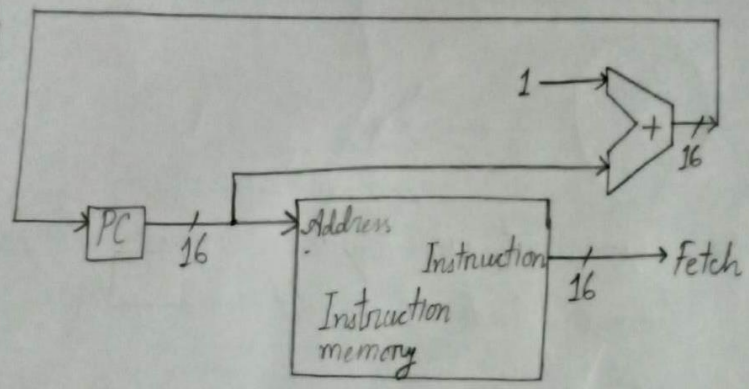
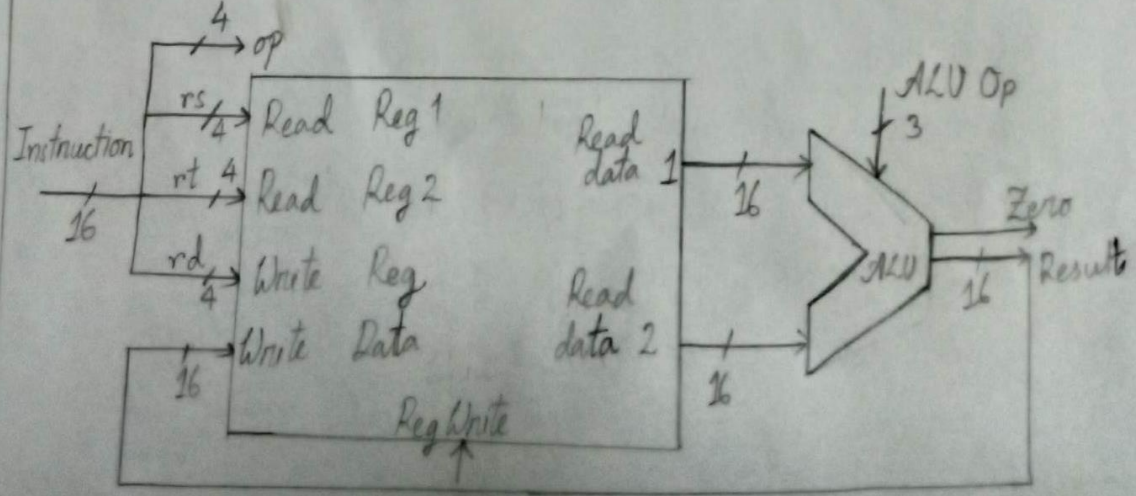
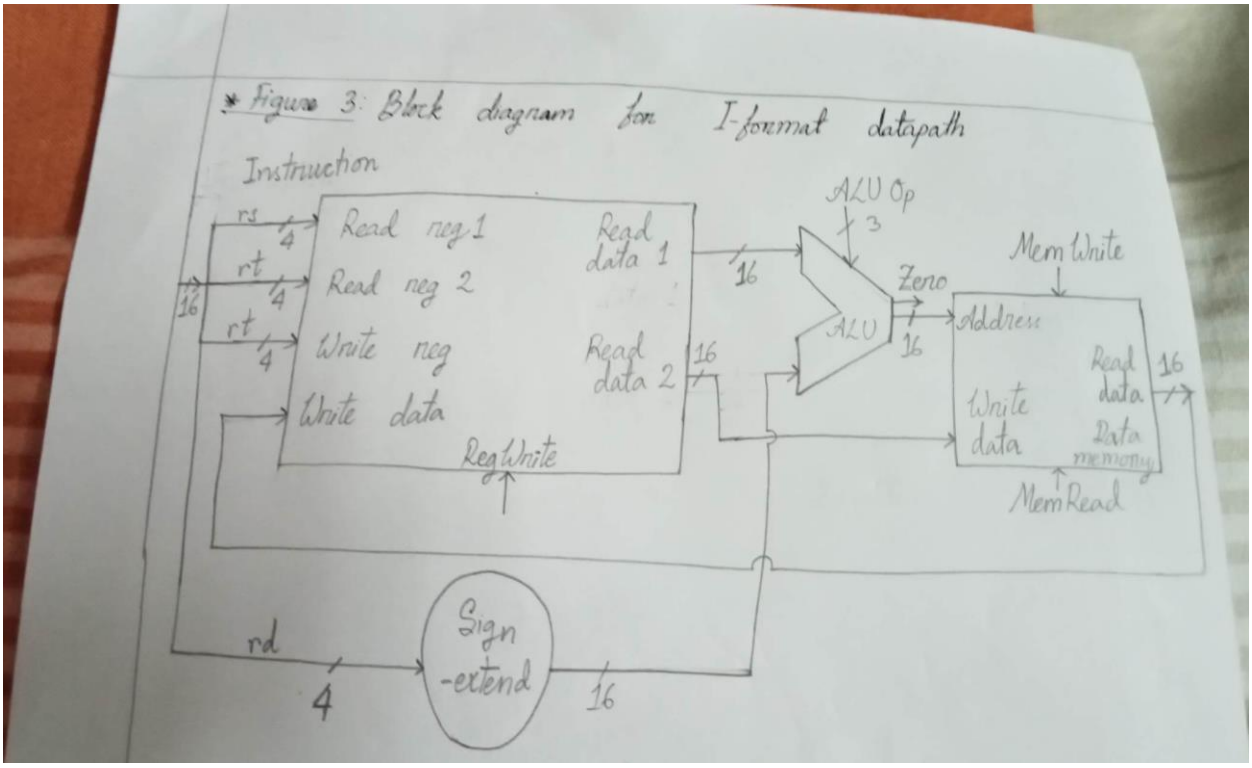


*Figure 2: Block diagram for R-format datapath





Circuit diagram:

Figure 4: Circuit diagram of Instruction Fetch unit

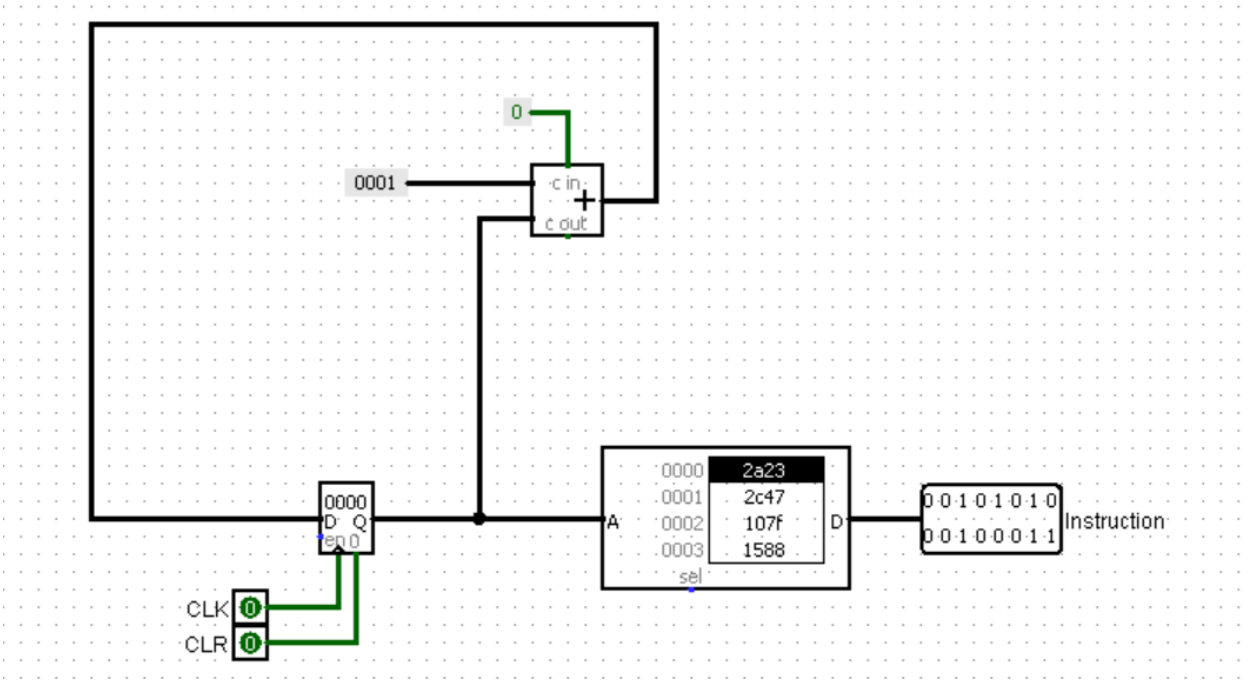


Figure 5: Circuit diagram of Instruction Fetch and R-format datapath

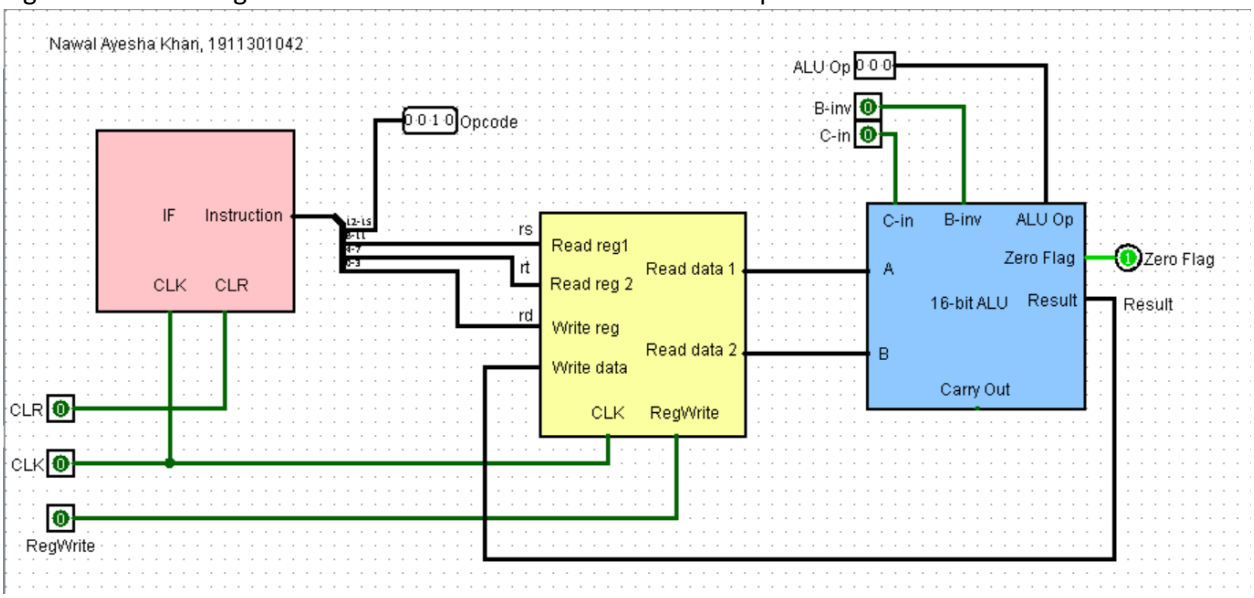
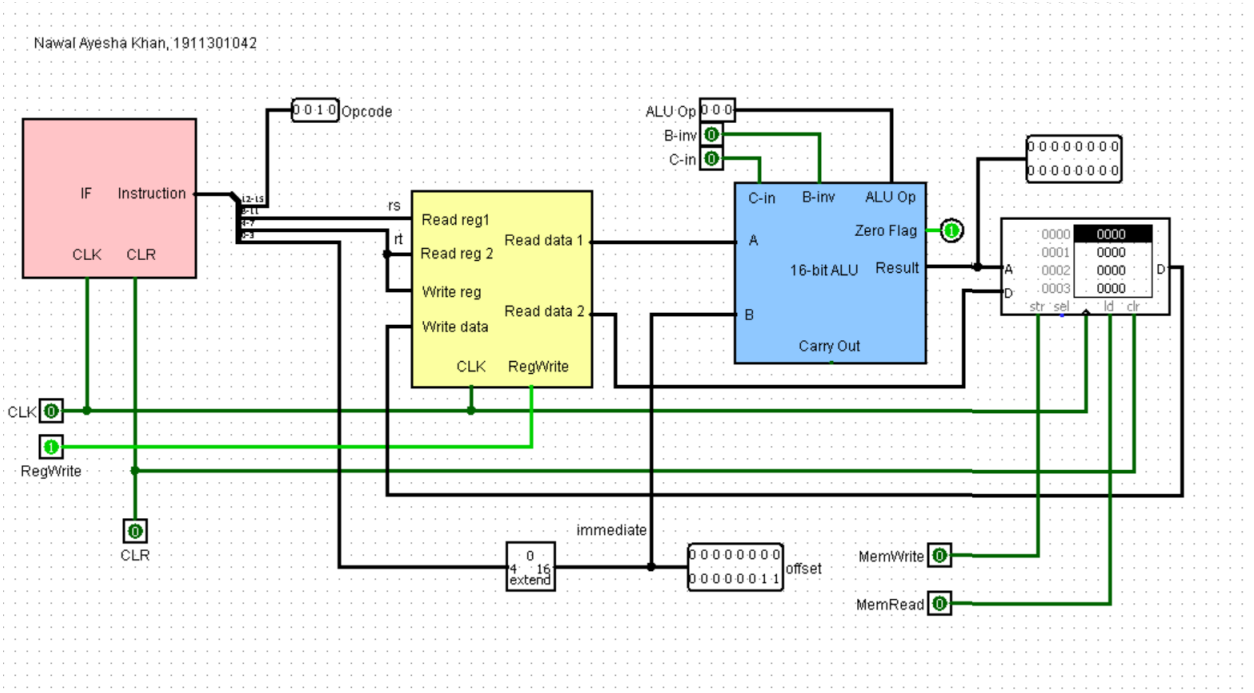


Figure 6: Circuit diagram of Instruction Fetch and I-format datapath



★ Discussion: In this experiment, we learned about designing datapaths for R-format and I-format instructions and Instruction fetch unit, using instruction memory, register file, ALU unit, sign-extension unit, and data memory. Based on 16-bit ISA, opcode and registers are determined to be 4-bits each. ALU operates on register data based on multiplexer input, and result is written back to destination register or is sent to data memory as effective address. We test circuit using various instruction values and observe values at each stage for both datapaths. There are no differences between theoretical and experimental values as it was done as a simulation. Since ~~out~~ values match the theoretical outputs of each stage, we can conclude that experiment was successful.