Lab Manual

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Experiment No: 07
Experiment Name: Build a pipelined datapath

Introduction:

In single cycle datapath, the datapath components execute an instruction concurrently, in one cycle. As a result, no datapath component can be used more than once per cycle. Here, we will use the single-cycle datapath components to create a multi-cycle (pipelined) datapath, where each step in the fetch-decode-execute sequence takes one cycle. In multicycle particularly in Pipelined datapath each functional unit (e.g., Register File, Data Memory, ALU) can be used more than once in the course of executing an instruction, which saves hardware (and, thus, reduces cost);

Objective:

We will have following objectives to fulfill:

1) Build a pipelined datapath

Experiment Details:

Assume, a 16 bit ISA with following fields. The formats of the instruction are as follows:

R-type

op (4 bit)	rs (4 bit)	rt (4 bit)	rd (4 bit)

I-type

op (4 bit)	rs (4 bit)	rt (4 bit)	immediate (4 bit)

J-type

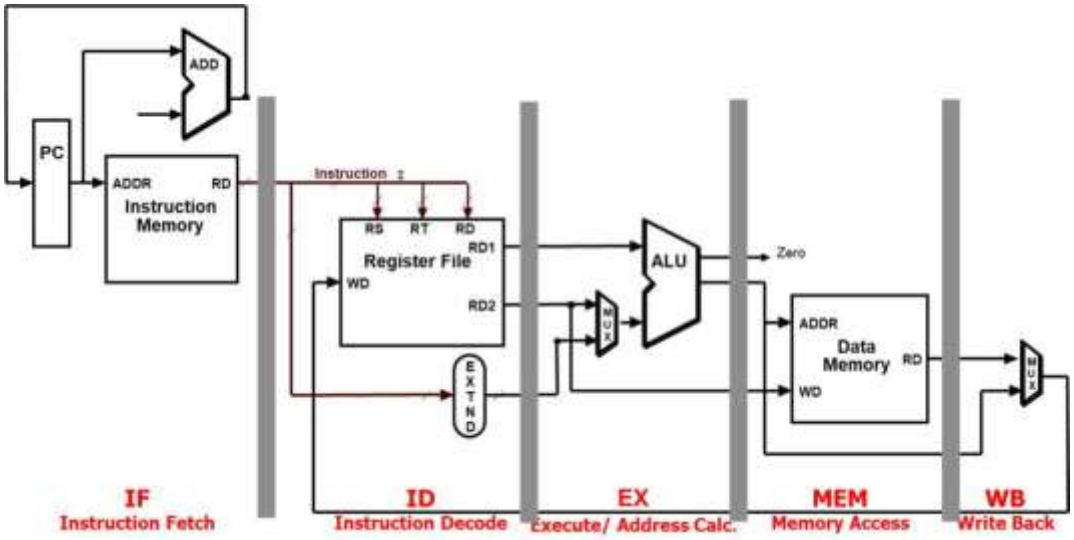
op (4 bit)	Target (12 bit)

Equipment/Tool

Logisim Tool

Pipelined Datapath:

Following is the schematic diagram of the complete single cycle datapath with pipeline registers inserted in between the stages.



Assignment:

1) **Prepare the lab report.**
2) **Take a screenshot of your implementation and later include it in your lab report.**