# TFT LCD +RTP Specification

## Model Name: GZ0270NA00730

## (ED027NA-02H ) Project

| Customer Signature |
| --- |
| |
| Date: 12/04/2017 |
| |

This technical specification is subjected to change without notice

**Table of Contents**

## 1. FEATURES

The 2.65" LCD module is the active matrix color TFT LCD module. TFT technology is applied with vertical and horizontal drivers built on the panel. Both of horizontal and vertical scan are reversible and controlled by the serial interface commands. The product is designed for the requirement of the green product, and the specification complies with CMI's "Green Product Chemical Substance Specification Standard Hand Book".

## 2. GENERAL SPECIFICATIONS

| Item | Description | Unit |
|---|---|---|
| Display Size (Diagonal) | 2.65 | Inch |
| Display Type | Transmissive | - |
| Aspect Ratio | 4:3 | - |
| Display | Landscape | - |
| Pixel per pitch (PPI) | 151 | - |
| Active Area (HxV) | 54X 40.5 | mm |
| Number of Dots (HxV) | 960 x 240 | dot |
| Dot Pitch (HxV) | 56.25 x 168.75 | um |
| Color Arrangement | RGB Delta | - |
| Outline Dimension (HxVxT) * | 63.5 X 46.6 X 3.46 | mm |
| Interface | Serial RGB,8bit | - |
| Weight (Display + RTP) | 20.57 +/- 0.3 | g |
| Panel surface treatment | HC | - |
| Dark gray scale inversion** | 6 o'clock | |

*Exclude FPC and protrusions.

*Without WV film

** FPC at right side

## 3. INPUT/OUTPUT TERMINALS

### 3.1 TFT LCD Panel

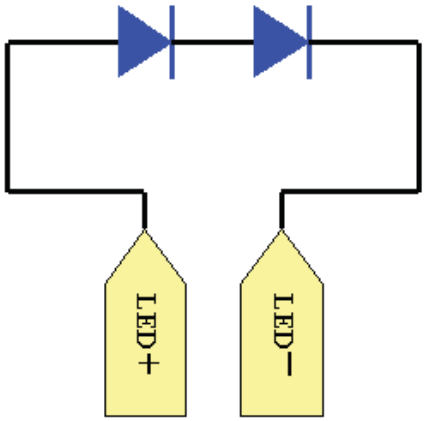
Recommend connector: Compatible with FH26-45S-0.3SHW(05)

| | | | | |
|---|---|---|---|---|
| 1 | NC | - | No Connection | |
| 2 | XR | I | Touch panel signal (Right electrode) | |
| 3 | YT | I | Touch panel signal (Top electrode) | |
| 4 | XL | I | Touch panel signal (Left electrode) | |
| 5 | YB | I | Touch panel signal (Bottom electrode) | |
| 6 | NC | - | No Connection | |
| 7 | $V_{COM}$ | O | Common Voltage | |
| 8 | CS | I | Serial command enable | |
| 9 | SDA | I/O | Serial command data input/output | |
| 10 | SCL | I | Serial command clock input | |
| 11 | HSYNC | I | Horizontal sync input | |
| 12 | VSYNC | I | Vertical sync input | |
| 13 | DCLK | I | Data clock input | |
| 14 | D7 | I | Data 7 ; MSB | |
| 15 | D6 | I | Data 6 | |
| 16 | D5 | I | Data 5 | |
| 17 | D4 | I | Data 4 | |
| 18 | D3 | I | Data 3 | |
| 19 | D2 | I | Data 2 | |
| 20 | D1 | I | Data 1 | |
| 21 | D0 | I | Data 0 ; LSB | |
| 22 | GND | P | Ground for Digital Circuit | |
| 23 | $V_{DD}$ | P | Power for Analog Circuit | |
| 24 | $D_{VDD}$ | C | Power setting capacitor connecting pin | |
| 25 | CP1P | C | Power setting capacitor connecting pin | |
| 26 | CP1M | C | Power setting capacitor connecting pin | |
| 27 | CP2P | C | Power setting capacitor connecting pin | |
| 28 | CP2M | C | Power setting capacitor connecting pin | |
| 29 | VINT1 | C | Power setting capacitor connecting pin | |
| 30 | CP3P | C | Power setting capacitor connecting pin | |
| 31 | CP3M | C | Power setting capacitor connecting pin | |
| 32 | VINT2 | C | Floating this pin | |

| | | | | |
|---|---|---|---|---|
| 33 | VINT3 | C | Floating this pin | |
| 34 | CP4P | C | Power setting capacitor connecting pin | |
| 35 | CP4M | C | Power setting capacitor connecting pin | |
| 36 | $V_{GH}$ | C | Power setting capacitor connecting pin | |
| 37 | $V_{GL}$ | C | Power setting capacitor connecting pin | |
| 38 | AGND | P | Ground for Analog Circuit | |
| 39 | FRP | O | Frame polarity output for panel $V_{COM}$ | |
| 40 | $V_{COM}$DC | O | $V_{COM}$ DC output | |
| 41 | VCAC | C | Power setting capacitor for $V_{COM}$ AC | |
| 42 | DRV | O | VLED boost transistor driving signal | |
| 43 | $V_{LED+}$ | P | Power for LED Backlight (anode) | **Note 1** |
| 44 | $V_{LED-}$ | P | Power for LED Backlight (cathode) | **Note 1** |
| 45 | $V_{COM}$ | O | Panel common voltage output | |

I: input, O: output, P: Power

**Note 1:** The figure below shows the connection of backlight LED.




## 4. ABSOLUTE MAXIMUM RATINGS

| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Power supply (pump) | VDD | -0.3 | 5.0 | V |
| Storage temperature | $T_{STG}$ | -30 | 80 | ℃ |
| Operating temperature | $T_{OPR}$ | -10 | 70 | ℃ |

## 5. ELECTRICAL CHARACTERISTICS

### Driving TFT LCD Panel

GND=0V, Ta=25℃

| Item | | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Power Supply Voltage | | VDD | 3.00 | 3.30 | 3.60 | V | Note 5-1 |
| Input Signal Voltage | Low Level | $V_{IL}$ | GND | - | 0.3x VDD | V | Input Signal Voltage |
| | High Level | $V_{IH}$ | 0.7x VDD | - | VDD | V | |
| Panel Power Consumption | | $W_P$ | - | 60 | - | mW | Note: 5-2 |
| Power Supply Voltage | | VDD | 3.00 | 3.30 | 3.60 | V | Note 5-1 |

Note 5-1: The VDD power is provided for overall panel module supply voltage.

Note 5-2: Test condition:

VDD = 3.3V, 8-bit RGB mode, DCLK=27MHz and Frame Rate=60Hz

### Driving Backlight

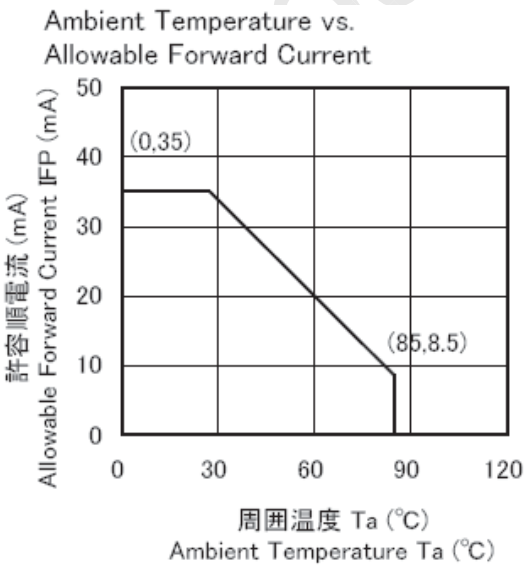
Ta=25℃

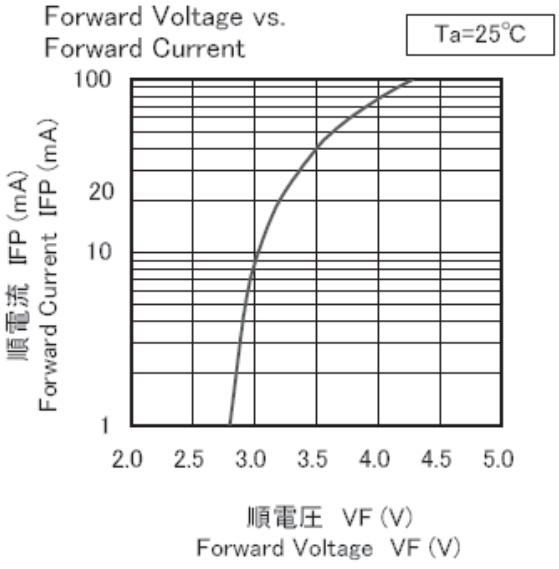
| Item | Symbol | MIN | TYP | MAX | Unit | Remark |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | -- | 25 | 27 | mA | Note 5-2 |
| Forward Current Voltage | $V_F$ | -- | 6.4 | 7 | V | |
| Backlight Power Consumption | $W_{BL}$ | -- | 160 | 189 | mW | |

Note 5-2: Backlight driving circuit is recommended as the fix current circuit.

* Ta: Ambient Temperature

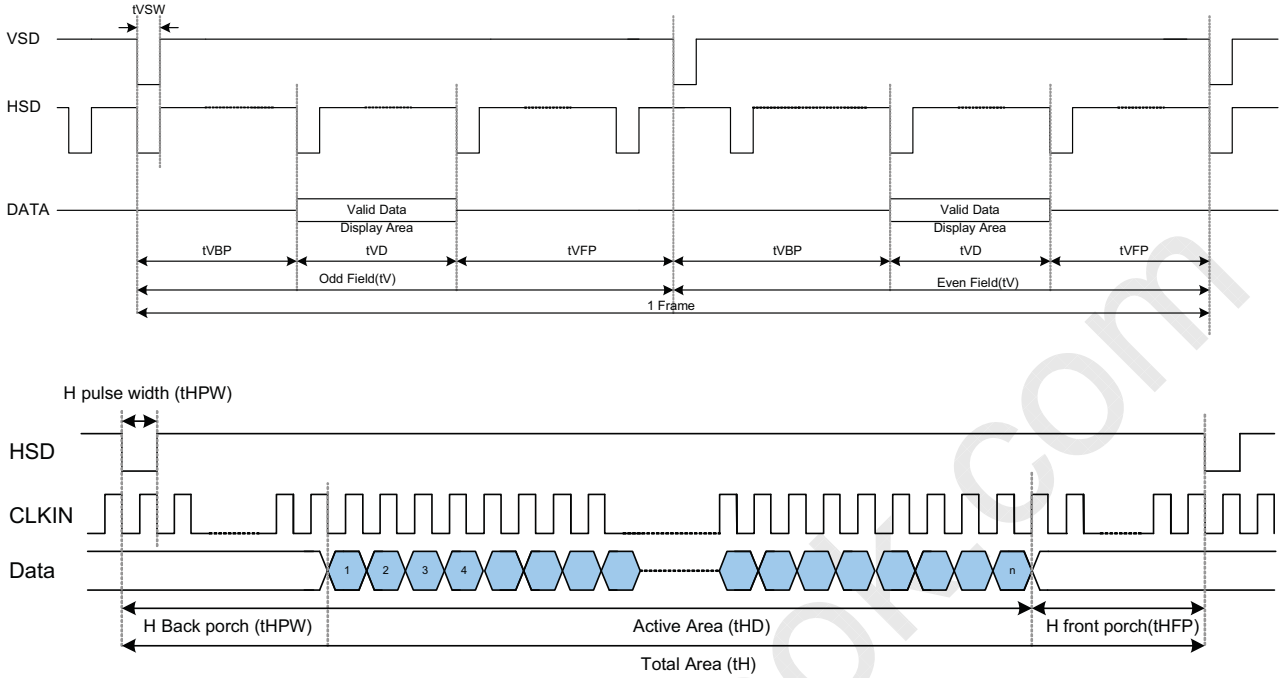
* High temperature operation: Test current refers the diagram as following



## 6. TIMING CHART

### 8-bit RGB/8-bit Dummy RGB/YUV Input Timing Chart







### 8-bit RGB input timing

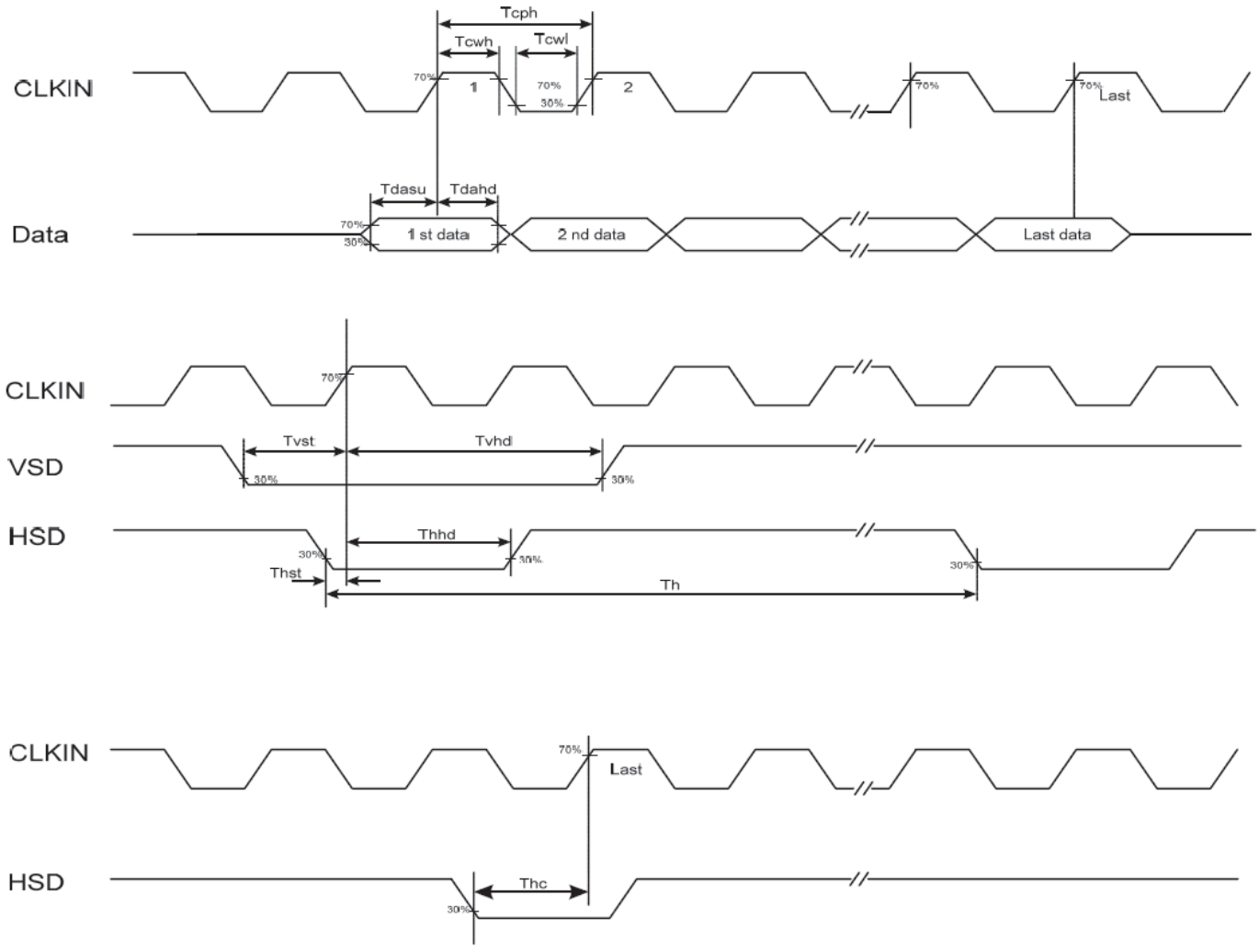
| Parameter | | Symbol | Interface | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| CLKIN frequency | | fCLKIN | 13.5 | 27 | 27.19 | MHz |
| Frame rate | | FR | - | 60 | - | Hz |
| HSD period | | tH | 1024 | 1716 | 1728 | CLKIN |
| HSD display period | | tHD | | 960 | | CLKIN |
| HSD back porch | | tHBP | 50 | 70 | 255 | CLKIN |
| HSD front porch | | tHFP | 14 | 686 | 718 | CLKIN |
| HSD pulse width | | tHSW | 1 | 1 | tHBP-1 | CLKIN |
| VSD period time | | tV | 242.5 | 262.5 | 450.5 | H |
| Vertical display area | | tVD | | 240 | | H |
| VSD back porch | Odd field | tVBP | 1 | 21 | 31 | H |
| | Even field | | 1.5 | 21.5 | 31.5 | |
| VSD front porch | Odd field | tVFP | 1.5 | 1.5 | 179.5 | H |
| | Even field | | 1 | 1 | 179 | |
| VSD pulse width | | tVSW | 1CLKIN | 1CLKIN | 6H | |
| 1 Frame | | | 485 | 525 | 901 | H |

**AC Electrical Characteristics**

(VDD =3.0~3.6V, VDDIO=AVDD=VDD, AGND=GND=0V, TA=25°C)

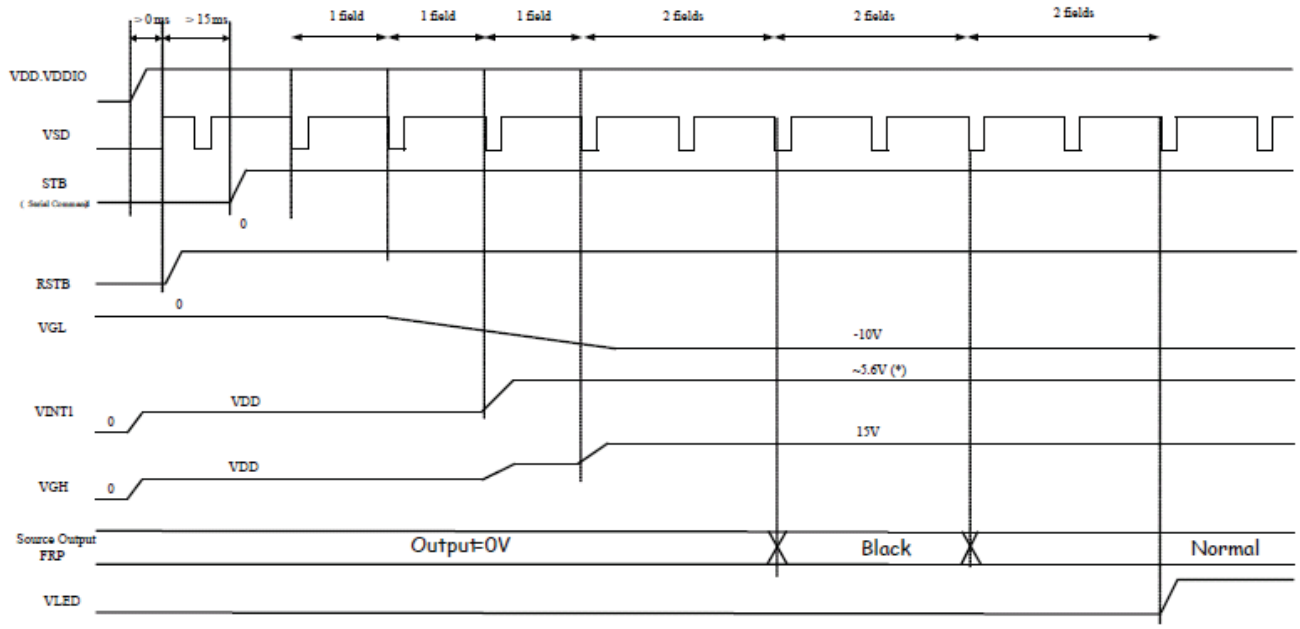
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Time that the HSD to CLKIN | Thc | - | - | 1 | CLKIN | |
| HSD period time | Th | 60 | 63.56 | 67 | us | |
| VSD setup time | Tvst | 12 | - | - | ns | |
| VSD hold time | Tvhd | 12 | - | - | ns | |
| HSD setup time | Thst | 12 | - | - | ns | |
| HSD hold time | Thhd | 12 | - | - | ns | |
| Data setup time | Tdsu | 12 | - | - | ns | DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN |
| Data hold time | Tdhd | 12 | - | - | ns | DR0~DR7, DG0~DG7, DB0~DB7 to CLKIN |

**Timing Waveform**

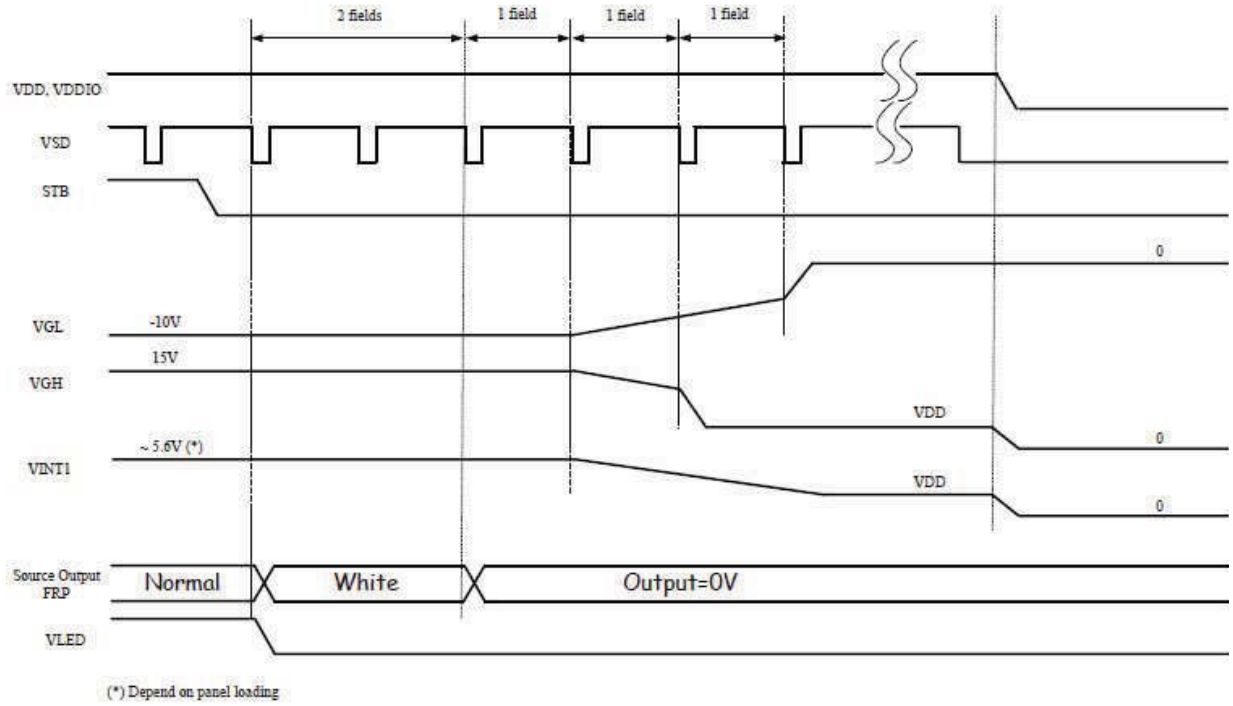


## 7. POWER SEQUENCE

### 7.1 Power On Sequence



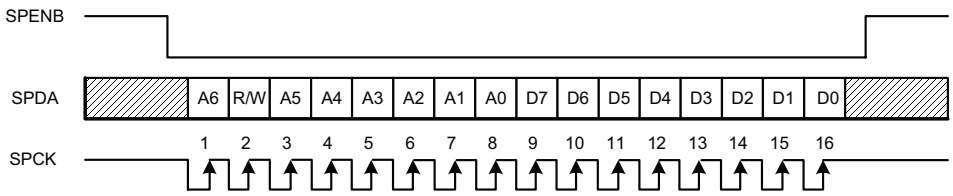

### 7.2 Power off Sequence




(*) Depend on panel loading

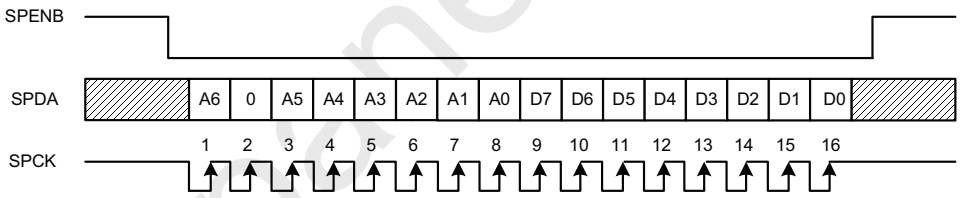
## 8. SERIAL INTERFACE

### 8.1 SPI command format

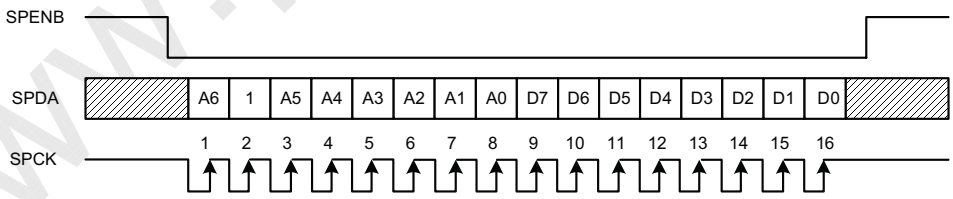



- Each serial command consists of 16 bits of data that is loaded one bit a time at the rising edge of se al clock SPCK. Command loading operation starts from the falling edge of SPENB and is completed at the next rising edge of SPENB.
- The serial control block is operational after power on reset, but commands are established by the VSD signal. If command is transferred multiple times for the same register, the last command before the VSD signal is valid.
- If less than 16 bits of SPCK are input while SPENB is low, the transferred data is ignored.
- If 16 bits or more of SPCK are input while SPENB is low, the first 16 bits of transferred data before the rising edge of SPENB pulse are valid data.
- Serial block operates with the SPCK clock.
- Serial data can be accepted in the power save modes.

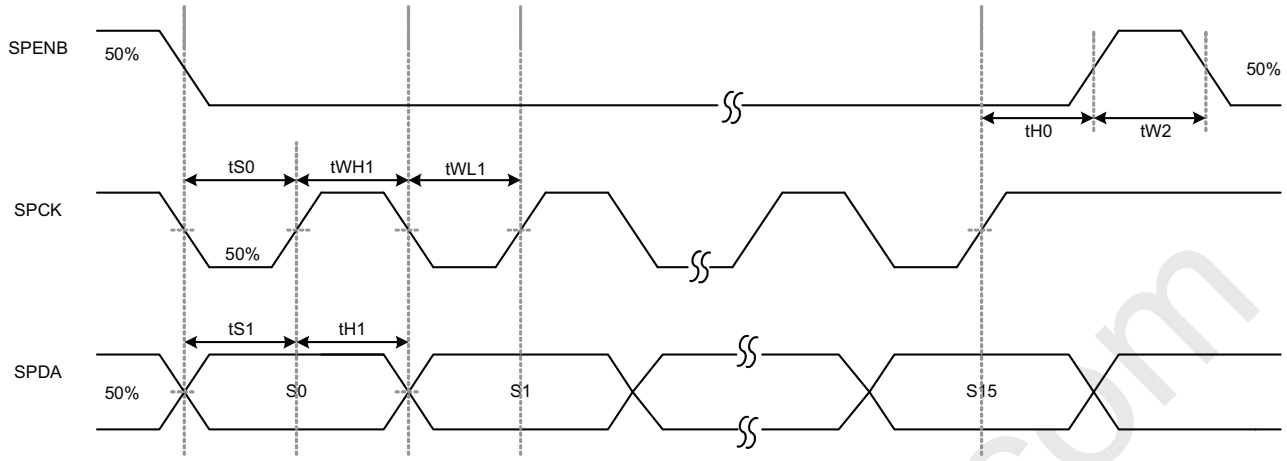
**Seiral Interface Write Sequence**




**Serial Interface Read Sequence**



### 8.2 SPI timing

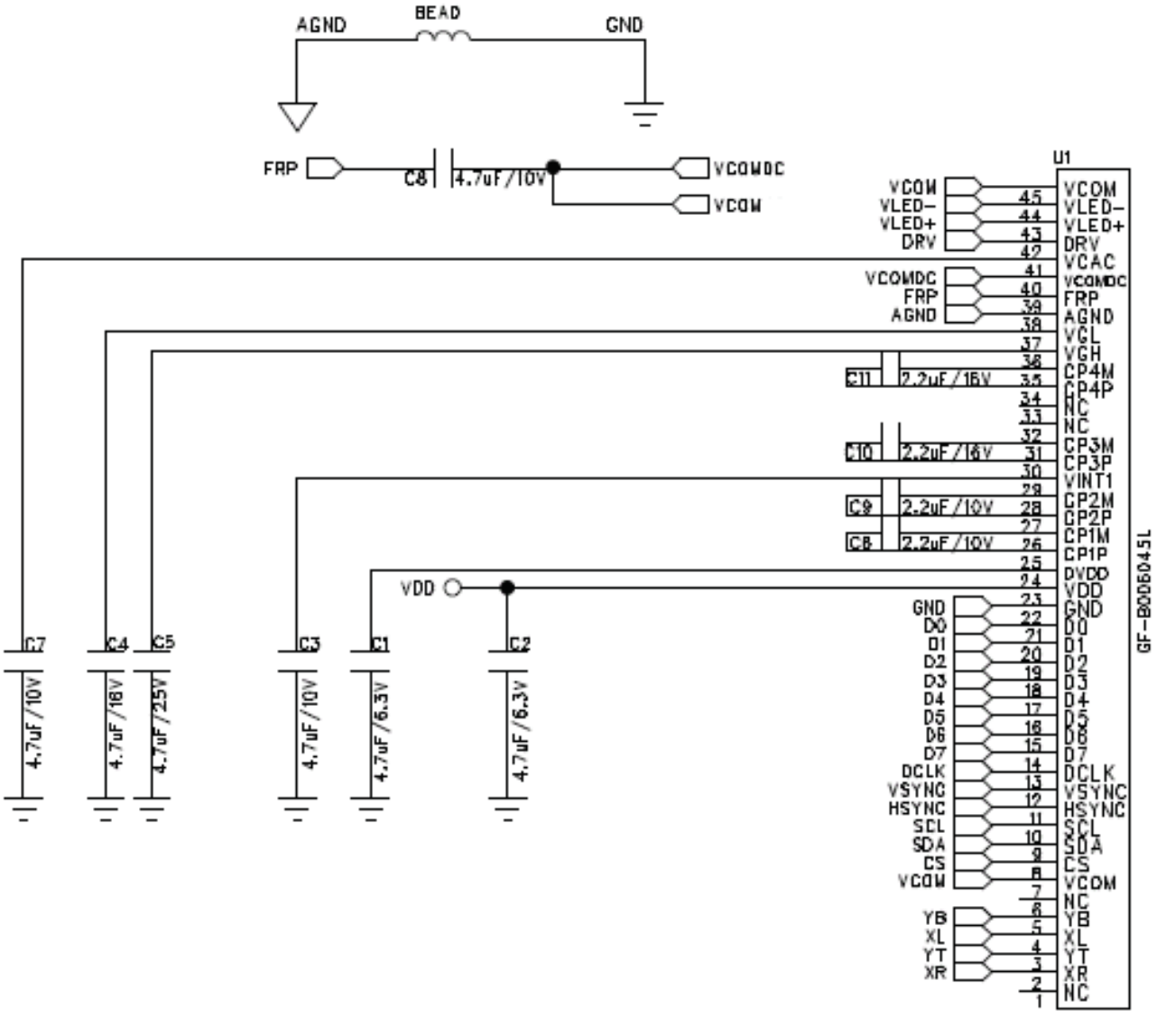



| Item | symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| SPENB input setup time | tS0 | 50 | | | ns |
| Serial data input setup time | tS1 | 50 | | | ns |
| SPENB input hold time | tH0 | 50 | | | ns |
| Serial Data Input hold time | tH1 | 50 | | | ns |
| SPCK pulse high width | tWH1 | 50 | | | ns |
| SPCK pulse low width | tWL1 | 50 | | | ns |
| SPENB pulse high width | tW2 | 400 | | | ns |

### 8.3 Instruction setting

| Register | Data | Remark |
|---|---|---|
| 0x05 | 0x1E | / Global reset |
| 0x00 | 0x0C | // Set VCOM voltage AC level |
| 0x01 | 0xAF | // Set VCOM voltage DC level |
| 0X04 | 0X0B | // Set Input data format (RGB through mode) |
| 0X13 | 0X01 | Stripe input: R13H = 01H |
| 0x16 | 0x00 | // Set Gamma Curve |
| 0x17 | 0x44 | |
| 0x18 | 0x31 | |
| 0x19 | 0x42 | |
| 0x1A | 0x43 | |
| 0x2B | 0x01 | // Sleep out |

## 9. Application circuit




| Pin Name | Capacitor | Pin Name | Capacitor |
|---|---|---|---|
| CP1P | 2.2uF / 10V | VINT1 | 4.7uF / 10V |
| CP1M | | VGH | 4.7uF / 25V |
| CP2P | 2.2uF / 10V | VGL | 4.7uF / 16V |
| CP2M | | VDD | 4.7uF / 6.3V |
| CP3P | 2.2uF / 16V | DVDD | 4.7uF / 6.3V |
| CP3M | | FRP-VCOMDC | 4.7uF / 10V |
| CP4P | 2.2uF / 16V | VCAC | 4.7uF / 10V |
| CP4M | | | |

## 10. OPTICAL CHARACTERISTICS

Optical Specification

| Item | | Symbol | Condition | MIN | TYP | MAX | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| Viewing Angles | | $\Theta_L$ | CR ＞ 10 | 30 | 40 | - | Degree | Note 10-1 |
| | | $\Theta_R$ | | 30 | 40 | - | | |
| | | $\Theta_T$ | | 10 | 20 | - | | |
| | | $\Theta_B$ | | 40 | 50 | - | | |
| Contrast Ratio | | CR | $\Theta$=0° | 200 | 300 | - | | Note 10-2 |
| NTSC | | (x,y) | | - | 45 | - | % | Note 10-5 |
| Response Time | | Tr+Tf | | - | 35 | 50 | ms | Note 10-3 |
| Luminance ($I_F$=25mA) | | L | | 180 | 220 | - | cd/m$^2$ | Note 10-4 |
| Chromaticity | White | $x_W$ | | 0.25 | 0.30 | 0.35 | | Note 10-5 |
| | | $y_W$ | | 0.29 | 0.34 | 0.39 | | |

10-1Basic Measure Conditions

(1) Driving voltage

VDD= 3.3 V

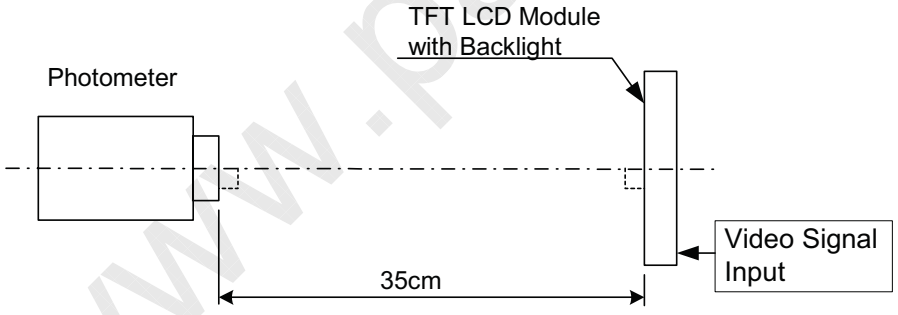
(2) Ambient Temperature: Ta=25℃

(3) Testing Point: Measure in the display center point and the test angle $\Theta$=0°

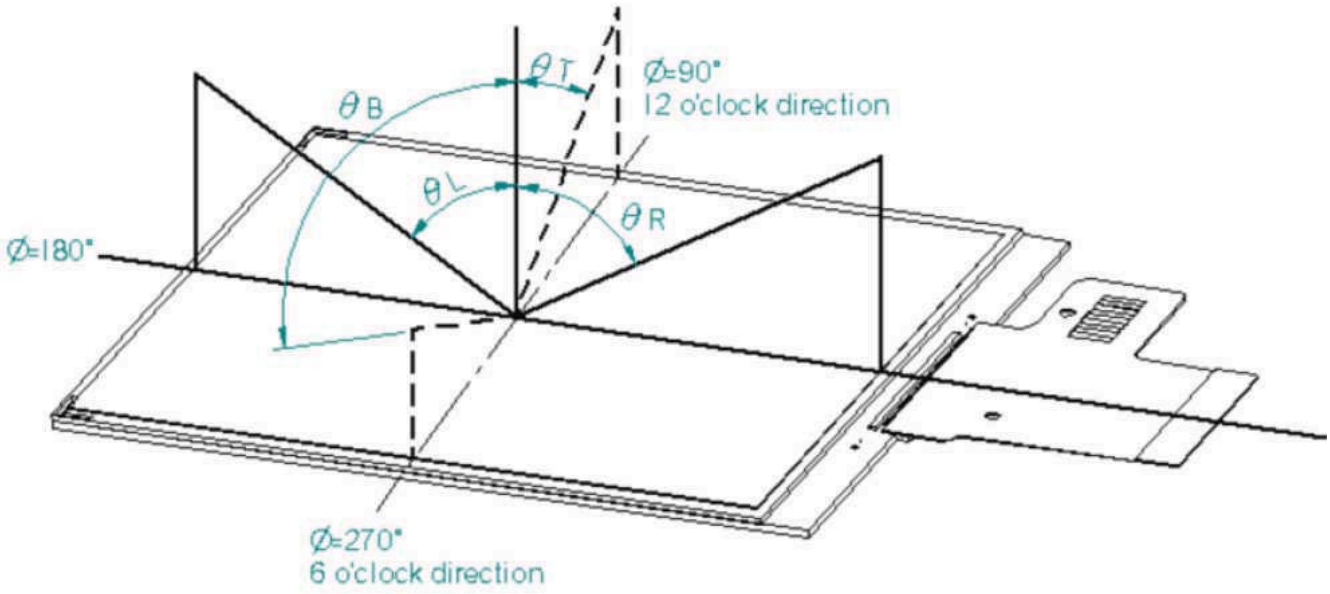
(4) LED Current: $I_F$=25mA.

(5) Testing Facility

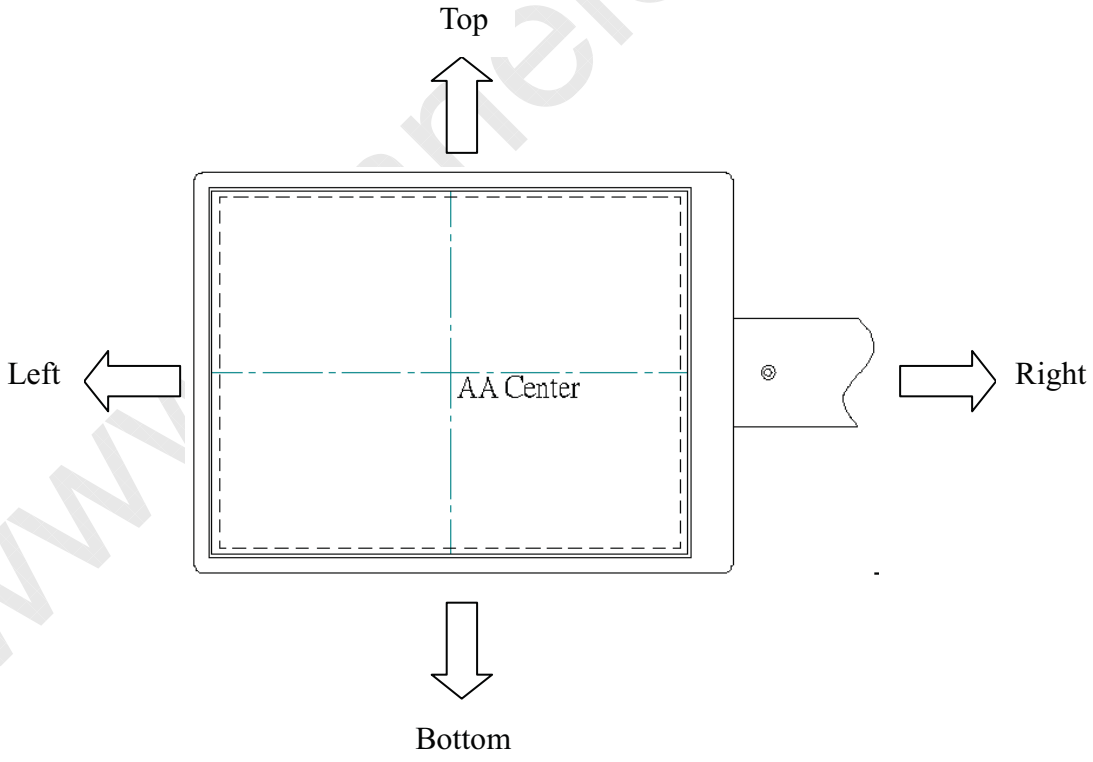
Environmental illumination: ≤ 1 Lux



Note 10-1: Viewing angle diagrams:




**Definition of viewing angle**



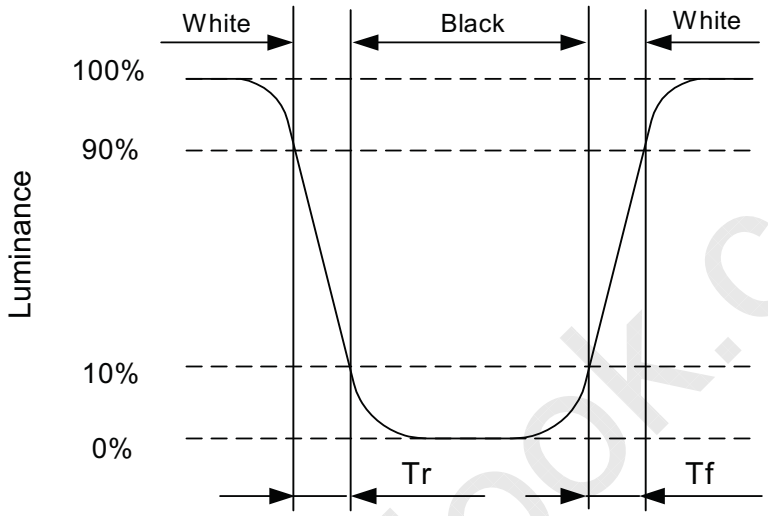

**Definition of viewing angle for display**

Note 10-2: Contrast Ratio:

Contrast ratio is measured in optimum common electrode voltage.

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 10-3: Definition of response time:




Note 10-4: Luminance:

Test Point: Display Center

Note 10-5: Chromaticity: The same test condition as Note 10-4.

## 11. RELIABILITY

| No | Test Item | Condition |
|---|---|---|
| 1 | High Temperature Operation | Ta=+70℃, 240hrs |
| 2 | High Temperature & High Humidity Operation | Ta=+40℃, 95% RH, 240hrs |
| 3 | Low Temperature Operation | Ta= -10℃, 240hrs |
| 4 | High Temperature Storage (non-operation) | Ta=+80℃, 240hrs |
| 5 | Low Temperature Storage (non-operation) | Ta=-30℃, 240hrs |
| 6 | Thermal Shock (non-operation) | -30℃←→80℃, 50 cycles<br>30 min 30 min |
| 7 | Resistance to Static Electricity Discharge (non-operation) | C=200pF, R=0Ω;<br>Discharge: ±150V<br>3 times / Terminal |
| 8 | Vibration (non-operation) | Frequency: 10~55Hz; Amplitude: 1.5mm<br>Sweep Time: 11min<br>Test Time: 2 hrs for each direction of X, Y, Z |
| 9 | Shock (non-operation) | Acceleration: 100G; Period: 6ms<br>Directions: ±X, ±Y, ±Z; Cycles: Twice |

Ta: Ambient Temperature

＊ For environment stress test, the image quality guarantee after recover time 2 hours at ambient environment.

＊ Polarizer cosmetic is not guarantee after reliability test.

## 12. HANDLING CAUTIONS

12.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommend ESD strategy

(1) In handling LCD panel, please wear non-charged material gloves. And the conduction ring connect wrist to the earth and the conducting shoes to the earth is necessary.

(2) The machine and working table for the panel should have ESD prohibition strategy.

(3) In handling the panel, ionize flowing decrease the charge in the environment is necessary.

(4) In the process of assembly the module, shield case should connect to the ground.

12.2 Environment

(1) Working environment of the panel should in the clean room.

(2) The front polarizer is easy damaged, handle it carefully and do not scratch it by sharp material.

(3) Panel has polarizer protective film in the surface please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

12.3 Others

(1) Turn off the power supply before connecting and disconnecting signal input cable.

(2) The connection area of FPC and panel is very weak, do not handle panel only by FPC or bend FPC.

(3) Water drop on the surface or condensation as panel power on will corrode panel electrode.

(4) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.

(5) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.

# 13. Touch Screen Panel Specifications:

## 13-1 基本特性(Bastic feasture)

| | |
|---|---|
| 吋別(Size) | 2.65” |
| 輸入模式(Input mode) | 觸控筆或手指(Stylus or Finger) |
| 類型(Type) | ☐ Capacitive<br>☐ Infrared<br>☐ Accoustic wave<br>☐ Electro-Magnetic<br>☐ Digital Resistive<br>■ 4-wire Analog Resistive<br>☐ 5-wire Analog Resistive<br>☐ 6-wire Analog Resistive<br>☐ 7-wire Analog Resistive<br>☐ 8-wire Analog Resistive |
| 結構(Structure) | ☐ Glass<br>☐ Glass + Glass<br>■ Film + Glass<br>☐ Film + Film<br>☐ Film + Plastic<br>☐ Film+Film+Glass<br>☐ Film + Film+ Plastic |
| 表面(Surface) | ☐ 亮面(Clear type)<br>■霧面(Anti-Glare type) |

**13-2. 機構尺寸(Mechanical Dimension)**

| 項目(Item) | 規格(Specification) | 備註(Remark) |
|---|---|---|
| 外觀尺寸(Outline Dimension) | 63 x 46.1 x 1.01 (mm) | **See ME Drawing** |
| 動作保證區(Active Area) | 55 x 41.5 (mm) | **See ME Drawing** |
| 透明區(View Area) | 56 x 42.5 (mm) | **See ME Drawing** |
| ITO Glass 厚度(ITO Glass Thickness) | 0.55 (mm) | |
| ITO Film 厚度(ITO Film Thickness) | 0.188 (mm) | |
| 重量(Weight) | TBD | |
| 出線端長度(Tail Length) | 12.68 (mm) (silicone glue width MAX 1.1mm) | **See ME Drawing** |

Notes:

1. Dimension Unit: mm.
2. Weight Unit: g.
3. Detailed outline specification refer to ME Drawing.

## 13-3. 機構強度特性&可靠度測試(Mechanical & RELIABILITY Characteristics)

| 項目(Item) | | 規格 (Specification) | 測試標準(Test standard) | 備註 (Remark) |
|---|---|---|---|---|
| 入力荷重 (Operation Force) | 筆(Pen) | 40gf Max. | Resistance between X & Y axis must be equal or lower than 2KΩ. ($R_{ON}$ ≦ 2KΩ). | **Note 1,2.** |
| | 指(Finger) | | | |
| 表面硬度(Hardness of Suface) | | 3H Min. | Per Pencil hardness test. Use 250gf test. | **JIS-K5600** |
| 筆記耐用性 (Durability-surface Scratching) | | 1000000 Min | | **Note 3** |
| 打點耐用性 (Durability-surface pitting) | | 100000000 Min | | **Note 3** |

Notes:

1, input method:

(1). Used stylus as the input method: When you used the stylus Operating or measuring must follow below conditions:

Stylus material: Polyacetal

Stylus tip size:SR 0.8 mm

(2). Used Finger as the input method : When you used the finger Operating or measuring must follow below conditions:

material 材料 :Silicon rubber (硬度:60ºHs)

Tip size :SR 8.0 mm

(3). Testing conditions: The normal atmospheric temperature and humidity

2. Active force testing conditions:

(1) Add DC5V in X asix use Polyacetal Stylus(R0.8) add force till the input voltage stable.

(2) Used Finger as the input method, Use R8 Silicon rubber tip

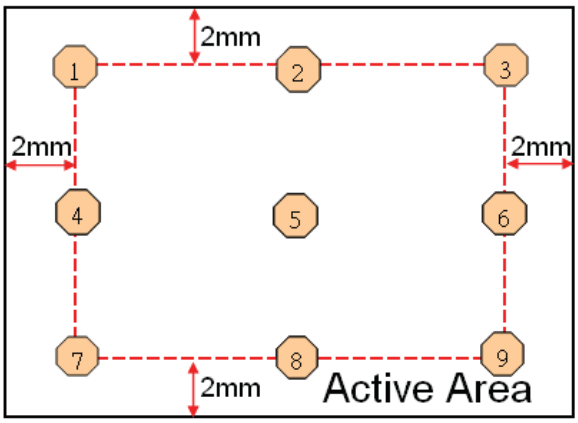
(3) Testing Point : 9 points

(4) Determine standard : After testing procedure must pass the Electrical Characteristics

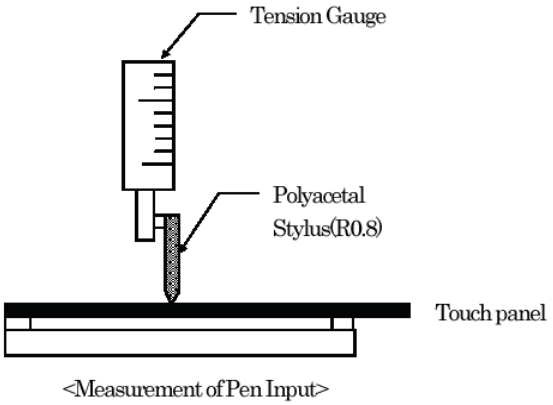
3: Pit 1,000,000 times on the film with a R0.8 silicon rubber.

-Force: 250gf.

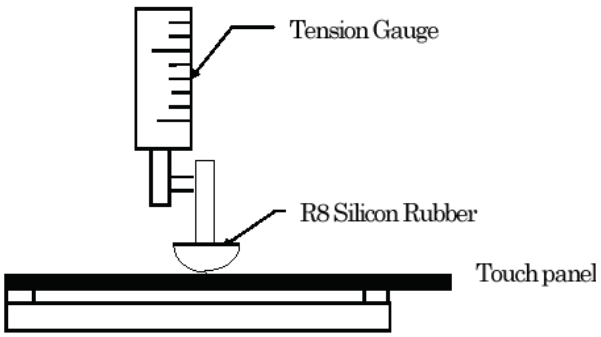
-Speed: 2times/sec.




## Activation Force Test




<Measurement of Pen Input>




<Measurement of Finger Input>

## 13-4. 電氣特性(Electrical Characteristics)

| 項目(Item) | | 規格(Specification) | 備註(Remark) |
|---|---|---|---|
| 操作電壓(Operating Voltage) | | DC 5V ;DC 7V Max | |
| 電極間電阻(Resistance Between Terminals) | X 軸(X-axis/Glass side) | 250~950Ω | |
| | Y 軸(Y-axis/Film side) | 250~950Ω | |
| 絕緣電阻(Insulation Resistance) | | ≧ 20MΩ | **At DC 25V, ≧60 sec** |
| 反應時間(Chattering) | | ≦ 10ms | |
| 線性(Linearity) | X 軸(X-axis) | ≦ ±1.5% | **Note1** |
| | Y 軸(Y-axis) | ≦ ±1.5% | **Note1** |
| 出線端型態(Tail Type) | | ■ 撓性電路板(FPC)<br>□ 熱壓導電紙(HSC) | **See ME Drawing** |
| 出線端連接方式(Tail connective Type) | | ■ 錫焊(Soldering)<br>□ ZIF<br>□ Connector | |

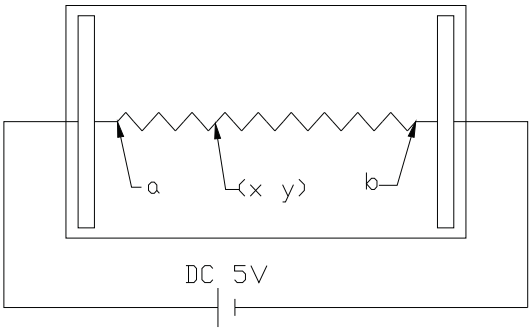
**Notes:**

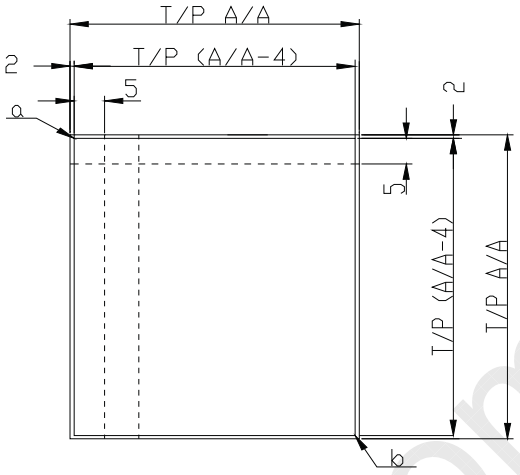
1. Linearity testing Method:

Linearity definition

Add DC5 voltage in x-axis and y-axis , use stylus push single point (X,Y). We can get the voltage value (Vx and Vy)….Fig.1

X Y direction each regards 5mm as the interval in the areas of A and B, it is the point measured that X Y overlaps the point of intersect of the cross interlocking….Fig.2




Draw in the output voltage of each measuring position into X Y direction voltage - position curve graph as Fig.3 And will lie between " a " and X (or Y) among " b " The electric potential difference of the direction is defined as " (Va-Vb) ,Can be in the theory voltage value and reducing and getting in the actual output voltage value of the measuring position of the measuring position among " a " and " b " " Vxi-Vxm "(or " Vyi-Vym " )

Linearity definition:

Linearity (X)= 〔 | Vxi-Vxm | /(Va-Vb) 〕×100%

Linearity (y)= 〔 | Vyi-Vym | /(Va-Vb) 〕×100%

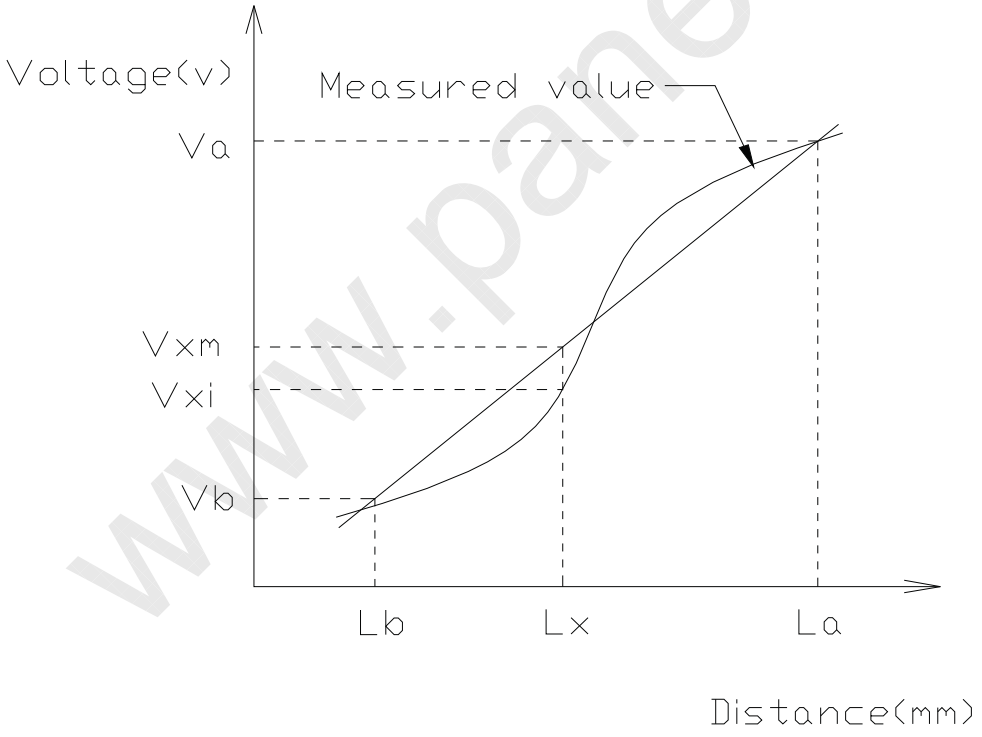
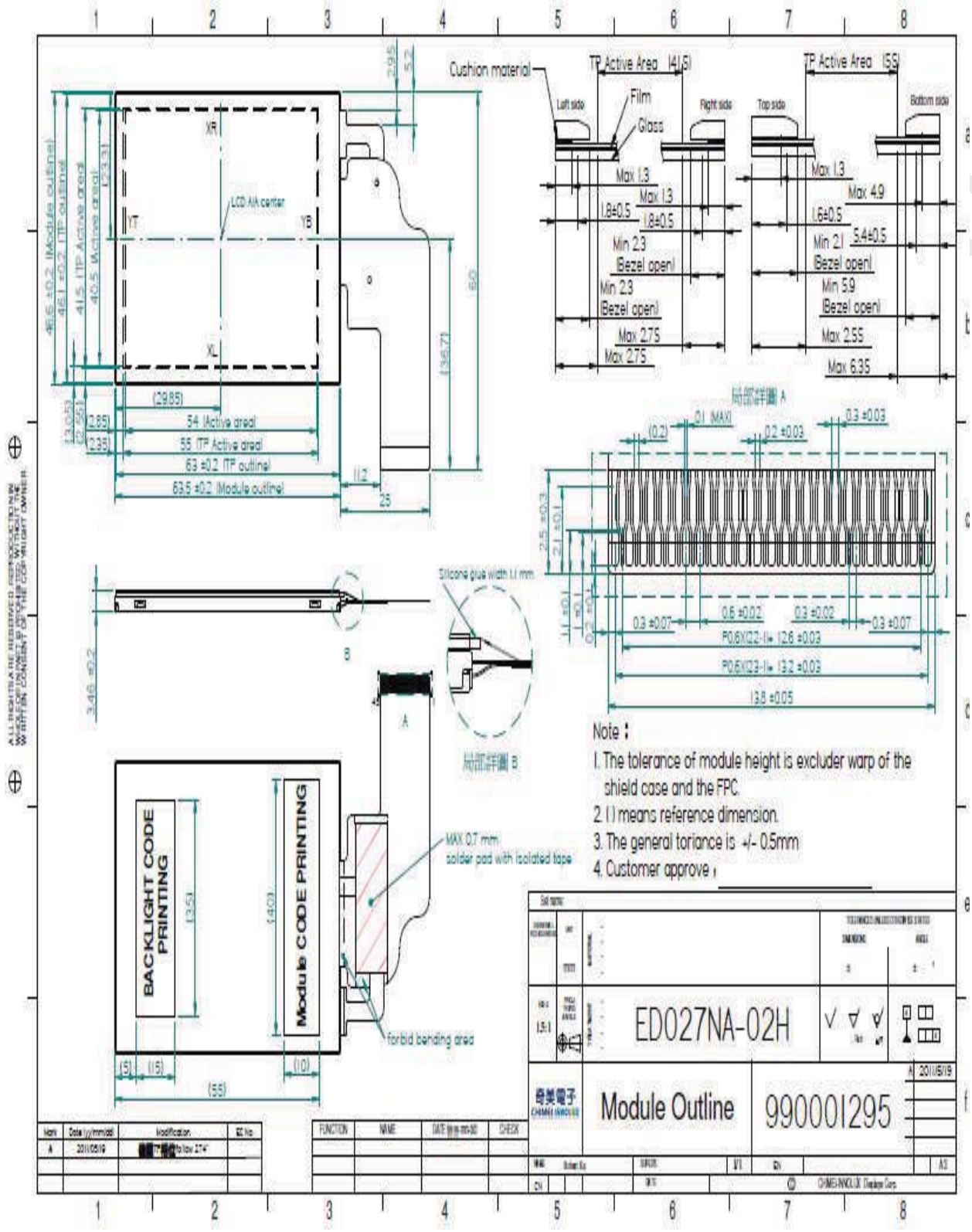
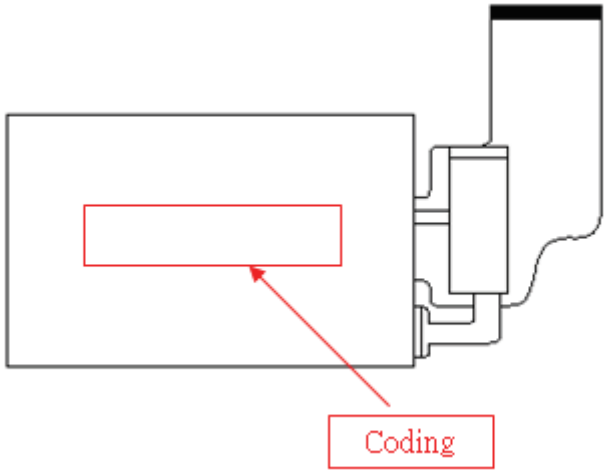



fig.3

## 14. Mechanical Drawing



**15. QR print code**

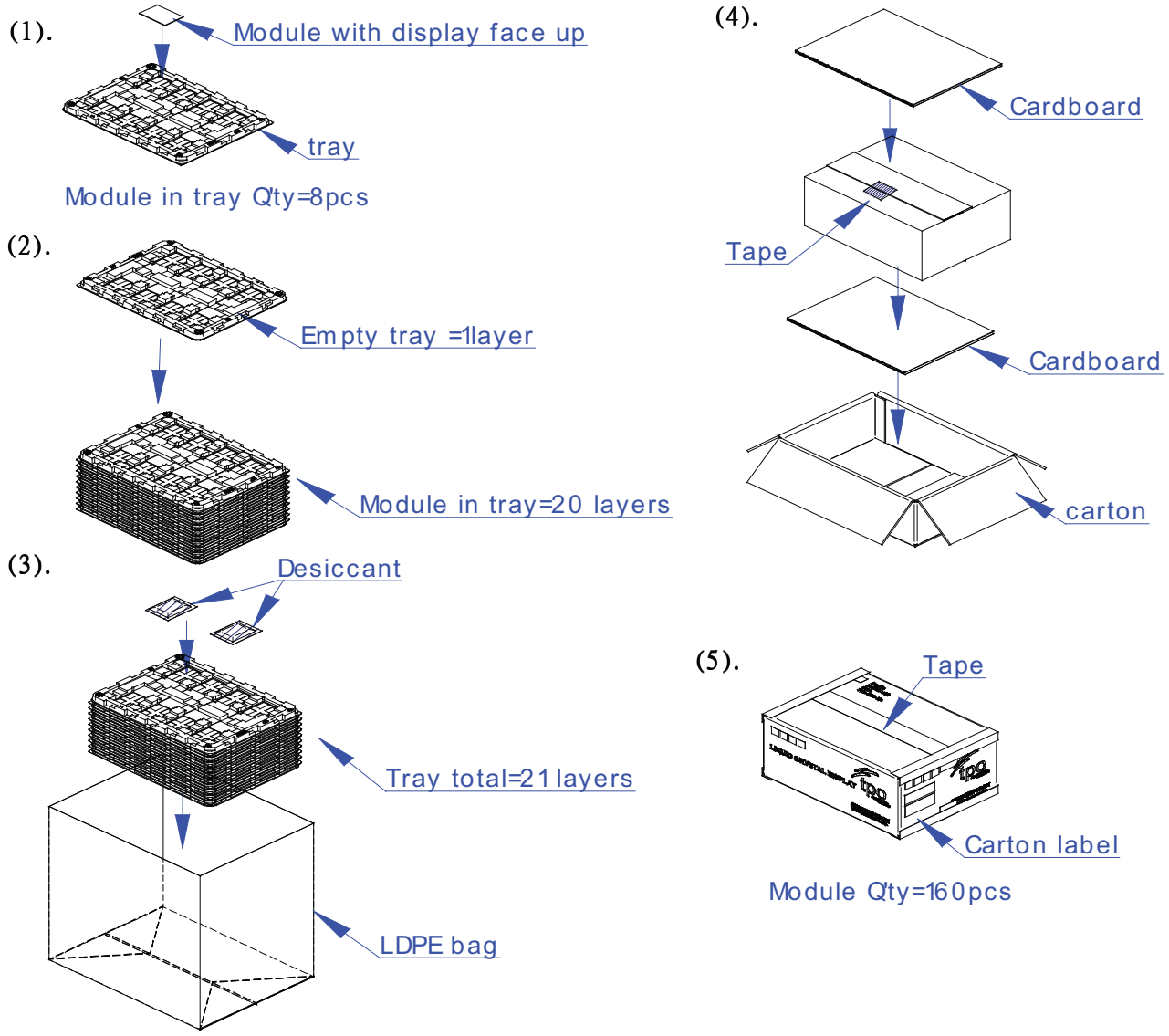



ED027NA-02H GZ0270NA00730
KEXXXXXXXX.XX (SN number)

Print rule of one piece code

SN number：Factory No Year–Month–Date–Serial No.
No.1 =Factory No.(K:LCM1 ; H:LCM2)
No.2 =Year("7"=2017)
No.3 –Month ("2"–Feb. ;A:Oct. ; B:Nov. ; C:Dec.)
No.4 =Day ("N"=22th)
( A:10th; B:11th; C:12th; D:13th; E:14th; F:15th; G:16th; H:17th; J:18th; K:19th; L:20th;M:21th; N:22th; P:23th; R:24th; S:25th; T:26th; V:27th; W:28th; X:29th; Y:30th; Z:31th)
No.5~10 =Serial number ("000001"; 000001~999999 reset by every day)

## 16. Packing Drawing




2.65" module (ED027NA-02H) delivery packing method

(1). Module packed into tray cavity (with Module display face up).

(2). Tray stacking with 20 layers and with 1 empty tray above the stacking tray unit.
2pcs desiccant put above the empty tray

(3). Stacking tray unit put into the LDPE bag and fix by adhesive tape.

(4). Put 1pc cardboard inside the carton bottom, and then pack the package unit into the carton.
Put 1pc cardboard above the package unit.

(5). Carton tapping with adhesive tape.