HCR 71821 Digital Transceiver

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1. **Introduction**

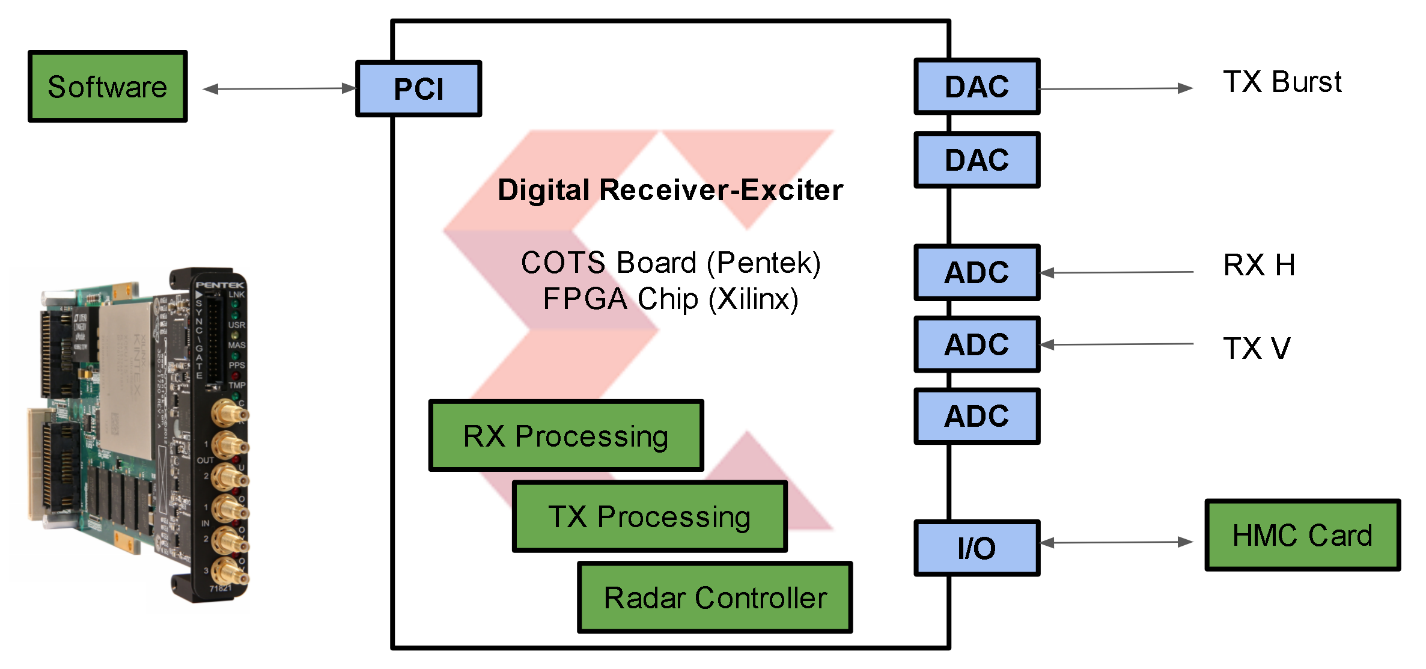
The HAIPER Cloud Radar (HCR) is a 94GHz airborne radar with Alternating Transmit Simultaneous Receive (ATSR) polarimetry. The Digital Transceiver (DRX) is based on the Pentek 71821 XMC card. It resides in a CompactPCI-based host.

1. **Digital Transceiver Overview**

The digital transceiver is a commercial XMC circuit board produced by Pentek, model number 71821. The 71821 contains the following:

* Three, 16 bit analog to digital converters (ADCs), up to 200 MHz
* Two, 16 bit digital to analog converters (DACs), up to 800 MHz
* Xilinx KU060 FPGA
* Five GB of DDR4 SDRAM (disabled to save power)
* A PCIe interface, bridged to PCI on the carrier card
* LVDS inputs and outputs (I/O) connected to the FPGA

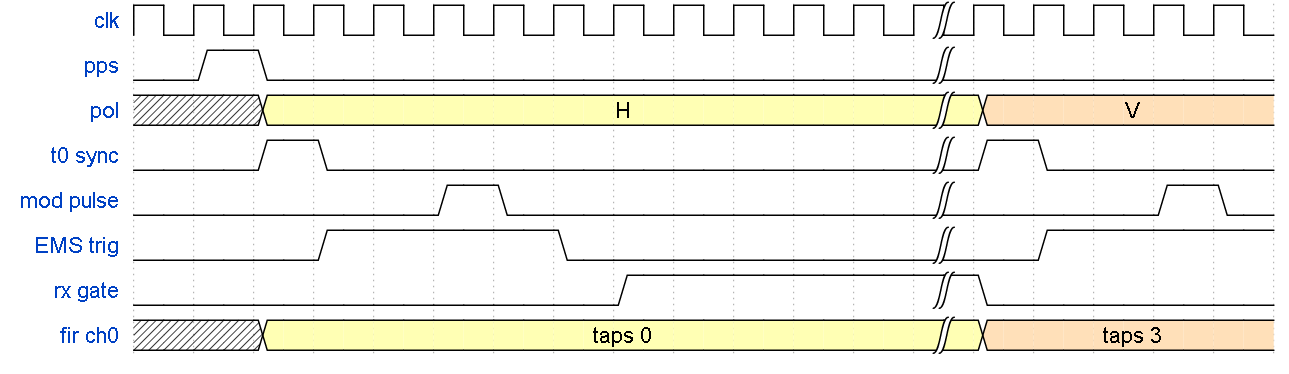
Although Pentek provides significant firmware infrastructure in the 78821, significant firmware customization is employed to suit the DRX application.



The primary components of the DRX are the TX Processing, RX processing, and the Radar Controller.

1. **Radar Controller**

The Radar Controller is responsible for managing the radar timeline. It does this via control lines to the TX and RX blocks, and to external systems through I/O lines to the Health Monitoring Card (HMC).

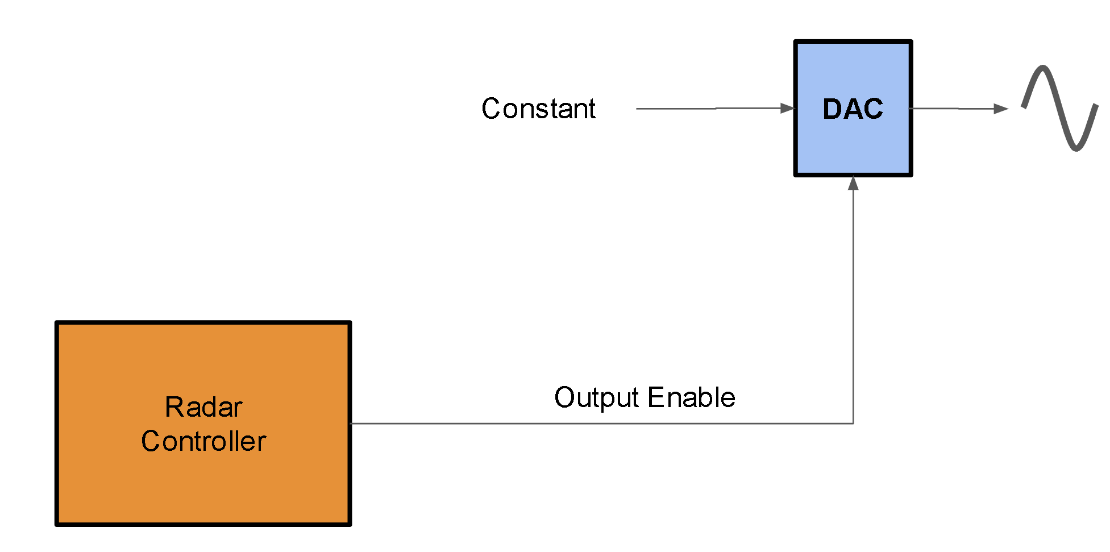


After the controller is configured and activated, it waits for a Pulse Per Second. It then begins issuing blocks of pulses. Each block has its own set of timings. The blocks are cycled through in turn. The bounds of this loop are configurable on-the-fly, for example one can be running Block 1 only, then select Blocks 3 through 5. The configurable parameters for each block are:

* The number of pulses in the block
* Pulse Repetition Time – single PRT or two PRTs staggered
* Eight counters (pulse widths and offsets), which include a synchronization pulse, EMS (latching RF circulator) control triggers, transmit modulation pulse, receive framing pulse.
* Polarization (H, V, or HHVV)
* Receiver filter tap bank select

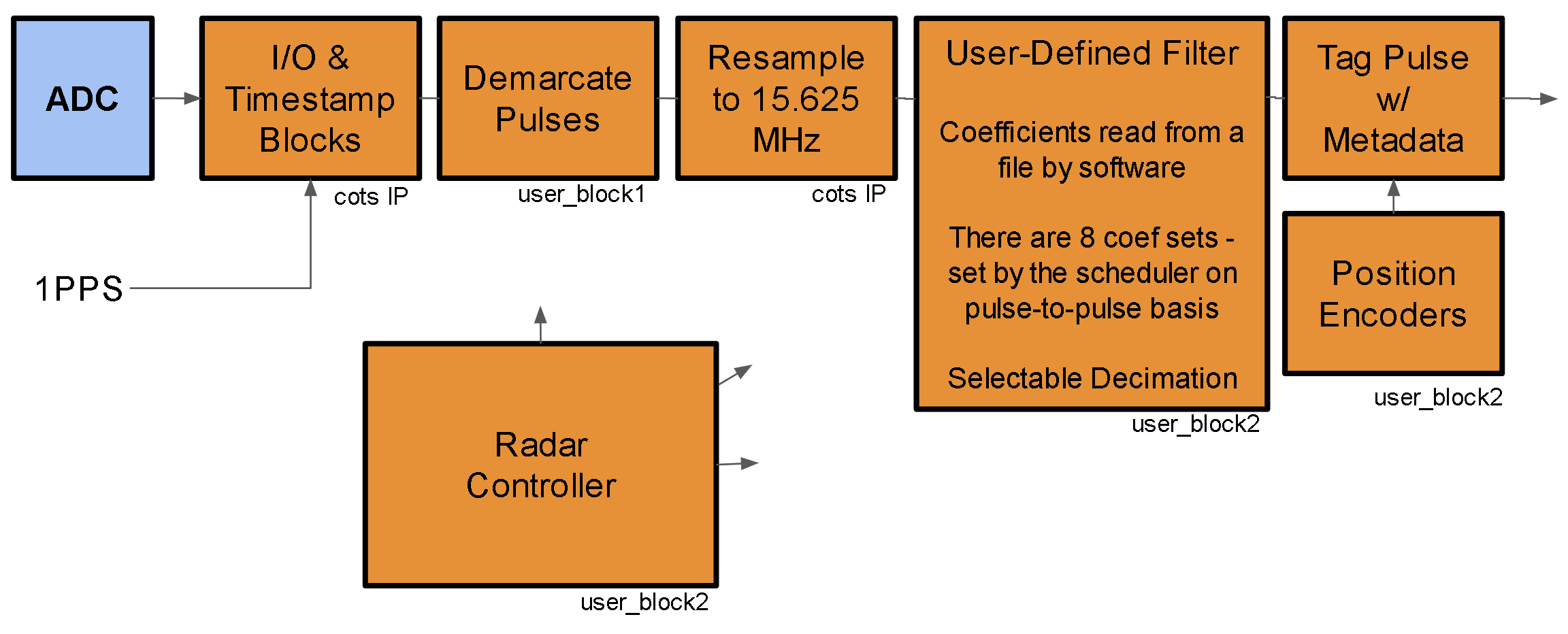
Example Schedule:  
 Block 1: 100 pulses, V transmit, 512ns pulse, PRT 1  
 Block 2: 100 pulses, V transmit, 256ns pulse, PRT2  
 Block 3: 100 pulses, H transmit, 512ns pulse, PRT1  
 Block 4: 120 pulses, HHVV, 256ns pulse, PRT3 & PRT4

1. **Transmit Processing**



The transmitter is relatively simple. The DAC’s modulator is programmed to the desired frequency and left to free-run. A fixed value is sent to the DAC. The Radar Controller’s TX timer is linked to the DAC’s Output Enable line.

1. **Receive Processing**



The receive processing pipeline is a mix of vendor-provided and custom blocks. Two channels are used, one for Horizontal and one for Vertical polarization. In the vendor blocks, the ADC inputs are timestamped, and transformed from the real-only Intermediate Frequency (IF) representation to a baseband I/Q representation. They are then resampled to 15.625 MHz. The user-defined blocks then apply a custom FIR filter, which has eight coefficient sets. The filter is typically a Gaussian shape matched to the pulse width. Since a schedule can cycle between several pulse widths, at the start of each pulse the Radar Controller selects the appropriate coefficient set. After this filter a configurable decimation is applied.

Finally the pipeline frames the data into pulses, and prepends a metadata block to each pulse. By default, the vendor DMA controller issues an interrupt each time the GATE framing signal goes from high to low. Due to the high pulse rate this behavior is undesirable. Therefore, a configurable number of pulses are bunched together by trimming the dead time between them. The interrupt only fires at the end of the bundle. The drx software application should configure its buffer size to hold the entire bundle.