brandywine communications

PC104-SG

Synchronizable Clock with PC104 Interface
Operation & Maintenance Manual

18 February 1997
P/N 8000003

Built exclusively for Brandywine Communications
By
JXI-2
2308 Lake Omega St.
El Paso
TX 79936
USA

phone: 915-856-0241
fax: 915-856-0245

Introduction

The PC104-SG is a digital clock with a PC-104 interface that will automatically synchronize to time reference signals. Programs running on the PC-104 host can read the clock time directly from registers. In many applications, no other user programming is needed. The advantages of the PC104-SG's digital clock over the host system include better resolution (µsec vs. 18 msec), easier access (single C statement vs. DOS system call) and - most importantly - stability and synchronization - ultimately to Universal Coordinated Time by locking to time reference signals.

The time reference signals can be standardized modulated "time code" signals like IRIG-B, IRIG-A, NASA-36, 2137 or XR3. Or, the reference can be a 1 PPS time pulse from a GPS or LORAN receiver. Even though the time reference occurs as slowly as once per second, the on-board clock maintains specified accuracy and resolution by using a phase locked 10MHz crystal oscillator. The user program can specify the propagation delay from the time code source to the PC104 or the 1 PPS source to the PC104 and the PC104-SG will automatically adjust the clock to compensate for the delay. A redundancy feature allows BOTH a 1 PPS signal and a time code to be used as references. The user can specify which reference is preferred. If the preferred reference is invalid, the secondary reference is used until the primary becomes valid again.

In addition to the registers that latch the time when a user program reads the clock, a second set of time registers is used to accurately capture the time of external "time tag" pulses (with 100 nanosecond resolution). Because external pulses may occur at unpredictable times a PC104 bus interrupt may be enabled by the user to signal the occurrence of an external event and cause the captured time to be stored in host memory, With modern host processor speeds, external pulse spacing as low as 20 µseconds may be supported.

Three user selected pulse rates from 1.5 Mpps to 45.77 PPS are locked to the clock frequency. One of the selected rates can cause "heartbeat" interrupts to periodically wake up host processes. The user program also has direct access to a comparator for generating "match" pulses or toggles at precise times.

The PC104-SG is designed so that the most common user applications require the least programming. For example, reading current time can be accomplished with a single C statement. Data and parameters that need fast access and update are assigned individual registers directly accessible over the PC104 bus, while a much larger number of infrequently (if ever) accessed status and control parameters are accessed by a Dual Port Ram occupying only two PC104 bus addresses.

Sample "C" source programs and definition files are supplied to speed programming operations.

The -AE2 option adds two additional time tag inputs at the P10 connector.

Rev B and later modules include a separate I/O connector for stacked connection to Zeli Systems SATPAK GPS receiver modules. A D/A converter option allows 10 MHz oscillator steering in addition to the standard time discipling. The -HQ option allows synchronizing to GPS satellite time from a user furnished GPS receiver with Havequick output (PLGR).

SPECIFICATIONS

Physical:	
Dimensions:	**3.550 in. X 3.775 in. (PC/104)**
Power:	**+5V ±5% .10A min.., .15A max.**
If modulated code in/out	**+12V± 5%: .06A typ. .10A max.**
If modulated code out-12V± 5%:	**.025A typ. .05A max.**
Fabrication:	**1.68 mm±.2 mm (.062 in±008 in.) FR4, 4 layer**
Temperature:	**0 to 55C operating, -40C to 85C storage**
Humidity:	**0 to 99% non-condensing**
Inputs:	
Input connector(mating supplied)	**5 pin (Molex 22-11-2052)**
Code input types:	**Modulated IRIG-A, B, NASA36. Check with factory for XR3, 2137 and IRIG-G**
Code input amplitude:	**150 mV to 10V pk/pk**
Code input modulation ratio:	**2:1 to 4:1**
Code input frequency error:	**100 PPM maximum**
Code input impedance:	**>10K**
Sync accuracy:	**IRIG-B, NASA36: 20µsec IRIG-A: 5 µsec 1PPS: 1µsec**
External event pulse input:	**Rising edge TTL**
Minimum event to event spacing (host interrupt mode):	**Limited only by host speed**
Minimum event to event spacing (RAM buffer mode):	**250 µsec**
1PPS input:	**TTL level positive edge**
Outputs:	
Modulated IRIG-B (option):	**2.5V±10% pk/pk into 600Ω**
DC Level Shift IRIG–B:	**TTL level**
Match:	**TTL pulse**
Status (Red LED):	**Flashes coded patterns**
Bus Interface (I/O Mapped)	
Base Address (factory configuration 300)	**2A0, 2C0, 2E0, 300, 320, 340,360 Foe -AE2 option: 240,280,2C0,300,340,380,3C0**
IRQ Levels (requires -P2 option)	**IRQ10, 11, 12, 15**

Register Assignments: ("(x)" for external event time latches)

Offset from Base ADDR	Bits Bit 0 is LSB	Read Usage	Write Usage
0	7..0	External Event RAM buffer	Read only
1		Status	Interrupt Enable
	7	External Event Interrupt Enable	External Event Interrupt Enable
	6	MATCH Flag Interrupt Enable	MATCH Flag Interrupt Enable
	5	Heartbeat Flag Interrupt Enable	Heartbeat Flag Interrupt Enable
	4	Heartbeat Flag	0 = Reset Heartbeat flag
	3	MATCH Flag	0 = Reset Match flag
	2	RAM FIFO buffer data available	0 = Simulate External Event
	1	In sync flag	0 = Release Board Reset
	0	External data latched flag	0 = Set Board Reset
2	7..0	Dual port data	Dual port data
3	4	n/u	
	3	n/u	
	2	External event polarity (0 = pos. edge, 1 = neg. edge)	External event polarity
	1	1 = Dual Port RAM Response Ready	
	0	1 = Dual Port Ram Write Not Ready 0 = Ready	
4	7	Time tag #2 data available (-AE2 option)	Read only
	6	Time tag #2 interrupt enable (-AE2 option)	Time tag #2 interrupt enable
	5	Time tag #1 data available (-AE2 option)	Read only
	4	Time tag #1 interrupt enable (-AE2 option)	Time tag #1 interrupt enable
	3	Time tag #2 polarity (0=pos. edge, 1=neg. edge) (-AE2 option)	Additional time tag #2 polarity
	2	Time tag #1 polarity (0=pos. edge, 1=neg. edge) (-AE2 option)	Additional time tag #1 polarity
	1..0	n/u	n/u
5	7..0	n/u	Match Time 10µs, 1µs
6	7..0	n/u	Dual Port RAM address
7	7..0	10s, 1s of years (if in code or set by user)	Match Time 1ms, 100µs
8	7..0	100s, 10s of days BCD time	n/u
9	7..0	1s of days , 10s of hours BCD time	n/u
A	7..0	1s of hours , 10s of minutes BCD time	n/u
B	7..0	1s of minutes 10s of seconds BCD time	n/u
C	7..0	1s of seconds, 100s of milliseconds BCD time	n/u
D	7..0	10s, 1s of milliseconds BCD time	n/u
E	7..0	100s, 10s of µseconds BCD time	n/u
F	7..0	1s of µseconds 100s of nsec BCD time. Reading base + 0F latches higher order time digits in base + 6..base + 0E	n/u
17	7..0	Ext. time tag 10s, 1s of years (if in code or set by user)	n/u
18	7..0	Ext. time tag 100s, 10s of days BCD time	n/u
19	7..0	Ext. time tag 1s of days , 10s of hours BCD time	n/u
1A	7..0	Ext. time tag 1s of hours , 10s of minutes BCD time	n/u
1B	7..0	Ext. time tag 1s of minutes 10s of seconds BCD time	n/u
1C	7..0	Ext. time tag 1s of seconds, 100s of milliseconds BCD time	n/u
1D	7..0	Ext. time tag 10s, 1s of milliseconds BCD time	n/u
1E	7..0	Ext. time tag 100s, 10s of µseconds BCD time	n/u
1F	7..0	Ext. time tag 1s of µseconds 100s of nsec BCD time. LOCATIONS 27..3F APPLY TO -AE2 OPTION ONLY	n/u
27	7..0	Time tag #1 10s, 1s of years (if in code or set by user)	n/u
28	7..0	Time tag #1 100s, 10s of days BCD time	n/u
29	7..0	Time tag #1 1s of days , 10s of hours BCD time	n/u
2A	7..0	Time tag #1 1s of hours , 10s of minutes BCD time	n/u
2B	7..0	Time tag #1 1s of minutes 10s of seconds BCD time	n/u
2C	7..0	Time tag #1 1s of seconds, 100s of milliseconds BCD time	n/u
2D	7..0	Time tag #1 10s, 1s of milliseconds BCD time	n/u
2E	7..0	Time tag #1 100s, 10s of µseconds BCD time	n/u
2F	7..0	Time tag #1 1s of µseconds 100s of nsec BCD time.	n/u
37	7..0	Time tag #2 10s, 1s of years (if in code or set by user)	n/u
38	7..0	Time tag #2 100s, 10s of days BCD time	n/u
39	7..0	Time tag #2 1s of days , 10s of hours BCD time	n/u
3A	7..0	Time tag #2 1s of hours , 10s of minutes BCD time	n/u
3B	7..0	Time tag #2 1s of minutes 10s of seconds BCD time	n/u
3C	7..0	Time tag #2 1s of seconds, 100s of milliseconds BCD time	n/u
3D	7..0	Time tag #2 10s, 1s of milliseconds BCD time	n/u
3E	7..0	Time tag #2 100s, 10s of µseconds BCD time	n/u
3F	7..0	Time tag #2 1s of µseconds 100s of nsec BCD time.	n/u

INPUT/OUTPUT CONNECTIONS

Reference Signal Input/Output (P6)

Type: (Molex 22-11-2052)
Pin 1: Time Code Input ("+" side if balanced input)
Pin 2: Time Code Input Ground (or "-" side if balanced input)
Pin 3: 1 PPS TTL level reference input
Pin 4: Optional modulated time code output
Pin 5: Ground

TTL level Input/Output (P10)

Type: 10 pin right angle unshrouded header
Pin 1: n/u
Pin 2: n/u
Pin 3: External time tag TTL level pulse input
Pin 4: IRIG-B DC level shift TTL level output
Pin 5: User programmable low rate TTL output
Pin 6: Match register TTL level output
Pin 7: -AE2 option: Additional Time tag 1 TTL level input
-GR, -GM, -GT option: serial TTL level GPS data in (from GPS receiver TTL level output)
Pin 8: User programmable Heartbeat TTL output
Pin 9: -AE2 option: Additional Time tag 2 TTL level input
-GR,-GM,-GT option: serial TTL level GPS interface out (to GPS receiver TTL level input)
Pin 10: User programmable pulse rate #3 TTL output

PC/104 Bus Connector (P1)

(per PC104 specification)

PC/104 Bus Connector (P2) (-P2 option only)

(per PC104 specification)

Stackable GPS Receiver I/O (P11) (-GM, -GR, -GT option only)

Pinouts compatible with Zeli Systems SATPAK-104 GPS Receiver carriers. Allows GPS receiver I/O without interconnecting cables by stacking SATPAK-104 and PC104-SG (Rev B and later only).

Havequick Receiver Input (P11) (-HQ option only)

Pin 1: Havequick Serial TTL Data (connect to Plugger Pin 7)
Pin 8: Havequick 1PPS (0/10V 50 ohm source impedance) (connecto to Plugger Pin 6)
Pin 9: Havequick Ground (Connect to Plugger Pin 2)
Pin 2,3,4,5,6,7,10: No Connect. MAKE NO CONNECTIONS.

CONFIGURATION, INSTALLATION & OPERATION

Configuration:

The user should check that the configuration of PC104-SG matches the configuration that is required by the user application. Factory default configurations are shown below.

PC/104 Base Address Configuration (P3)

The PC104-SG uses 20 (hex) contiguous I/O space addresses (40 hex for -AE2 option). The first (base) address is configured by P4 and decoded by U1. Assuming U1 is the standard 951007A pattern the possible I/O Base address configurations are:

I/O Base address (hexadecimal)	S1 jumper	S2 jumper	S4 jumper	
disabled	off	off	off	
2A0	off	on	on	
2C0	off	off	on	
2E0	off	on	off	
300	on	on	on	← factory configuration
320	on	off	on	
340	on	on	off	
360	on	off	off	

Units with the -AE2 option (assuming U1 is 960315A pattern):

I/O Base address (hexadecimal)	S1 jumper	S2 jumper	S4 jumper	
disabled	off	off	off	
2C0	off	on	on	
240	off	off	on	
380	off	on	off	
300	on	on	on	← factory configuration
280	on	off	on	
3C0	on	on	off	
340	on	off	off	

Interrupt Request Level (P4) (-P2 option ONLY)

P4 configures the IRQ level and shared/unshared mode. If the -P2 option (16 bit passthrough connector in location P2) is not installed, the P4 settings are irrelevant.

IRQ level	10 jumper	11 jumper	12 jumper	15 jumper	
10	ON	OFF	OFF	OFF	← factory configuration
11	OFF	ON	OFF	OFF	
12	OFF	OFF	ON	OFF	
15	OFF	OFF	OFF	ON	
Not used	OFF	OFF	OFF	OFF	

ISA/Shared/Pulldown Interrupt (P4) (-P2 option ONLY)

P4 also configures IRQ level ISA/shared/pulldown mode. If the -P2 option (16 bit passthrough connector in location P2) is not installed, the P4 settings are irrelevant.

IRQ mode	P3-7/8 jumper	P3-9/10 jumper	
ISA	OFF	OFF	← factory configuration
SHARED/PULLDOWN	ON	ON	
SHARED/ NO PULLDOWN	ON	OFF	

The PC104 specification describes a interrupt sharing option which allows a given IRQ signal to be shared between multiple interrupt requesters. In shared interrupt mode, exactly one PC104 device should have the pulldown for a given IRQ level. So determine if the PC104-SG will share the selected IRQ level and whether the PC104--SG or the sharing device should have the pulldown.
In ISA mode, the IRQ line is **always** driven by U1. (High if requesting an interrupt, else low). In shared mode, U1 never drives the IRQ line low and drives IRQ high only when requesting an interrupt. When using shared mode, **exactly** one PC104 module should enable a 1K passive pulldown resistor for each IRQ level that is used. The P3-9/10 jumper enables the passive pulldown on the PC104-SG.

Installation

The PC104 system should be powered down before the PC104-SG is added. Plug the PC104-SG into the appropriate location in the stack using the spacers provided with the PC104-SG for mechanical stability.

Double check and record configuration settings before stacking other PC104 modules on the PC104-SG.

Attach inputs and outputs before applying power to the PC104 stack.

If using the PC104-SG with the Zeli Systems SATPAK-104, connect the GPS TTL level I/O signals to P10 and the TTL level 1 PPS signal to P6 (pin 3).

Apply power.

OPERATION

The PC104-SG will start operation automatically when the PC104 bus RESET signal goes low. No manual operator intervention is possible or required.

LED Status Indication

Observe LED1 flashing pattern and verify appropriate status. LED1 will flash the DP_Extd_Sts (extended status) contents. A “1” bit will flash LONG and a “0” bit will flash SHORT. Trailing “0” bits
are not flashed. Bit 0 is sent first, then bit 1 etc:

Bit	“1”	“0”
0	On-board clock has not been verified to be within DP_Syncthr in last 5 seconds. Caused by bad or missing reference or by on-board clock catching up to reference.	On board clock has been verified to be within DP_Syncthr of reference in last 5 seconds.
1	Input time code unreadable Caused by incorrect time code selection, disconnected time code input, time code signal level bad, time jumps in input time code. Does not indicate a problem if GPS or 1 PPS is only clock reference.	Input time code readable
2	1 PPS pulses not 1 second apart. Cause by missing 1 PPS input, or invalid 1 PPS input. Does not indicate an error if only time code input is to be used for the clock reference.	1 PPS pulses appear OK
3	Major time has not been set for 1PPS input. If 1 PPS is only reference, user should set major time (seconds..years) using dual port RAM. Otherwise years..seconds are not synchronized to UTC. The -GR,-GM,-GT options set major time internally	Major time has been set
4	Years digits have not been set. Time codes do not contain year digits. If the user wishes the year digits to be valid, use DP Ram and the Set Year command. Years must be set for the on-board clock to know to count from 365 days to 366 days on the last day of a leap year.	Years have been set.

PROGRAMMING

Introduction

The PC104-SG is designed so that the most common user applications require the least programming. For example, reading current time can be accomplished with a single C statement. Data and parameters that need fast access and update are assigned individual registers directly accessible over the PC104 bus, while a much larger number of infrequently (if ever) accessed status and control parameters are accessed by a Dual Port Ram occupying only two PC104 bus addresses. The PC104DEF.H file in the program appendices contains the C source of the register definitions and the SGDPDEF.H file contains the Dual Port RAM assignments

Sample programs in the appendices show

1. Reading Current Time (`curtime.c`)
2. Reading External Time Tags using Interrupts (`extintr.c`)
3. Using the Match register to generate Match pulses at precise times (`mattime.c`)
4. Using the Dual Port RAM to initialize Major Time for timing using only 1 PPS time reference.(`setmajor.c`)
5. Using the RAM FIFO Port to buffer External Time Tags (`ramfifo.c`)
6. Using the Dual Port RAM to specify a Heartbeat Rate(`heart.c`)

Reading Current Time

The first I/O read operation (to address BASE+Usec1_Nsec100_Port) latches all the other current time bytes at same time. The clock continues to run and the LATCHED data for all the other digits may be read across the PC104 bus by following reads. So, the BASE+Usec1_Nsec100_Port must **always** be read before the other latched time ports are read - even if the user is uninterested in the units of microseconds and 100s of nanoseconds digits. The remaining latched time ports may be read in any order. Or, some may be ignored to reduce the amount of stored data or to speed up time reading. The 100 Nsec through 100 Millisecond bits remain latched until BASE+Usec1_Nsec100_Port is read again. The 200 millisecond through 80 years bits remain latched for at least 90 milliseconds after BASE+Usec1_Nsec100_Port is read.

Example: Reads current time with a single C statement:

```
for (i= Usec1_Nsec100_Port;i >= Year10_Year1_Port;i--)
      {timebyte[i-Year10_Year1_Port]= inp (BASE+i);}
```

will set timebyte[8] = current time (units of μsec, 100s of nsec)
timebyte[7]= current time (100s of μsec, 10s of μsec)
timebyte[6]= current time (10s of milliseconds, units of milliseconds)
timebyte[5]= current time (units of seconds, 100s of milliseconds)
timebyte[4]= current time (units of minutes, 10s of seconds)
timebyte[3]= current time (units of hours, 10s of minutes)
timebyte[2]= current time (units of days, 10s of hours)
timebyte[1]= current time (100s of days, 10s of days)
timebyte[0]= current time (10s of years, units of years)

Reading Status/ Enabling Interrupts in Status_Port.

Status_Port bit 0: Ext_Ready bit (READ ONLY) will be “1” if an External Time Tag pulse has occurred since the last read of any of the ExternalTime Tag data registers. It will be cleared when any of the External Time Tag data registers are read across the PC104 bus. See Status_Port bit 7.

Status _Port bit 1: The Sync_OK status bit (READ ONLY) will be “1” if the PC104 clock is synchronized to a time reference input. More extensive time synchronization status information can be read from the dual port RAM DP_Extd_Sts location.

Status_Port bit 2: The RAM_FIFO_Ready status bit (READ ONLY) will be “1” if there is PC104-SG FIFO buffered data available. Reading the RAM_FIFO_Port will clear RAM_FIFO_Ready until the next data byte is available.

Status Port bit 3: The Match bit (READ ONLY) toggles when the time programmed into Match_Usec10Usec1_Port and Match_Msec1_Usec100_Port matches the clock time. The Heartbeat latch can be cleared by writing Reset_Match to the Reset_Port.

Status Port bit 4: The Heartbeat bit (READ ONLY) is set when a heartbeat pulse occurs at the HRTPIN output of P10. The heartbeat is generated by dividing a 3 MHz signal by a user programmed divisor of 2 to 65535 (default divisor is 300 for 10K PPS heartbeat). The Heartbeat latch is cleared by writing Reset_Heartbeat to the Reset_Port.

Status_Port bit 5: The Heartbeat_Int_Enb bit (READ/WRITE) disables PC104-SG Heartbeat interrupts if 0 . If it is “1” and the Heartbeat latch bit is “1” the PC104-SG will assert the PC104 bus IRQ signal configured by P4. For an interrupt to occur and be vectored to user code requires that the host processor PIC (priority interrupt controller) be programmed to recognize the IRQ signal and generate the vector.

Status_Port bit 6: The Match_Int_Enb bit (READ/WRITE) disables PC104-SG Match interrupts if 0 . If it is “1” and the Match bit is “1” the PC104-SG will assert the PC104 bus IRQ signal configured by P4. For an interrupt to occur and be vectored to user code requires that the host processor PIC (priority interrupt controller) be programmed to recognize the IRQ signal and generate the vector.

Status_Port bit 7: The Ext_Ready_Int_Enb bit (READ/WRITE) =1 causes the user configured IRQ (“interrupt request”) level (factory configuration is IRQ 10) PC104 bus signal to be asserted if the Ext_Ready bit is also set. For an interrupt to occur and be vectored to user code requires that the host processor PIC (priority interrupt controller) be programmed to recognize the IRQ signal and generate the vector.

Reading External Time Tags

The simplest and fastest way to read external time tags uses the PC104-SG external time tag latches which may be read directly across the PC104 bus:

An example reads External Time Tag data with a single C statement:

```
for (i= Ext_Usec1_Nsec100_Port;i >= Ext_Year10_Year1_Port;i--)
      {timebyte[i-Ext_Year10_Year1_Port]= inp (BASE+i);}
```

will set timebyte[8] = time tag (units of μsec, 100s of nsec)
timebyte[7]= time tag (100s of μsec, 10s of μsec)
timebyte[6]= time tag (10s of milliseconds, units of milliseconds)
timebyte[5]= time tag (units of seconds, 100s of milliseconds)
timebyte[4]= time tag (units of minutes, 10s of seconds)
timebyte[3]= time tag(units of hours, 10s of minutes)

timebyte[2]= time tag(units of days, 10s of hours)
timebyte[1]= time tag(100s of days, 10s of days)
timebyte[0]= time tag (10s of years, units of years)

The external time tag latches can be read in any order and the user can select any or all bytes to read. When any of the external time tag latch ports are read, the External Time Tag Data Ready flag in Status_Register_Port is cleared. The 100 Nsec through 100 Millisecond bits remain latched until another external time tag occurs. The 200 millisecond through 80 years bits remain latched for at least 90 milliseconds after the external time tag occurs.

Simulating External Time Tags

For program testing purposes the user can simulate the occurrence of an external time tag by writing Trigger_Sim_Ext_Time_Tag to the Reset_Port.

Reading External Time Tags Using Interrupts

Reading external time tags at high tag rates is most efficiently accomplished by using the interrupt capabilities of the PC104-SG. The EXTINTR.C program in the appendix is an example of using External Time Tag Interrupts. The setvects() function call stores the previous interrupt vector and sets up a new vector pointing to the interrupt handler for the PC104-SG. The i_enable call sets the Interrupt Mask Register of the appropriate Priority Interrupt Controller to “0” to let it recognize when the IRQ line is asserted and enables the PC104-SG to drive the IRQ line if the Ext_Ready status is set. It is important for the user program to make a i_disable() call and a res_vects call before exiting so that the interrupts can be disabled and the previous vector restored.

Reading 2 Additional time tags (-AE2 option)

The -AE2 option adds two extra sets of time tag registers and two additional sets of interrupt enable and tag ready status bits per the register section in the Specifications. The two extra sets are programmed like the standard time tag except for the different and/or bit assignments.

Using the RAM FIFO to Buffer External Time Tags

A second way to read external time tags is to order the PC104-SG to store time tag data in an internal RAM First-In First-Out (FIFO) buffer. The RAM FIFO buffer can only be used with the standard external time tag. It does not apply to the 2 additional time tags of the -AE2 option. The on-board microprocessor will copy a byte at a time from the FIFO to the RAM_FIFO_Port as the user reads the RAM FIFO Port. The RAM FIFO approach is less efficient because of the byte at a time transfer from microprocessor to RAM FIFO Port and limited in minimum spacing between external events of 250 µsec but may be useful in cases where the user does not wish to use External Time Tag interrupts or polling of the Ext_Ready status bit. The size of the RAM FIFO is 2048 bytes. The default order of data in the RAM FIFO for each external time tag is:

1st Byte:	0xffH synchronizing byte
2nd Byte	External time tag 1µsec, 100 nsec digits
3rd byte	External time tag 100 µsec 10µsec digits
4th byte	External time tag 10 msec, 1msec digits
5th byte	External time tag 100 msec, 0 digits
6th byte	External time tag 10sec, 1sec digits
7th byte	External time tag 10 min, 1 min digits
8th byte	External time tag 10 hours 1 hour digits

9th byte External time tag 10 days 1 days digits
10th byte External time tag 1 years 100 days digits

See the “Sending Commands through the Dual Port RAM” in Dual Port RAM section for enabling RAM_FIFO_Port time tags. To reduce the transfer of unneeded data and increase the number of time tags that may be stored in the FIFO, the user can change the RAM FIFO First/Count digits in the Dual Port RAM.

Time Match Pulses/Toggles

The Match bit of the Status_Port toggles when the time programmed into Match_Usec10Usec1 and Match_Msec1_Usec100 matches the clock time. The MATCH bit is also output to a connector for use in triggering or gating other equipment. The user may clear the MATCH bit by writing Reset_Match to the Reset_Port. Depending on the application it may be desirable to clear MATCH right away (for example if the user is trying to generate a set of closely spaced pulses. In other applications (for example generating a logic gate enabling a A/D converter) MATCH may be allowed to remain set for longer times until another clock value is matched to toggle it off. Before writing new Match register settings, the user should write 0xFF (which cannot be matched) into both Match registers to avoid false matches.
Note that the Time Match only applies to 1 μsec through 8 msec bits. It is the user’s responsibility to check for correct upcoming 10 millisecond interval before writing the Match time registers. Refer to the Match_Int_Enb bit of the Status_Register for causing interrupts when Match times occur.

Heartbeat Pulses and Interrupts

The Heartbeat bit of the Status_Port will be set when a heartbeat pulse occurs at the HRTPIN of connector P10. HRTPIN is driven by the output pulses from a 82C54 programmable counter driven at 3 MHz. The 3 MHz is divided by a user controllable divisor of 2 to 65535 (default 300) to control the heartbeat rate. Refer to the Heart_Int_Enb bit of the Status_Register for causing interrupts when heartbeats occur. The heartbeat rate may be changed using the dual port RAM.

Dual Port RAM for Supplementary Status/Control

A 256 byte dual port RAM on the PC104-SG shares access between the microprocessor in the PC104-SG and the host PC104 computer. The first 128 locations are READ ONLY from the PC-104 bus. The last 128 locations are READ/WRITE from the PC-104 bus and are initialized after reset by the on-board processor. The dual port address assignments are listed in the SGDPDEF.H listing in the appendices.

Accessing Dual Port RAM

To reduce the number of I/O bus addresses needed for the dual port RAM, it is accessed over the PC104 bus in a two step operation. First, the user write the dual port address byte to the Dual_Port_Address_Port. After checking the Response_Ready flag in the Extended_Status_Port the current contents of the dual port address selected are available in the Dual Port _Data_Port. To change the current contents of the selected address, the user program writes the new data to the Dual_Port_Data_Port. The write operation is complete when the Response_Ready flag in the Extended_Status_Port is asserted. As a double check of correct user programming user may then read the Dual_Port_Data_Port and compare the read value with the written value. If the user attempts to write into the first 128 addresses of the dual port RAM, the read value returned after the write attempt will be 0xFF, regardless of the actual RAM contents or the rejected write value. So, if the user sees the read values doesn’t match the write value it is an indication of a rejected dual port RAM access.

Because accessing the dual port RAM causes interrupts to the microprocessor on the PC104-SG, the user should limit dual port RAM access rates to less than 2500 per second to avoid interfering with other PC104-SG functions. If the PC104-SG is being used with a reference input signal with large (over 1000 PPM) frequency error the dual port RAM access rates should be limited to 500 per second. These limitations should not limit the usability of the PC104-SG because dual port RAM is used only for data and control/status functions change infrequently.

Example:

```
/* Specify dual port address */
              outp (BASE+Dual_Port_Address_Port,DP_Control);
/* wait for PC104 to fetch old value */
              while (!inp((BASE+Extended_Status_Port )&Response_Ready) {;}
/* Calculate new DP_Control  value */
       new =(inp(BASE+Dual_Port_Data_Port) ||DP_Control_CodePriority)
/* write new value to DP RAM */
       outp (BASE+Dual_Port_Data_Port,new);
/* wait for PC104 to acknowledge */
       while (!inp((BASE+Extended_Status_Port )&Response_Ready) {;}
       if (inp(BASE+Dual_Port_Data_Port) != new) {user program error }
```

Sending Commands through the Dual Port RAM.

The DP_Command location in the dual port RAM is used to send commands to the PC104-SG. Illegal commands will be echoed as 0xFF. The legal commands are:

Command_Set_Major copies time from dual port major time locations to clock
Command_Set_Years copies time from dual port years to clock
(To avoid incorrect clock settings when major time or year has only been partially initialized, the commands signal from the user to the PC104 that the major time or year is ready to use.)
Command_Set_RAM_FIFO tells the PC104-SG to use RAM_FIFO mode for External Time Tags
Command_Reset_RAM_FIFO tells the PC104-SG to stop using RAM_FIFO mode for External Time Tags.
Command_Clear_RAM_FIFO tells the PC104-SG to set the External RAM FIFO to empty.

Setting Leap Year Control in Dual Port RAM

The DP_Control_Leapyear bit of dual port RAM addressDP_Control_0 tells the PC-104SG if the current year is a leap year. Because time code inputs do not contain year information, the PC104-SG requires the user to tell the PC104-SG if the current year is a leap year. This information is only used by the PC104-SG at 365 days 23 hours 59 minutes 59 seconds (or 60 seconds if leap second day =365) to determine if the next day should be 366 (leap year control =1) or 001 (leap year control =0). The DP_Control_Leapyear flag is initialized to 0 when the PC104-SG does power -on reset. If set incorrectly, the PC104-SG will detect the correct new day about half a time code frame into the new day (.5 seconds for IRIG-B, NASA36, 2137 or .05 seconds for IRIG-A, .005 seconds for IRIG-G) and set the onboard clock time to the correct value. The DP_Control_Leapyear bit is only used if the year in the DP_Year10_Year1 and DP_Year1000_Year100 locations is invalid. If they are valid, the PC104-SG can automatically determine leap year status.

If the only reference input to the 104-SG is a 1 PPS pulse it is VERY IMPORTANT to maintain the correct value of the DP_Control_Leapyear bit or to set the year in the DP_Year1000_Year100 and

DP_Year10_Year1 locations. If correct values are not maintained, the PC104-SG may make an incorrect decision on the day value following julian day 365.

Selecting 1PPS or Time Code Reference Priority in Dual Port RAM

The PC104-SG allows redundant use of a time code input and a 1 PPS input simultaneously as reference. The DP_Control0_CodePriority bit of the DP_Control0 dual port RAM location will be "1" if the time code is the primary reference and "0" if the 1PPS is the primary reference. Default is for 1PPS to be the primary reference.

Setting Time Code Propagation Delay Polarity in Dual Port RAM

The PC104-SG allows negative propagation delay correction for use in installations where the time code "on-time" position is ahead of on time. Setting the DP_Control0_NegCodePropD bit in the DP_Control0 specifies that the DP_CodePropDel digits specify a NEGATIVE propagation delay correction. DP_Control0_NegCodePropD is cleared on power on or reset.

Setting PPS Propagation Delay in Dual Port RAM

The PC104-SG allows negative propagation delay correction for use in installations where the 1 PPS "on-time" position is ahead of on time. Setting the DP_Control0_NegPPSPropD bit in the DP_Control0 specifies that the DP_CodePropDel digits specify a NEGATIVE propagation delay correction. DP_Control0_NegPPSPropD is cleared on power on or reset.

Specifying Modulated Input Code Format in Dual Port RAM

The PC104-SG allows the user to specify the format of the modulated input time code in the DP_Code_Select dual port RAM address by writing the following constants defined in SGDPDEF.H. Default is IRIG-B unless -AOUT or -N36OUT options are installed. If the -AOUT option is installed, the default input code is IRIG-A. If the -N36OUT is installed, the default input code is NASA36.

IRIG-B:	CodeSelect_IRIGB	(0x0b)
NASA36:	CodeSelect_NASA36	(0x06)
IRIG-A:	CodeSelect_IRIGA	(0x0a)
2137:	CodeSelect_2137	(0x07) (requires -2137IN option support)
XR3:	CodeSelect_XR3	(0x03) (requires -XR3IN option support)
IRIG-G	CodeSelect_IRIGG	(0X0f) (requires -IGIN option support)
IRIG-E	CodeSelect_IRIGE	(0X0e) (requires -IEIN option support)

Specifying Leap Second Day in Dual Port RAM

UTC time (Universal Coordinated Time) has an extra second added periodically (about once every 18 months) to keep UTC time aligned with astronomical time. The added second (called a LEAP SECOND) occurs at the end of a specified day so that the last second of that day is at 23 hours 59 minutes 60 seconds. In order for the PC104-SG clock to maintain correct UTC time, the PC104-SG must know by the PRECEDING second if a given second is a leap second. Warning of upcoming leap seconds is broadcast by GPS satellites starting about 10 days before the leap second occurs. PC104-SG units with -GPS option will initialize the Leap Second Day locations if the selected GPS receiver allows the PC104-SG to decode it. The standard modulated time codes do not provide leap second advisory information, so the user is allowed to set a value based on user program support.

The specified day is usually June 30 or December 31. It is usually announced several months in advance. 10s and 1s of the Julian date are specified in dual port RAM locations DP_Leap_SecDay10Day1 (for 10s and units) and DP_Leap_SecDay1000Day100 for 100s of days. Power on and reset initializes both to FF. For example, say a leap second is to occur on

Dec. 31 in a non-leap year. Then the user should set DP_Leap_SecDay10Day1 = 0x65 and DP_Leap_SecDay1000Day100=0x03.
If the Leap Second Day is not set and a leap second occurs, starting with the leap second the PC104-SG will be 1 second fast until:
1. If using modulated time code input: about 1/2 way into the next modulated time code field (.5 sec for IRIG-B, NASA36,XR3,2137, .05 sec for IRIG-A, .005 second for IRIG-G)
2. If using PPS reference without time code until a Set Major Time command is issued by the user with the correct time of the most recent PPS pulse set correctly.

Setting Time Code Propagation Delay in Dual Port Ram

DP_CodePropDel-ms100ms10 specifies time code propagation delay 100ms and 10 ms digit.
DP_CodePropDel_ms1us100 specifies time code propagation delay 1ms and 100 µs digits.
DP_CodePropDel_us10us1 specifies time code propagation delay 10µs and 1 µs digits.
DP_CodePropDel_ns100ns10 specified time code propagation delay 100 ns and 10 ns deigns.
Power on and reset default setting are 0 for all digits.

For achieving µsecond accuracy it is necessary for the user to set the propagation delay correction for each PC104SG installation. The correct values for propagation delay correction can be estimated base on cable lengths and propagation speed of the cable used, but the effects of capacitive loading usually require that the 10s and units of µsecond digits and below be determined experimentally. Refer to the installation section of the manual.

Setting PPS Propagation Delay in Dual Port Ram

DP_PPS_PropDel-ms100ms10 specifies PPS pulse propagation delay 100ms and 10 ms digit.
DP_PPS_PropDel_ms1us100 specifies PPS pulse propagation delay 1ms and 100 µs digits.
DP_PPS_PropDel_us10us1 specifies PPS pulse propagation delay 10µs and 1 µs digits.
DP_PPS_PropDel_ns100ns10 specifies PPS pulse propagation delay 100 ns and 10 ns digits.
Power on and reset default setting are 0 for all digits.

For PC104 installations using the Zeli Systems SATPAK-104 the default values of 0 are adequate for µsecond accuracy.
For achieving better accuracy it is necessary for the user to set the propagation delay correction for each PC104SG installation. Refer to the installation section of the manual.

Setting Major Time in Dual Port RAM

If the 1 PPS input is the sole timing reference, the major time (seconds through days) must somehow be set once the minor time (fractional seconds) is synchronized to the 1 PPS input. The minor time will be synchronized within a few seconds of a 1 PPS input with the correct pulse to pulse spacing. One way to set the major time is for the user to set the DP_Major_Time_s10s1 byte (for seconds) through DP_ Major_Time_d1000d100 digits and then write a Command_Set_Major command to the dual port ram command address. If there is a time code input, the PC104-SG can determine major time (except years) from the time code. If the -GR, -GM, or -GT option is used, the PC104-SG can determine major time (including years) from the GPS receiver serial output.

Using BATTIM option to automatically set Major Time (with 1 PPS input)

The BATTIM option is an on-board low power battery operated clock that keeps time when board power is off or when the PC104SG is reset. If the BATTIM option is installed, after RESET the PC104-SG firmware will wait until the PC104-SG time (which starts at 000 00:00:00 after reset) matches the minutes digits (specified in Dual Port RAM location DP_BATTIM_Holdoff_m10m1) and the minor time is synchronized to the 1 PPS input and then copies the BATTIM option clock

time to the PC104-SG major time. The delay allows the 1PPS source to stabilize. If the user's 1PPS source requires more time, the user should change the value in the DP_BATTIM_Holdoff_m10m1 location before the PC104-SG copies the BATTIM clock to the major time. If the user sets DP_BATTIM_Holdoff_m10m1 to 0xFF, the PC104-SG will ignore the 1 PPS input. Typically the 1 PPS comes from a GPS receiver which is powered up about the same time as the PC104-SG, and needs about a minute after power on to generate an accurate 1 PPS. The -BATTIM clock has poor stability compared with higher power crystal oscillators, so the length of power-off time it can stay within 1/2 second of the correct time (as required if the power-on major time is to be set correctly) is 6 hours maximum at 25 degrees C. The valid power-off hold time degrades to 3 hours at 0° C to 50° C, 1.5 hours at -10° C to +60° C, and 45 minutes at -20° C to +70° C. Once the PC104-SG synchronizes to the 1PPS input and sets the major time from the BATTIM clock, it periodically updates the BATTIM clock to correct for BATTIM clock drift, so only the power-off time (plus time without an accurate 1 PPS input) affects the BATTIM clock accuracy. The user system should generate a clean SRESET bus reset signal on power up and power down to insure that the PC104SG processor does not corrupt the BATTIM option time on power up or power down.

In most applications there will be occasional power-off periods (or 1 PPS inaccurate periods) that exceed the maximums - then requiring the user to use other methods to set the major time.

Using BATTIM option to automatically set Major and Minor Time (without 1 PPS input)

The BATTIM option is an on-board low power battery operated clock that keeps time when board power is off or when the PC104SG is reset. If the BATTIM option is installed, after RESET the PC104-SG firmware will wait until the PC104-SG time (which starts at 000 00:00:00 after reset) matches the seconds digits (specified in Dual Port RAM location DP_BATTIM_Jam_s10s1) and then copies the BATTIM option clock time to the PC104-SG major time. The delay allows the user program to prevent the copying operation (by changing DP_BATTIM_s10s1 to 0xFF in case the user wants to use the 1 PPS input and set only major time from the -BATTIM option. Setting major & minor time from the -BATTIM option is most useful in cases when an accurate 1PPS is unavailable. Because the on-board 10 MHz crystal oscillator drifts much less over wide temperature ranges than the watch-style oscillator in the -BATTIM option, setting major & minot time for the -BATTIM option can also extend the time that the -BATTIM error can be kept below 1/2 second. Once the PC104-SG sets the major and minor time from the BATTIM clock, it periodically updates the BATTIM clock to correct for BATTIM clock drift. Each time the BATTIM clock time is copied to major & minor time, a 1 to 2 millisecond error may be added, so the user may wish to set DP_BATTIM_s10s1 to 0xFF (to prevent the copying) if a large number of reset cycles will occur before the time is needed.

Setting Year in Dual Port RAM

Time codes do not contain years data. To allow the PC104-SG to determine when it should count from 365 days to 366 days (Dec. 31 of leap years), the user must set the year. Otherwise the days portion of the time for day 366 will show day 001 for the first two seconds. The user can set DP_Year10Year1 and DP_Year1000Year100 for the clock. If the -GR, -GM, or -GT option is used, the PC104-SG can determine year from the GPS receiver serial output.

Changing Heartbeat, Lowrate and Rate2

The Lowrate signal (P10 pin 3), the Heartbeat signal (P10 pin 8), and the Rate2 signal (P10 pin 10) are generated by three sections (0,1, and 2 respectively) of a programmable 82C54 clock IC. Each section divides an input signal by a programmable divisor of 2-65535. The input signal for section 0 is a 100 PPS pulse synchronized to the clock. The input signal for sections 1 and 2 is a 3 MHz pulse rate also synchronized to the clock. Because all inputs are synchronized to the clock, they share the same frequency disciplining. So the generated clock outputs will track the reference input like the main clock does. The factory default divisor for LOWRATE is 100, so

LOWRATE will be 1PPS. The factory default divider for HEARTBEAT is 3000, so HEARTBEAT will be 1000 PPS. The factory default for RATE2 is 39, so RATE2 will be 76.923 KHZ which can be used for a 16X 4800 baud rate clock when the on-board SIO is used for direct communication with a GPS receiver.

To change the settings from the factory default, the user can change the DP_Ctr2_ctl ,, DP_Ctr0_lmsb values in dual port RAM. A Command_Set_Ctr0, Command_Set_Ctr1 or Command_Set_Ctr2 command can be issued to cause the changed parameters to be changed immediately. or, a Command+Rejam can cause all counters to be set to the new parameters at the start of the next second. The rejam method is used when it is important that a rate not only be synchronized in frequency to the clock, but also with a specific phase. Rejam will force the clock and the counters to resynchronize to the input signal at the start of the next second.

Each of the 3 counters has a control byte (DP_Ctr0_ctl, DP_Ctr1_ctl, DP_Ctr2_ctl) and a 16 bit divide count split into a most significant byte (DP_Ctr0_msb, DP_Ctr1_msb, DP_Ctr2_msb) and a low order byte (DP_Ctr0_lsb, DP_Ctr1_lsb, DP_Ctr2_lsb).

Counter Control Byte Bit Assignments

Bit <0>

Bit value	Mnemonic	Description
0	DP_ctl_bcd	bcd count
1	DP_ctl_bin	binarycount

Bit <3:1>

Bit value	Mnemonic	Description
000	DP_ctl_mode0	“Stop at Terminal Count”. Seldom used. Causes output to go low when Command_Set_Ctrx or Command_Rejam command is issued and to remain low until counter reaches 0. Then output goes high and stays high.
001	DP_ctl_mode1	“Hardware Retriggerable One-Shot”. Seldom used. Output goes low when jam sync occurs and stays low until count=0. Then goes hi until next jam sync.
010	DP_ctl_mode2	“Divide by N Counter”. Out is high until count=0, then low for one CLKx pulse.
011	DP_ctl_mode3	“Square Wave”. Out is high for first half of count and low for second half.
100	DP_ctl_mode4	“Software Trigger”. Seldom used. Output is high until count=0, then low for one CLKx pulse. Sequence is restarted by writing new count.
101	DP_ctl_mode5	“Hardware Triggered Strobe” . Seldom used. Output is high until jam sync. Then after count=0 output goes low one CLKx cycle and then goes high again.

Bit <5:4> should always be 11 (“DP_ctl_rw”)
Bit<7:6>:

Bit value	Mnemonic	Description

00	DP_Ctr0_ctl_sel	Select counter 0
01	DP_Ctr1_ctl_sel	Select counter 1
11	DP_Ctr2_ctl_sel	Select counter 2

GPS Satellite Tracking and Navigation Data (except Have-Quick receivers)

PC104-SG units equipped with serial interface to GPS receivers (-GM,-GR,-GT options) provide access to GPS receiver output data. Data may be accessed through dual port RAM locations defined in `gpsdef.h`. The data is updated once per second. Latitude & longitude data is available in both BCD format (DP_GPS_Lat_MinEM34 .. DP_GPS_Lon_Deg32) and in raw binary format. See `gpsdat.c` for example of using BCD format data. Because the raw binary format does not lose any accuracy in firmware conversion to BCD, it should be used when resolution better than one arc second is required for the application. The raw binary format is GPS receiver type dependant:

For the Motorola Oncore series, the raw binary format is 32 bit twos complement. The value of the LSB is 1 milliarcsecond. Negative values indicate S latitude or W latitude. See `gpsbin.c` for example of using raw binary format data.

Preventing/Correcting Data Change While Reading Position

Once per second the PC104-SG firmware takes about 50 milliseconds to receive and convert binary position data arriving from the receiver. The firmware waits until latitude and longitude is received and converted and then copies the converted data in a burst to the dual port RAM. Even though the burst copy only takes a few microseconds every second there is a small possibility that some dual port position byte reads could mix data from two different seconds. Even for static (non moving) applications this could result in wrong data. For example, suppose the latitude is sometimes N 50 degrees 0.00 minutes and sometimes 49 degrees 59.9999 minutes. If data from two different seconds was mixed the user might get 49 degrees 0.00 minutes or 50 degrees 59.9999 minutes. To prevent wrong data the user can:

1. Read a set of lat/lon dual port data and then read a second set. If both sets agree the data is OK. If they don't agree, read a third time. The third set will be OK.

2. As part of an initialization procedure, detect (approximately) when in the second the dual port data is updated. You can determined when the data is updated by doing repeated dual port RAM position reads until a change is detected. The change will always occur at the same point in the second give or take 10 milliseconds. By reading time from the SYNCCLOCK32, the user program can avoid dual port position reads during the update times.

3. Use a semaphore (dual port RAM location DP_GPS_Semaphore) to prevent write/read overlap. The semaphore is 0 after power on reset. Before the firmware copies converted location data to dual port RAM, the firmware decrements the semaphore to attempt a "locked for write" condition. If the result is < 0, the firmware will perform the copy. If the semaphore was >0 before the decrement, a "locked for read" condition prevents the copy. The best way for the user program to lock the DP_GPS_Semaphore for reading is to send the GPS_Readlock command to the dual port DP_Command address. The semaphore value after the (attempted) lock will be returned in the Response port. If it is >0 it is safe to read the dual port RAM. After reading the position data, the user should send the GPS_Readunlock command to the dual port DP_Command address.

4. Test dual port RAM location DP_GPS_UpdateFlag for non 0 (on-board firmware sets non 0 after copying new position data into dual port RAM). New data is available when non 0. After reading data, write 0 into dual port RAM location DP_GPS_UpdateFlag so that it will not be non-0 until next set of new data is written by firmware. See `gpsbin.c` example. The DP_GPS_UpdateFlag is only implemented on units shipped after 25 June 1997.

For compatibility with code written before the lock/unlock commands were added to firmware, the user can read DP_GPS_Semaphore. If <0 copy is under way, so read until 0. If 0, write 1 for "locked for read" condition, read data , and then write a 0 to unlock. This "compatibility" method is not 100% reliable, because there is a small probability that the "lock for write" will be asserted between the "0" read and the "1" write.

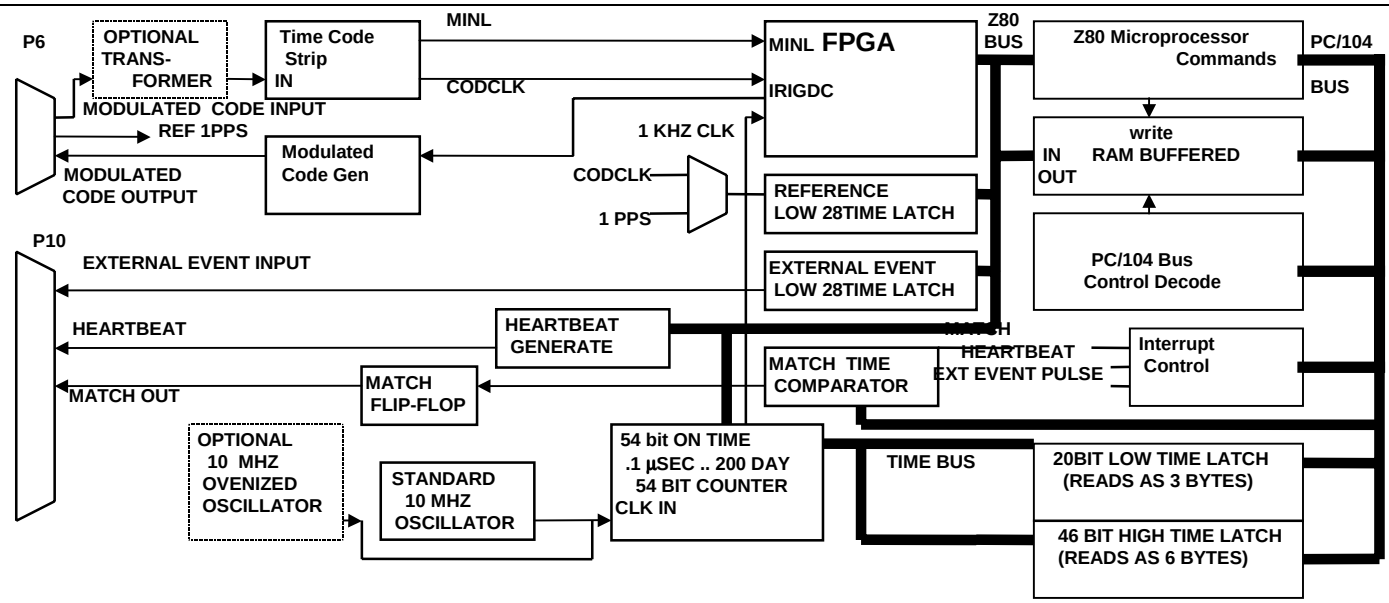
GPS Satellite Data (Have-Quick receivers)

GPS receiver Time Figure-of-Merit may be accessed through dual port RAM locations DP_HQ_TFOM (defined in `gpsdef.h).` The data is updated once per second. The TFOM meaning is:

<0	No information
9	1PPS accuracy no better than 10 milliseconds
8	1 PPS accuracy 1 to 10 milliseconds
7	1 PPS accuracy 100 μsec to 1 millisecond
6	1 PPS accuracy 10 μsec to 100 μsec
5	1 PPS accuracy 1 μsec to 10 μsec
4	1 PPS accuracy .1 μsec to 1 μsec (typical for Plugger)
3	1 PPS accuracy .01 μsec to .1 μsec
2	1 PPS accuracy .001 μsec to .01 μsec
1	1 PPS accuracy better than 1 nsec
0	"Normal" (used when HQ receiver cannot compute actual TFOM)

Because the Have Quick signal does not contain navigation information, only time and TFOM are available.GPS Satellite Tracking and Navigation Data (except Have-Quick receivers)

Theory of Operation



BLOCK DIAGRAM

Time Code Stripping

Time code stripping uses a zero crossing detector combined with a voltage divider and a negative peak detector to produce a sampling trigger and a high amplitude cycle pulse to send to a burst decoder in the FPGA device.

Input Signal Coupling

If the “T” option is implemented, transformer T1 couples the isolated CODEIN+ and CODEIN- inputs to the CODEIN and board ground. If no T option, CODEIN+ connects by jumper JPT1-4 to CODEIN and CODEIN- connects by jumper JPT1-3/6 to board ground. Capacitor C1 translates the input signal from + and - voltages around ground to + and - relative to the +5 volts through R5 and R6. The input signal impedance is 10.1K ohms (the series resistance of R5 + R6).

Zero Crossing Detector

The + side of C1 is the modulated signal input referenced to +5 volts. It is applied to the + side of a LM339 (U4) comparator section at pin U4-5. The - side of the comparator (U4-4) is connected to +5. A 3.3K pull-up resistor pulls up U4-2 whenever U4-4 is HIGHER than U4-4. The open collector output of U4-2 pulls low when U4-5 is LOWER than U4-4. So a +5V/0V square wave in phase with the analog input signal appears at U4-2. Of course there are switching transients showing up as

false transitions near the correct zero crossing points that must be dealt with in subsequent processing.

Voltage Divider

The analog reference signal swing + and - around +5 V is applied to one end of voltage divider R5 and R6. The other end of the divider is +5 volts. Because R6 is about twice the value of R5, the peak to peak AC voltage at the R5/R6 junction will be 2/3 the peak to peak AC voltage at C1 + side - but still centered on +5 V.

Peak Detector

Because the 2/3 scaled voltage at R5/R6 junction connects to comparator section U4-9 "+" side input, if U4-9 value is ever LESS than the comparator output voltage U4-14 then U4-14 will be driven lower. This makes U4-14 follow the NEGATIVE peak of the 2/3 scaled signal. A long time constant R7/C4 combination slowly increases the U4-14 voltage if the input signal amplitude decreases. The U4-14 level is the ideal comparison level to separate low and high amplitude input signal cycles. Because "low" amplitude cycles are 1/3 the amplitude of "high" amplitude cycles the 2/3 point is halfway between low and high. U4-14 is applied to U4-10 and compared with the full amplitude signal at U4-11. Whenever the full amplitude signal instantaneous signal is less than the U4-14 level the U4-13 signal will be pulled low, generating negative TTL pulses at about 15% duty cycle.

Burst Decoder

The FPGA includes a precision digital programmable time retriggerable one-shot which trigger on the negative going edge of the zero crossing comparator. The one-shot rearms when the zero crossing comparator output is high. So, the one-shot generates an edge a programmable time delay (about 25 µsec for IRIG-A and 250 µsec for other codes) after the zero crossing negative transition. Noise transitions that have a LOW time less than the programmable time are rejected for noise immunity. By using a counter to generate delay, the temperature varying errors of RC based approaches are avoided. Each delayed edge shifts in the amplitude comparator data for the corresponding cycle of the input code. Logic inside the FPGA detects the beginning of each burst (a burst starts when a large cycle follows a small cycle) and transfers the high/low amplitude information for each cycle of the burst to the microprocessor.

FPGA Clock

The FPGA contains a conventional BCD clock (optional binary) that counts the 10 MHz crystal oscillator pulses. Disciplining is achieved by periodic advance/retard techniques as used in conventional packaged and board level time code generators. The hardware counter covers the 100 ns bit through the 100 ms bit.

200ms .. 80 Year Bits

Higher order bits (200 ms .. 80 years) are maintained in two sets of latches. One set of latches contains the high order bits for "even" 100 millisecond intervals and the other set contains the high order bits for "odd" intervals. By latching the state of the 100 millisecond counter bit the rest of the high order bits are selected. The high order latches are updated in a leap-frog fashion. Just before the end of a ODD 100 millisecond interval, the EVEN latches are updated to contain correct data for the NEXT even interval. And, just before the end of the EVEN interval, the ODD latches are updated. This approach allows the user to have plenty of time (90 msec) to retrieve time measurements will also allowing economical implementation of high order bits.

Error Measurement

The FPGA contains internal “reference” latches for capturing the time of the clock when the one-shot sampling pulses occur (or one sample per burst for high speed codes like IRIG-A). The on-board microprocessor uses the captured times to estimate the difference between the clock time and the modulated code time. If the time code input has priority for error correction, the difference information from the burst capture is used for disciplining. The PC104-SG firmware can also capture the time of a reference 1PPS input. By sharing the reference latches between the between time code and 1 PPS pulses, redundant operation is possible.

10 MHz Oscillator Steering

Rev B and later modules may optionally be equipped with a 12 bit D/A converter (U3) and a voltage controlled 10 MHz crystal oscillator. The D/A allows direct frequency control of the 10 MHz to about 5 parts in 10^9 . The D/A control voltage is updated periodically (once/64 seconds) based on averaged time discipling values.

Latch Times

The FPGA contains two 8 bit comparators directly accessible across the PC-104 bus to allow the user to toggle the MATCH flip flop when the user programmed times match the clock time. Direct bus access and an associated interrupt allow user’s to generate very tightly spaced pulses at arbitrary times that cannot be achieved in conventional approaches which maintain the comparators under microcomputer control.

Heartbeat Rates

A conventional Intel architecture 82C54 triple 16 bit counter is used to generate three user controlled rates / frequencies. The rates and frequencies will track the on-board clock because they are generated from the same disciplining clock frequencies.

Microcomputer

The microcomputer section is a conventional Z80 microprocessor (U5), 8K X 8 EPROM (U6), 8K X 8 RAM (U7) and triple programmable counter (U8). The dual port RAM accessed by the host program is maintained in part of U7 by U5 control. The microprocessor runs at 5 MHz derived from XO1 (10 MHz) divided by 2 inside the FPGA (U10). The FPGA generates Z80 interrupts for code reading, disciplining, external time tag processing (if user enabled), and ODD.EVEN latch updating and dual port RAM support.

PC-104 Bus Interface

Bus address decoding and IRQ bus drive are done in a GAL16V8 programmable logic device (U1). Three address configuration select lines select one of 7 addresses to decode. The 8th selection disables the bus interface. This approach allows sufficient flexibility on address selection without the pin count of address comparator approaches. The PC-104 interrupt sharing option is also implemented in U1.

SCHEMATIC DRAWINGS

PARTS LIST

PROGRAM LISTINGS