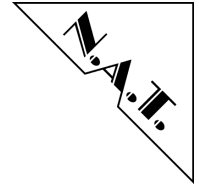


N.A.T. GmbH

N.A.T. Eth29-FC

Hardware Manual

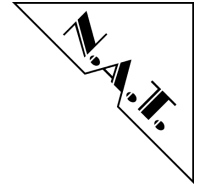
Version 2.2



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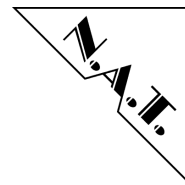
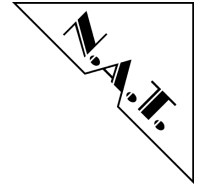


Table of Contents

1	INTRODUCTION	5
1.1	TECHNICAL SPECIFICATIONS.....	6
2	HARDWARE DESCRIPTION.....	8
2.1	ETH29-FC – HARDWARE OVERVIEW.....	8
2.2	VMEBUS INTERFACE	9
2.3	PROCESSOR BLOCK – MOTOROLA COLD FIRE	9
2.4	NETWORK INTERFACE.....	9
2.5	MULTI-PORTED RAM.....	10
2.6	REAL TIME CLOCK SUPPORT	10
2.7	SERIAL LINE INTERFACES	10
3	ETH29-FC - JUMPER SETTINGS.....	11
3.1	SETTING THE BOARD'S BASE ADDRESS	11
3.2	SETTING THE VMEBUS INTERRUPT VECTOR/LEVEL.....	11
3.3	SYSRESET / SYSFAIL	11
3.4	BDM TEST CONNECTOR.....	12
4	ETHERNET / CHEAPER NET – OPERATION.....	12
5	THE ETH29-FC FRONT-PANEL	13
5.1	RESET SWITCH.....	14
5.2	BOARD STATUS INDICATOR LEDS.....	14
5.3	NETWORK INDICATOR LEDS	14
5.4	SERIAL INTERFACES - S1 AND S2	15
5.5	CHEAPER NET CONNECTOR – NET	15
5.6	10/100BT CONNECTOR	16
5.7	ETHERNET CONNECTOR – AUI.....	16
6	ADDRESS RANGES	17
6.1	VMEBUS – ADDRESSES	17
6.2	COLD FIRE CPU - MEMORY MAP	18
7	ACCESSING MAILBOX AND SOFTWARE-RESET LOCATIONS	18
8	BUS INTERRUPTER MODULE.....	18
9	DOCUMENT'S HISTORY.....	19



1 Introduction

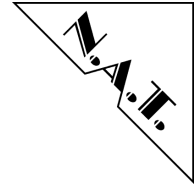
The Eth29-FC is an intelligent high performance VMEbus Ethernet controller board. It has been designed to support extremely high data transfer rates with a minimum of impact on the system load of the host system.

The board combines a true 32-bit architecture with a powerful RISC processor to enable the utilization of the Ethernet network's maximum throughput. A Motorola Coldfire processor handles all of the local network protocols up to layer 4 and thus enables an effective transfer rate of up to 3 MByte/sec with all network protocols.

The Eth29-FC board supports all of today's standard protocols (TCP/IP, DECNet, ISO/OSI protocol) and is prepared for tomorrow's demands. All of the N.A.T. network protocols are based on N.A.T.'s Universal Protocol Stack Architecture (UPSA) which supports the simultaneous and independent execution of different network protocols on the Eth29-FC board.

The Eth29-FC handles the processor-intensive network protocols onboard. Thus, the system's main processor is free and the real-time capability of the system is undiminished by even high network traffic. The board's VMEbus interface achieves extremely short bus cycles through the use of intelligent access modes. Thus, high network data transfer rates are also achieved with standard (D16) CPU boards that provide no support for Block-Transfer or DMA.

The Eth29-FC board is delivered with the multi-tasking kernel OK1 (Open Kernel 1). OK1 supplies all of the operating system resources required by the network software. For a detailed description of the OK1 kernel please refer to the "N.A.T. OK1 Reference Manual".



1.1 Technical Specifications

Bus Interface:

- VMEbus Rev. C1, ANSI/IEEE STD1014-1987
- D32/A32, D16/A24
- all standard and extended addressing modes
- Block mode data transfers
- VMEbus interrupter and Mailbox IRQs
- Auto Slot ID cycle support

Processor:

- Motorola Coldfire

CPU-Type	Speed	
MCF5307FT66B	66 MHz	optional
MCF5307FT90B	90 MHz	optional
MCF5407FT162	162MHz	assembled (standard)

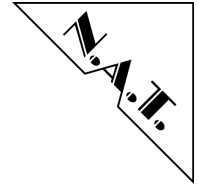
- 3.3 V
- 4 KByte SRAM
- Multiply-Accumulate (MAC) unit and Divide unit
- 8 KByte Unified Cache
- 4-channel DMA controller
- DRAM Controller, supports SDRAM, EDO and page mode DRAM
- 2 Universal Synchronous/Asynchronous Receiver/Transmitters (UART)
- Dual 16-Bit General-Purpose Multimode Timers
- I²C®-Compatible Bus
- System Interface
- System Debug Support
- Clock Multiplied PLL
- 16-bit general-purpose parallel I/O port
- 70 MIPS at 90 MHz (MCF5307)
- 257 MIPS at 162MHz (MCF5407)
- Available at 66 and 90 MHz (MCF5307) or 162MHz (MCF5407)

Memory:

- Communication RAM: 4 MB dual ported RAM
- Processor RAM: 16 MB SDRAM
- 2 MB Flash EEPROM for onboard firmware

Network:

- 32 bit PCI Ethernet controller DEC21143



- Ethernet (AUI) interface
- 10 Mbit Thin-Wire Ethernet (Cheapernet) interface
- 10/100 Mbit twisted pair interface 10 BaseT, 100BaseT

I/O:

- 2 serial Line Interfaces RS232
- Battery back up Real Time clock M48T37 (optional)

Protocols:

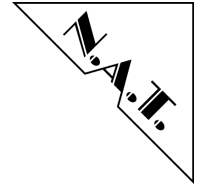
- TCP/IP
- DECNet
- ISO/OSI
- OS-9 Net
- simultaneous handling of different protocols onboard

Host Driver Support:

- OS9
- VxWorks

Throughput:

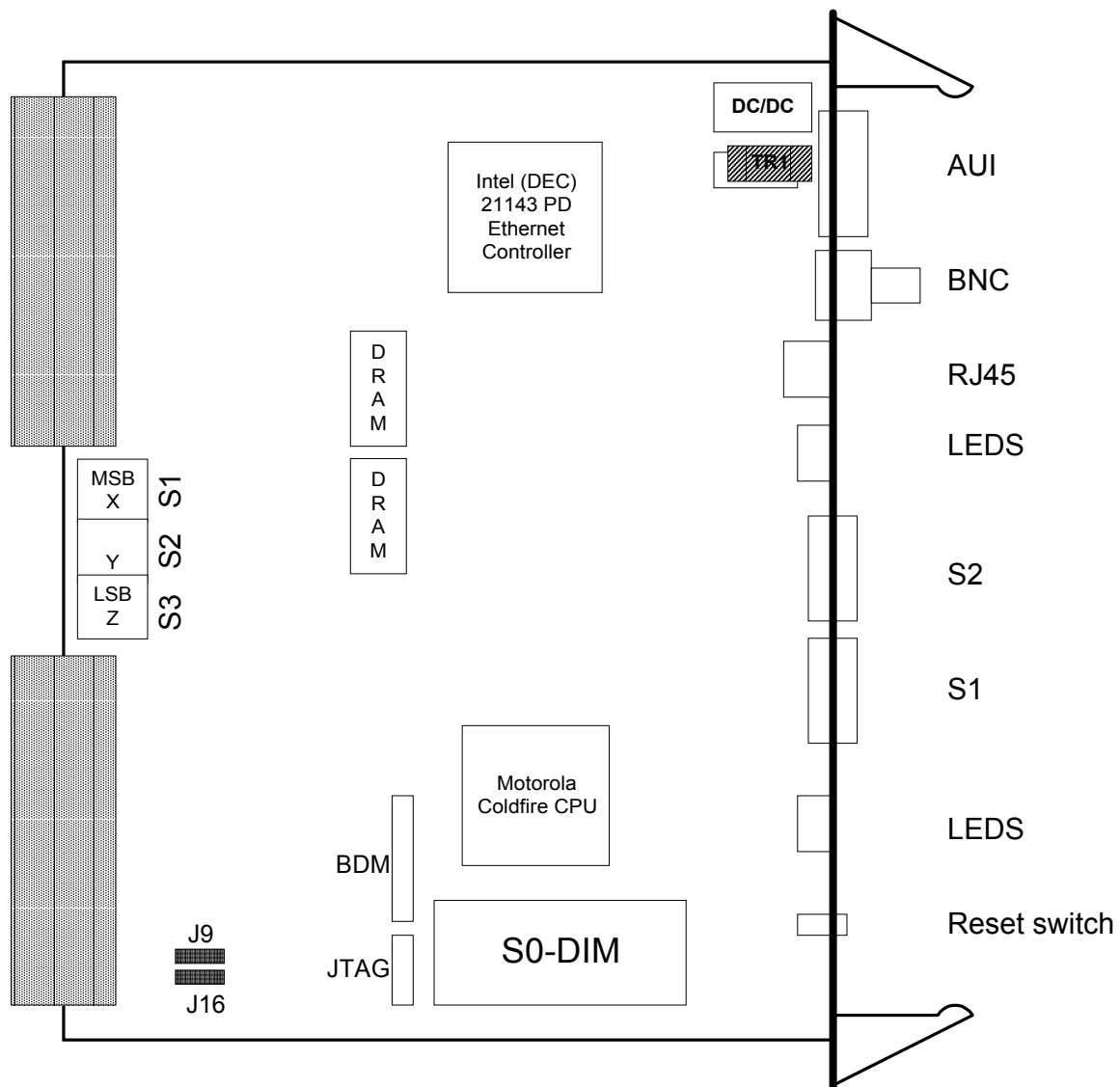
- 4 MByte/sec at the packet layer (100BT)
- up to 2.5 MByte/sec with TCP/IP and 100BT interface

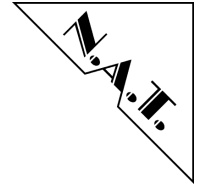


2 Hardware Description

This chapter contains a brief description of the functional blocks of the Eth29-FC board.

2.1 Eth29-FC – Hardware Overview





2.2 VMEbus Interface

The VMEbus interface on the Eth29-FC Ethernet board meets the VMEbus standard Rev. C.1 (ANSI/IEEE STD1014-1987). In the basic configuration, the Eth29-FC is a slave board. The board can be operated in either D32/A32 or D16/A24 modes. It supports all standard and extended address modes. It always occupies a 1 or 4 MByte address range on the VMEbus (factory setting), which also includes cells for mailbox interrupts and a software reset (see chapter 7). The board can trigger a level 1 - 6 VMEbus vector interrupt.

As an aid in locating hardware failures on the system bus, the VMEbus SYSFAIL function is supported.

Additionally the new generation Eth29-FC Boards will support the Auto Slot ID cycle according to the VME64 specification. This includes an area of memory where configuration and version informations are stored (even if the auto Slot ID mechanism is not used). This memory area is accessible from the VMEbus side.

2.3 Processor Block – Motorola Coldfire

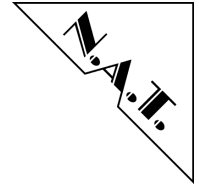
The Motorola Coldfire®, MCF5307/MCF5407, are high performance, low-cost, highly integrated microprocessors, designed for embedded control applications, which combine a Version 3/4 ColdFire® processor core with a Multiply Accumulate (MAC) unit, DRAM controller, DMA controller, timers, and parallel and serial interfaces. The Coldfire® packaging provides common system functions on chip and glueless interfaces to 8-, 16-, and 32-bit DRAM, SRAM, ROM, and I/O devices. Support for standard and synchronous DRAM (SDRAM) is also present.

2.4 Network Interface

In the standard configuration, the Eth29-FC board comes with an interface to connect an external network adapter (Medium Attachment Unit, MAU) via a 15 pin transceiver cable, a Cheapernet interface with a BNC connector and a RJ45 connector for 10/100BT interface. All network connectors are located on the board's front-panel.

The DEC DEC21143, which has a 32-bit PCI bus interface, is used as the Ethernet controller. The processor can communicate with the Ethernet Controller as a slave device or by DMA transfer, with the network packets being written to and read from the multiport RAM.

The DEC21143 has several interface options and can drive itself the AUI interface, the 10BT interface and two version of 100MBit symbol bus (MII and PHY). The AUI I/O signals are directly connected to the front panel AUI connector or can be routed to the onboard Cheapernet (Coax) interface circuitry by fitting the TR1 Transformer at the appropriate location. For the 100BT and 10BT the Level One Semiconductor LXT972 chip is used as the



physical layer controller. All network signals are compatible to the Ethernet-2, IEEE802.3, and 10Base2 (Cheapernet), 10/100BaseT standards.

2.5 Multiported RAM

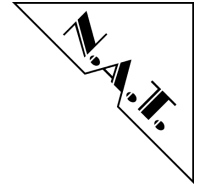
Communication between the VMEbus interface, onboard processor, and network controller is done via a fast multiported RAM which can be accessed simultaneously from all three ports. The multiport RAM can be equipped with either 512 KByte or 1 MByte of SRAM or 4 MByte of DRAM, as needed for the desired number of simultaneous connections. All N.A.T. network protocols are written to use the minimum number of copy operations; thus, user data that is written by the master CPU board into the multiport RAM can be transferred by the Ethernet controller using DMA transfers directly into the network.

2.6 Real Time Clock Support

For special applications requiring onboard date/time informations an battery backed up real time clock can be equipped (SGS M48T37). This is an assembly option

2.7 Serial Line Interfaces

Along with the network interface, the Eth29-FC also has two serial (RS232) ports S1 and S2. The serial ports can be used as needed (e.g., for serial line IP, or for debug purposes).



3 Eth29-FC - Jumper Settings

The Eth29-FC has been design to adapt into a customers system by a minimum of hardware switches and jumpers.

The location of the switches and jumpers is shown in section 2.1, "Eth29-FC - Hardware Overview".

3.1 *Setting the Board's Base Address*

The board's VMEbus base address is set within the 32 bit address range using the hexadecimal rotary switches S1-S3. S1 is used to set the 4 higher order bits (A31-A28) and S3 sets the 4 lower bits (A23-A20).

The default setting is:

Base address = \$50C00000

In systems with a 24 bit address range, the base address is set using S3 only.

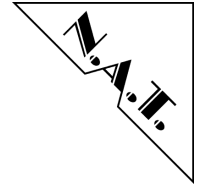
3.2 *Setting the VMEbus Interrupt Vector/Level*

On the Eth29-FC the VMEbus interrupt vector and level is setable by software only.

3.3 *SysReset / SysFail*

J16 brings the VMEbus SYSRESET signal onto the board. This signal enables a synchronous reset of all boards on the bus. J16 should always be set for normal operation.

J9 enables the board to drive the VMEbus SYSFAIL signal. This Signal is expected by some mother boards as part of the power up sequence. To enable the SYSFAIL functionality set J9.



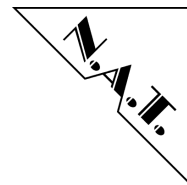
3.4 BDM Test Connector

The following table shows the pin out of the BDM connector. This connector is used for debugging and factory testing only.

BDM Port				
	PIN			
-	1		2	/BKPT
GND	3		4	DSCK
GND	5		6	-
/RESET	7		8	DSDI
+3V	9		10	DSDO
GND	11		12	DDATA7
DDATA6	13		14	DDATA5
DDATA4	15		16	DDATA3
DDATA2	17		18	DDATA1
DDATA0	19		20	GND
10K to GND	21		22	-
GND	23		24	PSTCLK
+3V	25		26	/TA

4 Ethernet / Cheapernet – Operation

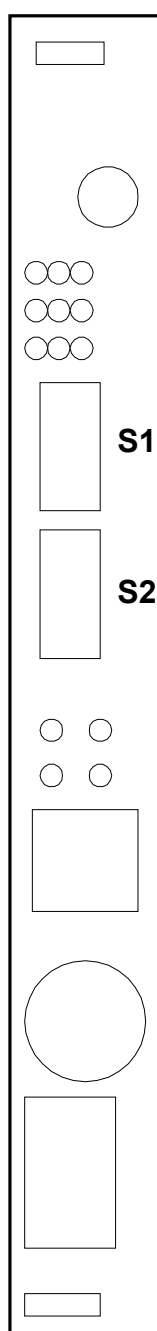
The standard configuration of the Eth29-FC board is for operation with Cheapernet (Thin-Wire Ethernet). The connection to the network is made directly with a BNC connector on the front panel of the board. If the board is used on an Ethernet network, the connection is made using a 15 pin transceiver (AUI) cable. The decision between the two interfaces is made by plugging the Ethernet isolation transformer (TR1) into the appropriate position (see Fig. 1).



5 The Eth29-FC Front-Panel

Mounted on the Eth29-FC front panel are connectors for the serial and network interfaces, a reset switch, and a number of indicator LEDs.

This chapter contains a detailed description of the various components mounted on the front panel.



Board Status Indicator LEDs:

CPU Access / MBOX / RESET

VME Access / VINT / unused

LAN Access / LIRQ / unused

Serial Line Interfaces

Network Indicator LEDs:

Match / Link Ok

100BT / RX/TX active

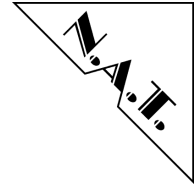
10/100 BT Interface Connector

RJ45

Cheapernet Interface Connector

BNC

AUI Connector



5.1 Reset Switch

This switch can be used to locally reset the Eth29-FC board. After the reset, the board does a self-test and then initializes the basic firmware. A reset should never be made while the network is in operation, since this may have unpredictable consequences for the Master CPU.

5.2 Board Status Indicator LEDs

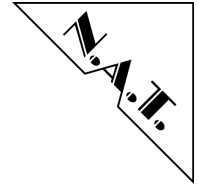
The board indicator LEDs are showing operational status for the onboard devices (listed in their order on the front panel from top to bottom):

Function	Description
RESET	Lights when the board is doing a reset. This LED lights for about one second at power up or following a manual reset using the reset switch.
CPU	Lights when the CPU accesses the multiported communications RAM.
VME	Lights when the multiported communications RAM is accessed over the VMEbus.
LAN	Lights when the Ethernet controller chip accesses the multiported communications RAM.
VIRQ	Lights when the board has triggered a VMEbus interrupt.
MBOX	Lights when the board has received a mailbox interrupt from the VMEbus.
LIRQ	Lights when an interrupt from the Ethernet controller is awaiting ist service.

5.3 Network Indicator Leds

The network indicator LEDs are indicating the actual network line state.

Function	Description
Match	Indicates that a packet has passed the controller's address recognition algorithm
LinkOK	Indicates that the 10/100 MBit Link is OK
100BT	Indicates that the interface is operating at 100Mbit
RX/TX	Indicates network traffic



5.4 Serial Interfaces - S1 and S2

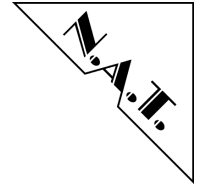
The Eth29-FC has two serial (RS232) interfaces which can be used at rates up to 38400 baud. The interfaces can be used as additional communications channels (e.g., for serial line IP or other serial communications protocols). The standard settings assign S1 as the output port for the firmware's debugging and error messages.

Each serial interface uses a 9 pin Sub-D connector with the following pin assignment:

Pin	Assignment
1	NC
2	RXD
3	TXD
4	NC
5	GND
6	NC
7	NC
8	NC
9	NC

5.5 Cheapernet Connector – NET

The BNC connector (labeled "NET") on the Eth29-FC front-panel is used for the direct connection to a Cheapernet (Thin-Wire-Ethernet) network.



5.6 10/100BT Connector

This RJ45 is provided as the interface connector for 10BT and 100BT network connection. Its pin-out is as follows:

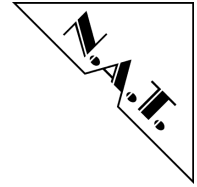
Pin	Assignment
1	TX+
2	TX-
3	RX+
4	75 Ohm Termination
5	75 Ohm Termination
6	RX-
7	75 Ohm Termination
8	75 Ohm Termination

5.7 Ethernet Connector – AUI

The standard Ethernet transceiver cable connector (labeled "AUI") can be used with any suitable Ethernet transceiver.

The following table shows the transceiver cable (AUI) connector pin assignment:

Pin	Assignment
1	CI Shield
2	CI+
3	TX+
4	RX Shield
5	RX+
6	Ground
7	NC
8	Shield
9	CI
10	TX
11	TX Shield
12	RX
13	+12 V
14	+12 V Shield
15	NC
Shell	Protective GND - Chassis (Front-Panel)



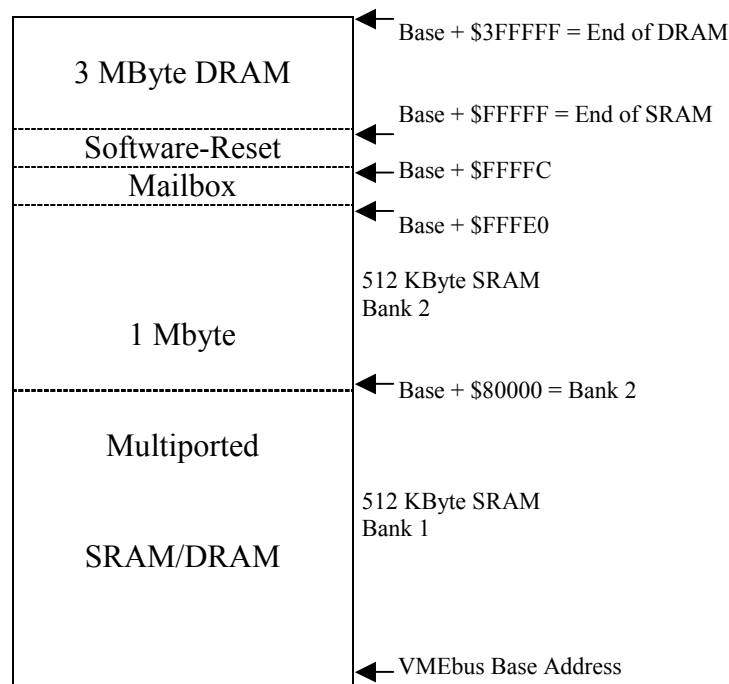
6 Address Ranges

This chapter presents the Eth29-FC VMEbus and Coldfire memory maps.

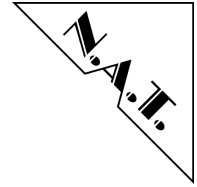
6.1 VMEbus – Addresses

The Eth29-FC occupies an address range of 1 or 4 MB on the VMEbus (factory setting). When accessed from the VMEbus these addresses are seen as a 1 or 4 MB bank of RAM (multiported communications SRAM/DRAM between the CPU, VMEbus, and the Ethernet controller chip). This memory can be equipped with 512KByte or 1 MByte fast SRAM or with 4MByte DRAM. The standard Eth29-FC is equipped with 4MByte of DRAM.

The boards base address is set using the hexadecimal switches S1 - S3 (see section 3.1). When the board is used within a 24 bit VMEbus address range, switch S3 is used only.



The cells for the mailbox interrupt and the software-reset are located in the upper addresses.



6.2 Coldfire CPU - Memory Map

The CPU's memory map is shown below in figure 3. The multiported RAM at address 0x40000000 is used for the communication between the VMEbus, the local CPU 29K, and the Ethernet controller chip.

Address	Device
0xF0000000	Flash Memory
0xE0000000	I/O Devices
0x40c00000	LAN Controller Chip
0x40100000-0x40c00000	Multiported RAM
0x400ffffc	Software Reset Cell
0x400fffe0	Mailbox Cell
0x400fffc0	BIM
0x40000000-0x400fff00	Multiported RAM
0x20000000	Coldfire internal RAM
0x10000000	Coldfire internal Registers
0x0 – 0x01000000	CPU SDRAM - 16 MByte

7 Accessing Mailbox and Software-Reset Locations

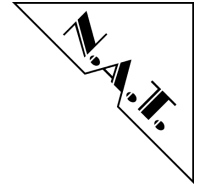
A mailbox interrupt or a software reset can be triggered by writing to the appropriate memory cell. When read, these cells appear as normal RAM and it is thus possible to read which value was previously written to trigger the event.

Since the protocol firmware zeroes the mailbox interrupt cell after servicing the interrupt, it is possible to avoid triggering a new interrupt before the previous one has been handled. This characteristic allows the mailbox-cells to be used as semaphores between the Master board and the Slave board.

Both cells may be accessed as byte, word, or long-word.

8 Bus Interrupter Module

The Eth29-FC board can trigger level 1-6 VMEbus vectored interrupts. The desired interrupt level can be set by software. The vector number is generally set by a user-modifiable program module (under OS-9, for example, the Device-Descriptor), which is passed to the firmware during initialization of the slave board and then written to the Bus Interrupter Module .



9 Document's History

Version	Date	Description	Author
1.0	1990	Initial Version	hl
2.0	21.07.1999	Portation of Framemaker Version to Wordfile	as
2.1	04.12.2000	Reworked for Eth29-FC – intermediate version	as
2.2	23.05.2001	Completed rework for Eth29-FC	hl