Model 314
Channel Adapter 14/125
Hardware Reference Manual

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1.0 Introduction

1.1 Contents and Structure

This manual describes the Model 314 Channel Adapter hardware and in conjunction with the items listed in the supporting documents of section 1.2 provides a complete description of the capabilities and operation of this product. The focus of this manual is the electrical function of the hardware including control structure, signal flow, clock distribution, external interfaces and key components. Other Channel Adapter manuals focus on software and the internals of the FPGA.

The manual is divided into eight sections as follows:

Section	Description
Section 1	Introductory information about the manual.
Section 2	Product overview.
Section 3	Hardware specifications.
Section 4	Absolute maximum conditions without damage.
Section 5	Receiver performance characteristics.
Section 6	Detailed hardware description.
Section 7	External interface descriptions and connector pinouts.
Section 8	Hardware build options

The latest product documentation and software is available for download from the Red Rapids web site (www.redrapids.com) by following the Technical Support link.

1.2 Supporting Documents

Author	Number	Title
Red Rapids	REF-320-001	Channel Adapter and Channel Adapter Plus Installation Guide
Red Rapids	REF-320-002	Channel Adapter Software Reference Manual
Red Rapids	REF-320-003	Channel Adapter FPGA Core Manual
Red Rapids	DSK-820-000	Model 314 Power Calculator (Excel™)
IEEE	1386.1-2001	IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)
PCI SIG	PCI Rev 2.2	PCI Local Bus Specification
PICMG	PICMG 2.0 R3.0	CompactPCI® Specification

1.3 Conventions

This manual uses the following conventions:

- Hexadecimal numbers are prefixed by “0x” (e.g. 0x00058C).
- *Italic* font is used for names of registers.
- **Bold** font is used for names of directories, files and OS commands.
- Palatino font is used to designate source code.

- Active low signals are followed by '#', For example, TRST#.

☞	Text in this format highlights useful or important information.

!	Text shown in this format is a warning. It describes a situation that could potentially damage your equipment. Please read each warning carefully.

The following are some of the acronyms used in this manual.

- **ADC** Analog to Digital Converter
- **API** Application Program Interface
- **CMC** Common Mezzanine Card
- **CPCI** CompactPCI
- **DAC** Digital to Analog Converter
- **DCM** Digital Clock Manager
- **DMA** Direct Memory Access
- **GPIO** General Purpose Input/Output
- **IDELAY** Virtex-4 Input Delay Element
- **IDELAYCTRL** Virtex-4 Input Delay Control Element
- **IOB** Virtex-4 Input/Output Block
- **MSPS** Mega Samples per Second
- **PCI** Peripheral Component Interconnect
- **PMC** PCI Mezzanine Card
- **QDR** Quad Data Rate
- **SFDR** Spur Free Dynamic Range
- **SINAD** Signal-to-Noise and Distortion
- **SNR** Signal-to-Noise Ratio
- **TCXO** Temperature Compensated Crystal Oscillator
- **UCF** Virtex-4 User Constraints File

1.4 Manual Compatibility

The applicable hardware part numbers are defined as follows:

- Model 314-XXX[(1)] *Channel Adapter 14/125*

[(1)] XXX is a three digit number that indicates the hardware variant.

1.5 Revision History

Version	Date	Description
R00	8/14/06	Initial release.
R01	11/02/06	Added references to inlet air, channel isolation specifications
R02	11/21/06	Corrected PCI Controller GPIO description (output only).
R03	02/23/07	Added ADC offset and external clock waveform notes. Increased minimum external clock power requirement.
R04	06/20/07	Added 3.3V PCI signaling restrictions.

2.0 Overview

The Channel Adapter product family provides the ideal platform to rapidly field application specific I/O functions minus the expense of custom hardware development. The architecture features a high performance front-end tightly coupled to a Xilinx Virtex-4 FPGA. The FPGA communicates with the host processor through a dedicated PCI controller chip, leaving the majority of logic uncommitted. Simple interfaces to the I/O, SRAM, and local bus are easily integrated with user application logic.

The Channel Adapter product family offers several different front-end hardware options. The Model 314, illustrated in Figure 2-1, provides a quad channel digitizer based on the Linear Technology LTC2255 14-bit A/D converter (ADC).

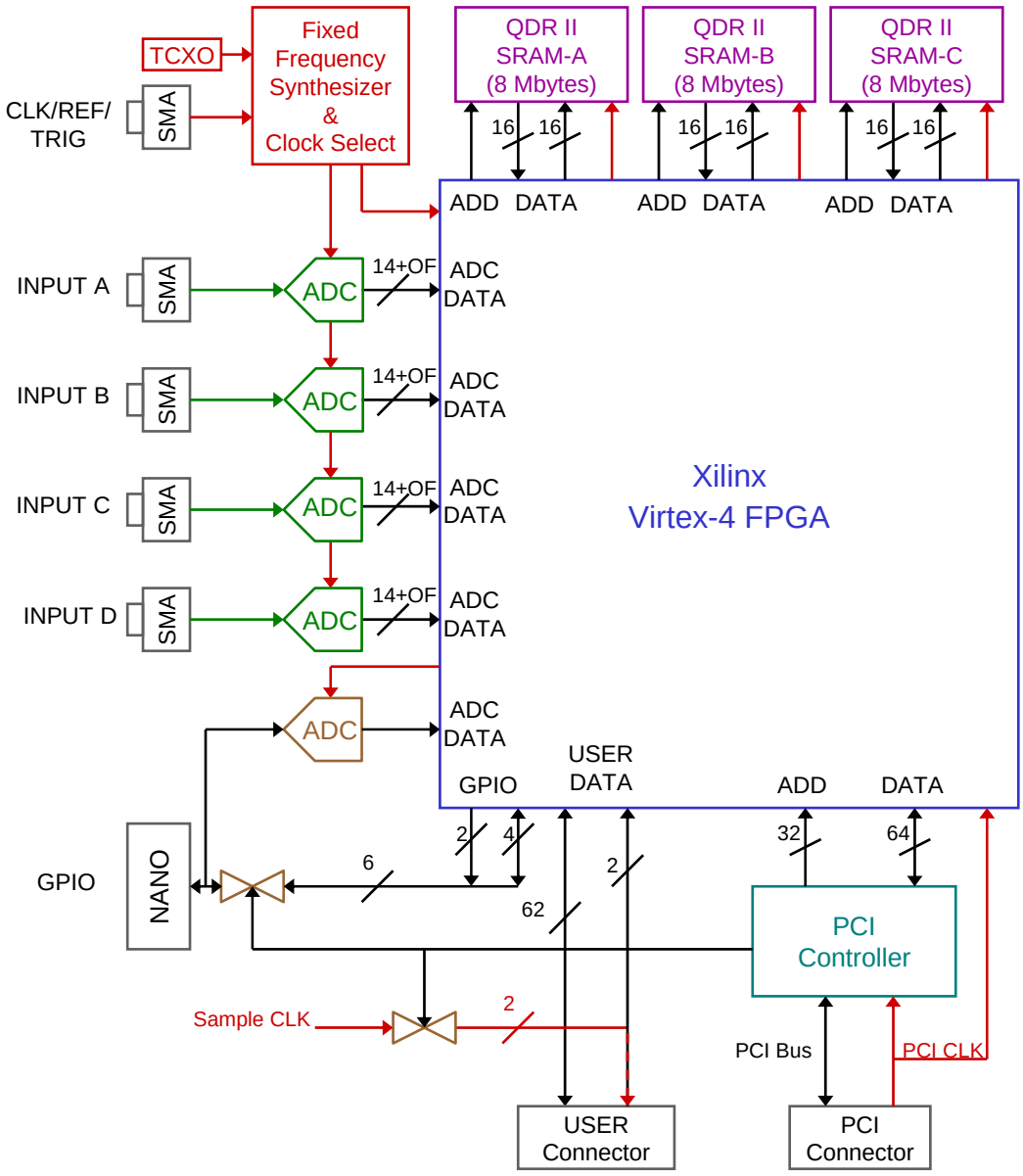


Figure 2-1 Model 314 Block Diagram

The ADC sample clock is supplied by an on-board frequency synthesizer or an external source. The frequency synthesizer can be phase locked to the local 10 MHz temperature compensated crystal oscillator (TCXO) or an external reference can be used to achieve system-wide phase coherence.

The FPGA can be selected from the Virtex-4 high performance logic (LX) or signal processing (SX) platforms. A variety of size and speed grade options are offered to further optimize the price/performance ratio over a wide range of applications.

The FPGA can be connected to three optional 16-bit QDR SRAMs for high speed local data storage. The QDR SRAM provides separate read and write ports to maximize data transfer into and out of memory. This memory can also be used as a high-speed snapshot recorder to store segments of data without interruption from PCI bus traffic.

A high density connector supplies six bidirectional general purpose I/O links for digital control signals as well as a single analog telemetry port for acquisition of low speed auxiliary data.

A DMA FPGA core is provided to manage data transfers between the *Channel Adapter* and host memory. The DMA engine allows the receiver to automatically initiate a PCI burst transaction when a predetermined number of samples are available. An interrupt is generated by the Channel Adapter when the specified number of data blocks have been written.

There are also more sophisticated DMA features built into the core. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency. Refer to the product *Channel Adapter FPGA Core Manual* for further details.

The Virtex-4 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the Channel Adapter. VHDL source code for the ADC, SRAM, and local bus interface logic are also provided. Both the FPGA and the configuration PROM can be programmed directly over the PCI bus. The PROM can also be loaded through an optional JTAG connector using the Xilinx iMPACT software.

The Channel Adapter product is intended for users with significant experience in FPGA design. Red Rapids offers a line of fixed function products to meet standard data acquisition needs which require no FPGA design experience.

3.0 Hardware Specifications

All specifications estimated unless otherwise noted.

3.1 Board Specification Summary

Specification	Value
Physical	
Form Factor	
PMC	IEEE Standard 1386-2001 (CMC)
PCI	Universal Short Card
CPCI	3U or 6U
Weight	
PMC	3.8 ounces
PCI	7.5 ounces
CPCI	7.7 ounces
Electrical	
Supply Voltages	3.3 V, 5.0 V, +12 V, -12 V
Bus Protocol	PCI 2.2 (64-bit / 66 MHz) , 3.3V signaling only.
Power (max)[(1)]	
Analog (DC-Coupled)	6.2 W
Analog (AC-Coupled)	4.8 W
Digital (No SRAM)	0.6 W (Not including FPGA)
Digital (24 MB SRAM)	8.2 W (Not including FPGA)
Host Interface	
Bus Protocol	PCI 2.2
Type	32/64-bit DMA Master and Target
PCI Clock Speed	33 and 66 MHz
Signaling Voltage (VIO)	3.3V signaling only.
Interrupt Support	Single Interrupt (INTA)
Vendor ID (Hex)	0x17D2
Device ID (Hex)	0x00CA
Environmental[(2)]	
Airflow (minimum)	250 LFM
Operating (Inlet Air)	
Temperature	0°C to 35°C Ambient
Humidity	90% maximum (non-condensing)
Altitude	15,000 Feet
Non-Operating	
Temperature	-20°C to 65°C Ambient
Humidity	95% maximum (non-condensing)
Altitude	40,000 Feet

[(1)]The power dissipation of the FPGA is not included in section 3.1 since it depends on the specific application bitstream that is loaded. A power calculator spreadsheet is offered by Red Rapids to assist in the total power calculation for a specific application.

[(2)]The hardware has not been tested to the environmental specification listed in section 3.1.

Download the Model 314 Power Calculator to determine the power requirements for your application.

3.2 Receiver Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		50		Ohms
ADC Offset Error(1)	-12	+/- 2	+12	mV
DC Coupling Offset Error(1)		+/-50		mV
Full Scale Input (0 dBFS, 50 ohms)				
High Voltage Range				
Input Voltage		2		Vpp
Input Power		+10		dBm
Low Voltage Range				
Input Voltage		1		Vpp
Input Power		+4		dBm

Notes: (1) ADC offset dominates when AC coupled; DC coupling circuit offset dominates when DC coupled.

3.3 Reference/Clock/Trigger Input Levels

Parameter	Min	Typ	Max	Unit
External Reference (REF)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	1.5		3.5	Vpp
Input Power (50 Ohms)	+7		+14.8	dBm
Frequency	10		10	MHz
External Clock Input (CLK IN)				
Input Impedance		50		Ohms
Input Voltage (50 Ohms)	1.0	2.8	2.8	Vpp
Input Power (50 Ohms)	+4	+13	+13	dBm
Frequency	32		125	MHz
Trigger Input (TRIG)				
Input Impedance		50		Ohms
VIL	-0.5		0.8	V
VIH	2.4		5.5	V

3.4 Telemetry ADC Input Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		1k		Ohms
Input Voltage Range	-2.5		+2.5	V
DC Offset	-100		+100	mV
Conversion Rate			100	kHz
Resolution		12		bits

3.5 Receiver Performance

> ☞ Performance may vary depending on the quality of the power supply and EMI environment of the host..

3.5.1 AC-Coupled Option Performance

Measurement conditions: T = 25°C, Supply Voltages (+12, -12, 5, 3.3) nominal

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	1		150	MHz
3 dB	0.1		250	MHz
SNR[2]				
20.17 MHz Input				
High Voltage Range		70		dB
Low Voltage Range		62		dB
70.17 MHz Input				
High Voltage Range		69.8		dB
Low Voltage Range		62.6		dB
125.17 MHz Input				
High Voltage Range		65.3		dB
Low Voltage Range		61.2		dB
SINAD[2]				
20.17 MHz Input				
High Voltage Range		69		dB
Low Voltage Range		61.6		dB
70.17 MHz Input				
High Voltage Range		69.5		dB
Low Voltage Range		62.3		dB
125.17 MHz Input				
High Voltage Range		64.9		dB
Low Voltage Range		60.9		dB
SFDR[2]				
20.17 MHz Input[3]				
High Voltage Range		85[3]		dB
Low Voltage Range		84[3]		dB
70.17 MHz Input				
High Voltage Range		80.7		dB
Low Voltage Range		79		dB
125.17 MHz Input				
High Voltage Range		79.5		dB
Low Voltage Range		75.9		dB
Channel-to-Channel Isolation		90		dB

Notes:

[1]Measured across band from ADC output.

[2]Measured using external clock @ 125 MHz and an internal clock @ 104 MHz.

[3]Estimated due to test equipment limitations.

3.5.2 DC-Coupled Option Performance

Measurement conditions: T = 25℃, Supply Voltages (+12, -12, 5, 3.3) nominal

Parameter	Min	Typ	Max	Unit
Passband [1]				
1 dB	DC		175	MHz
3 dB	DC		200	MHz
SNR[2]				
20.17 MHz Input				
High Voltage Range		66		dB
Low Voltage Range		62		dB
70.17 MHz Input				
High Voltage Range		66.5		dB
Low Voltage Range		60.7		dB
125.17 MHz Input				
High Voltage Range		62.5		dB
Low Voltage Range		59.6		dB
SINAD[2]				
20.17 MHz Input				
High Voltage Range		65.5		dB
Low Voltage Range		61.7		dB
70.17 MHz Input				
High Voltage Range		58.1		dB
Low Voltage Range		54.9		dB
125.17 MHz Input				
High Voltage Range		44.4		dB
Low Voltage Range		47.2		dB
SFDR[2]				
20.17 MHz Input				
High Voltage Range		76.7		dB
Low Voltage Range		76.7		dB
70.17 MHz Input				
High Voltage Range		57.3		dB
Low Voltage Range		58.7		dB
125.17 MHz Input				
High Voltage Range		45.2		dB
Low Voltage Range		48.3		dB
Channel to Channel Isolation		80		dB

Notes:

[1]Measured across band from ADC output.

[2]Measured using external clock @ 125 MHz and an internal clock @ 104 MHz.

3.6 Internal Clock Performance

Parameter	Min	Typ	Max	Unit
Internal Sample Clock				
Frequency (default)		125		MHz
Phase Noise				
1 kHz offset		-90		dBc/Hz
10 kHz offset		-100		dBc/Hz
100 kHz offset		-120		dBc/Hz
Internal Reference				
Frequency (default)		10		MHz
Stability	-1.5		+1.5	ppm
Phase Noise				
1 kHz offset		-125		dBc/Hz
10 kHz offset		-145		dBc/Hz
100 kHz offset		-148		dBc/Hz

3.7 GPIO Voltage Levels

Parameter	Min	Typ	Max	Unit
Input Impedance		10k		Ohms
VIL	-0.5		0.8	V
VIH	2.4		5.5	V
VOH	2.4			V
VOL			0.4	V
IOH at VOH	-24			mA
IOL at VOL	24			mA
3.3V Power				
Voltage	3.1	3.3	3.5	V
Current			500	mA

3.8 USER IO Voltage Levels

Parameter	Min	Typ	Max	Unit
3.3V VCCO				
VIH	2.0		3.6	V
VIL	-0.5		0.8	V
VOH	2.6			V
VOL			0.4	V
2.5V VCCO				
VIH	1.7		2.7	V
VIL	-0.5		0.7	V
VOH	1.9			V
VOL			0.4	V
I IN		+/-5		uA
IOH at VOH	-24			mA
IOL at VOL	24			mA

4.0 Absolute Maximum Specifications

Stresses above those listed in Table 4-1 may cause damage to the unit. The operation of the unit at these or any other conditions outside of those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect unit reliability.

Table 4-1 Absolute Maximum Specifications

Parameter	Min	Typ	Max	Unit
Environmental (Inlet Air)				
Operating Temperature	-30		50	C
Non-Operating Temperature	-30		85	C
Airflow	250			LFM
Signal Inputs **(AC-Coupled)**				
DC Input Voltage	-10		10	Ohms
AC Input Voltage Swing			5	Vpp
AC Input Power			+18	dBm
Signal Input **(DC-Coupled)**				
DC Input Voltage	-2.5		2.5	V
AC Input Voltage Swing			5	Vpp
AC Input Power			+18	dBm
Reference Clock Input (50 ohm)				
DC Level	-10		10	V
AC Swing			4.7	Vpp
AC Power			+17.5	dBm
External Clock Input (50 ohm)				
DC Level	-10		10	V
AC Swing			3.2	Vpp
AC Power			+14	dBm
GPIO	-0.5		7.0	V
USER IO				
2.5 V IO Power Rail			2.8	V
3.3 V IO Power Rail			3.6	V

5.0 Typical Performance Characteristics

The performance plots section is divided into two groups reflecting the coupling options available for the Model 314. The Model 314 is available in an AC or DC coupled configuration as a build option.

Each section contains frequency response and spectral plots of the hardware. The spectral plots provide an indication of receiver performance for a limited set of conditions. Many of the plots are presented in pairs to contrast the performance of the ADC when commanded to its high and low input voltage range.

5.1 Receiver Performance (AC-Coupled Option)

All data is measured with an external sample clock unless otherwise noted.

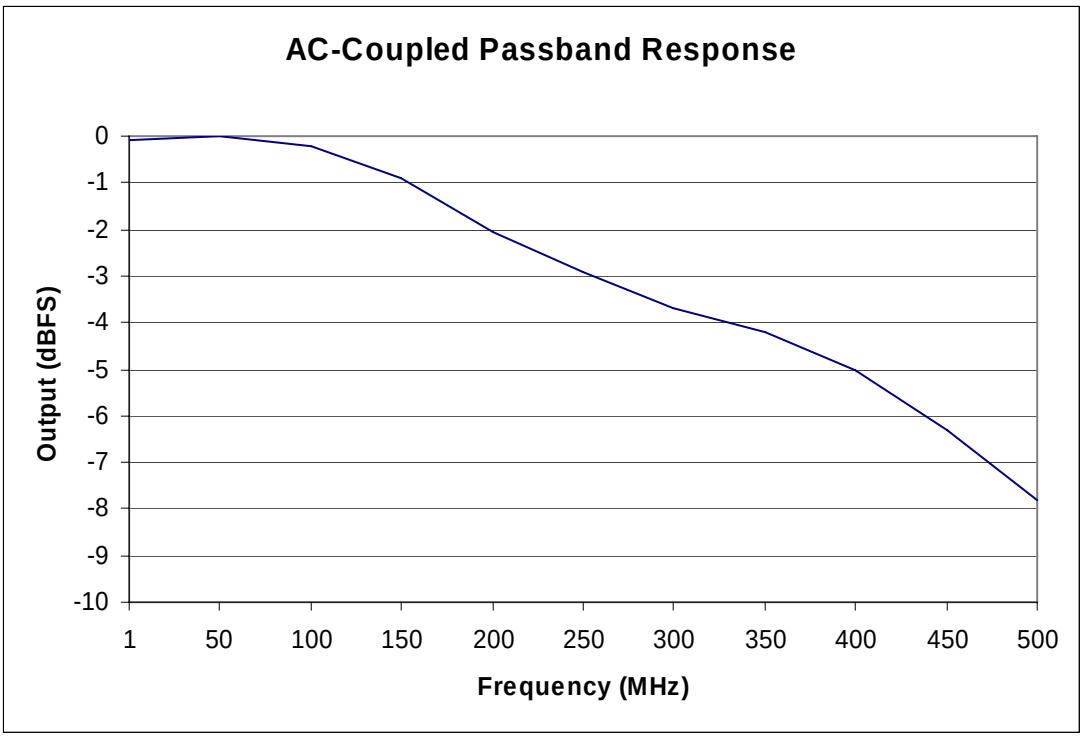


Figure 5-1 AC-Coupled Passband Profile 100 kHz to 500 MHz

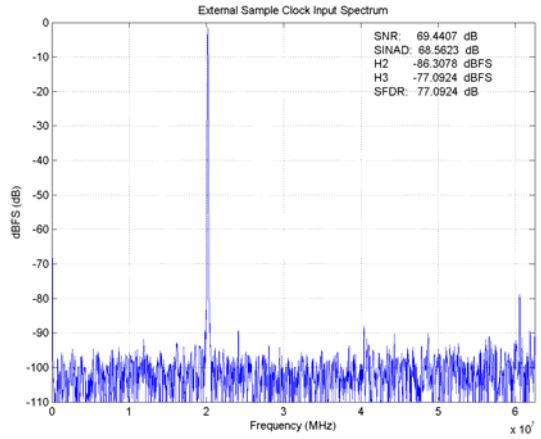


Figure 5-2 High Voltage Range, 125 MSPS, -1.6 dBFS, 20.17 MHz(1)

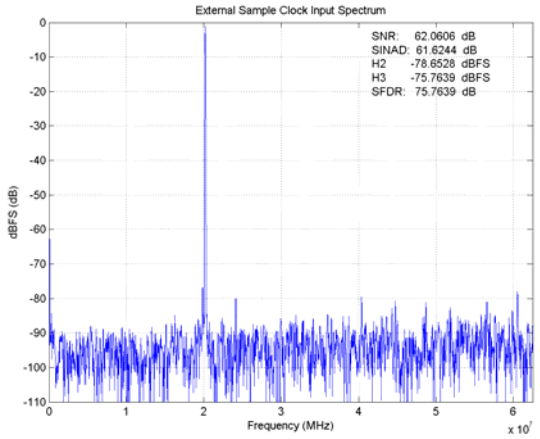


Figure 5-3 Low Voltage Range, 125 MSPS, -1 dBFS, 20.17 MHz(1)

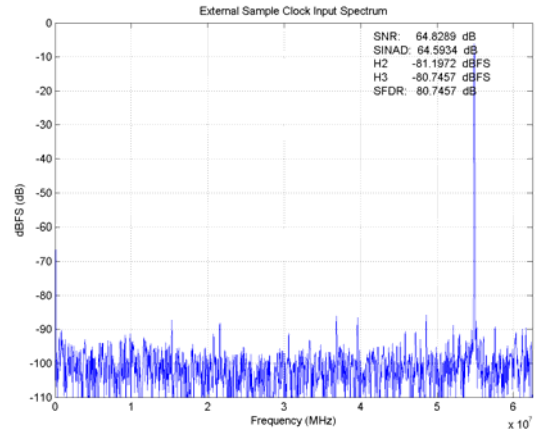


Figure 5-4 High Voltage Range, 125 MSPS, -6 dBFS, 70.17 MHz

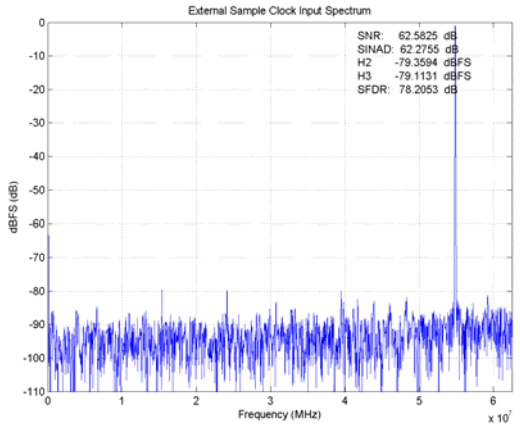


Figure 5-5 Low Voltage Range, 125 MSPS, -1 dBFS, 70.17 MHz

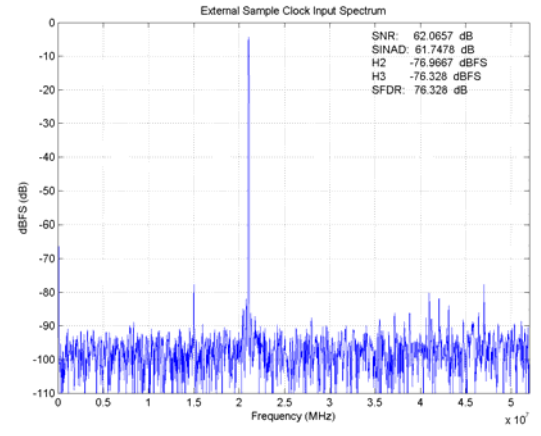


Figure 5-6 High Voltage Range, 104 MSPS, -4.2 dBFS, 125.17 MHz

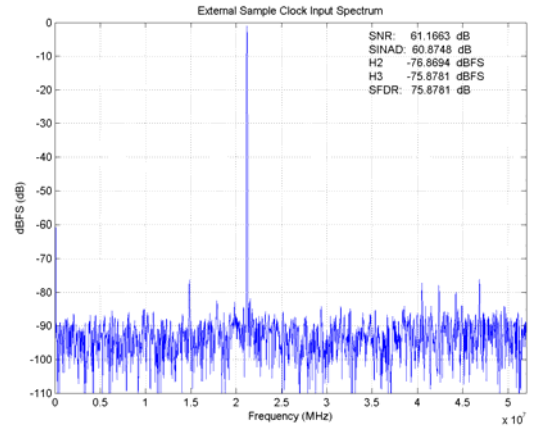


Figure 5-7 Low Voltage Range, 104 MSPS, -1 dBFS, 125.17 MHz

(1)Third harmonic level high due to test equipment limitations.

5.2 Receiver Performance (DC-Coupled Option)

Performance characterization plots of the receiver channel with dc-coupling are provided on the following pages. All of the data is measured with an external sample clock unless otherwise noted.

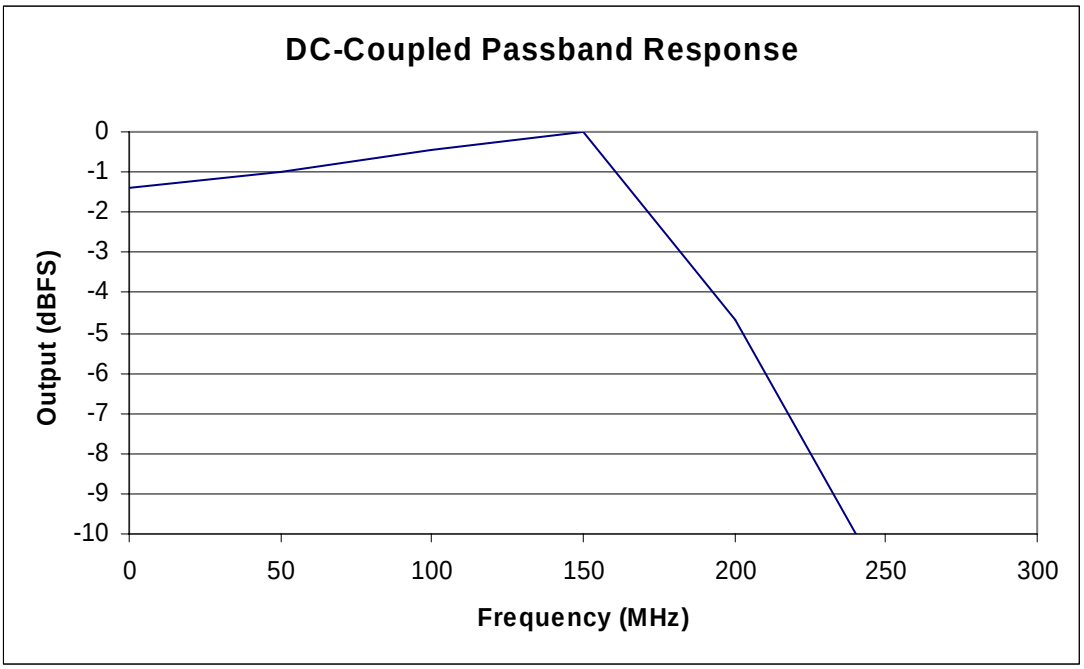


Figure 5-8 DC-Coupled Passband Profile DC to 300 MHz

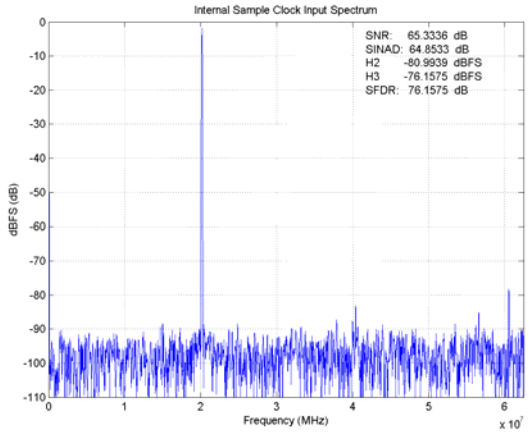


Figure 5-9 High Voltage Range, 125 MSPS, -1.7 dBFS, 20.17 MHz

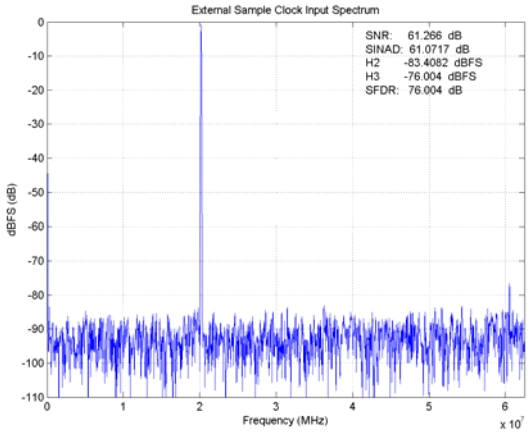


Figure 5-10 Low Voltage Range, 125 MSPS, -1.7 dBFS, 20.17 MHz

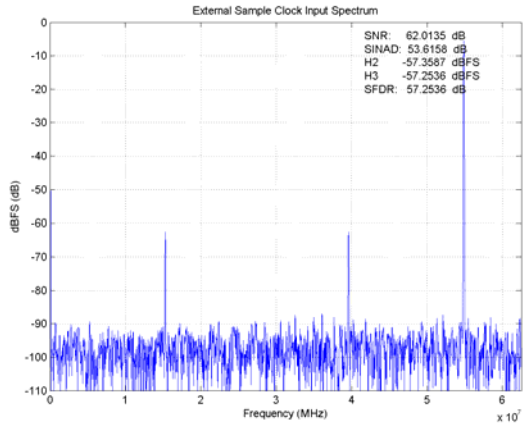


Figure 5-11 High Voltage Range, 125 MSPS, -5.5 dBFS, 70.17 MHz

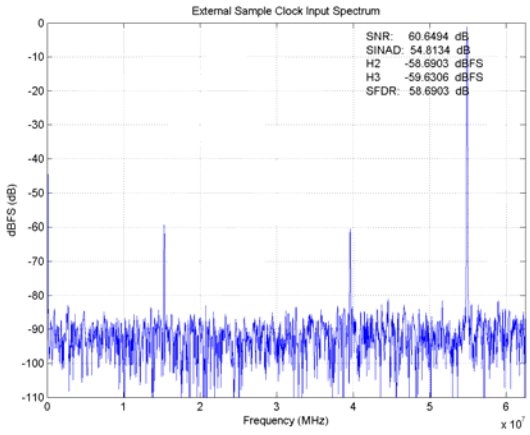


Figure 5-12 Low Voltage Range, 125 MSPS, -1.1 dBFS, 70.17 MHz

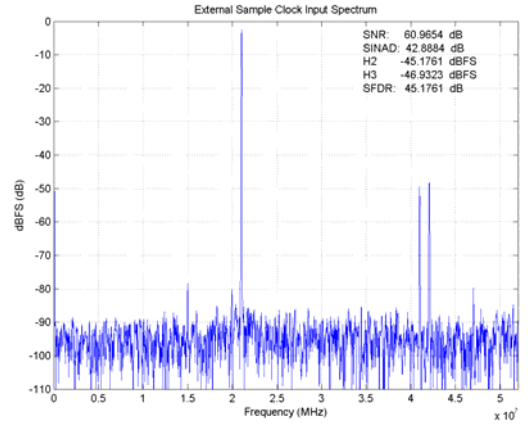


Figure 5-13 High Voltage Range, 104 MSPS, -2.5 dBFS, 125.17 MHz

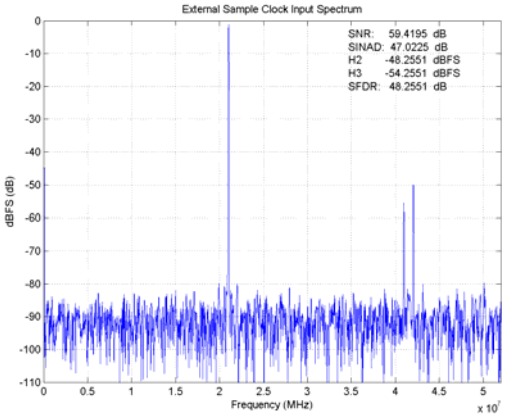


Figure 5-14 Low Voltage Range, 104 MSPS, -1.2 dBFS, 125.17 MHz

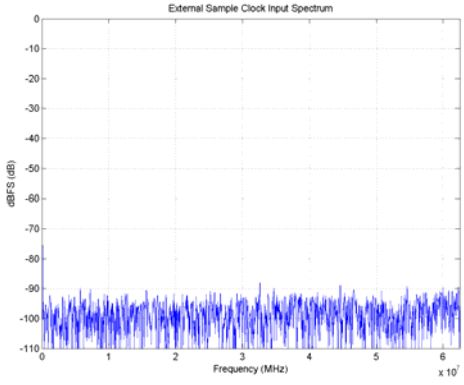


Figure 5-15 High Voltage Range, 125 MSPS, Terminated Input

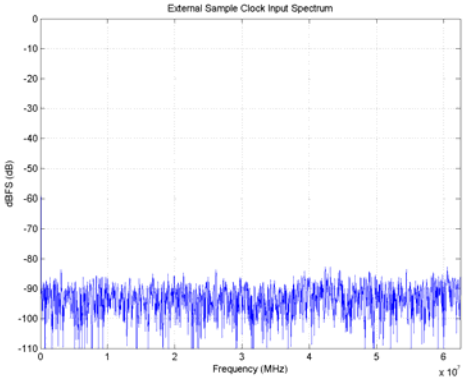


Figure 5-16 Low Voltage Range, 125 MSPS, Terminated Input

6.0 Hardware Description

A high-level block diagram of the M314 Channel Adapter hardware is shown in Figure 6-1. The hardware is divided into six sections consisting of FPGA, receiver, sample clock distribution, SRAM, PCI Interface and IO. The following paragraphs provide a detailed description of each section.

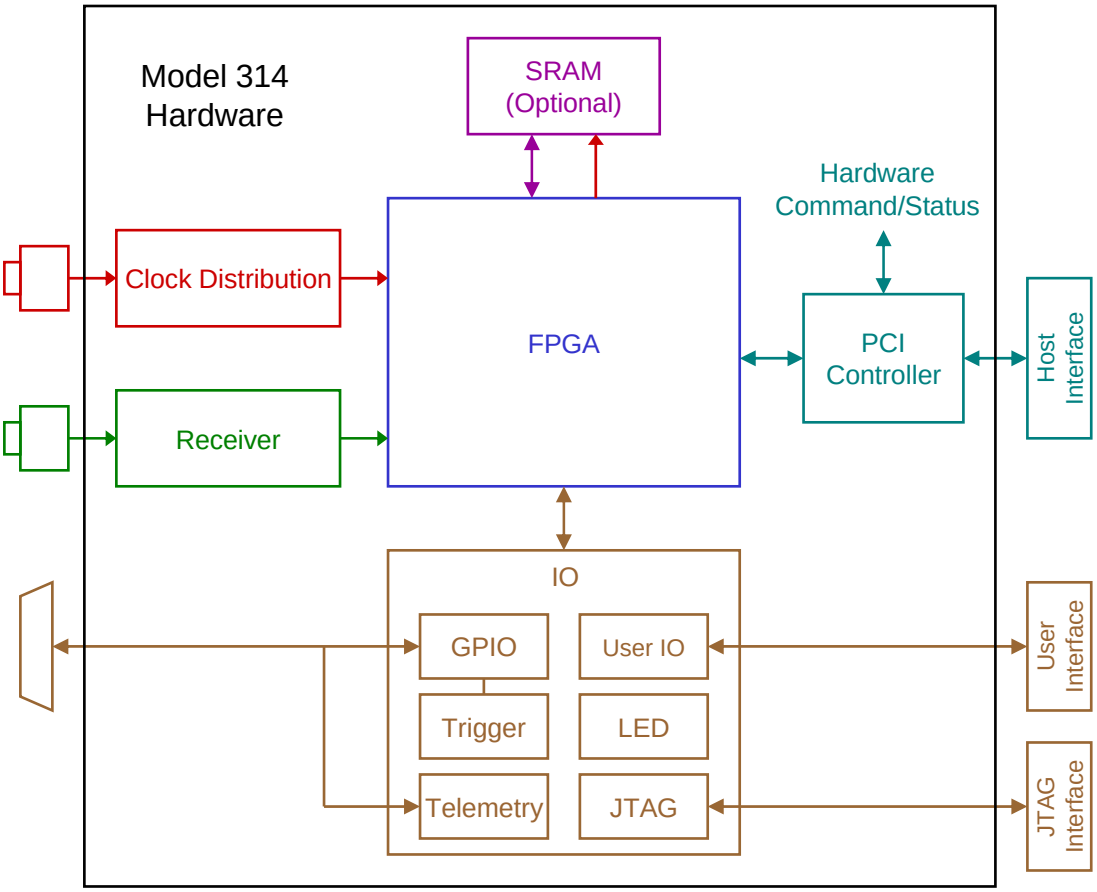


Figure 6-1 Model 320 Hardware Block Diagram

6.1 FPGA

A high-level block diagram of the FPGA with internal cores and interfaces is shown in Figure 6-2. Red Rapids provides FPGA cores to the SRAM, Receiver and PCI Controller to ease integration of FPGA application code with the Channel Adapter hardware. The IO interfaces are governed by the FPGA User Constraints File (UCF) supplied along with the cores.

The Channel Adapter FPGA support package includes VHDL source code for the ADC and SRAM interface cores, the Local Bus interface core is supplied as an NGC file. Red Rapids also provides two FPGA diagnostic configurations in Xilinx Serial Vector Format (XSVF) to help verify the health of the Channel Adapter hardware. Details regarding the cores can be found in the *Channel Adapter FPGA Core Manual*. Diagnostic information can be found in the *Channel Adapter FPGA Software Manual.*

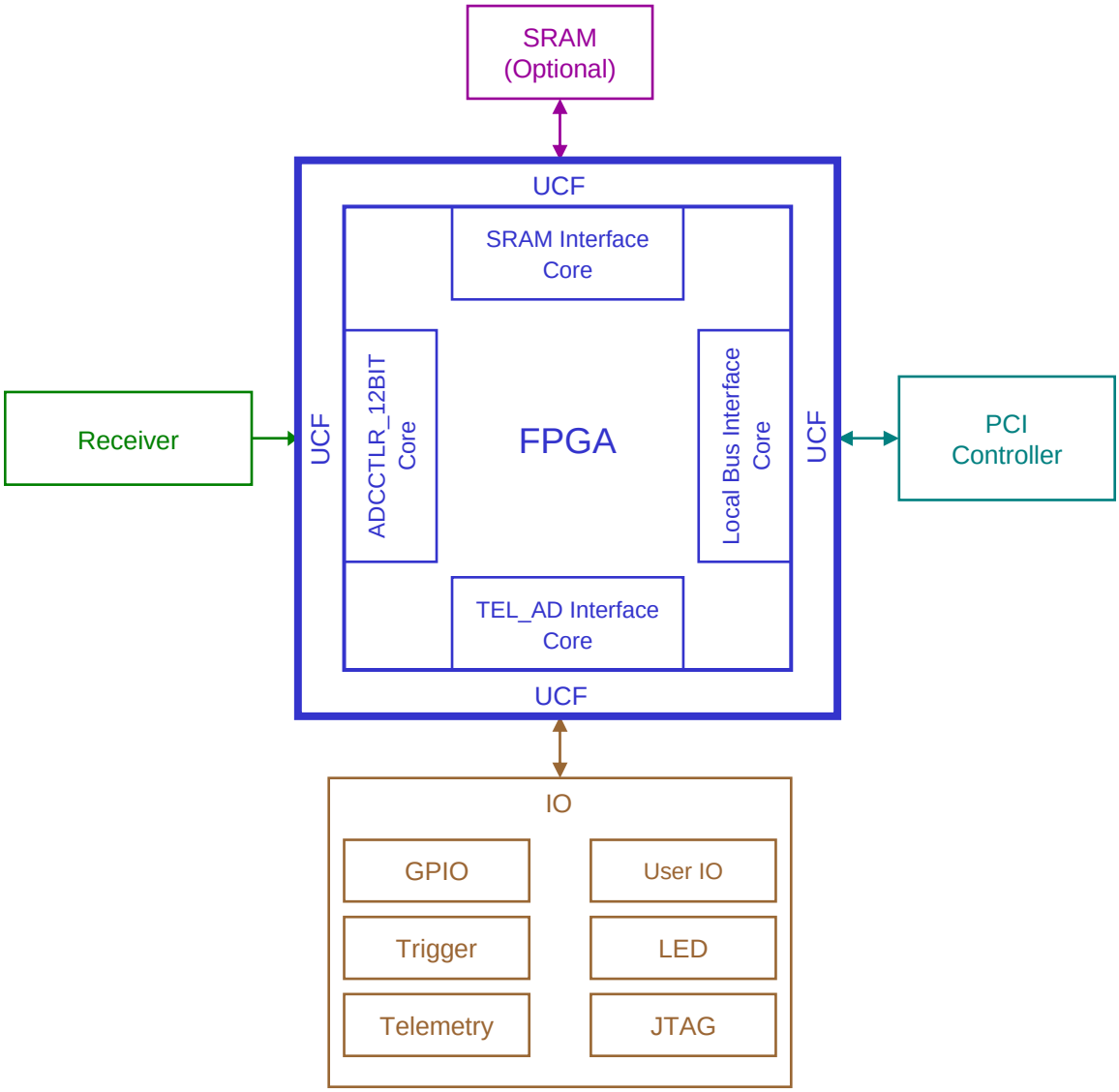


Figure 6-2 FPGA Cores and Interfaces

The Channel Adapter family provides for a wide selection of FPGA build options enabling the user to optimize their hardware for a variety of applications. The list of supported Virtex-4 FPGA devices can be found in Table 6-1.

Table 6-1 FPGA Options

Component	Part Number	Vendor	Comments
Virtex-4 FPGA	XC4VLX40 XC4VLX60 XC4VSX25 XC4VSX35	Xilinx	Virtex-4 FPGA LX: High-performance logic SX: Ultra-high-performance DSP

User configurations are developed using Xilinx standard design flow and tools. Once designs are compiled they can be loaded into the FPGA using one of three methods:

1. The FPGA can be loaded directly over the PCI bus using a software utility supplied with the product.

2. The FPGA can be loaded indirectly from a configuration PROM available for non-volatile storage of a bitstream that will load automatically at power-on.

3. The FPGA can be loaded directly through the JTAG connector using the Xilinx iMPACT software.

More information on FPGA programming can be found in section 6.6.4.

6.2 Receiver

A block diagram of the receiver is shown in Figure 6-3. The receiver consists of four independent analog channels labeled A through D. Each channel is accessed through an SMA connector and sampled by an ADC. The ADC sample clock is sourced by the clock distribution section. Each ADC output consists of a 14-bit data word and an overflow bit that connects to the FPGA. See the *Channel Adapter FPGA Core Manual* for more information on the ADC/FPGA interface.

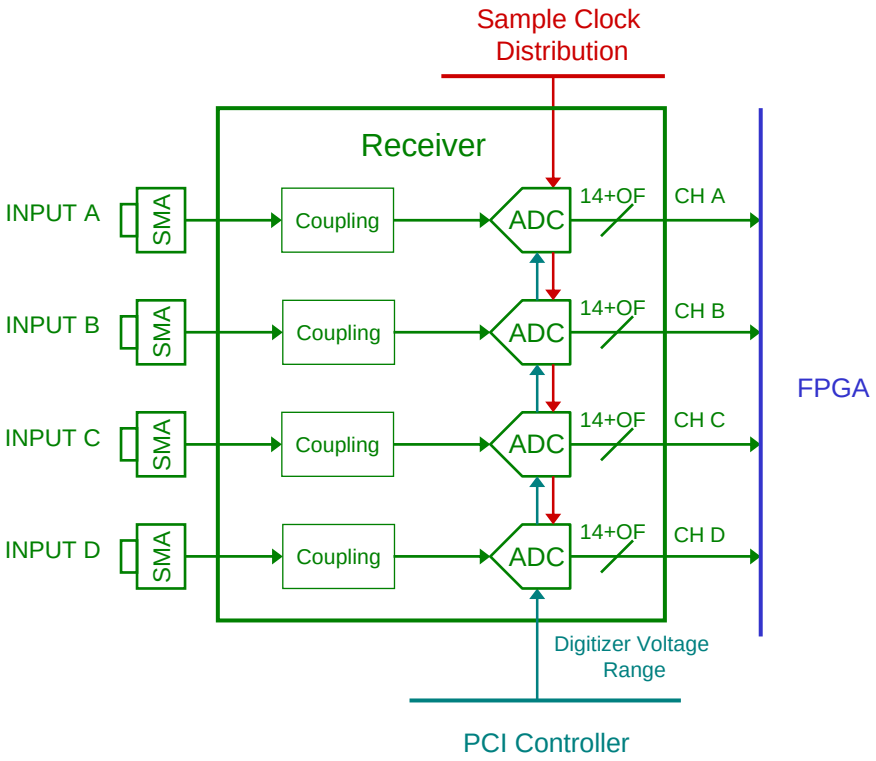


Figure 6-3 Receiver Block Diagram

The Model 314 receiver is available in one of two coupling options, AC or DC. The AC-coupled option provides better dynamic performance at the expense of low frequency response. The DC-coupled option provides better low frequency coverage. There are two ADC input voltage ranges selectable through the PCI controller that enable the user to trade SNR performance for lower input levels.

Receiver input levels are listed in the receiver interface description of section 3.2. Performance specifications can be found in section 3.5.

6.3 Sample Clock Distribution

The board sample clock synchronizes the digitization and data movement functions of the Channel Adapter. A block diagram of the Model 314 sample clock distribution system is shown in Figure 6-4. The clock can be sourced internally or externally and serves to time data acquisition into the FPGA as well as data transfer to SRAM and over the USER IO interface. The following paragraphs provide more detail.

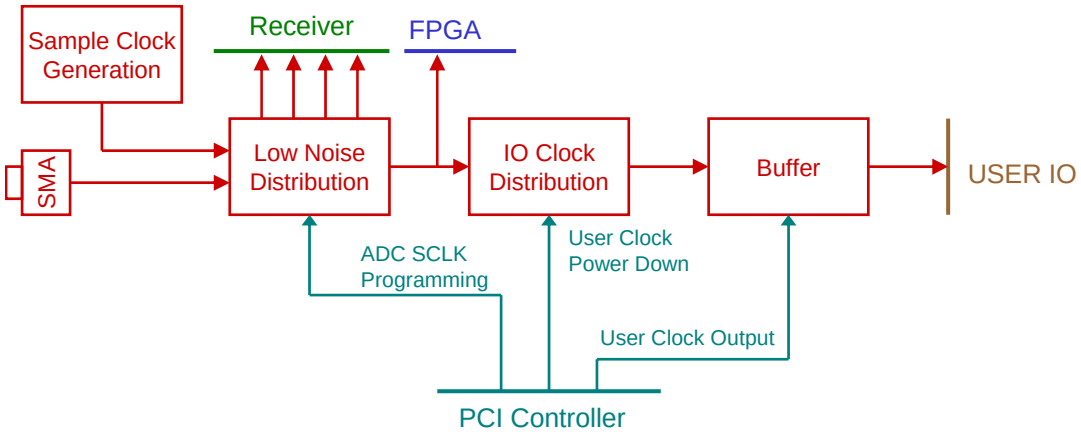


Figure 6-4 Model 314 Clock Distribution

6.3.1 Sample Clock Generation

The Model 314 sample clock may be generated from an on-board fixed frequency synthesizer or a user supplied external clock as shown in Figure 6-5. The sample clock source is selected using the *Adapter_SampleClkSelect* function as described in the Channel Adapter Software Manual.

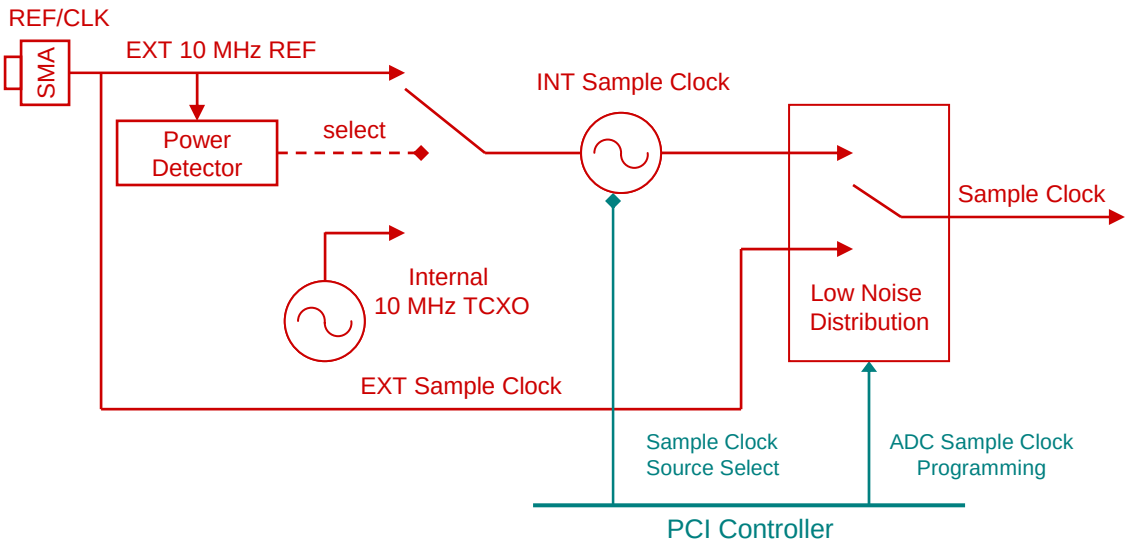


Figure 6-5 Sample Clock Generation

☞	The external sample clock will interfere with the internal sample clock if an internal clock is selected and an external clock is applied.

An external sample clock signal is usually supplied by a high quality source that can provide good frequency stability (< +/- 2ppm) and low phase noise (<90 dBc/Hz @ 10 kHz, <1 ps rms jitter). Quality RF Test equipment may be used as a sample clock source as long as it meets the Model 314 frequency and power requirements.

> ☞ The user supplied external sample clock may be sinusoidal or square in nature so long as it possesses a low phase noise/jitter characteristic.

The frequency synthesizer can be phase locked to an external 10 MHz system reference to achieve system-wide phase coherence by simply connecting a source to the reference clock SMA. The AC power level on the reference input is continuously monitored to automatically detect the presence of an external source. If the power level exceeds the established threshold, the internal TCXO power is automatically turned off. There is hysteresis built into the detection circuit to prevent oscillation around the threshold. Only a high quality low phase noise (< -145 dBc/Hz @ 10 kHz) source should be used as an external reference. Clock input level requirements can be found in section 0.

> ☞ Generally the synthesized output of an RF signal generator should not be used as a 10 MHz reference source rather the rear panel 10 MHz reference output should be used instead.

6.3.2 FPGA Clock Distribution

A copy of the sample clock is available to the FPGA from the low noise distribution chip. The low noise distribution clock is routed to a DCM within the FPGA and used to acquire data from each ADC and transfer data to the SRAM interface. More information on the ADC and SRAM FPGA interface can be found in the *Channel Adapter FPGA Core Manual.*

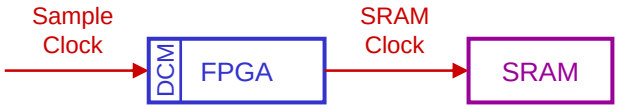


Figure 6-6 FPGA Clock Distribution

6.3.3 USER IO Clock Distribution

The USER IO interface has the capability to use a sample clock sourced by the IO distribution chip or the FPGA. See the USER IO clock section in paragraph 6.6.3.1 for more details.

6.4 SRAM (Build Option)

The Channel Adapter can be ordered with an optional three banks of 250 MHz QDR II SRAM for an additional 24 Mbytes of storage external to the FPGA as shown in Figure 6-7. Each SRAM block represents a single Samsung QDR II SRAM device (K7R641882M-FC25). The chip is organized as 4M x 18 bits, but only 16 bits of input and output are wired to the FPGA due to the limited number of pins available. The user interface to each SRAM is organized as 2M x 32 bits to ease the timing constraints on the application logic.

There is a delay-locked loop (DLL) internal to each SRAM that operates over a limited range of input frequencies (119 MHz to 250 MHz). A DCM inside the FPGA can multiply the sample clock to meet the SRAM frequency range requirement.

> ☞ The SRAM will not operate correctly if the input clock period is outside the range of 4.0 ns to 8.4 ns.

The Channel Adapter FPGA core library includes a DCM that automatically configures this device to the minimum allowable operating frequency greater than or equal to the ADC sample rate. However there may be some instances where the user may wish to operate at a higher legal multiple of the sample clock rate to process data.

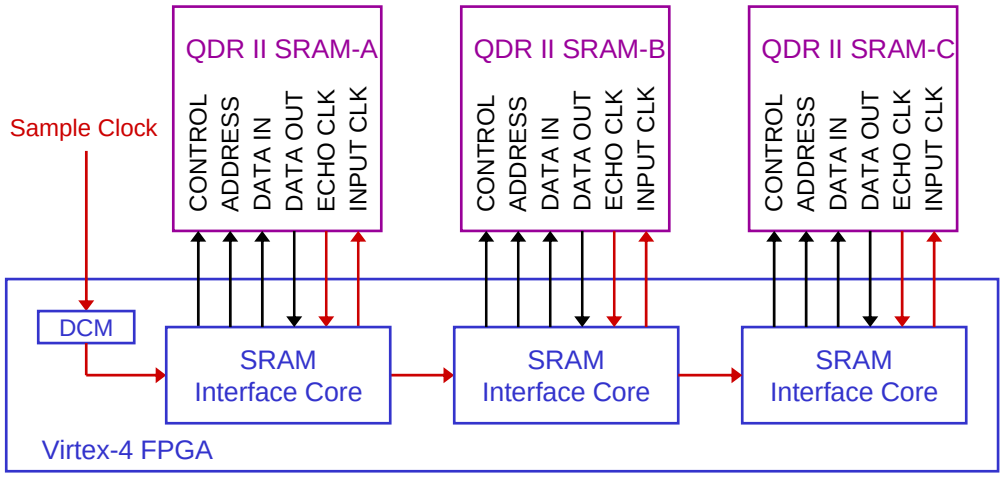


Figure 6-7 External SRAM Interconnect

The SRAM interface core in the FPGA manages the clock domain crossing between data collected at the sample rate and the SRAM running at an integer multiple of this value. Even if the sample and SRAM clock frequencies are matched, a single SRAM can continuously store date from two input channels since both the read and write ports operate at double data rate.

The SRAM interface FPGA core simplifies user interaction with the memory by managing all of the critical timing, including a self-calibration procedure that runs each time the hardware is reset. Please see the *Channel Adapter FPGA Core Manual* for more information.

6.5 PCI Controller

The PCI controller, shown in Figure 6-8, manages communication between the host and the local bus connection to the FPGA. It also includes command/status registers that control the various hardware functions on the card (temp sensor, User interface settings, etc.). Details of the command register functions can be found in the *Channel Adapter Software Manual.*

The local bus interface FPGA core provides the functions needed to efficiently transfer data from the FPGA to host memory. It includes an integrated bus master DMA engine and handles all control of the PCI Controller chip. More information on the Local Bus Interface Core can be found in the *Channel Adapter FPGA Core Reference Manual*.

The PCI Controller facilitates host programming of the FPGA and Configuration PROM over the PCI Bus. User developed configuration files in Xilinx Serial Vector Format (XSVF) can be targeted to either the FPGA or Configuration PROM by selecting the appropriate command line switch. For more information please see the *Channel Adapter Software Manual.*

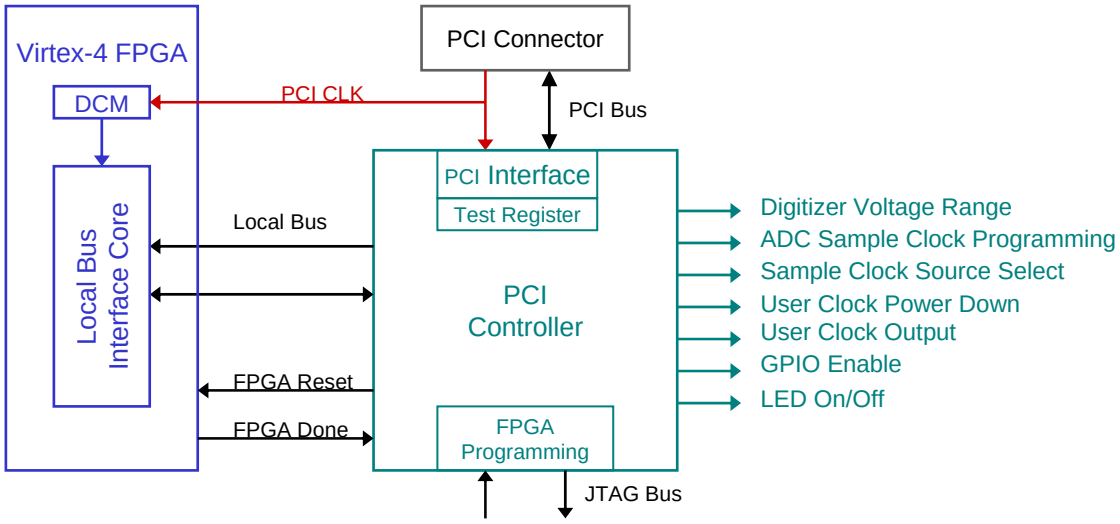


Figure 6-8 PCI Controller Block Diagram

6.6 IO

A block diagram of the Model 314 IO interface is shown in Figure 6-9. There are four user ports connected to the FPGA in addition to a number of LED indicators. The following paragraphs provide a summary of the IO functions found on the Model 314. Some Interface details can be found in the external interface section of paragraph 7.0.

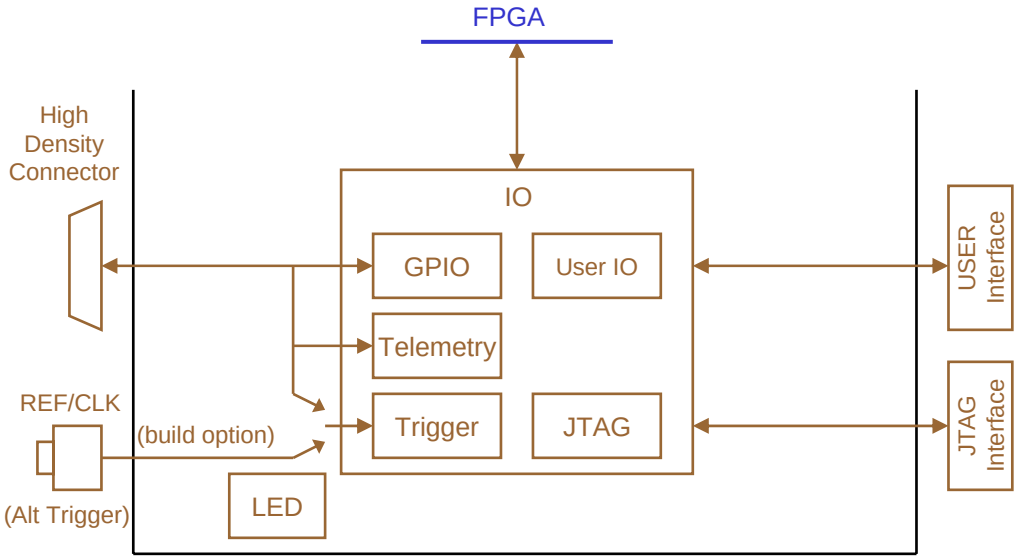


Figure 6-9 IO Block Diagram

6.6.1 GPIO and Telemetry ADC Interface

The Model 314 includes a 15-pin high density front panel connector to support general purpose I/O and an analog telemetry signal. The pin assignments for the GPIO connector are summarized in Table 7-2.

6.6.1.1 GPIO

There are six GPIO signals available on the Model 314; four GPIO signals are connected to pins on the Virtex-4 FPGA and two output only signals are connected

to the PCI Controller as shown in Figure 6-10. All GPIO are routed through a 5 V tolerant FET switch (SN74CB3T3245) enabled by a control signal from the PCI Controller. The protocol for the M314 GPIO is 3.3V LVTTL. The output drive source voltage for all designated FPGA GPIO pins is set to 3.3 V.

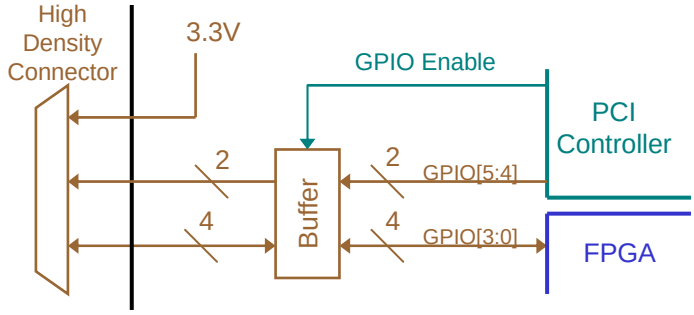


Figure 6-10 GPIO Block Diagram

One of the GPIO pins can be used to source up to 500mA of 3.3V power to an external circuit.

6.6.1.2 Telemetry ADC

The Model 314 features a 12-bit "Telemetry" ADC for digitizing low frequency ancillary signals. The dc-coupled AD7896 from Analog Devices digitizes an analog signal input to the front panel high density connector and passes serial data to the FPGA as shown in Figure 6-11. The ADC is capable of sampling at rates up to 100 KHz. A telemetry_ADC core is provided by Red Rapids to simply the FPGA/telemetry ADC interface. Please see the *Channel Adapter Core Manual* for more information. Telemetry ADC input levels are specified in section 3.4. Telemetry ADC connector information is available in section 7.1.

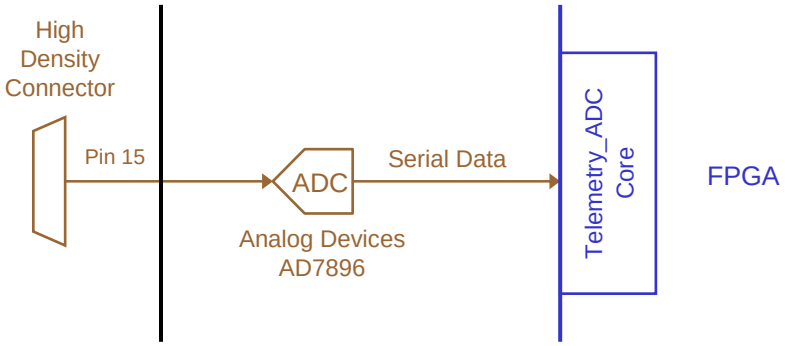


Figure 6-11 Telemetry ADC

6.6.2 Coaxial Trigger (Build Option) Interface

The Model 314 REF/CLK coaxial port can be connected to a 50 Ohm terminated LVTTL buffer as a build option. The output of the buffer is routed to the FPGA for use as a user trigger, gate or window function as shown in Figure 6-12. Trigger input levels are specified in section 0. Trigger connector information is available in section 7.1.

The external reference and sample clock functions are not available if the coaxial trigger build option is selected. .

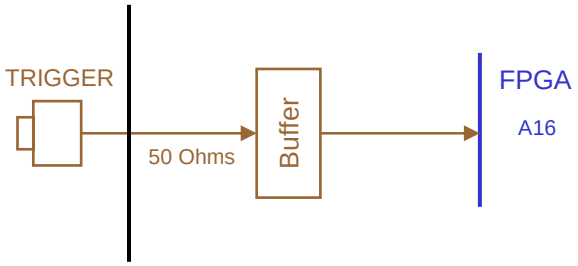


Figure 6-12 Coaxial Trigger (Option)

6.6.3 USER IO Interface

The Channel Adapter is equipped with a user defined connector that is wired directly to the FPGA as shown in Figure 6-13. This is the P4 connector on a PMC module, an optional SCSI connector on a PCI card and the J2 interface on a CPCI card. See section 0 for connector details. The default PMC build configuration supports 2.5V LVDS with up to 27 differential pairs plus clock.

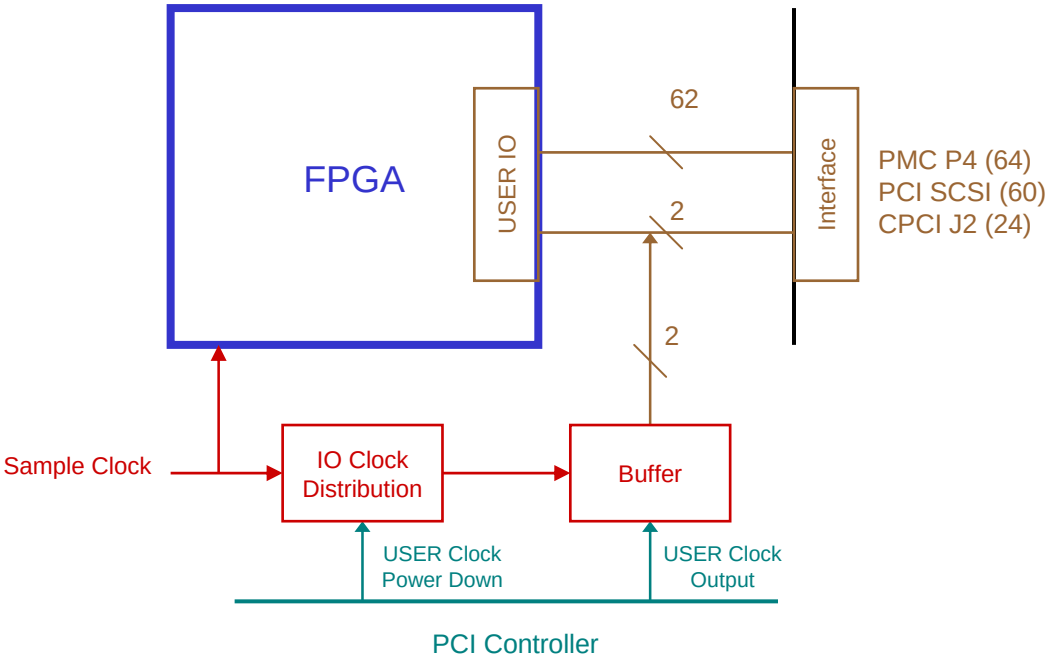


Figure 6-13 USER IO Interface

6.6.3.1 USER IO Clock Lines

Two of the USER IO lines (USER61/USER63) can be used as dedicated clock lines as shown in Figure 6-14. These lines are connected to the FPGA as a clock input and to the sample clock distribution network as a clock output. This structure gets around a restriction in the Virtex-4 IOB that prohibits low capacitance inputs optimized as clock receivers from driving LVDS. The circuit of Figure 6-14 enables the user to drive an LVDS clock out of one Channel Adapter into the clock input of another Channel Adapter.

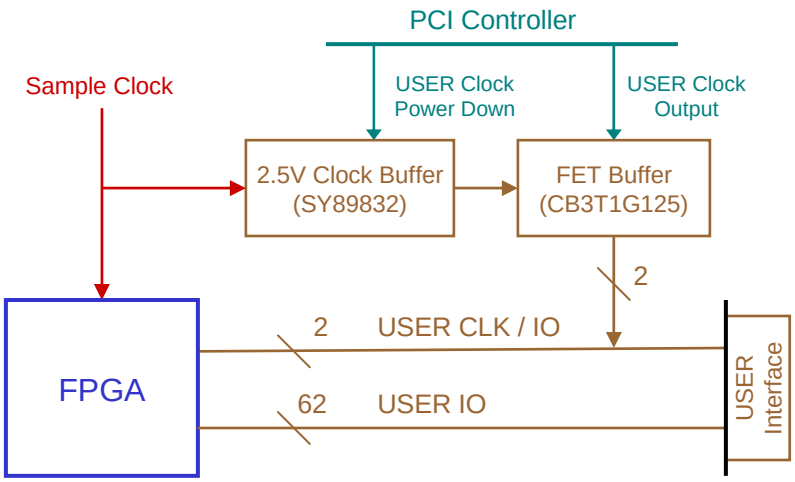


Figure 6-14 User Clock Interface

Clock output is controlled by the *USER Clock Control* register described in the *Channel Adapter Software Manual*. The User may drive the clock lines by enabling the User Clock Output.

> **!** A conflict will occur if User Clock Output is enabled and FPGA IO pins D25 and D26 are programmed as outputs.

Users do not have to use the dedicated clock output, the FPGA may output a clock on any of the User IO lines subject to the IOB limitations of Virtex-4. IO lines highlighted in yellow in Table 7-3, Table 7-4 and Table 7-5 emanate from low capacitance IO blocks and are subject to restrictions.

Users need to account for timing differences between the USER IO at the FPGA pins and USER Clock at its buffer output. A copy of the ADC sample clock is provided to the FPGA and USER Clock interfaces. The User Clock passes through a 2.5V LVDS buffer (SY89832) and FET gate (CB3T1G125) prior to exiting the board. Timing data is available from the vendor data sheets listed in Table 6-2.

6.6.3.2 USER I/O Standards

The Virtex-4 FPGA supports a wide variety of I/O standards through different combinations of driver voltages, reference voltages, and termination schemes. Some standards are not supported by virtue of the Channel Adapter hardware configuration. The following paragraphs describe the hardware options available for the USER IO interface. Users should refer to the Virtex-4 User Guide to determine which standards are supported.

The driver voltage of the USER defined I/O bank can be tied to either 2.5 V (default) or 3.3 V. The VRP/VRN (USER62/USER64) default connection is to IO bank voltage and ground respectively. The VRP/VRN jumper resistors can be removed as a build option to free up USER62 and USER64 for use as IO as shown in Figure 6-15. There are no terminations external to the Virtex-4, the mechanism for termination is the digitally controlled impedance (DCI) feature of the IOB.

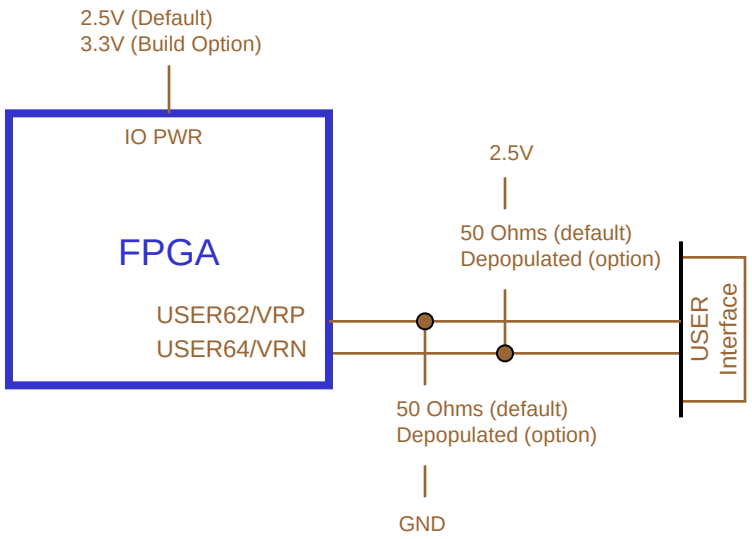


Figure 6-15 USER IO Options

There are no provisions to supply power to the reference voltage pins of the FPGA I/O bank assigned to the USER defined connector.

!	USER IO is hardwired directly to the FPGA. Users must ensure that system IO levels do not exceed FPGA I/O bank voltage maximums. Failure to do so may result in severe FPGA damage.

6.6.4 JTAG Interface

The FPGA and Configuration PROM are user programmable devices that can be loaded with application logic directly from the host through the PCI Controller or through the JTAG pins located on the back of the card. As shown in Figure 6-16, the JTAG chain is composed of the Configuration PROM followed by the FPGA.

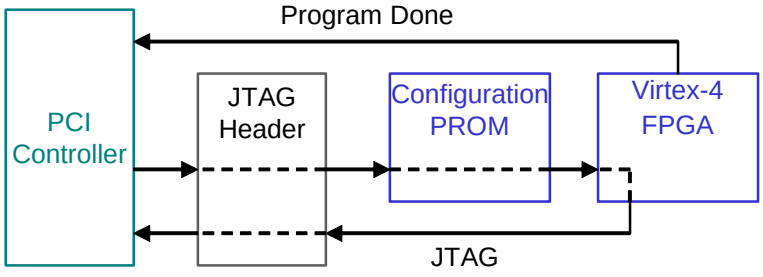


Figure 6-16 JTAG Chain

A JTAG interface header provides access to the Xilinx Configuration PROM and Virtex-4 FPGA. The JTAG port can be directly connected to a Xilinx programming cable to configure the devices using the Xilinx iMPACT™ tool or perform debug with Xilinx ChipScope™. See section the *Channel Adapter FPGA Core Manual* for information on programming the PROM and FPGA via the JTAG port. See section 7.3.1 for JTAG header location and pin descriptions.

6.6.5 LED Indicators

Several LED indicators are available on the Model 314 to provide visual configuration confirmation and support integration and test efforts. A detailed list of LED functions and locations can be found in section 7.3 of this document.

6.7 Key Components

The key hardware components for the Model 314 assembly are listed in Table 6-2. This information is supplied to assist in the development of custom application logic for the FPGA.

Table 6-2 Key Hardware Components

Component	Part Number	Vendor	Comments
Receiver ADC	LTC2255	Linear Technology	14-bit, 125 MSPS, A/D Converter
Telemetry ADC	AD7896	Analog Devices	12-bit, 100 kSPS, serial A/D Converter
Virtex-4 FPGA	XC4VLX40 XC4VLX60 XC4VSX25 XC4VSX35	Xilinx	Virtex-4 FPGA LX: High-performance logic SX: Ultra-high-performance DSP
Config PROM	XCF16P XCF32P	Xilinx	The XCF16P Configuration PROM supports all of the Virtex-4 FPGA options except the LX60. Cards built with the LX60 option are equipped with the XCF32P.
PCI Controller	QL5064	QuickLogic	The PCI Bridge is designed to operate with the Red Rapids Local Bus Interface FPGA core.
SRAM (Optional)	K7R641882M-FC25	Samsung	QDR II SRAM, 250 MHz
8-bit FET Bus Switch	SN74CB3T3245	TI	2.5V/3.3V Low-voltage with 5V tolerant level shifter.
2.5V Clock Buffer	SY89832U	Micrel	1:4, 2.5V differential LVDS buffer
Single FET Bus Switch	CB3T1G125	TI	Single FET bus switch
Frequency Synth	ASY-801-026	Red Rapids	125 MHz (default) fixed frequency synthesizer.
TCXO	OSC-1	Vectron	Oscillator, 10 MHz, ± 1.5 ppm
GPIO Connector	A28100-015	Omnetics	Dual Row Nano 15-position connector
GPIO Mating Connector	A29000-115	Omnetics	Dual Row Nano 15-position connector with 18 inch pigtail

7.0 External Interfaces

7.1 Front Panel Interface

There are six external connectors located along the face of the Model 314 module as shown in Figure 7-1. The five coaxial SMA connectors are 50 Ohm terminated analog inputs. Four of the connectors are assigned to the A, B, C and D receiver channel signal inputs. The remaining SMA is available for an external reference, sample clock or trigger depending on the assembly build option. A 15-pin high-density connector is also provided for general purpose I/O (GPIO) that includes six digital signals and an analog input.

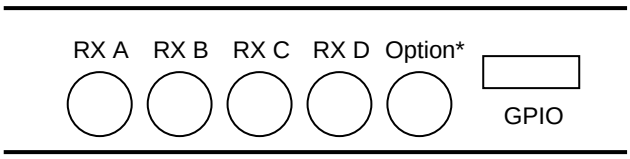


Figure 7-1 Model 314 Front Panel Connectors

The Model 314 front panel connections are summarized in Table 7-1. Input level and performance data can be found in section 3.0.

Table 7-1 Front Panel Connectors

Des	Label	Connector	Description
J1	RX A	SMA	Receiver Channel A
J2	RX B	SMA	Receiver Channel B
J3	RX C	SMA	Receiver Channel C
J4	RX D	SMA	Receiver Channel D
J5	REF/CLK	SMA	10 MHz reference/Sample Clock/Trigger
P5	GPIO	High Density 15pin	General Purpose IO

GPIO is supplied through a Omnetics Dual Row Nano 15-position connector (PN A28100-015). The pinout for the connector is shown in Table 7-2. The FPGA and buffer output drive source voltage for all designated I/O pins is set to 3.3 V. The GPIO pins use 3.3V LVTTL protocol, voltage levels are listed in section 3.7. The 3.3V power pin can supply up to 500 mA of current. The reserved pin should not be connected. The analog input specifications for the telemetry ADC are provided in section 3.4.

The mating connector assembly is available from Red Rapids or directly from Omnetics (PN A29000-115). Red Rapids supplies one mating connector cable assembly with each unit. The cable assembly consists of a single mating connector and an 18 inch minimum pigtail. Connector details are shown in Figure 7-3 and Figure 7-3.

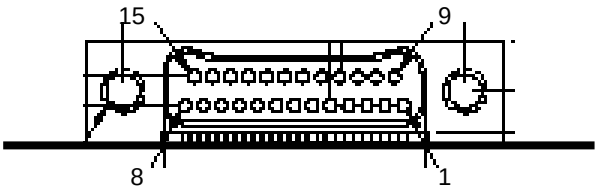
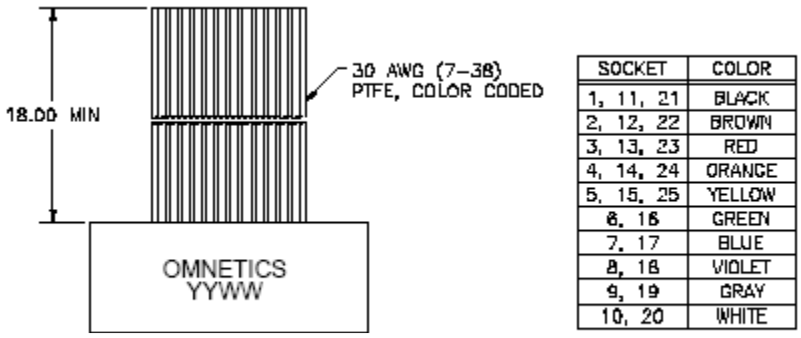


Figure 7-2 General Purpose I/O Connector Detail



SOCKET	COLOR
1, 11, 21	BLACK
2, 12, 22	BROWN
3, 13, 23	RED
4, 14, 24	ORANGE
5, 15, 25	YELLOW
6, 16	GREEN
7, 17	BLUE
8, 18	VIOLET
9, 19	GRAY
10, 20	WHITE

Figure 7-3 General Purpose I/O Mating Cable Connector

Table 7-2 General Purpose I/O Connector Pinout

Pin	Signal Type	Signal Name	FPGA Pin
1	GND		
2	GND		
3	GND		
4	GND		
5	GND		
6	GND		
7	Power	3.3V	
8	Reserved		
9	I/O	GPIO2	Y10
10	I/O	GPIO3	AA10
11	I/O	GPIO0	AA9
12	I/O	GPIO1	Y9
13	Output	GPIO4	(PCI CTLR)
14	Output	GPIO5	(PCI CTLR)
15	Analog	Telemetry Data	

7.2 Host Interface

The Channel Adapter family is available in three form factors, PMC, PCI and CPCI. Each form factor has a unique PCI and USER interface. The Model 314 uses PCI 2.2 protocol to communicate over the host PCI interface. The USER interface is hard wired to the FPGA for user configuration. The following sections describe pin assignments for each of the Channel Adapter form factors.

!	The Model 314 can only be used in a 3.3V signaling environment. Installing the unit in a 5V signaling slot will damage the card.

7.2.1 PMC Host Interface

The PMC versions of the Model 314 contain four host interface connectors designated as P1-P4. The PCI interface is implemented on the P1 – P3 connectors, the P4 connector is used for USER IO.

7.2.1.1 PMC PCI Interface (P1-P3)

The pin assignments for the P1-P3 connectors are governed by IEEE standard 1386.1-2001, “IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)”. The PCI protocol is governed by the PCI Local Bus Specification, revision 2.2.

7.2.1.2 PMC P4 USER IO

The PMC P4 pinout, provided in Table 7-3, follows the VITA 46 convention for assignment of differential signals. The listing is organized by positive and negative differential pairs as defined by the FPGA I/O bank.

Table 7-3 PMC USER Defined Connector Pinout

Name	P4 Pin	FPGA Pin (Negative)	FPGA Pin (Positive)	P4 Pin	Name
USER1	1	F17	E17	3	USER3
USER2	2	D17	C17	4	USER4
USER5	5	E18	F18	7	USER7
USER6	6	A18	B18	8	USER8
USER9	9	F19	G19	11	USER11
USER10	10	D18	C19	12	USER12
USER13	13	E24	E25	15	USER15
USER14	14	A19	A20	16	USER16
USER17	17	G20	H20	19	USER19
USER18	18	E20	F20	20	USER20
USER21	21	H21	H22	23	USER23
USER22	22	B20	C20	24	USER24
USER25	25	B21	C21	27	USER27
USER26	26	A21	A22	28	USER28
USER29	29	E22	E23	31	USER31
USER30	30	C22	D22	32	USER32
USER33	33	H23	H24	35	USER35
USER34	34	C23	D23	36	USER36
USER37	37	C24	D24	39	USER39
USER38	38	B23	B24	40	USER40
USER41	41	H25	H26	43	USER43
USER42	42	G25	G26	44	USER44
USER45	45	D19	D20	47	USER47
USER46	46	E26	F26	48	USER48
USER49	49	C25	C26	51	USER51
USER50	50	D21	E21	52	USER52
USER53	53	G23	G24	55	USER55
USER54	54	A23	A24	56	USER56
USER57	57	F23	F24	59	USER59
USER58	58	G17	G18	60	USER60
USER61/CLKN	61	D25	D26	63	USER63/CLKP
USER62/VRP	62	G21	G22	64	USER64/VRN

Notes:

(1) Pins highlighted in yellow are subject to IOB limitations as low capacitance pins and cannot be used as LVDS drivers.
(2) USER61/USER62 and CLKN/CLKP can be switched by software.
(3) VRP/VRN are tied to a DCI voltage reference resistor (default). They can be used as USER IO as a build option.

7.2.2 PCI Card Host Interface

The PCI versions of the Model 320 implement the PCI bus on the card edge connector that runs along the bottom edge of the PCI carrier. USER IO is supported though a SCSI connector mounted on the board back plate.

7.2.2.1 PCI Card PCI Interface

The pin assignment for the card edge connector is governed by the “PCI Local Bus Specification Revision 2.2“. Please refer to the specification for more information regarding these signals.

7.2.2.2 PCI Card Rear Panel USER IO Interface

The USER IO PCI SCSI pinout is provided in Table 7-4. The listing is organized by positive and negative differential pairs as defined by the FPGA I/O bank.

Table 7-4 PCI USER Defined Connector Pinout

Name	SCSI Pin	FPGA Pin (Negative)	FPGA Pin (Positive)	SCSI Pin	Name
USER1	1	F17	E17	35	USER3
USER2	2	D17	C17	36	USER4
USER5	3	E18	F18	37	USER7
USER6	4	A18	B18	38	USER8
USER9	5	F19	G19	39	USER11
USER10	5	D18	C19	40	USER12
USER13	7	E24	E25	41	USER15
USER14	8	A19	A20	42	USER16
USER17	9	G20	H20	43	USER19
USER18	10	E20	F20	44	USER20
USER21	11	H21	H22	45	USER23
USER22	12	B20	C20	46	USER24
USER25	13	B21	C21	47	USER27
USER26	14	A21	A22	48	USER28
USER29	15	E22	E23	49	USER31
USER30	16	C22	D22	50	USER32
USER33	17	H23	H24	51	USER35
USER34	18	C23	D23	52	USER36
USER37	19	C24	D24	53	USER39
USER38	20	B23	B24	54	USER40
USER41	21	H25	H26	55	USER43
USER42	22	G25	G26	56	USER44
USER45	23	D19	D20	57	USER47
USER46	24	E26	F26	58	USER48
USER49	25	C25	C26	59	USER51
USER50	26	D21	E21	60	USER52
USER53	27	G23	G24	61	USER55
USER54	28	A23	A24	62	USER56
USER57	29	F23	F24	63	USER59
USER58	30	G17	G18	64	USER60
USER61/CLKN	31	D25	D26	65	USER63/CLKP
USER62/VRP	32	G21	G22	66	USER64/VRN
GND	33			67	GND
3.3 V	34			68	5.0 V

Notes:

(1) Pins highlighted in yellow are subject to IOB limitations as low capacitance pins and cannot be used as LVDS drivers.

(2) USER61/USER62 and CLKN/CLKP can be switched by software.

(3) VRP and VRN are tied to a DCI voltage reference resistor (default). They can be used as USER IO as a build option.

7.2.3 CPCI Card Host Interface

The CPCI versions of the Model 320 communicate through two high density 64-pin connectors labeled J1 and J2 opposite the front panel. The 32-bit PCI bus is implemented on the J1 connector. 64-bit bus implementation requires the J1 and J2 connectors. USER IO is limited to 24 pins on the J2 connector.

7.2.3.1 CPCI Card PCI Interface

The pin assignment for the PCI interface on the CPCI connector is governed by PICMG 2.0, "CompactPCI® Specification". Please refer to the specification for more information regarding these signals.

7.2.3.2 CPCI Card USER IO Interface

The USER IO pin assignments for the CPCI J2 connector are provided in Table 7-5. There are 24 USER IO available for the CPCI version of the Model 320.

Table 7-5 CPCI USER Defined Connector Pinout

Name	CPCI J2	FPGA Pin	FPGA Pin	CPCI J2	Name
USER1	A19	F17	E17	B19	USER3
USER2	A21	D17	C17	B21	USER4
			F18	D19	USER7
			B18	D21	USER8
USER9	E19	F19			
USER10	E21	D18			
USER13	A16	E24	E25	B16	USER15
USER14	A18	A19	A20	B18	USER16
			H20	D15	USER19
			F20	D17	USER20
USER21	E15	H21			
USER22	E17	B20			
			A22	C1	USER28
USER30	B2	C22			
USER34	C3	C23	D23	B4	USER36
USER53	D1	G23	G24	D3	USER55
			F24	E1	USER59
USER61/CLK	E3	D25			

Notes:

(1) Pins highlighted in yellow are subject to IOB limitations as low capacitance pins and cannot be used as LVDS drivers.

(2) USER61/CLK can be switched by software.

7.3 Board Interface

7.3.1 JTAG Interface

Figure 7-4 illustrates the location of the JTAG connector on the Model 320 close to the Virtex-4 FPGA. The header consists of six recessed pin receptacles spaced on 0.1 inch centers. The receptacle will accept a 0.022 inch to 0.034 inch diameter pin or a 0.025 inch square pin. The flying leads supplied with the Xilinx programming cable are compatible with the receptacles. All of the pins except TRSTB must be connected for programming.

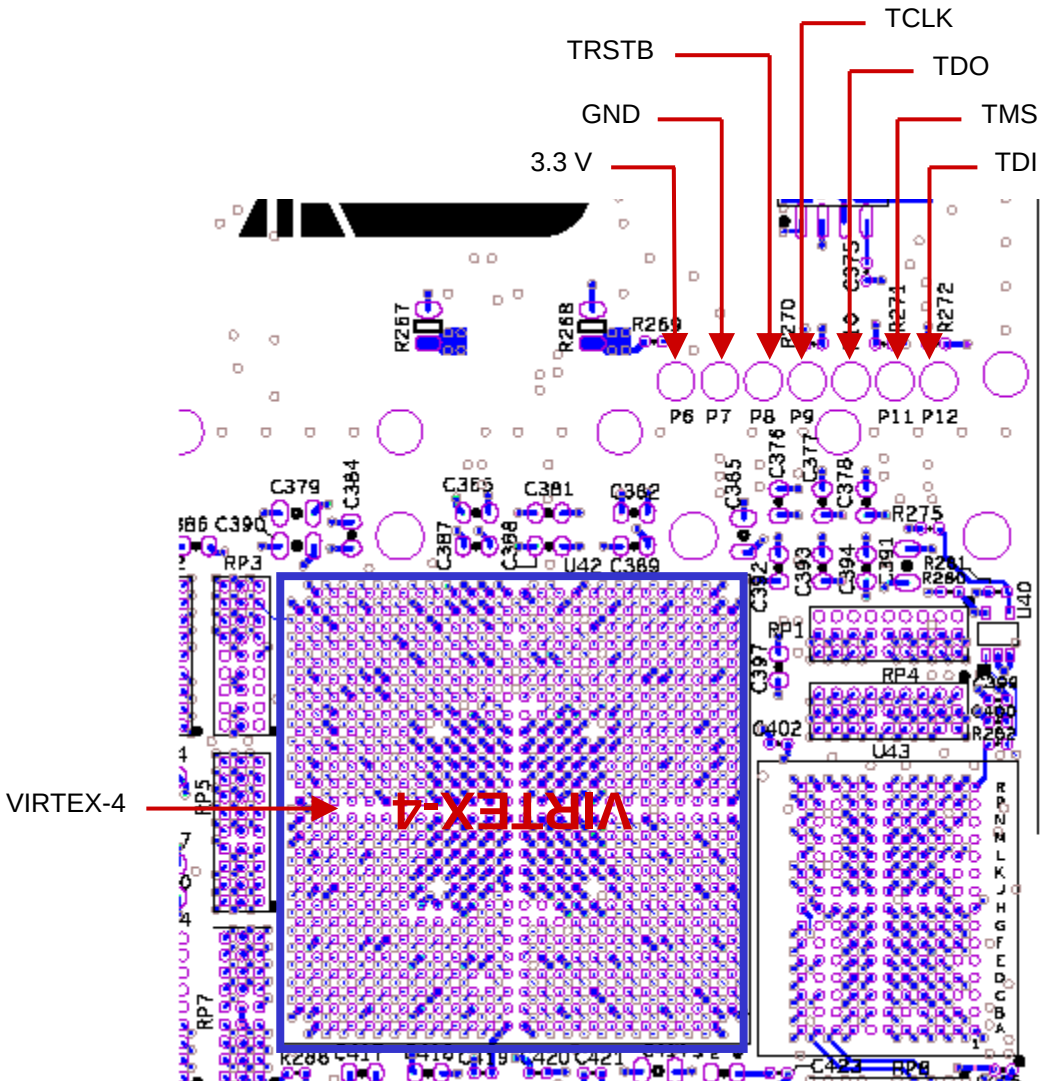


Figure 7-4 JTAG Header Location

Table 7-6 lists the mapping of pin reference designators on the PWB to the corresponding JTAG signal name.

Table 7-6 JTAG Header Signal Mapping

Reference Designator	Signal Name
P6	3.3 V
P7	GND
P8	TRSTB
P9	TCLK
P10	TDO
P11	TMS
P12	TDI

7.3.2 PMC LED Indicators

There are several LED indicators that report various hardware status functions as listed in Table 7-7. Two of the LEDs (D2 & D3) are tied to a bit in the *LED Control* register which can be toggled from application software. Some of the indicators are not present on hardware preceding revision R01.

Table 7-7 LED Operating Status Indicators

Reference Designator	Color	Status (Illuminated)
D1	Red	Frequency synthesizer fault (not locked).
D2	Yellow	External 10 MHz reference active.
D3	Green	Internal 10 MHz reference active.
D4	Green	User programmable from software (LED B).
D5	Yellow	User programmable from software (LED A).

The location of the diodes are shown in Figure 7-5.

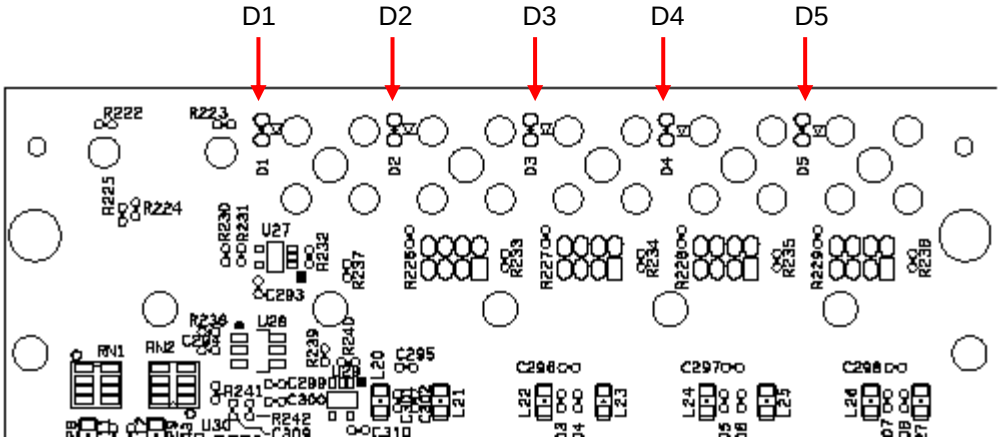


Figure 7-5 Diode Locations

7.3.3 PCI LED Indicators

The PCI version of the hardware includes additional LED indicators that report information on the power supply status from the host bus as described in Table 7-8

Table 7-8 LED PCI Power Status Indicators

Reference Designator	Color	Status (Illuminated)
D1	Yellow	Host PCI bus is signaling at 3.3 V.
D2	Green	Host PCI bus is signaling at 5.0 V.
D3	Blue	-12 V power is present.
D4	Blue	+12 V power is present.
D5	Yellow	3.3 V power is present.
D6	Green	5.0 V power is present.

The location of the PCI diodes are shown in Figure 7-6.

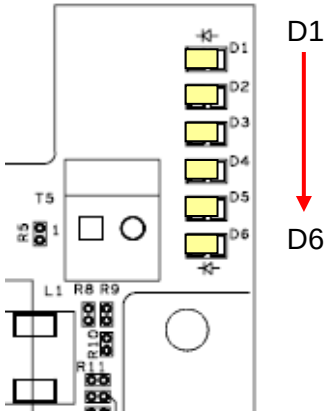


Figure 7-6 PCI Diode Location

8.0 Build Options

Red Rapids typically stocks the board configurations listed in Table 8-1 and standard on-board synthesizer frequencies shown in Table 8-2.

Table 8-1 Model 314 Standard Board Configurations

FPGA	Coupling	SRAM	J5 Coax Connector	USER DCI/ IO	USER IO Voltage
XC4VSX35-11	AC	No SRAM	CLK	DCI	2.5V
XC4VLX60-11	AC	No SRAM	CLK	DCI	2.5V

Table 8-2 Model 314 Standard Synthesizer Frequencies

Standard Synthesizer Frequencies (MHz)
56, 93, 125

The Model 314 can be ordered with different build options as listed in Table 8-3. Build options may be ordered independent of one another.

Table 8-3 Model 314 Build Options

Item	Optons
FPGA	XC4VLX40 XC4VLX60* XC4VSX25 XC4VSX35*
FPGA Speed Grade	-11* -12
Coupling	AC* DC
SRAM	No SRAM* 24 MB SRAM
J5 Coaxial Connector	REF/CLK* Trigger
USER DCI/IO	DCI* (USER 62/64 used for VRP/VRN) USER IO 62/64 Available
User IO Voltage	2.5V* 3.3V
Custom Synthesizer	25 – 125 MHz

Note: * items are default/standard

Non-standard configurations are built to order and subject to being non-cancelable/non-returnable. Delivery lead times are subject to component availability at time of order.

9.0 Technical Support

Please feel free to contact us if you have a technical question about or problem with our product. We understand that our customers have tight deadlines and time is of the essence in development and production cycles. We will make every effort to resolve problems as quickly as possible.

Web: www.redrapids.com/tech-support.htm

Email: support@redrapids.com

Phone: 972-671-9570

Fax: 972-671-9572

Please include the following information with your correspondence:

Contact Information

Product Model

Host Card or System (PC, PCI Carrier, Single Board Computer)

Operating System