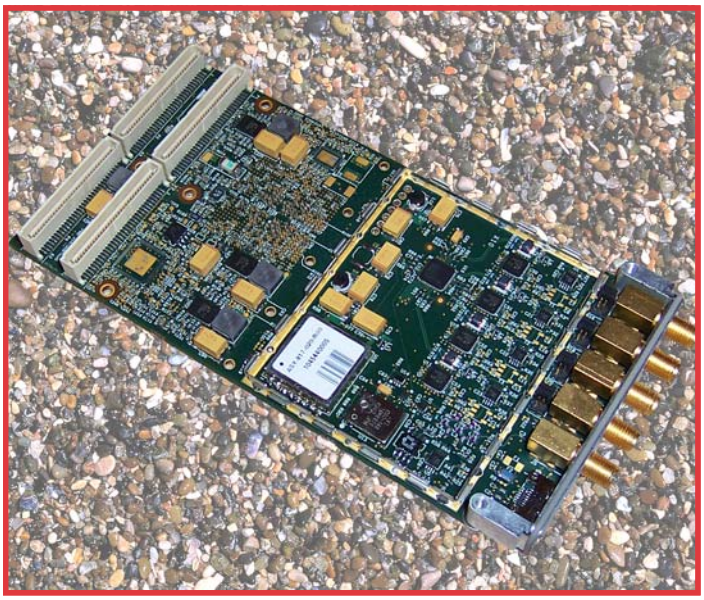
Red Rapids

Channel Adapter 14/125

Model 314



- *Available in PMC/PCI/CPCI form factors*
- *Quad or Dual 14-bit A/D converters*
- *Xilinx Virtex-4 LX or SX FPGA*
- *24 Mbytes of QDR SRAM in three banks*
- *AC or DC Coupled Analog Inputs*
- *32 to 125 MHz sample clock frequency*
- *On-board fixed frequency synthesizer*
- *FPGA core library for data interfaces*
- *PCI bus master with scatter-gather DMA*
- *32/64-bit and 33/66 MHz PCI support*
- *Windows, Linux, VxWorks drivers & API*
- *Reference design with source code*

FPGA Configurable Quad/Dual Channel Receiver

The *Channel Adapter* product family provides the ideal platform to rapidly field application specific I/O functions minus the expense of custom hardware development. The architecture features a high performance interface tightly coupled to a Xilinx Virtex-4 FPGA. The FPGA communicates with the host processor through a dedicated PCI bridge, leaving the majority of logic uncommitted. Simple interfaces to the I/O and local bus are easily integrated with user configuration code.

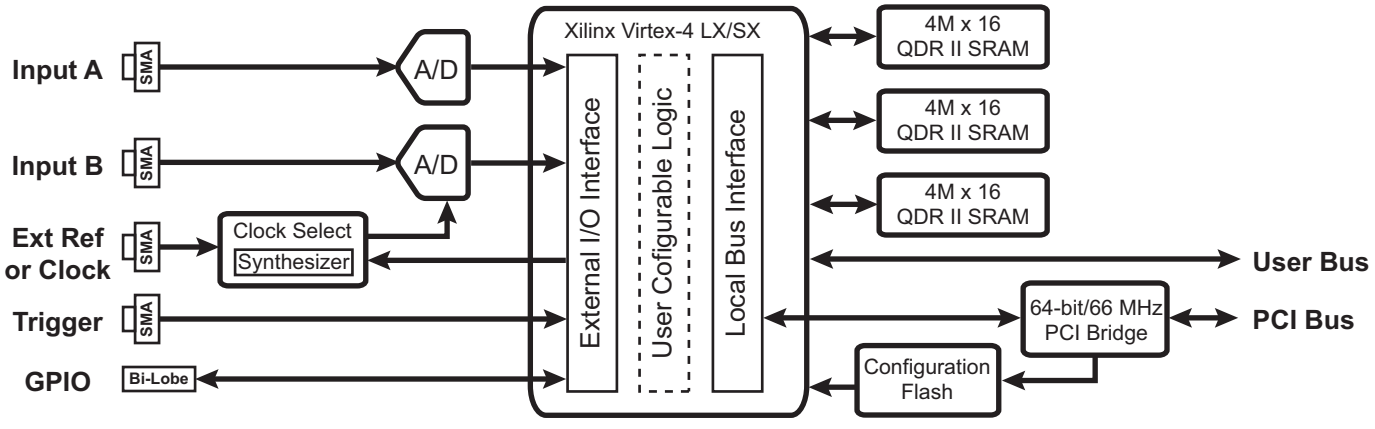
The *Channel Adapter 14/125* quad or dual channel receiver is based on the Linear Technology LTC2255 14-bit A/D converter. The sample clock is supplied by an on-board frequency synthesizer or an external source. The frequency synthesizer is phase locked to a local 10 MHz TCXO or an external reference can be used to achieve system-wide phase coherence.

The analog inputs can be either AC or DC coupled to the A/D converters. The AC coupled configuration supports direct IF sampling (bandpass sampling) beyond the first Nyquist zone.

The FPGA can be selected from the Virtex-4 high performance logic (LX) or signal processing (SX) platforms. A variety of size and speed grade options are offered to further optimize the price/performance ratio over a wide range of applications.

The FPGA is connected to three optional 16-bit QDR SRAMs for high speed local data storage. The QDR SRAM provides separate read and write ports to maximize data transfer into and out of memory. This memory can also be used as a high-speed snapshot recorder to store segments of data without interruption from PCI bus traffic.

The external interfaces include a header connected to the FPGA for general purpose I/O signals. These can be used to provide triggers to/from external equipment, timing strobes, or synchronization signals. A low-speed A/D converter is available to digitize an analog telemetry input, such as an IRIG timing waveform.



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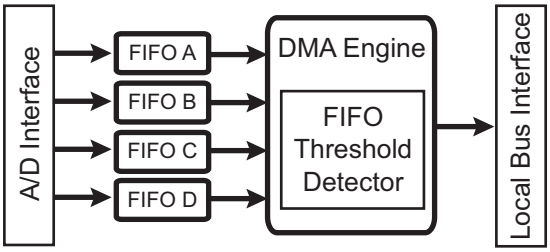
A DMA FPGA core is provided to manage data transfers between the *Channel Adapter* and host memory. The DMA engine allows the receiver to automatically initiate a PCI burst transaction when data is available. An interrupt is generated by the *Channel Adapter* when the specified number of data blocks have been written.

There are also more sophisticated DMA features built into the core. DMA chaining and scatter-gather techniques are supported by both the hardware and software to optimize data transfer efficiency.

The *Channel Adapter* product is distributed with VHDL and C source code to a reference design that exercises the DMA function of the local bus interface. This combined hardware and software example can be used as a template for other applications.

The Virtex-4 FPGA is supported by a robust set of development tools from Xilinx. Creation of user configuration code follows the standard design flow using a pin assignment file supplied with the *Channel Adapter*. Cores are provided for the ADC, SRAM, and local bus interface. Both the FPGA and the configuration PROM can be programmed directly over the PCI bus. The PROM can also be loaded through an optional JTAG connector using the Xilinx iMPACT software.

The *Channel Adapter* product ships with diagnostic firmware preloaded in the PROM to quickly verify hardware and software integrity when it is installed on the host computer. The diagnostic software performs a snapshot signal capture on all receiver channels simultaneously. The data from each channel is stored in a separate disk file for analysis. A verification utility is also provided to analyze the data and report the characteristics of the signal that was captured.



FPGA Diagnostic Function (Quad Channel Signal Acqusition)

Typical Applications

- *Multi-channel data acquisition*
- *Multi-channel software defined radio receiver*
- *Signal intelligence (SIGINT) collection*
- *Receiver algorithm prototyping*
- *Beamforming / TDOA*
- *Signal recorder*

Receiver Performance

Measured characteristics*:
- 3 dB passband (AC): 0.1 to 250 MHz
- 3 dB passband (DC): DC to 200 MHz
- SNR (AC): 70 dB
- SNR (DC): 66 dB
- SFDR (AC): 85 dB
- SFDR (DC): 85 dB
- Channel isolation: 90 dB (typical)

Phase noise: -100 dBc/Hz (10 kHz offset)

Internal reference: 10 MHz +/- 1.5 ppm

**Consult the Hardware Reference Manual for details.*

Hardware

Form factor: PMC, PCI, or CPCI

PCI bus: Universal, 32/64-bit, 33/66 MHz

GPIO: 6-bit LVTTL or LVDS

Telemetry ADC: 12-bit, 100 kSPS

External reference or sample clock option

External trigger input (50 ohms)

User bus: 64-bit LVTTL or LVDS

Power dissipation: 10 to 22 Watts

Airflow: 250 LFM at 35 degrees C

Software

Fedora Linux kernel 2.4 or 2.6

Windows 2000, XP, or Server

VxWorks 6.5 (CHAMP IV default target)

Build Options

Virtex-4 FPGA:

LX40-11, LX40-12, LX60-11, LX60-12

SX25-11, SX25-12, SX35-11, SX35-12

Synthesizer frequency:

125 MHz (Maximum ADC specification)

93.33 MHz (70 MHz IF sampling)

112 MHz (140 MHz IF sampling)

Depopulate SRAM for cost/power savings

Red Rapids

797 North Grove Rd, Suite 101

Richardson, TX 75081

Phone: 972-671-9570

Fax: 972-671-9572

www.redrapids.com