1. INTRODUCTION

This document describes the operation of the XPOL Controller (ALP) board (075005-0003).

2. REFERENCE DOCUMENTATION

SCHEMATIC, XPOL BOARD 075005-0001

3. FUNCTIONAL DESCRIPTION

3.1. **Basic Operation**

The major function blocks of the ALP board are an Ethernet interface, an FPGA which controls timing and radar system interface, Flash memory for storing FPGA configuration file, and an analog interface to measure four RTDs, a resistive fuel-level sensor and two input voltages. The host computer communicates with the SRA controller through the Ethernet connection. Aside from normal communication, the Ethernet interface may also be used to reprogram the FPGA configuration file stored in the on-board Flash memory.

3.2. **Communications**

The ALP board communicates with the remote host through a 10/100 BaseT Ethernet LAN port. The IP address of the board is set to: 192.168.85.192 port 10001. All successfully received normal operating commands will cause the ALP to transmit an ACK (06) character to the host.

3.3. **Input Clock**

The ALP board requires an external 80MHz clock on J10 in the range of -10 dBm to +14 dBm (200mV p-p to 3.3 V p-p).

4. OPERATION

The messages transmitted to the ALP board may be divided into two types: *Operational Messages* and *Configuration Messages*. Operational Messages control the normal operation of the board, such as setting timing parameters and reading analog inputs. Configuration Messages generally interface with the configuration Flash memory, which contains the configuration file that programs the main FPGA and establishes the functions of the board. Refer to the Appendix for details of each message.

4.1. **Configuration Messages**

4.1.1. **Flash Erase**

This command will erase the on-board Flash memory. The Flash memory MUST be erased prior to downloading a new configuration file or Configuration Status Block. An ACK (06) will be transmitted to

the host upon successful completion of the erase cycle, which usually takes about five seconds.

4.1.2. **Force Configuration**
This command forces the configuration file stored in the Flash to be uploaded to the FPGA. On power-up this automatically occurs, but if a new configuration file is downloaded to the Flash this command may be executed rather than cycling power to reconfigure the device.

4.1.3. **Download Configuration File**
This command will download 145902 bytes to the Flash memory. The download must be performed in 256 byte blocks(except for the last block), as the Flash can only be programmed 256 bytes at a time. After a block has been programmed the ALP board will respond with an ACK, signifying that it is ready for the next block. Each block takes approximately 5 milliseconds to program.

4.1.4. **Write Configuration Status**
This command will download a 28 byte status block to the Flash. Since the Flash must be erased prior to writing new data to it, this command should generally be executed at the same time the Download Configuration File command is executed. The data in the block will be the configuration file name, the Revision level and the date.

4.1.5. **Read Configuration Status**
This command will read back the previously programmed Configuration Status Block.

4.1.6. **Reset Board**
Forces a master reset, similar to pushing the reset button on the board.

4.2. **Operational Messages**

4.2.1. **Timing Message** (Refer to Timing Diagrams in Appendix)
Sets timing parameters for output signals. There are twelve parameters that define the ALP output signals.

4.2.1.1. **MODE**
Selects IDLE, Single Pulse Pair (SPP), Dual Pulse Pair (DPP) or FFT mode and enables/disables the AD TRIGGER output.

4.2.1.2. **T1, T2, T3**
Determines the cycle-to-cycle time. In SPP mode only T1 and T2 are used. In DPP mode, all three are used.

4.2.1.3. **P1**
Determines the width of the TX PULSE signal. It is limited to 1.2µ-Sec.

4.2.1.4. **P2**

Determines the delay from the start of the cycle to the start of TX PULSE.

4.2.1.5. **P3**

Determines the delay from the start of the cycle to the start of TX SAMPLE SWITCH active.

4.2.1.6. **P4**

Determines the delay from the end of TX PULSE to the end of TX SAMPLE SWITCH.

4.2.1.7. **NFFT**

Determines the number of cycles per FFT group.

4.2.1.8. **TF1, TF2 TF3**

Determines the cycle-to-cycle time in FFT mode. TF1 is the delay for the odd groups of cycles, TF2 is the delay for even groups, and TF3 is the time between groups.

4.2.2. **Get Analog Input Message**

Requests temperature and voltage values from eight inputs. ALP board will respond with an ACK(06) followed by two dummy bytes and eight two-byte values.

Channel 5 represents the signal from the fuel-level sensor.

Channels 6 and 7 (pins 11,12 and 13,14) of J1 are configured to measure positive voltages between zero and 5.5 volts.

5. INPUT/OUTPUT

(Refer to Board Layout drawing in the Appendix for location of connectors.)

5.1. **Power (J13, J14)**

The ALP board receives three input voltages on J13, +5V, +28V and -15V. The +5V is the main power for the ALP board and is regulated down to +3.3V and +1.8V for powering the logic. The -15V is used only to drive a regulator which produces -5V at up to 200mA that is presented on J14. The +28V is passed through to 4 EMS switch connectors (J6, J8, J9, J11), which are not used at present. All three power inputs have separate returns. It is assumed that the system power supply grounds are tied together at a common point elsewhere in the system.

TABLE 1

Connector	Power connection	Current
J13-1	+5V	<1A
J13-2	+5V return	
J13-3	-15V	<200mA
J13-4	-15V return	
J13-5	+28V	Not used
J13-6	+28V return	
J14-1	-5V out	<200mA
J14-2	-5V return(-15V return)	

5.2. **CLOCK IN(J10)**

This is the master clock for the board. It should be 80 MHz at a nominal 0dBm.

5.3. **AD TRIGGER(J5)**

High current output, 400 nanosecond wide, that occurs at the start of each cycle.

5.4. **Analog inputs(J1)**

The ALP board is configured to accept 100Ω RTDs connected between pins 1,3,5 and 9 and common.

The four RTD values can be converted to temperature according to the following equation:

$$T(\deg C) = \frac{Code - 282}{6.214}$$

where *Code* is the 12-bit value returned in the message.

The input on pin 11 has a 1K-ohm pullup to 5Volts. Using a Sunpro CP7583 resisitive fuel sensor (connected to common) the resistance will vary between 33 ohms (Full) to 240 ohms (Empty). The output codes will be:

FULL	65
½ FULL	235
EMPTY	396

Channels 6 and 7 (pins 11,12 and 13,14) of J1 are configured to measure positive voltages between zero and 5.5 volts. The scaling is:

$$Vin = .00547 \times Code$$

Table 2 summarizes the analog input connector.

TABLE 2

J1 PIN	FUNCTION
1	RTD1
3	RTD2
5	RTD3
7	RTD4
9	Resistive Fuel Sensor
11	Voltage 1(+)
13	Voltage 2(-)
15	Not Used
2,4,6,8,10,12,14,16	Common

5.5. **TX PULSE(J3)**

TX PULSE is presented on pin 1 and its complement on pin 2. Circuitry is included to limit the maximum width of TX PULSE to about 1.2uSEC.

TABLE 3

PIN	FUNCTION
1	TX PULSE+
2	TX PULSE-
3	Common
4	Common

5.6. **TX SAMPLE SWITCH(J4)**

Active-low switch enable signal.

5.7. **EMS SWITCHES(J6, J8, J9, J11)**

These connectors provide the interface to EMS switches, which are not used at present.

5.8. **MOSFET OUTPUT(J2)**

An open-drain MOSFET output is available on pin 1 of J2. It is not used at present.

APPENDIX

Flash Erase Message

Header byte	Command byte
14h	20h

Force Configuration Message

Header byte	Command byte
14h	07h

Download Configuration File Message

Header byte	Command byte	Message Length LSB	Message Length NSB	Message Length MSB	Sub-Command byte	145902 DATA bytes
14h	09h	EEh	39h	02h	02h	

Download Configuration Status Message

Header byte	Command byte	Message Length	20 ASCII Bytes	2 ASCII Bytes	6 ASCII Bytes
14h	24h	1Ch	Filename	REV	MMDDYY

Read Configuration Status Message

Header byte	Command byte
14h	28h

SOFTWARE RESET MESSAGE

Header byte	Command byte
14h	03h

TIMING CONFIGURATION MESSAGE

Header byte	Command byte	Message Length LSB	Message Length NSB	Message Length MSB	Sub-Command byte	29 DATA bytes
14h	21h	1Eh	00h	00h	30h	See Table 2

STATUS REQUEST COMMAND

Header byte	Command byte	Message Length LSB	Message Length NSB	Message Length MSB	Sub-Command byte
14h	21h	01h	00h	00h	37h

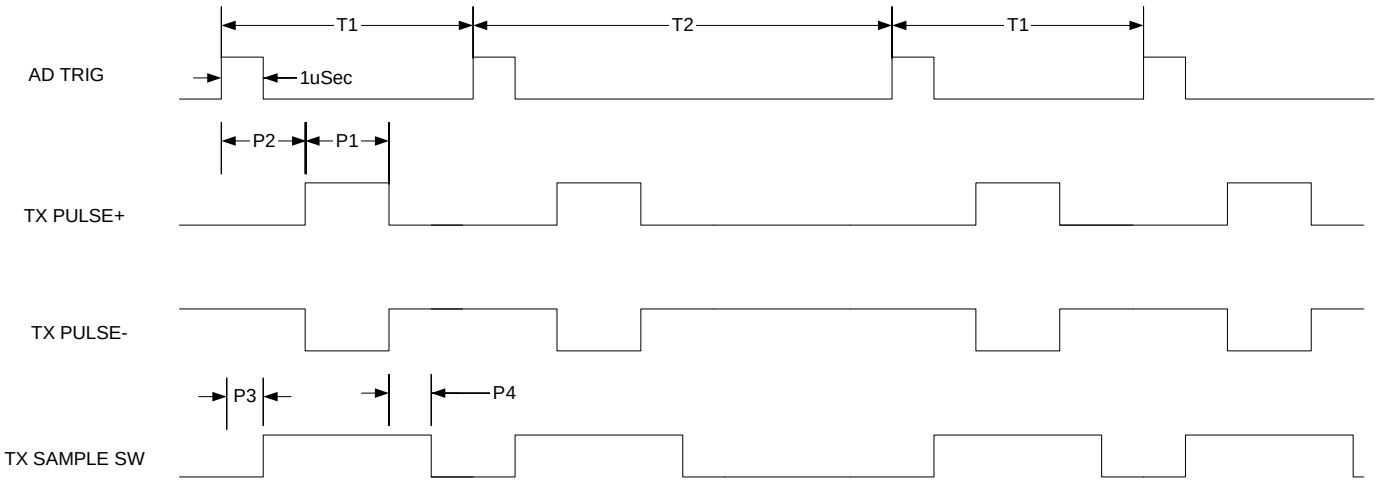
TABLE 4
TIMING PARAMETERS

BYTE #	PARAMETER	FUNCTION	Units	RANGE
0-2	TP1	Cycle-to-cycle delay 1→2	10 n-Sec	0-167 m-Sec
3-5	TP2	Cycle-to-cycle delay 2→1(SPP) or 2→3(DPP)	10 n-Sec	0-167 m-Sec
6-8	TP3	Cycle-to-cycle delay 3→1	10 n-Sec	0-167 m-Sec
9-A	P1	TX PULSE width	10 n-Sec	0-655 µ-Sec
B-C	P2	TX PULSE delay	10 n-Sec	0-655 µ-Sec
D-E	P3	TX SAMP SW on delay	10 n-Sec	0-655 µ-Sec
F-10	P4	TX SAMP SW off delay	10 n-Sec	0-655 µ-Sec
11-13	TF1	Cycle-to-cycle delay-odd group (FFT mode)	10 n-Sec	0-167 m-Sec
14-16	TF2	Cycle-to-cycle delay-even group (FFT mode)	10 n-Sec	0-167 m-Sec
17-19	TF3	FFT delay	10 n-Sec	0-167 m-Sec
1A-1B	NFFT	Number of cycles per FFT		1-65535
1C	MODE	**BITS 0-3:** x0h→IDLE x1→SPP x2→DPP x3→FFT **BIT 4(AD TRIG ENABLE):** 1→ENABLED 0→DISABLED		

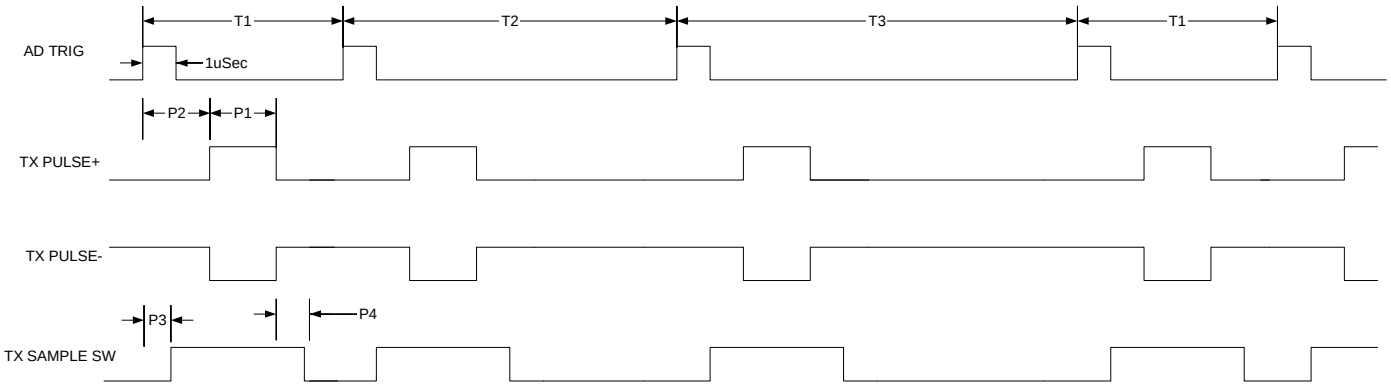
Table 5
STATUS MESSAGE

Bytes 0 & 1	SPARE
Bytes 3&2	RTD 1 (12 bit value)
Bytes 5&4	RTD 2 (12 bit value)
Bytes 7&6	RTD 3 (12 bit value)
Bytes 9&8	RTD 4 (12 bit value)
Bytes 11&10	Fuel-Level Sensor
Bytes 13&12	Voltage 2 (12 bit value)

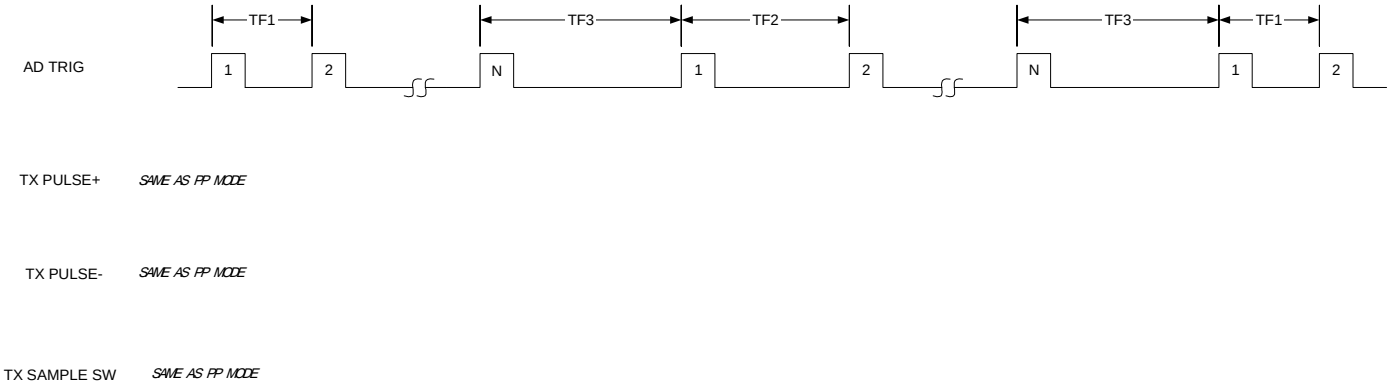
Bytes 15&14	Voltage 3 (12 bit value)
Bytes 17&16	Not used



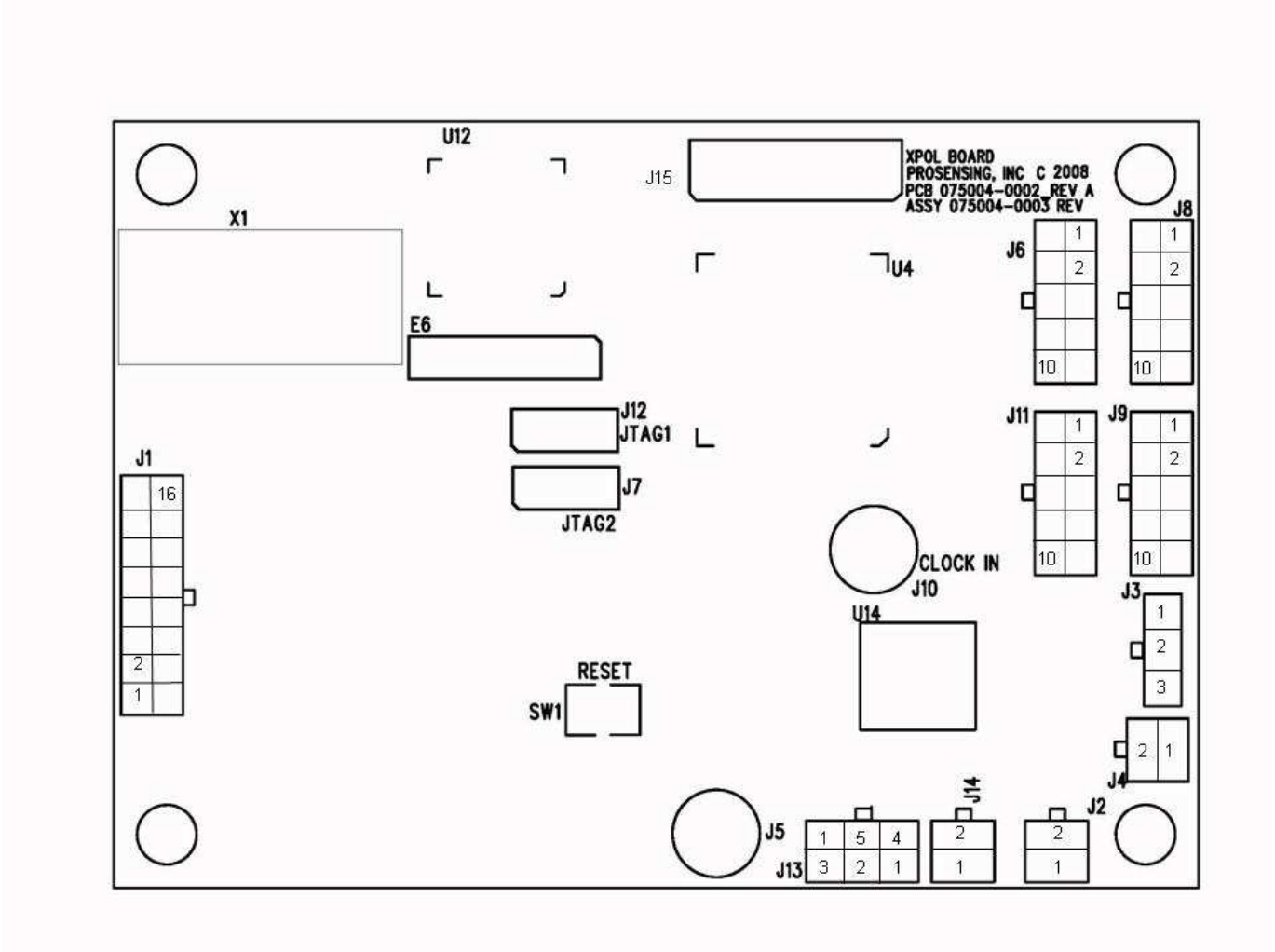
TIMING DIAGRAM
SPP MODE



TIMING DIAGRAM
DPP MODE



TIMING DIAGRAM
FFT MODE



Board Layout