



# ECV4-2-2R130-SL-PMCX

## Two-Channel FPGA Based Digital Receiver

High-Speed A/D Conversion, 16-Bit Resolution

- Processing power from a user-programmable Virtex™-4 SX55, LX100, OR LX160
- Optimized for wideband multi-channel data processing
- 64-Bit PCI-X interface at up to 133MHz
- 16-Bit Analog to Digital (A/D) conversion with 100dB multi-tone SFDR typical



ECV4-2-2R130-SL-PMCX

The ECV4-2-2R130-SL-PMCX module combines high performance A/D conversion with powerful, DSP optimized FPGA resources in a state-of-the-art PMCX card. A large, user programmable FPGA provides resources for the demanding pre-processing algorithms typically found in SIGINT, ELINT, Radar, HEP, and Medical Imaging applications. An I/O control FPGA supports a high bandwidth PCI-X interface capable of streaming two channels of data to and from a host system.

### Data Conversion

The ECV4-2-2R130-SL-PMCX accepts IF frequencies up to 350MHz. Input data conversion is accomplished with two LTC2208 A/D converters, both providing 16-bit conversion at sample rates up to 130 MHz.

### Clock Input

This PMCX card will accept a single clock input between 33 MHz and 130 MHz via a front panel SSMC. The clock directly drives the A/D converters and is made available to the on-board FPGAs for internal timing functions.

### Sync Structure

On-board sync is accomplished via an external sync in or a software defined event. The sync is qualified by the A/D clock and is output on the sync out connector to allow daisy chaining of multiple boards to a sync event. The data collection and transmission resources can be individually controlled directly by the sync event or by counters that are, in turn, controlled by the A/D clock and the sync. An input is also available for 1PPS signaling or time stamping.

### User Programmable FPGA

Customers may choose their user programmable FPGA from several members of the Xilinx Virtex-4 FPGA family including the SX55, LX100, and LX160. This variety of FPGA's allows the user

to run custom algorithms such as digital up/down conversion, Fast Fourier Transforms (FFT), and filtering directly on the board. Data from the A/D's may be passed to the PCI-X interface and the user-defined I/O pins via this FPGA. The Sync-In, A/D Clock, DDR SDRAM, and 2 MB of DDR2 SRAM are also available to this FPGA.

### Memory

Included on this PMCX card are two banks of 128 MB DDR SDRAM, which operate at rates up to 200 MHz. These memory banks may optionally be configured as 256MB each, operating at up to 166MHz. Additional memory capacity is provided by 2 MB of DDR2 SRAM operating at rates up to 250 MHz. The ECV4-2-2R130-SL-PMCX also supports up to 8MB of Flash memory that is used to program both FPGA's.

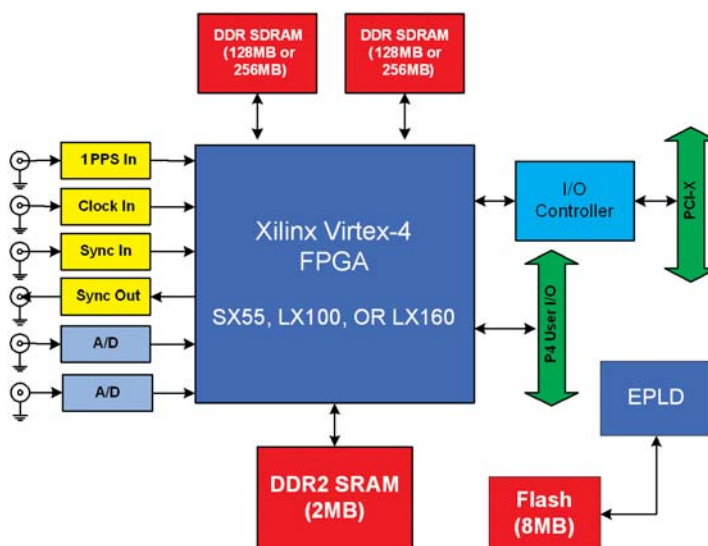


Figure 1. Functional Block Diagram

## PCI-X Interface

An IP core in the Control FPGA provides an industry standard PCI-X interface which is capable of operating at speeds of 133MHz, 100MHz, or 66MHz at 64-bits. If a PCI-X interface is not available, the board may operate at 33MHz at 64-bits PCI.

## FPGA Configuration

IP for the user programmable FPGA can be developed using standard industry programming tools available from multiple sources. An FPGA core image is loaded over the PCI Bus to Flash memory, which has sufficient size to hold multiple images. The FPGA image can be loaded automatically on power up or at any time under user control. Both the FPGA and the Flash memory are capable of being reprogrammed at any time.

## IP Options

Standard IP provided with card includes:

- Two wideband receivers which include I/Q data, a 32-bit NCO, a 5th order CIC filter (D:2 to D:4096 in integer steps), and a decimating FIR filter (D:2 to D:16 in integer steps).
- Simultaneous streaming or counted burst collection from both channels
- A skip counter is provided to delay the start of the collection from the trigger.
- Data output can be either the ADC, an internal test counter, internal test counter through the receiver, or ADC data through the receiver.
- Test engines are provided to exercise all DDR SDRAM and DDR2 SRAM interfaces at speed.
- Auto incrementing DMA engine to minimize software intervention.
- Source files of the IP in the User FPGA are provided.

## Software Support

Mercury provides driver applications for the ECV4-2-2R130-SL-PMC X supported by the following operating systems:

- Red Hat Enterprise Linux® 4
- VxWorks® 5.5

## Available Configurations

Part Number	FPGA	Memory
12-0277/CC086A	SX55	2x128MB
12-0277/CC094	SX55	2x256MB
12-0277/CC095	LX100	2x128MB
12-0277/CC096	LX100	2x256MB
12-0277/CC097	LX160	2x128MB
12-0297/CC098	LX160	2x256MB

## Specifications

### FPGAs

1 User FPGA	Xilinx Virtex-4 SX55, LX100, or LX160.
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1 Control FPGA	Xilinx Virtex-4 LX25
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### Memory

DDR SDRAM	256MB with two banks of 2x32M 16-Bit chips or 512MB with two banks of 2 x 64M x 32-bit chips
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DDR2 SRAM	2MB, 512KB x 36-Bit chip
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Flash	8MB, 1/2 of 8MB x 16-Bit chip
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### Data Paths

DDR2 SRAM to User FPGA	2 GB/s Theoretical Max (up to 250MHz)
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DDR SDRAM to User FPGA	Two Identical Banks, 1.6GB/s per bank Theoretical Max (up to 200MHz)
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User FPGA to Control FPGA	Two 800 MB/s parallel LVDS buses, each configurable in either direction
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User FPGA P4 I/O interface	42 Pins for user-defined I/O
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## Environmental Specifications

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Temperature	
Operating	0°C to 40°C with 300 ft/min appropriate air flow
Storage	-40°C to +85°C

Cooling	Commercial grade, cooled by blown air, for use in lab environments and software development applications
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### Corporate Headquarters

199 Riverneck Road  
Chelmsford, MA 01824-2820 USA  
+1 (978) 967-1401 • +1 (866) 627-6951  
Fax +1 (978) 256-3599  
www.mc.com

### Worldwide Locations

Mercury Computer Systems has R&D, support and sales locations in France, Germany, Japan, the United Kingdom and the United States.

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