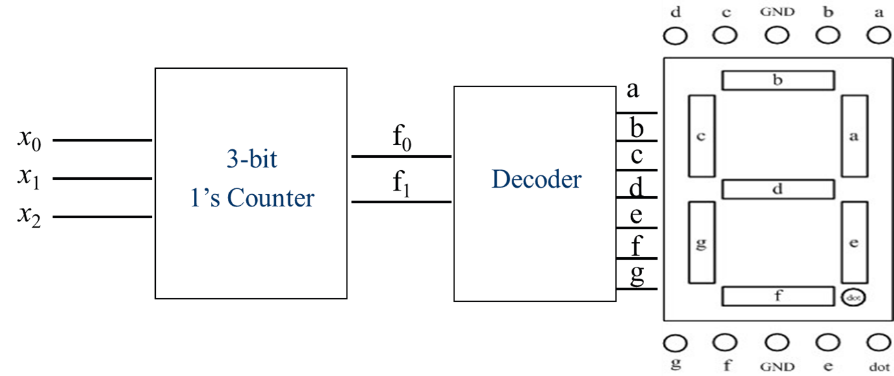
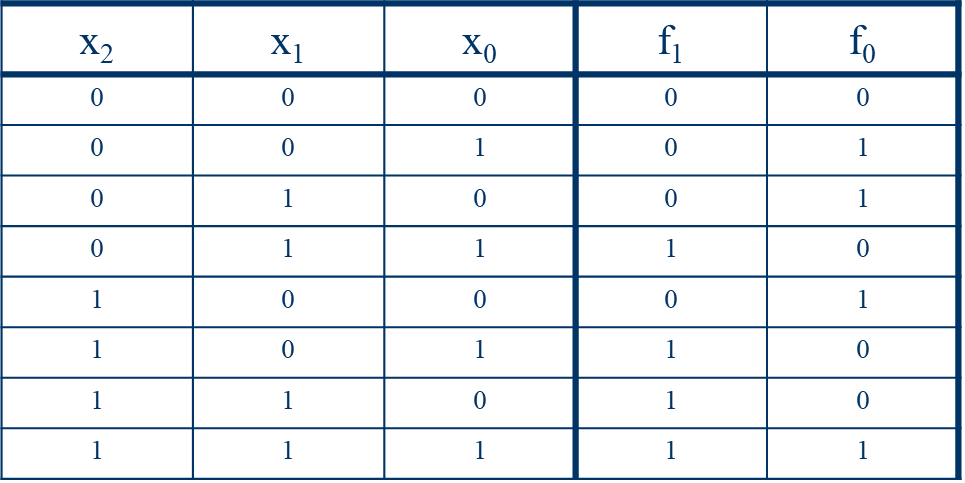
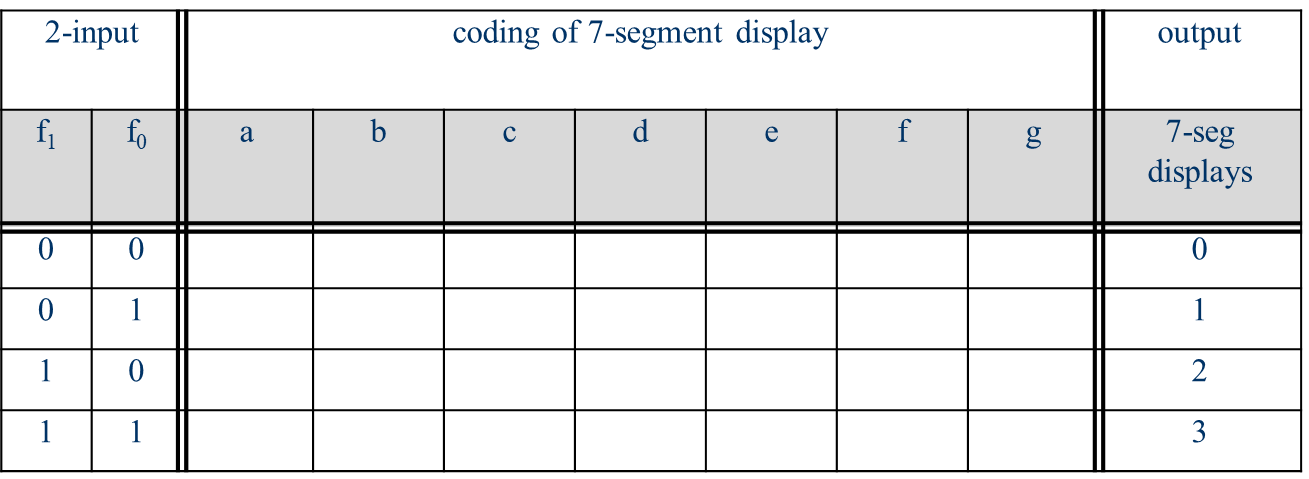
**邏輯設計實驗 - Lab06 2018/04/18 09:10~12:00**

Lab06實習內容：

1. 3-bit 1’s Counter
2. 將3-bit 1’s Counter輸出結果用7-segment display表示

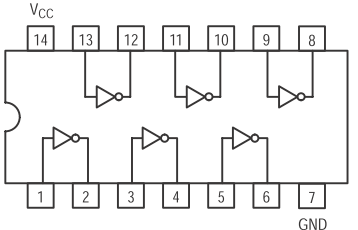
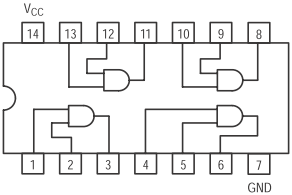
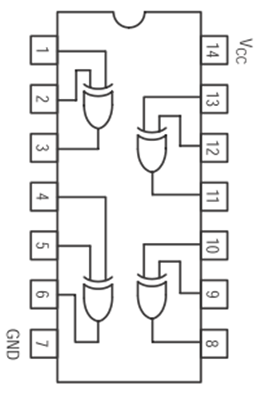
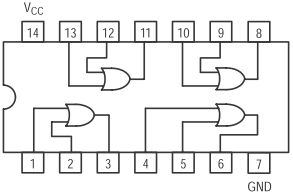






◎TTL IC Connection diagram：

NOT (7404) AND2 (7408) XOR(7486) OR2 (7432)

組別:\_\_\_\_\_\_\_\_\_\_\_

組員:\_\_\_\_\_\_\_\_\_\_\_ 學號:\_\_\_\_\_\_\_\_\_\_\_ 分數:\_\_\_\_\_\_\_\_\_\_\_

組員:\_\_\_\_\_\_\_\_\_\_\_ 學號:\_\_\_\_\_\_\_\_\_\_\_ 分數:\_\_\_\_\_\_\_\_\_\_\_