**邏輯設計實驗–Lab12 2018/06/06 09:10~12:00**

lab12實習內容：

一、實作Mod 6 conuter，透過BCD to 7-seg(7448)顯示在7-Segment Display上

( Input：En為SW0、**Clock**為Pulse generator)

說明：

(1) 當En = 0時: 計數器停止計時並停留在目前數字。

(2) 當En = 1時: 計數器從目前的數字繼續計數。

* **D-FF中的Preset跟Clear都要”接訊號”**

Design circuit diagram：Mod 6 counter (with synchronous reset)

Mod 6 Counter

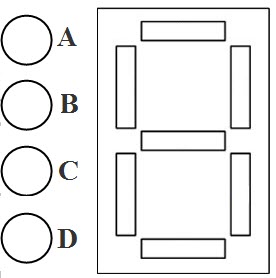
Enable

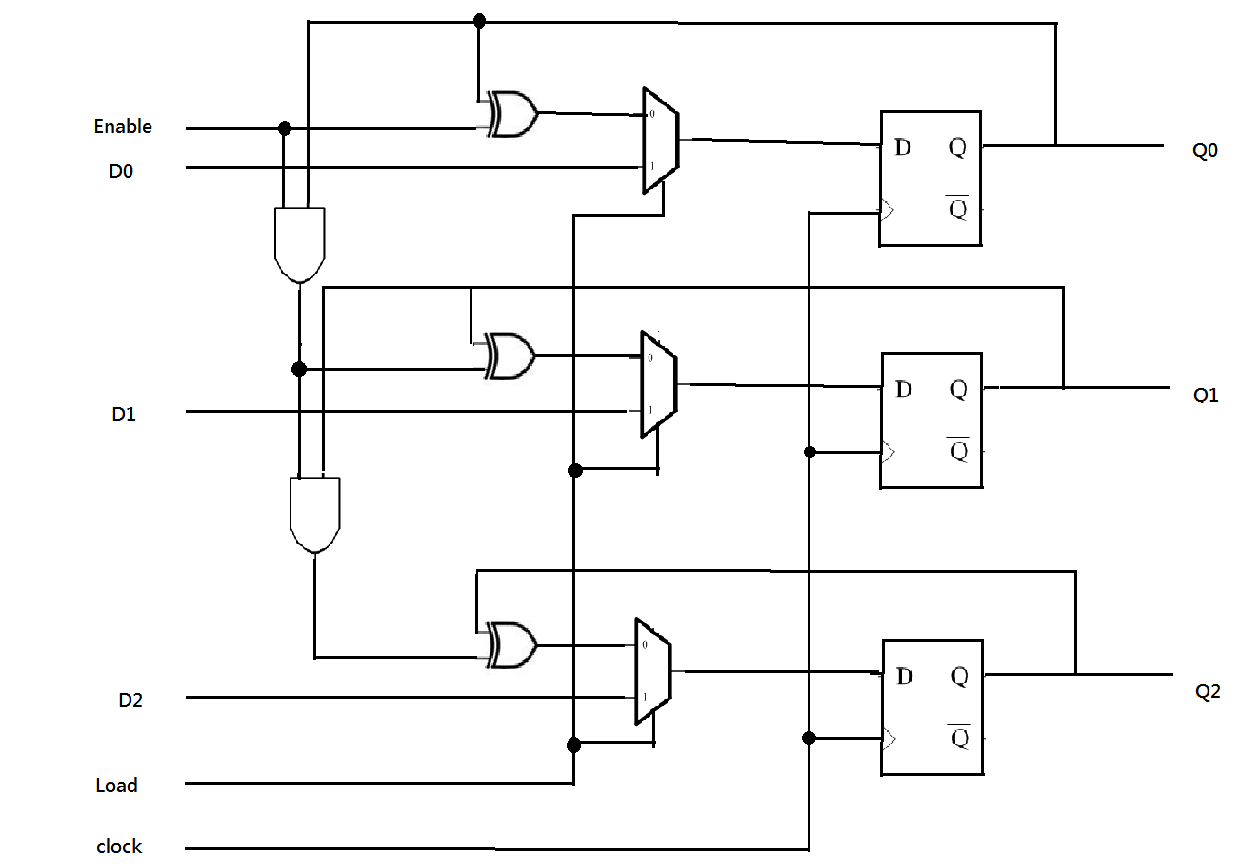
Q0

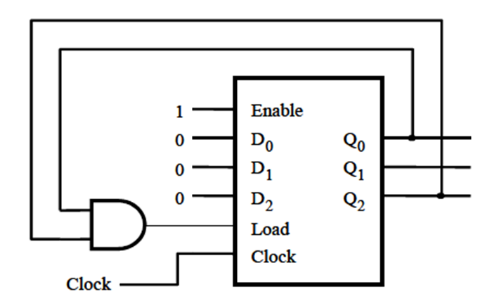
Q1

Q2

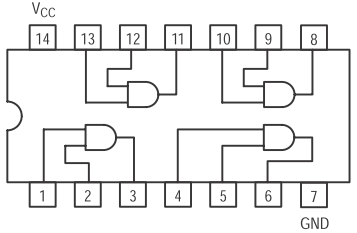
Clock

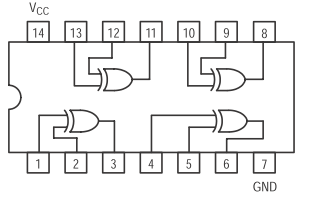




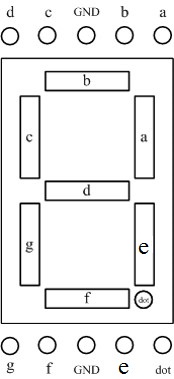
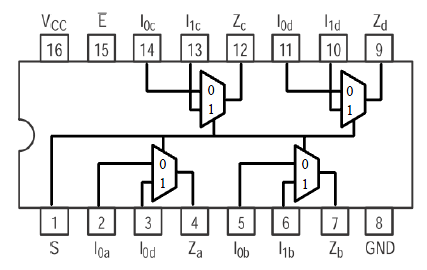


◎TTL IC Connection diagram：

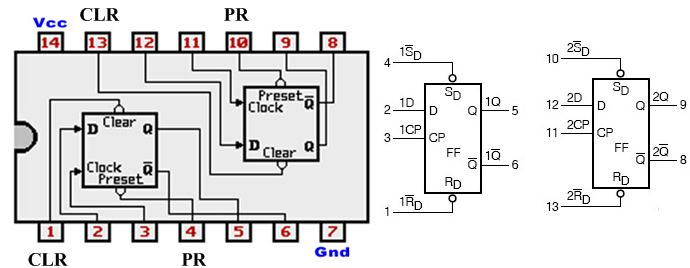
 AND2(7408) XOR2 gate (7486)



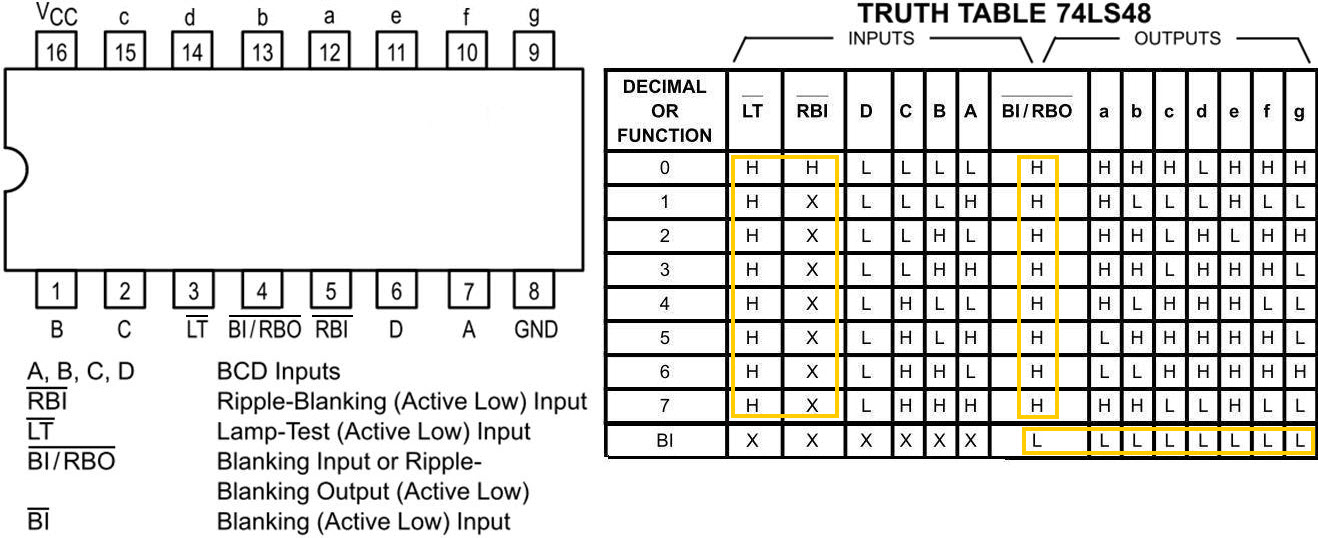
2-1 MUX (74157) 7-segment display

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D-FF(7474)



BCD to 7-seg decoders/drivers (7448)



組別:\_\_\_\_\_\_\_\_\_\_\_

組員:\_\_\_\_\_\_\_\_\_\_\_ 學號:\_\_\_\_\_\_\_\_\_\_\_ 分數:\_\_\_\_\_\_\_\_\_\_\_

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