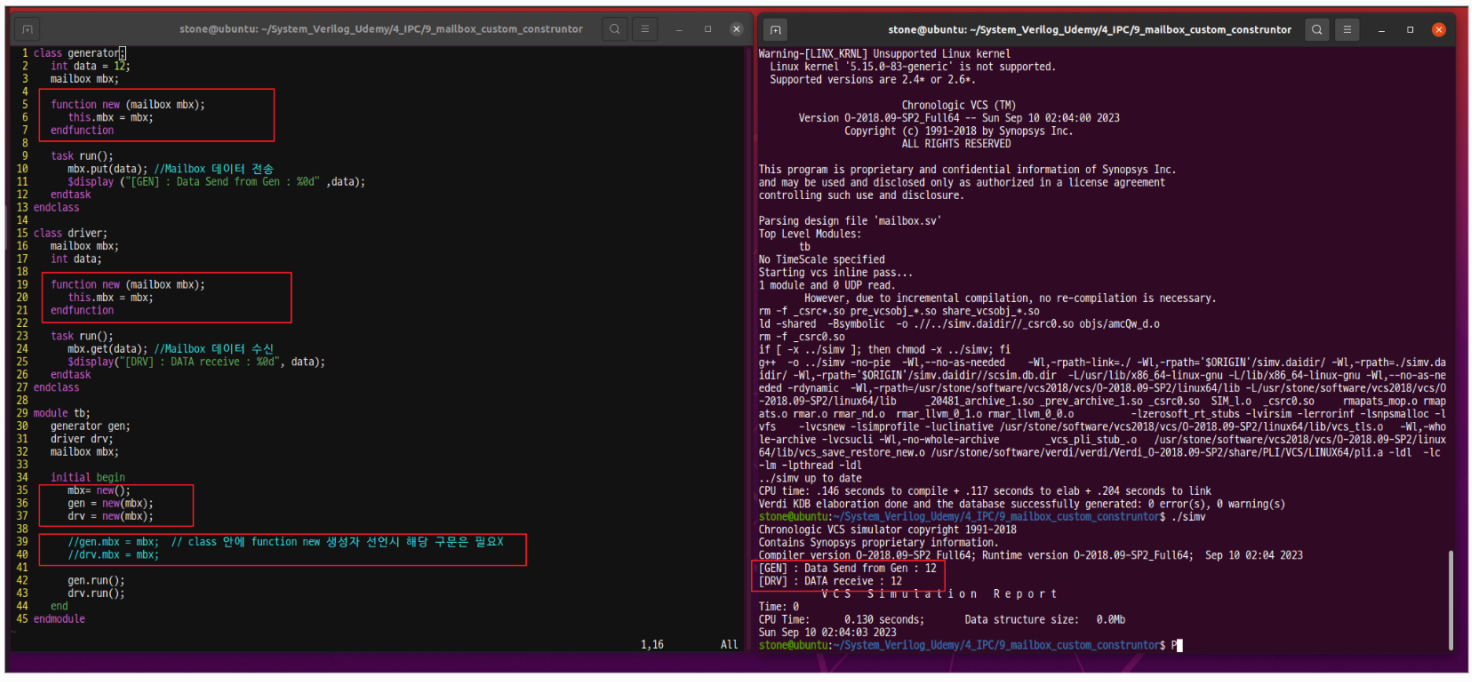
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/9_mailbox_custom_construntor
class generator;
int data = 12;
mailbox mbx;
function new (mailbox mbx);
this.mbx = mbx;
endfunction
task run();
mbx.put(data); //Mailbox 데이터 전송
$display ("[GEN] : Data Send from Gen : %0d" ,data);
endtask
endclass
class driver;
mailbox mbx;
int data;
function new (mailbox mbx);
this.mbx = mbx;
endfunction
task run();
mbx.get(data); //Mailbox 데이터 수신
$display("[DRV] : DATA receive : %0d", data);
endtask
endclass
module tb;
generator gen;
driver drv;
mailbox mbx;
initial begin
mbx= new();
gen = new(mbx);
drv = new(mbx);
//gen.mbx = mbx; // class 안에 function new 생성자 선언시 해당 구문은 필요X
//drv.mbx = mbx;
gen.run();
drv.run();
end
endmodule
1,16 All
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/9_mailbox_custom_construntor
Warning-[LINX_KRNL] Unsupported Linux kernel
Linux kernel '5.15.0-83-generic' is not supported.
Supported versions are 2.4* or 2.6*.
Chronologic VCS (TM)
Version O-2018.09-SP2_Full64 -- Sun Sep 10 02:04:00 2023
Copyright (c) 1991-2018 by Synopsys Inc.
ALL RIGHTS RESERVED
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Parsing design file 'mailbox.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
However, due to incremental compilation, no re-compilation is necessary.
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _20481_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .146 seconds to compile + .117 seconds to elab + .204 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/9_mailbox_custom_construntor$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 10 02:04 2023
[GEN] : Data Send from Gen : 12
[DRV] : DATA receive : 12
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Sun Sep 10 02:04:03 2023
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/9_mailbox_custom_construntor$ P