stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor

File Edit View Search Terminal Help

```
1 class first;
2    int data1;
3    bit [7:0] data2;
4    shortint data3;
5
6    function new(input int data1 = 0, input bit[7:0] data2 = 8'h00, input shortint data3 =0);
7       this.data1 = data1; //this 클래스 내부 Function new 안에 사용되고 클래스안의 객체 자체를 가리키는 포인터
8       this.data2 = data2;
9       this.data3 = data3;
10   endfunction
11 endclass
12
13 module tb;
14   first f1;
15
16   initial begin
17      f1 = new(32);
18      $display ("Data : %0d",f1.data);
19   end
20 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor

File Edit View Search Terminal Help

```
1 class first;
2    int data1;
3    bit [7:0] data2;
4    shortint data3;
5
6    function new(input int data1 = 0, input bit[7:0] data2 = 8'h00, input shortint data3 =0);
7       this.data1 = data1; //this 클래스 내부 Function new 안에 사용되고 클래스안의 객체 자체를 가리키는 포인터
8       this.data2 = data2;
9       this.data3 = data3;
10   endfunction
11 endclass
12
13 module tb;
14   first f1;
15
16   initial begin
17      f1 = new(23,4,35);
18      $display ("Data1 : %0d, Data2 :%0d, Data3:%0d",f1.data1, f1.data2, f1.data3);
19   end
20 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/7_Mu...

```
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'using_define.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN
'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.d
ir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic
 -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/so
ftware/vcs2018/vcs/O-2018.09-SP2/linux64/lib   objs/amcQw_d.o    _44752_archive_1.so
SIM_l.o       rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0
.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -l
simprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs
_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o
 /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /us
r/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -l
c -lm -lpthread -ldl
../simv up to date
CPU time: .139 seconds to compile + .114 seconds to elab + .191 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 war
ning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 23
04:14 2023
Data1 : 23, Data2 :4, Data3:35
                    V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Wed Aug 23 04:14:55 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor$
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor

File Edit View Search Terminal Help

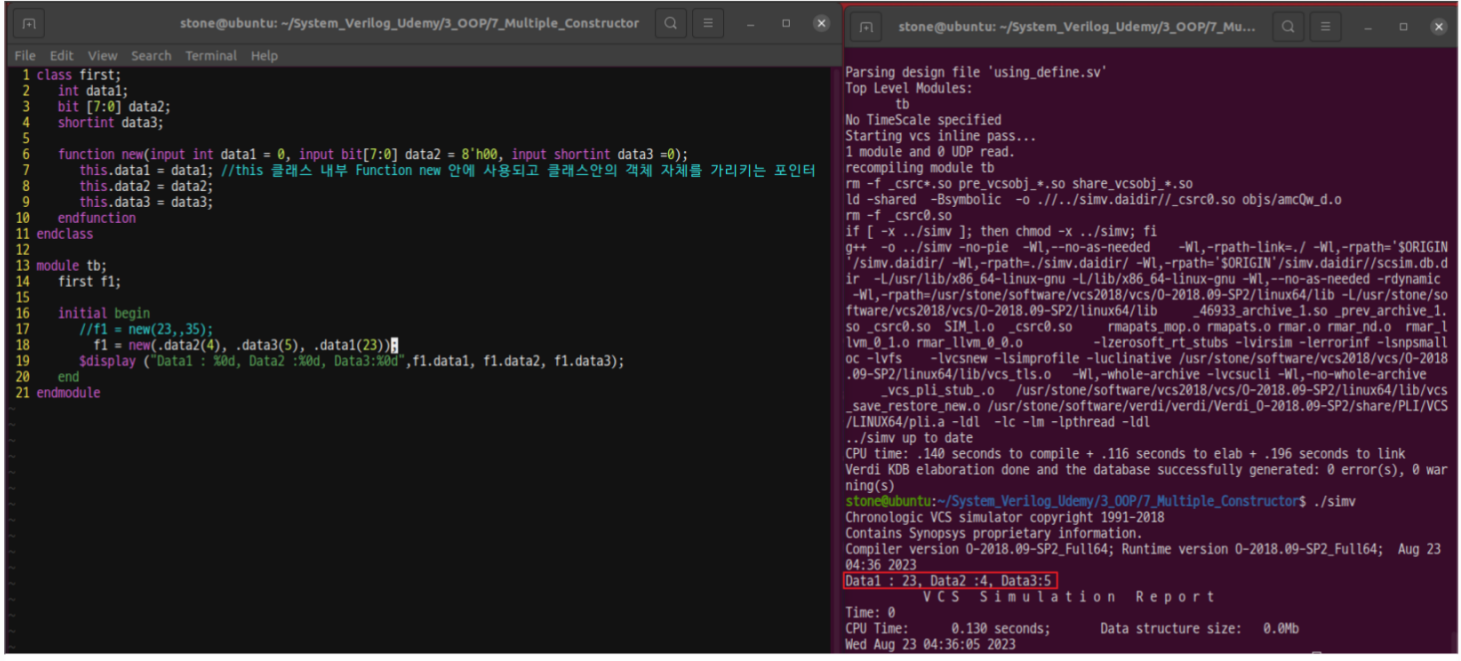
```
1 class first;
2    int data1;
3    bit [7:0] data2;
4    shortint data3;
5
6    function new(input int data1 = 0, input bit[7:0] data2 = 8'h00, input shortint data3 =0);
7       this.data1 = data1; //this 클래스 내부 Function new 안에 사용되고 클래스안의 객체 자체를 가리키는 포인터
8       this.data2 = data2;
9       this.data3 = data3;
10   endfunction
11 endclass
12
13 module tb;
14   first f1;
15
16   initial begin
17      f1 = new(23,,35);
18      $display ("Data1 : %0d, Data2 :%0d, Data3:%0d",f1.data1, f1.data2, f1.data3);
19   end
20 endmodule
```

"using_define.sv" 20L, 509C written 17,15-19 All

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/7_Mu...

```
Parsing design file 'using_define.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN
'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.d
ir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic
 -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/so
ftware/vcs2018/vcs/O-2018.09-SP2/linux64/lib     _45620_archive_1.so _prev_archive_1.
so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_l
lvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmall
oc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018
.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive
     _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs
_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS
/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .139 seconds to compile + .117 seconds to elab + .195 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 war
ning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 23
04:18 2023
Data1 : 23, Data2 :0, Data3:35
                    V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.140 seconds;       Data structure size:   0.0Mb
Wed Aug 23 04:18:16 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/7_Multiple_Constructor$
```

생성자 인자에 값을 넣지 않을시 초기값인 **0**으로 반환



이전 방법은 객체순서대로 값을 넣었지만 이방법은 객체를 직접 선택하여 값을 지정