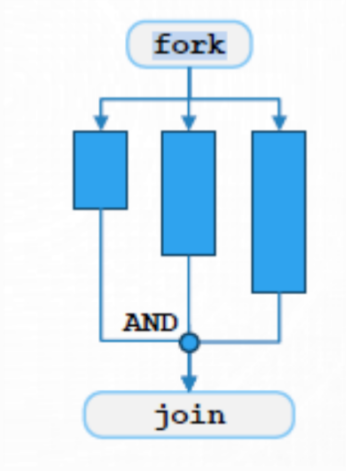
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/4_Multiple_Process...

```
module tb;
   int i= 0;
   bit [7:0] data1, data2;
   event done;
   event next;

   task generator();
      for (i=0; i<10; i++) begin
         data1 = $urandom();
         $display("Data Sent : %0d", data1);
         #10;

         wait(next.triggered);
      end
      ->done;
   endtask

   task receiver();
      forever begin
         #10;
         data2 = data1;
         $display("Data Receive :%0d",data2);
         ->next;
      end
   endtask

   task wait_event();
      wait(done.triggered);
      $display("Completed Sending all Stimulus");
      $finish();
   endtask

   initial begin
      fork //fork Join 은 모든 Thread 가 완료되어야 다음 구문으로 진행
            generator();
            receiver();
            wait_event();
      join
   end
endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/4_Multiple_Process_for...

```
file -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-a
rchive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2
018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/sh
are/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .523 seconds to compile + .255 seconds to elab + .241 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/4_Multiple_Process_fork_join$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  6 23:43 2023
Data Sent : 185
Data Receive :185
Data Sent : 108
Data Receive :108
Data Sent : 167
Data Receive :167
Data Sent : 163
Data Receive :163
Data Sent : 156
Data Receive :156
Data Sent : 52
Data Receive :52
Data Sent : 57
Data Receive :57
Data Sent : 131
Data Receive :131
Data Sent : 20
Data Receive :20
Data Sent : 246
Data Receive :246
Completed Sending all Stimulus
$finish called from file "fork_join_1.sv", line 30.
$finish at simulation time                  100
                 V C S   S i m u l a t i o n   R e p o r t
Time: 100
CPU Time:      0.340 seconds;       Data structure size:   0.0Mb
Wed Sep  6 23:43:11 2023
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/4_Multiple_Process_fork_join$
```



stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/4_Multiple_Process...

```
module tb;
   task first();
      $display ("Task 1 start at %0d",$time);
      #20;
      $display ("Task 1 completed at %0d",$time);
   endtask

   task second();
      $display("Task 2 Started at %0t",$time);
      #30;
     $display("Task 2 Completed at %0t",$time);
    endtask

    task third();
      $display("Reached next to Join at %0t",$time);
    endtask

   initial begin

   fork
      first();
      second();
   join

      third(); //fork join 구문 완료후 실행

   end
endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/4_Multiple_Process_for...

```
Parsing design file 'fork_join_2.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/
-Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gn
u -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O
-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib     _18702_arch
ive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd
.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -l
vfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/
vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/
software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verd
i/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .148 seconds to compile + .117 seconds to elab + .203 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/4_Multiple_Process_fork_join$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  7 02:58 2023
Task 1 start at 0
Task 2 Started at 0
Task 1 completed at 20
Task 2 Completed at 30
Reached next to Join at 30
                 V C S   S i m u l a t i o n   R e p o r t
Time: 30
```