stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/16_Polymorphism

```
class first;  ///부모 클래스

  int data = 12;

  function void display();
     $display("FIRST : Value of data : %0d", data);
  endfunction



endclass

class second extends first; //자식 클래스

  int temp = 34;

  function void add();
    $display("secomd:Value after process : %0d", temp+4);
  endfunction


  function void display();
    $display("SECOND : Value of data : %0d", data);
  endfunction



endclass

module tb;

  first f;
  second s;


  initial begin
    f = new();
    s = new();

    f = s;
    f.display();

  end


```

자식 객체을 부모 객체에 할당
그러나 여전히 부모 객체의 함수가 출력

14,44-40 Top

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/16_Polymorphism

```
CPU Time:      0.140 seconds;       Data structure size:   0.0Mb
Sun Aug 27 05:54:55 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/15_Class_Extend$ vcs -l vcs.log -sverilog -kdb -debug_access+all
class_extend.sv  csrc/            simv            simv.daidir/    ucli.key        vcs.log
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/15_Class_Extend$ cd ..
stone@ubuntu:~/System_Verilog_Udemy/3_OOP$ cd 16_Polymorphism/
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/16_Polymorphism$ vcs -l vcs.log -sverilog -kdb -debug_access+all Polymorphism.sv

Warning-[LINX_KRNL] Unsupported Linux kernel
  Linux kernel '5.15.0-79-generic' is not supported.
  Supported versions are 2.4+ or 2.6+.

                         Chronologic VCS (TM)
       Version O-2018.09-SP2_Full64 -- Sun Aug 27 06:15:12 2023
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Parsing design file 'Polymorphism.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$
ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/
software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib   objs/amcQw_d.o    18921_archiv
e_1.so  SIM_l.o       rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerr
orinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-w
hole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_r
estore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .143 seconds to compile + .117 seconds to elab + .196 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/16_Polymorphism$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 27 06:15 2023
FIRST : Value of data : 12
          V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Sun Aug 27 06:15:16 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/16_Polymorphism$
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/16_Polymorphism

```
class first;  ///부모 클래스

  int data = 12;

  virtual function void display();
     $display("FIRST : Value of data : %0d", data);
  endfunction



endclass

class second extends first; //자식 클래스

  int temp = 34;

  function void add();
    $display("secomd:Value after process : %0d", temp+4);
  endfunction


  function void display();
    $display("SECOND : Value of data : %0d", data);
  endfunction



endclass

module tb;

  first f;
  second s;


  initial begin
    f = new();
    s = new();

    f = s;
    f.display();

  end


```

부모 클래스 함수에 Virual 이라고 선언하면
자식 클래스의 함수가 호출된다

1 change; before #39 4 seconds ago 5,10 Top

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/16_Polymorphism

```
          V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Sun Aug 27 06:15:16 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/16_Polymorphism$ vcs -l vcs.log -sverilog -kdb -debug_access+all Polymorphism.sv

Warning-[LINX_KRNL] Unsupported Linux kernel
  Linux kernel '5.15.0-79-generic' is not supported.
  Supported versions are 2.4+ or 2.6+.

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Parsing design file 'Polymorphism.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$
ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/
software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib    _20046_archive_1.so _csrc0.s
o  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -
lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -W
l,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_sa
ve_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .173 seconds to compile + .122 seconds to elab + .206 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/16_Polymorphism$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 27 06:29 2023
SECOND : Value of data : 12
          V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Sun Aug 27 06:29:30 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/16_Polymorphism$
```