1. := 같은 가중치 값을 가짐

dist { 0 := 10, [1:3] := 60 }

⇓

{ 0 : 10 , 1 : = 60, 2 : = 60, 3 : = 60 }

⇓

$P(0) = \frac{10}{190}$, $P(1) = P(2) = P(3) = \frac{60}{190}$

2. :/ 가중치 값을 항목 갯수로 나누고 각각 같은 값을 가짐

dist { 0 :/ 10 , [1:3] :/ 60 }

⇓

{ 0 : /10 , 1 : /20 , 2 : /20, 3 : /20 }

$P(0) = \frac{10}{70}$, $P(1) = P(2) = P(3) = \frac{20}{70}$

stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/7_Weighte...

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```
1 class first;
2    rand bit [1:0] var1;
3    rand bit [1:0] var2;
4
5    constraint data {
6       var1 dist {0 := 30, [1:3] := 90 }; // 0= 30/300, 1,2,3= 90/300 ->같은 가중치 값을 가짐
7       var2 dist {0 :/ 30, [1:3] :/ 90 }; // 0,1,2,3 = 30/120 -> [1:3] 의 경우는 각각 1개당 30의
  가중치 값을 가짐
8    };
9
10 endclass
11
12 module tb;
13    first f;
14
15    initial begin
16       f = new();
17
18       for (int i=0; i<15; i++) begin
19          f.randomize();
20          $display ("Value var1(:=) : %0d and var2(:/) : %0d",f.var1 , f.var2);
21       end
22    end
23 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/7_Weig...

```
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib    _20222_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive       _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .155 seconds to compile + .117 seconds to elab + .197 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/7_Weighted_distribute$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  4 04:07 2023
Value var1(:=) : 1 and var2(:/) : 3
Value var1(:=) : 0 and var2(:/) : 1
Value var1(:=) : 2 and var2(:/) : 0
Value var1(:=) : 3 and var2(:/) : 2
Value var1(:=) : 1 and var2(:/) : 2
Value var1(:=) : 1 and var2(:/) : 2
Value var1(:=) : 3 and var2(:/) : 2
Value var1(:=) : 0 and var2(:/) : 1
Value var1(:=) : 2 and var2(:/) : 3
Value var1(:=) : 1 and var2(:/) : 0
Value var1(:=) : 1 and var2(:/) : 1
Value var1(:=) : 0 and var2(:/) : 1
Value var1(:=) : 1 and var2(:/) : 3
Value var1(:=) : 1 and var2(:/) : 0
Value var1(:=) : 3 and var2(:/) : 1
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
```