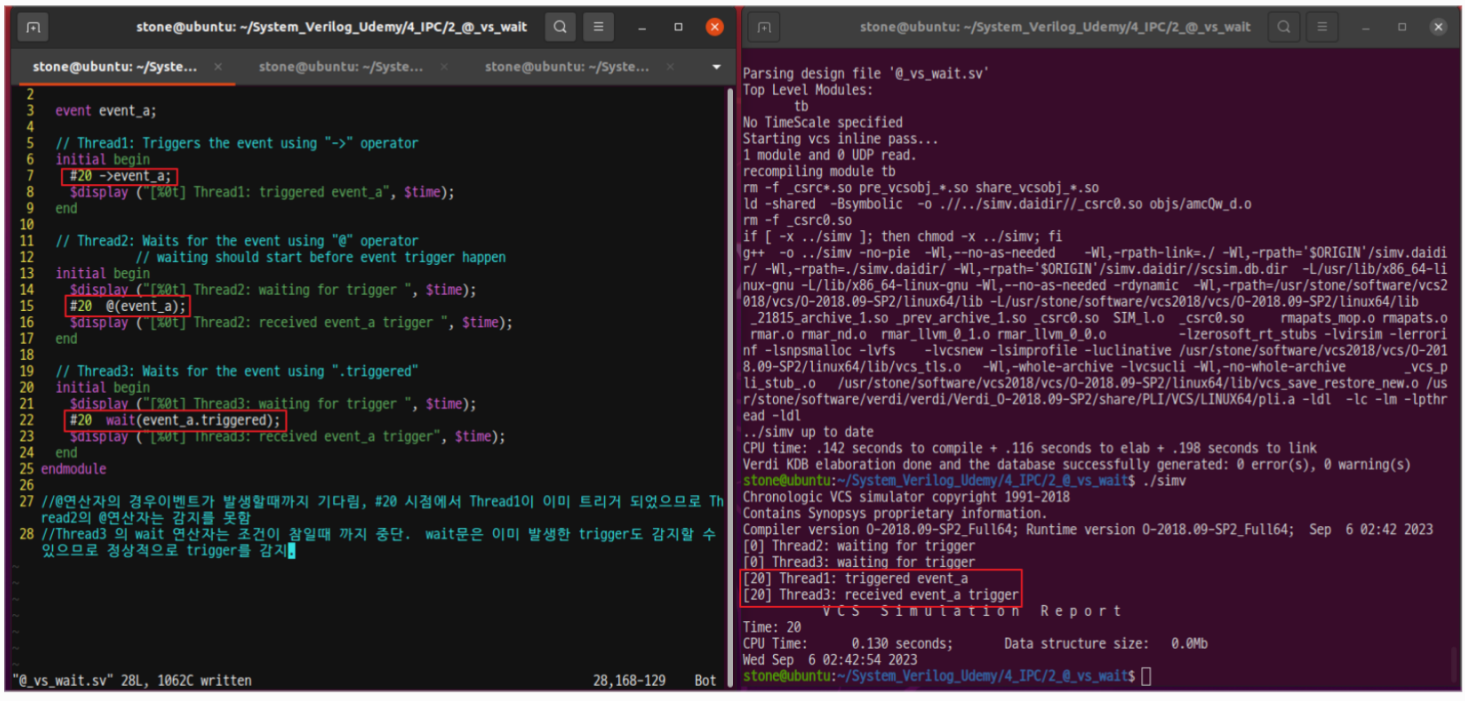
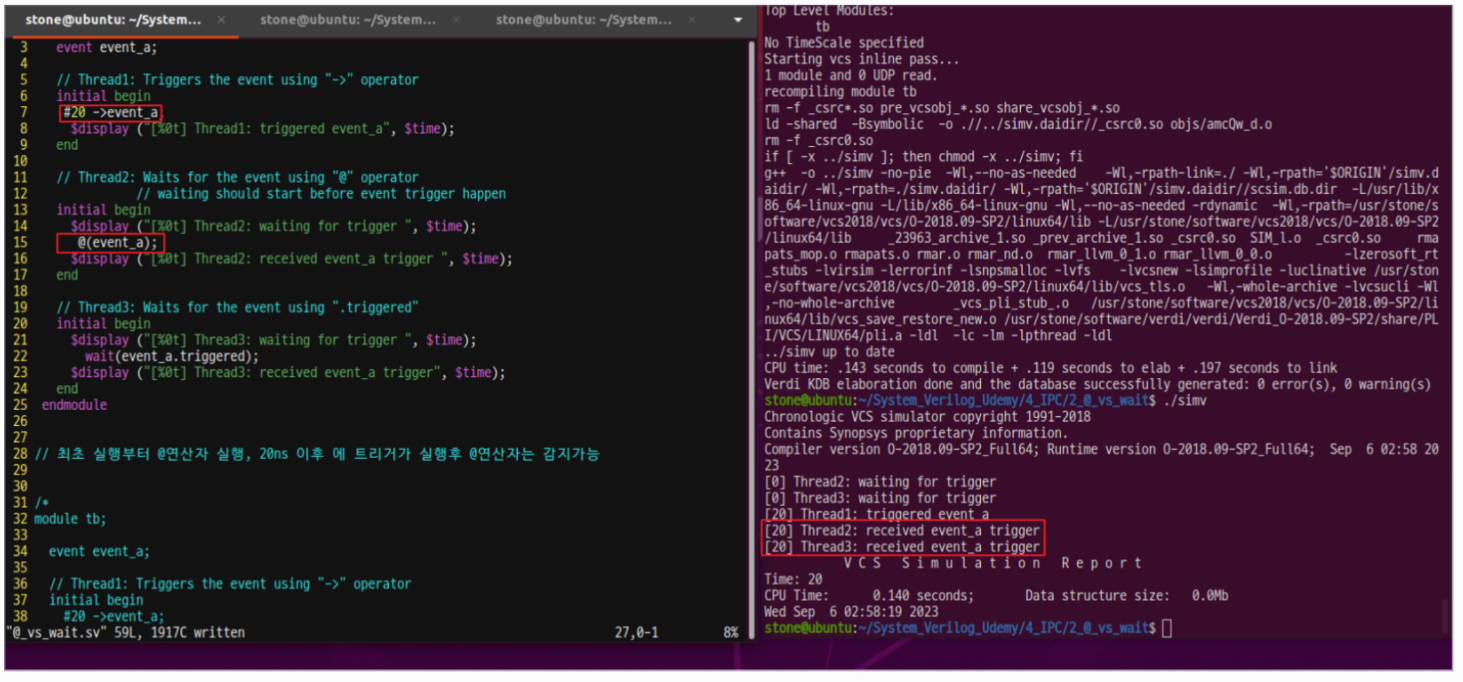

stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/2_@_vs_wait
stone@ubuntu: ~/Syste...
stone@ubuntu: ~/Syste...
stone@ubuntu: ~/Syste...
2
3 event event_a;
4
5 // Thread1: Triggers the event using "->" operator
6 initial begin
7 #20 ->event_a;
8 $display ("[%0t] Thread1: triggered event_a", $time);
9 end
10
11 // Thread2: Waits for the event using "@" operator
12 // waiting should start before event trigger happen
13 initial begin
14 $display ("[%0t] Thread2: waiting for trigger ", $time);
15 #20 @(event_a);
16 $display ("[%0t] Thread2: received event_a trigger ", $time);
17 end
18
19 // Thread3: Waits for the event using ".triggered"
20 initial begin
21 $display ("[%0t] Thread3: waiting for trigger ", $time);
22 #20 wait(event_a.triggered);
23 $display ("[%0t] Thread3: received event_a trigger", $time);
24 end
25 endmodule
26
27 //@연산자의 경우이벤트가 발생할때까지 기다림, #20 시점에서 Thread1이 이미 트리거 되었으므로 Th
read2의 @연산자는 감지를 못함
28 //Thread3 의 wait 연산자는 조건이 참일때 까지 중단. wait문은 이미 발생한 trigger도 감지할 수
있으므로 정상적으로 trigger를 감지
"@_vs_wait.sv" 28L, 1062C written
28,168-129 Bot
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/2_@_vs_wait
Parsing design file '@_vs_wait.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib
_21815_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o
rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrori
nf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-201
8.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_p
li_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /us
r/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthr
ead -ldl
../simv up to date
CPU time: .142 seconds to compile + .116 seconds to elab + .198 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/2_@_vs_wait$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 6 02:42 2023
[0] Thread2: waiting for trigger
[0] Thread3: waiting for trigger
[20] Thread1: triggered event_a
[20] Thread3: received event_a trigger
V C S S i m u l a t i o n R e p o r t
Time: 20
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Wed Sep 6 02:42:54 2023
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/2_@_vs_wait$


stone@ubuntu: ~/System...
stone@ubuntu: ~/System...
stone@ubuntu: ~/System...
3 event event_a;
4
5 // Thread1: Triggers the event using "->" operator
6 initial begin
7 #20 ->event_a
8 $display ("[%0t] Thread1: triggered event_a", $time);
9 end
10
11 // Thread2: Waits for the event using "@" operator
12 // waiting should start before event trigger happen
13 initial begin
14 $display ("[%0t] Thread2: waiting for trigger ", $time);
15 @(event_a);
16 $display ("[%0t] Thread2: received event_a trigger ", $time);
17 end
18
19 // Thread3: Waits for the event using ".triggered"
20 initial begin
21 $display ("[%0t] Thread3: waiting for trigger ", $time);
22 wait(event_a.triggered);
23 $display ("[%0t] Thread3: received event_a trigger", $time);
24 end
25 endmodule
26
27
28 // 최초 실행부터 @연산자 실행, 20ns 이후 에 트리거가 실행후 @연산자는 감지가능
29
30
31 /*
32 module tb;
33
34 event event_a;
35
36 // Thread1: Triggers the event using "->" operator
37 initial begin
38 #20 ->event_a;
"@_vs_wait.sv" 59L, 1917C written
27,0-1 8%
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.d
aidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x
86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/s
oftware/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2
/linux64/lib _23963_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rma
pats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt
_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/ston
e/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl
,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/li
nux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PL
I/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .143 seconds to compile + .119 seconds to elab + .197 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/2_@_vs_wait$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 6 02:58 20
23
[0] Thread2: waiting for trigger
[0] Thread3: waiting for trigger
[20] Thread1: triggered event_a
[20] Thread2: received event_a trigger
[20] Thread3: received event_a trigger
V C S S i m u l a t i o n R e p o r t
Time: 20
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Wed Sep 6 02:58:19 2023
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/2_@_vs_wait$