stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/9_Using...

```
1 class first;
2    int data=20;
3 endclass
4
5 class second;
6    first f1;
7
8    function new();
9       f1 = new();
10   endfunction
11
12 endclass
13
14 module tb;
15
16   second s;
17
18   initial begin
19      s = new();  //생성자
20      $display ("Value of data : %0d", s.f1.data);
21   end
22 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_C...

```
Parsing design file 'class_in_class.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib   o
bjs/amcQw_d.o   _9645_archive_1.so  SIM_l.o       rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_
llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs
 -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs
_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/
software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/v
erdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .505 seconds to compile + .265 seconds to elab + .226 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_Class$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 25 23:37 2023
Value of data : 20
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.350 seconds;       Data structure size:   0.0Mb
Fri Aug 25 23:37:52 2023
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/9_Using...

```
1 class first;
2    int data=20;
3    task display();
4          $display ("Value of data : %0d",data);
5    endtask
6 endclass
7
8 class second;
9    first f1;
10
11   function new();
12      f1 = new();
13   endfunction
14
15 endclass
16
17 module tb;
18
19   second s;
20
21   initial begin
22      s = new();  //생성자
23      $display ("Value of data : %0d", s.f1.data);
24      s.f1.display();// 클래스 안의 함수 접근
25   end
26 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_C...

```
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib
 _10783_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o
 rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrori
nf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-201
8.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_p
li_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /us
r/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthr
ead -ldl
../simv up to date
CPU time: .171 seconds to compile + .120 seconds to elab + .200 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_Class$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 25 23:46 2023
Value of data : 20
Value of data : 20
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Fri Aug 25 23:46:01 2023
```

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stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/9_Using...

```
1 class first;
2    int data=20;
3    task display();
4          $display ("Value of data : %0d",data);
5    endtask
6 endclass
7
8 class second;
9    first f1;
10
11   function new();
12      f1 = new();
13   endfunction
14
15 endclass
16
17 module tb;
18
19   second s;
20
21   initial begin
22      s = new();  //생성자
23      $display ("Value of data : %0d", s.f1.data);
24      s.f1.display();// 클래스 안의 함수 접근
25
26      s.f1.data = 43; //first 클래스안의 data 멤버 값 변경
27      s.f1.display();
28   end
29 endmodule
```

22,22-25 All

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_C...

```
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib
 _11398_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o
 rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrori
nf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-201
8.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_p
li_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /us
r/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthr
ead -ldl
../simv up to date
CPU time: .141 seconds to compile + .117 seconds to elab + .197 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_Class$ ./
bash: ./: Is a directory
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_Class$ ./s
bash: ./s: No such file or directory
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_Class$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 25 23:49 2023
Value of data : 20
Value of data : 20
Value of data : 43
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Fri Aug 25 23:49:16 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/9_Using_Class_in_Class$
```