stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/17_super_keyword

```sv
class first;
   int data;

   function new(input int data); //생성자를 정의하기 위한 특별한 함수
      this.data = data;
   endfunction

endclass

class second extends first;
   int temp;

   function new(input int data, input int temp);
      super.new(data); //부모 클래스의 함수에 값 할당 (Super 키워드)
      this.temp = temp;
   endfunction

endclass

module tb;

   second s;

   initial begin
      s = new(67,54);

      $display ("Value of data : %0d , temp : %0d",s.data,s.temp);
   end

endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/17_super_keyword

```
Time: 0
CPU Time:      0.140 seconds;       Data structure size:   0.0Mb
Sun Aug 27 07:05:31 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/17_super_keyword$ vcs -l vcs.log -sverilog -kdb -debug_access+all super_keyword.sv

Warning-[LINX_KRNL] Unsupported Linux kernel
  Linux kernel '5.15.0-79-generic' is not supported.
  Supported versions are 2.4* or 2.6*.

                         Chronologic VCS (TM)
       Version O-2018.09-SP2_Full64 -- Sun Aug 27 07:06:05 2023
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controlling such use and disclosure.

Parsing design file 'super_keyword.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
         However, due to incremental compilation, no re-compilation is necessary.
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpat
ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/st
software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib      _23639_archive_1.so _pre
chive_1.so _csrc0.so  SIM_l.o _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzeros
rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/lin
/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09
/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpth
 -ldl
../simv up to date
CPU time: .145 seconds to compile + .118 seconds to elab + .200 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/17_super_keyword$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 27 07:06 2023
Value of data : 67 , temp : 54
                    V c s   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Sun Aug 27 07:06:09 2023
```