stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/9_Equivalence_ope...

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```
1  class generator;
2     randc bit [3:0] a;
3     rand  bit ce;
4     rand  bit rst;
5
6     constraint control_rst{
7        rst dist {0:=50, 1:=50};
8     };
9
10    constraint control_ce{
11       ce dist {1:=50, 0:=50};
12    };
13
14    constraint control_rst_ce{
15       (rst == 1 ) <-> (ce ==1); //등가 연산 노트의 표참고
16    };
17
18 endclass
19
20 module tb;
21    generator g;
22
23    initial begin
24       g = new();
25
26       for (int i=0; i<15; i++) begin
27          g.randomize();
28          if (g.randomize)
29                $display ("Value of rst : %0d and ce :%0d" ,g.rst, g.ce);
30          else
31                $display ("Randomization Failed!");
32       end
33    end
34 endmodule
```

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```
CPU time: .143 seconds to compile + .115 seconds to elab + .195 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/8_Implication_Operator$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  4 05:15 2023
Value of rst : 0 and ce :1
Value of rst : 0 and ce :1
Value of rst : 0 and ce :1
Value of rst : 0 and ce :0
Value of rst : 0 and ce :1
Value of rst : 0 and ce :0
Value of rst : 1 and ce :1
Value of rst : 0 and ce :1
Value of rst : 1 and ce :1
Value of rst : 1 and ce :1
                V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Mon Sep  4 05:15:53 2023
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/8_Implication_Operator$ cd ..
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion$ cd 9_Equivalence_operator/
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/9_Equivalence_operator$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  4 05:18 2023
Value of rst : 1 and ce :1
Value of rst : 1 and ce :1
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Value of rst : 0 and ce :0
Value of rst : 1 and ce :1
Value of rst : 0 and ce :0
                V C S   S i m u l a t i o n   R e p o r t
```

- **Equivalence** (p <-> q)
  - Biconditional operator
  - p<->q is True whenever the truth values of p and q are same
  - expr1 <-> expr2 is same with
    ((expr1->expr2)&&(expr2->expr1))

p	q	p->q
T	T	T
T	F	F
F	T	F
F	F	T