stone@ubuntu: ~/System_Verilog_Study/5_Interface/5_modport

stone@ubuntu: ~/System_Verilog_Study/5_Interf... × stone@ubuntu: ~/System_Verilog_Study/5_Interf...

```
1 `timescale 1ns/100ps
2 interface add_if;
3    logic  [3:0] a;
4    logic  [3:0] b;
5    logic  [4:0] sum;
6    logic        clk;
7
8    modport DRV (output a,b, input sum,clk);  //modport는 Interface 신호의 방향지정
9 endinterface
10
11 class driver;
12    virtual add_if.DRV aif; // class 의 Interface 에도 modport 선언
13
14
15    task run();
16       forever begin
17          @(posedge aif.clk);
18          aif.a <= 2;
19          aif.b <= 3;
20          $strobe ("Interface Trigger");
21       end
22    endtask
23 endclass
24
25
26 module tb;
27    add_if aif();
28
29    add dut (.a(aif.a), .b(aif.b), .sum(aif.sum), .clk(aif.clk));
30
31    driver drv;
32
33    initial begin
34       aif.clk =0;
35    end
36
37    always #10 aif.clk = ~aif.clk;
38
39    initial begin
40       drv = new();
41       drv.aif = aif;
42       drv.run();
43    end
44
45    initial begin
46       $fsdbDumpvars; //Verdi 디버깅 파일 생성
47       #100;
```

12,67-65 Top

stone@ubuntu: ~/System_Verilog_Study/5_Interface/5_modport

```
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib     _28293_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/5_Interface/5_modport/csrc'
CPU time: .145 seconds to compile + .174 seconds to elab + .153 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
./simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep 12 02:11 2023
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
*Verdi* Loading libsscore_vcs201809.so
FSDB Dumper for VCS, Release Verdi_O-2018.09-SP2, Linux x86_64/64bit, 02/21/2019
(C) 1996 - 2019 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'novas.fsdb'
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
Interface Trigger
Interface Trigger
Interface Trigger
Interface Trigger
Interface Trigger
$finish called from file "interface.sv", line 48.
$finish at simulation time                1000
           V C S   S i m u l a t i o n   R e p o r t
Time: 100000 ps
CPU Time:      0.140 seconds;       Data structure size:   0.0Mb
Tue Sep 12 02:11:33 2023
stone@ubuntu:~/System_Verilog_Study/5_Interface/5_modport$ ./a
```

stone@ubuntu: ~/System_Verilog_Study/5_Interface/5_modport

stone@ubuntu: ~/System_Verilog_Study/5_Interf... × stone@ubuntu: ~/System_Verilog_Study/5_Interf...

```
1 `timescale 1ns/100ps
2 interface add_if;
3    logic  [3:0] a;
4    logic  [3:0] b;
5    logic  [4:0] sum;
6    logic        clk;
7
8    modport DRV (input a,b, input sum,clk);   //modport 와 DUT 의 신호 방향이 맞지 않을시 컴파일에러
9 endinterface
10
11 class driver;
12    virtual add_if.DRV aif; // class 의 Interface 에도 modport 선언
13
14
15    task run();
16       forever begin
17          @(posedge aif.clk);
18          aif.a <= 2;
19          aif.b <= 3;
20          $strobe ("Interface Trigger");
21       end
22    endtask
23 endclass
24
25
26 module tb;
27    add_if aif();
28
29    add dut (.a(aif.a), .b(aif.b), .sum(aif.sum), .clk(aif.clk));
30
31    driver drv;
32
33    initial begin
34       aif.clk =0;
35    end
36
37    always #10 aif.clk = ~aif.clk;
38
39    initial begin
40       drv = new();
41       drv.aif = aif;
42       drv.run();
43    end
44
```

stone@ubuntu: ~/System_Verilog_Study/5_Interface/5_modport

```
stone@ubuntu:~/System_Verilog_Study/5_Interface/5_modport$ make
vcs -l vcs.log -sverilog -kdb -debug_access+all interface.sv  add.v +vcs+vcdpluson

Warning-[LINX_KRNL] Unsupported Linux kernel
  Linux kernel '5.15.0-83-generic' is not supported.
  Supported versions are 2.4* or 2.6*.

                         Chronologic VCS (TM)
       Version O-2018.09-SP2_Full64 -- Tue Sep 12 02:15:39 2023
               Copyright (c) 1991-2018 by Synopsys Inc.
                         ALL RIGHTS RESERVED

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and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Parsing design file 'interface.sv'
Parsing design file 'add.v'
Top Level Modules:
       tb
TimeScale is 1 ns / 100 ps

Error-[MPCBD] Modport port cannot be driven
interface.sv, 18
$unit, "aif.a"
  Port 'a' of modport 'DRV' has been restricted as an input port. Input ports
  cannot be driven.


Error-[MPCBD] Modport port cannot be driven
interface.sv, 19
$unit, "aif.b"
  Port 'b' of modport 'DRV' has been restricted as an input port. Input ports
  cannot be driven.

2 errors
CPU time: .071 seconds to compile
make: *** [Makefile:15: compile] Error 255
stone@ubuntu:~/System_Verilog_Study/5_Interface/5_modport$
```