stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/8_Implication_Oper...

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```
1 class generator;
2    randc bit [3:0] a;
3    rand  bit ce;
4    rand  bit rst;
5    bit result;
6
7    constraint control_rst{
8       rst dist {0:=80, 1:=20};
9    };
10
11   constraint control_ce{
12      ce dist {1:=80, 0:=20};
13   };
14
15   constraint control_rst_ce{
16      (rst == 0 ) -> (ce ==1); //암시적 연산 노트의 표참고 (rst 가 1또는 0일때 ce는 1또는 0출력)
17   };
18
19 endclass
20
21 module tb;
22    generator g;
23
24    initial begin
25       g = new();
26
27       for (int i=0; i<10; i++) begin
28          g.randomize();
29          if (g.randomize)
30                $display ("Value of rst : %0d and ce :%0d" ,g.rst, g.ce );
31          else
32                $display ("Randomization Failed!");
33       end
34    end
35 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/8_Impl...

```
controlling such use and disclosure.

Parsing design file 'implication_operator.sv'
Top Level Modules:
        tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib     _28378_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o  rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .148 seconds to compile + .117 seconds to elab + .200 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/8_Implication_Operator$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  4 05:08 2023
Value of rst : 0 and ce :1
Value of rst : 0 and ce :1
Value of rst : 0 and ce :1
Value of rst : 1 and ce :0
Value of rst : 0 and ce :1
Value of rst : 1 and ce :0
Value of rst : 1 and ce :1
Value of rst : 0 and ce :1
Value of rst : 1 and ce :1
Value of rst : 1 and ce :1
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
```

- **->** implication operator

```
typedef enum { low, mid, high, any } AddrTyp_e;
class MyBus;
  rand bit[7:0] addr;
  rand AddrTyp_e atype;
  constraint addr_range {
   (atype == low ) -> addr inside { [0:15] };
   (atype == mid ) -> addr inside { [16:127] };
   (atype == high) -> addr inside { [128:255] };
  }
endclass
```

```
//if (atype == low)  addr inside { [0:15] };
//else if (atype == mid)  addr inside { [16:127] };
//else if (atype == high) addr inside { [128:255] };
```

- Note:
  - `a -> b is (!a || b)`. This states that if the expression is true, then random numbers generated are constrained by the constraint (or constraint set). Otherwise, the random numbers generated are unconstrained.
  - For the constraints in this example, `atype` can never be randomized to `any`.
    (Because three cases (low/mid/high) already covered full range!)

p	q	p->q
T	T	T
T	F	F
F	T	T
F	F	T