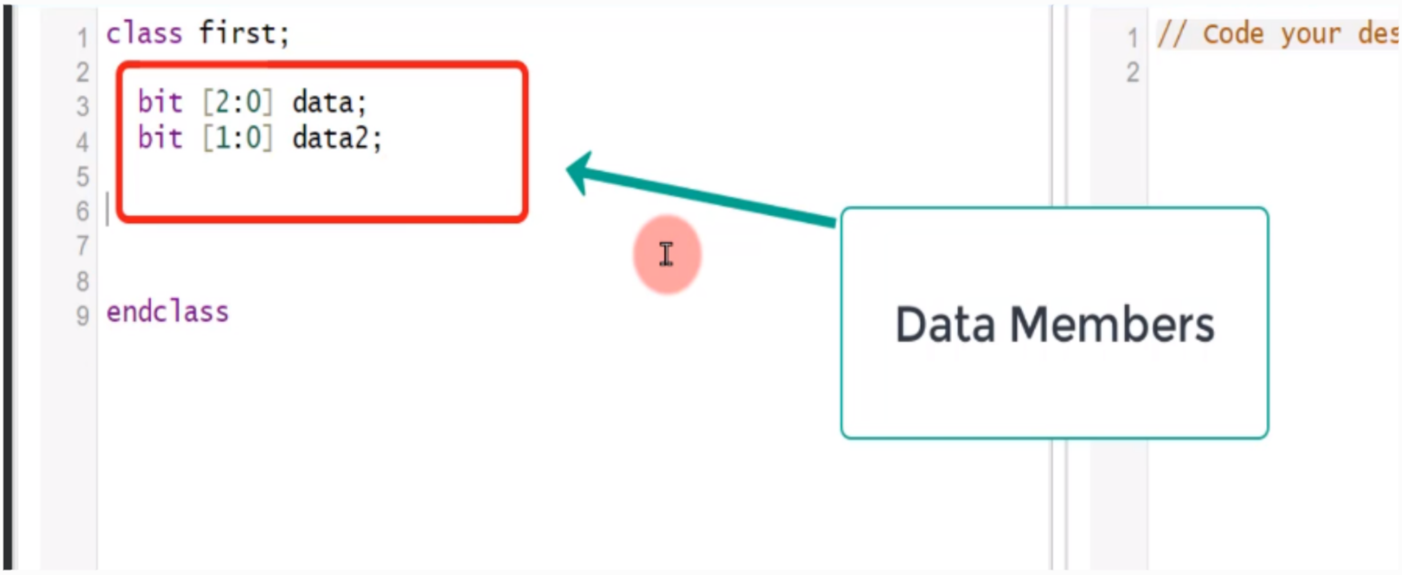
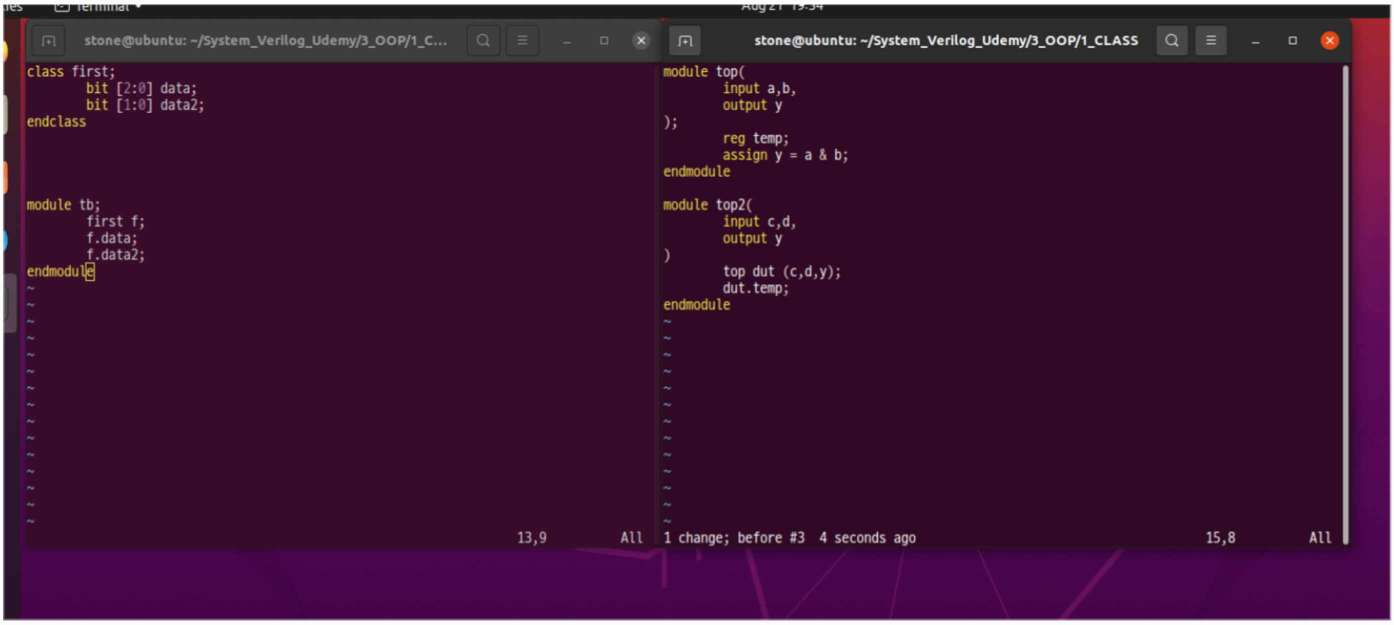
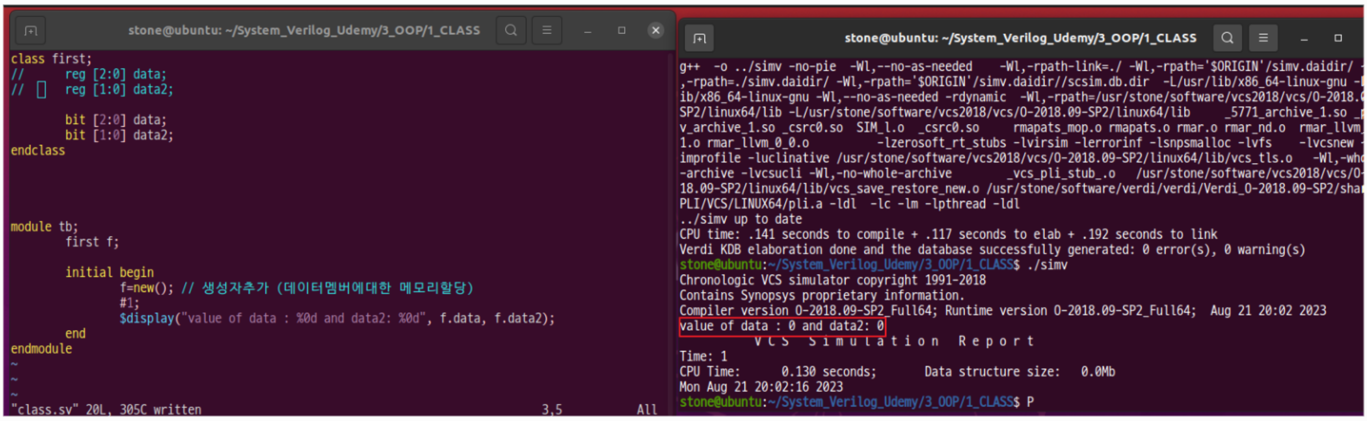
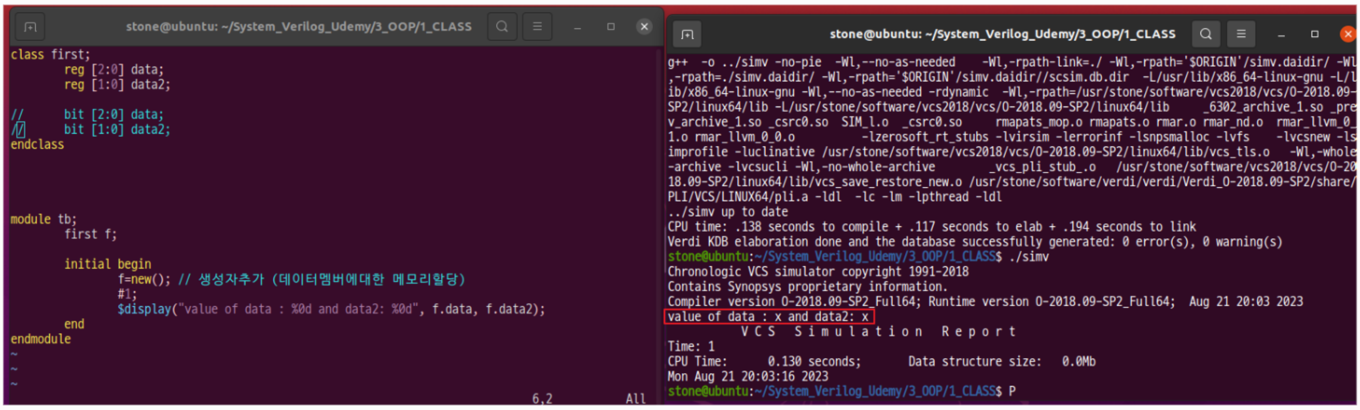

class first;
bit [2:0] data;
bit [1:0] data2;
endclass
// Code your des
Data Members


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_C...
class first;
bit [2:0] data;
bit [1:0] data2;
endclass
module tb;
first f;
f.data;
f.data2;
endmodule
13,9 All
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
module top(
input a,b,
output y
);
reg temp;
assign y = a & b;
endmodule
module top2(
input c,d,
output y
)
top dut (c,d,y);
dut.temp;
endmodule
1 change; before #3 4 seconds ago
15,8 All


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
class first;
// reg [2:0] data;
// reg [1:0] data2;
bit [2:0] data;
bit [1:0] data2;
endclass
module tb;
first f;
initial begin
f=new(); // 생성자추가 (데이터멤버에대한 메모리할당)
#1;
$display("value of data : %0d and data2: %0d", f.data, f.data2);
end
endmodule
"class.sv" 20L, 305C written
3,5 All
../simv up to date
CPU time: .141 seconds to compile + .117 seconds to elab + .192 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 21 20:02 2023
value of data : 0 and data2: 0
V C S S i m u l a t i o n R e p o r t
Time: 1
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Mon Aug 21 20:02:16 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ P


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
class first;
reg [2:0] data;
reg [1:0] data2;
// bit [2:0] data;
// bit [1:0] data2;
endclass
module tb;
first f;
initial begin
f=new(); // 생성자추가 (데이터멤버에대한 메모리할당)
#1;
$display("value of data : %0d and data2: %0d", f.data, f.data2);
end
endmodule
6,2 All
../simv up to date
CPU time: .138 seconds to compile + .117 seconds to elab + .194 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 21 20:03 2023
value of data : x and data2: x
V C S S i m u l a t i o n R e p o r t
Time: 1
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Mon Aug 21 20:03:16 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ P


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS

```
class first;
        reg [2:0] data;
        reg [1:0] data2;

//      bit [2:0] data;
//      bit [1:0] data2;
endclass



module tb;
        first f;

        initial begin
//              f=new(); // 생성자추가 (데이터멤버에대한 메모리할당)
                #1;
                $display("value of data : %0d and data2: %0d", f.data, f.data2);
        end
endmodule
~
~
~
                                                        16,2          All
```

```
../simv up to date
CPU time: .136 seconds to compile + .117 seconds to elab + .194 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 21 20:08 2023

Error-[NOA] Null object access
class.sv, 18
  The object at dereference depth 0 is being used before it was
  constructed/allocated.
  Please make sure that the object is allocated before using it.

  #0 in tb at class.sv:18
  #1 in tb


                 V C S   S i m u l a t i o n   R e p o r t
Time: 1
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Mon Aug 21 20:08:09 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ P
```

메모리 할당을 하지 않을시 NULL POINTER에 접근하므로 에러 발생

```
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
class first;
        reg [2:0] data;
        reg [1:0] data2;

//      bit [2:0] data;
//      bit [1:0] data2;
endclass



module tb;
        first f;

        initial begin
                f=new(); // 생성자추가 (데이터멤버에대한 메모리할당)
                f.data = 3'b010;
                f.data2 = 2'b10;
                #1;
                $display("value of data : %0d and data2: %0d", f.data, f.data2);
        end
endmodule
~
~
~
~
"class.sv" 22L, 345C written                            18,18-32      All
```

```
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl
,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/l
ib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-
SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib     _12815_archive_1.so _pr
ev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0
_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -l
simprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whol
e-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2
018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share
/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .144 seconds to compile + .117 seconds to elab + .194 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 21 21:45 2023
value of data : 2 and data2: 2
                 V C S   S i m u l a t i o n   R e p o r t
Time: 1
CPU Time:      0.140 seconds;       Data structure size:   0.0Mb
Mon Aug 21 21:45:06 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ P
```

```
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
class first;
        reg [2:0] data;
        reg [1:0] data2;

//      bit [2:0] data;
//      bit [1:0] data2;
endclass



module tb;
        first f;

        initial begin
                f=new(); // 생성자추가 (데이터멤버에대한 메모리할당)
                f.data = 3'b010;
                f.data2 = 2'b10;
                f = null; // 생성자 삭제 (객체삭제)
                #1;
                $display("value of data : %0d and data2: %0d", f.data, f.data2);
        end
endmodule
~
~
~
                                                        22,4-11       All
```

```
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/1_CLASS
simprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whol
e-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2
018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share
/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .141 seconds to compile + .119 seconds to elab + .194 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 21 21:56 2023

Error-[NOA] Null object access
class.sv, 21
  The object at dereference depth 0 is being used before it was
  constructed/allocated.
  Please make sure that the object is allocated before using it.

  #0 in tb at class.sv:21
  #1 in tb


                 V C S   S i m u l a t i o n   R e p o r t
Time: 1
CPU Time:      0.140 seconds;       Data structure size:   0.0Mb
Mon Aug 21 21:56:08 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/1_CLASS$ P
```