stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/3_Multiple_Initial_block

```
module tb;
   int data1,data2;
   event done;

   int i =0;

   //generator
   initial begin
      for (i=0; i<10; i++) begin
         data1 = $urandom();  //32비트 Unsigned 랜덤값
         $display ("Data sent : %0d", data1);
         #10;
      end
      -> done; //for문 종료시 done 트리거 발생
   end

   //Driver
   initial begin
      forever begin
      #10;
      data2 = data1;
      $display ("Data Receive : %0d", data2);
      end
   end

   initial begin
      wait (done.triggered);
      $finish(); //done 트리거 감지시 시뮬레이션 종료
   end

endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/3_Multiple_Init...

```
   _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .141 seconds to compile + .114 seconds to elab + .187 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/3_Multiple_Initial_block$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  6 04:12 2023
Data sent : 98710838
Data sent : 1474208060
Data Receive : 1474208060
Data sent : -1098913923
Data Receive : -1098913923
Data sent : 816460770
Data Receive : 816460770
Data sent : 41501707
Data Receive : 41501707
Data sent : -1179418145
Data Receive : -1179418145
Data sent : -212817600
Data Receive : -212817600
Data sent : -719881993
Data Receive : -719881993
Data sent : 1837005222
Data Receive : 1837005222
Data sent : 819246107
Data Receive : 819246107
Data Receive : 819246107
$finish called from file "mitiple.sv", line 28.
$finish at simulation time                  100
           V C S   S i m u l a t i o n   R e p o r t
Time: 100
```