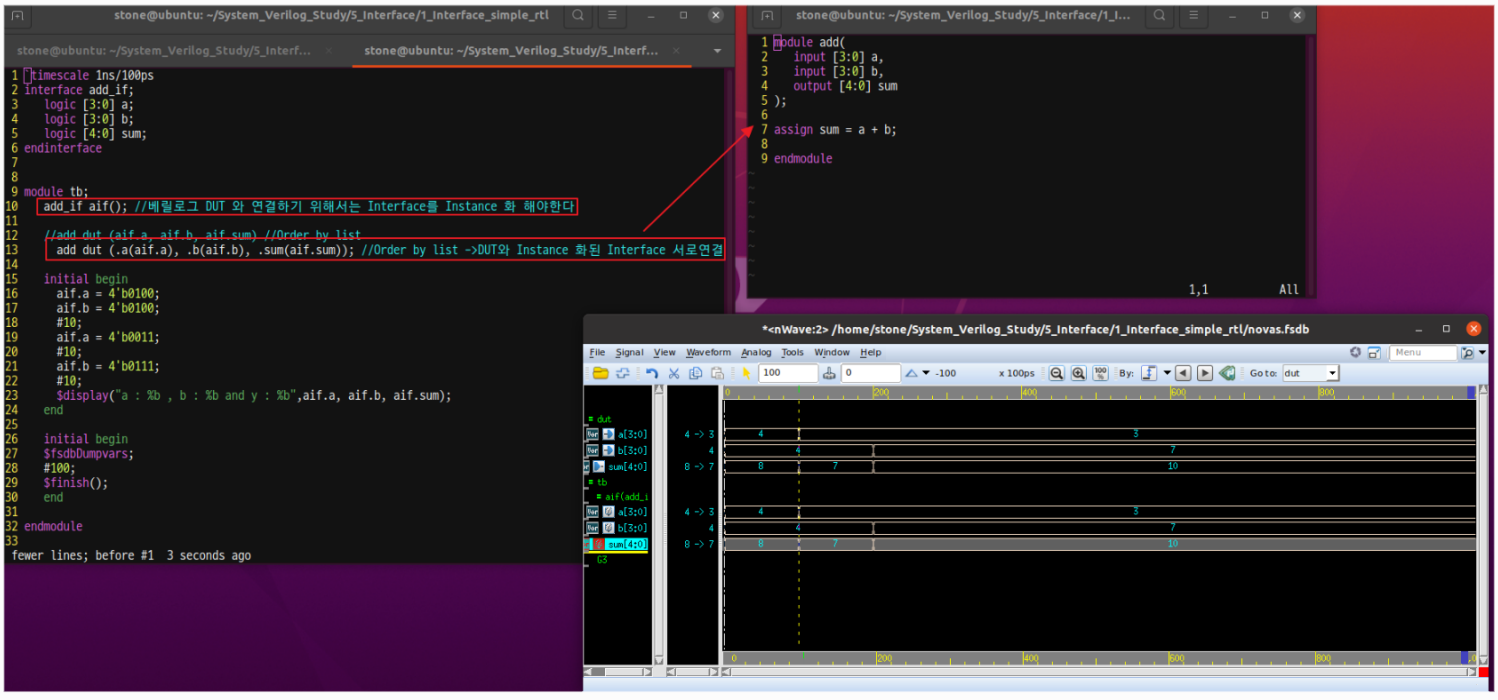
stone@ubuntu: ~/System_Verilog_Study/5_Interface/1_Interface_simple_rtl
stone@ubuntu: ~/System_Verilog_Study/5_Interf...
stone@ubuntu: ~/System_Verilog_Study/5_Interf...
1 `timescale 1ns/100ps
2 interface add_if;
3 logic [3:0] a;
4 logic [3:0] b;
5 logic [4:0] sum;
6 endinterface
7
8
9 module tb;
10 add_if aif(); //베릴로그 DUT 와 연결하기 위해서는 Interface를 Instance 화 해야한다
11
12 //add dut (aif.a, aif.b, aif.sum) //Order by list
13 add dut (.a(aif.a), .b(aif.b), .sum(aif.sum)); //Order by list ->DUT와 Instance 화된 Interface 서로연결
14
15 initial begin
16 aif.a = 4'b0100;
17 aif.b = 4'b0100;
18 #10;
19 aif.a = 4'b0011;
20 #10;
21 aif.b = 4'b0111;
22 #10;
23 $display("a : %b , b : %b and y : %b",aif.a, aif.b, aif.sum);
24 end
25
26 initial begin
27 $fsdbDumpvars;
28 #100;
29 $finish();
30 end
31
32 endmodule
33
fewer lines; before #1 3 seconds ago
stone@ubuntu: ~/System_Verilog_Study/5_Interface/1_I...
1 module add(
2 input [3:0] a,
3 input [3:0] b,
4 output [4:0] sum
5);
6
7 assign sum = a + b;
8
9 endmodule
1,1 All
*<nWave:2> /home/stone/System_Verilog_Study/5_Interface/1_Interface_simple_rtl/novas.fsdb
File Signal View Waveform Analog Tools Window Help
Menu
100
0
-100
x 100ps
By:
Go to:
dut
dut
a[3:0]
b[3:0]
sum[4:0]
tb
aif(add_i
a[3:0]
b[3:0]
sum[4:0]
4 -> 3
4
8 -> 7
4 -> 3
4
8 -> 7
0
200
400
600
800