

https://verificationguide.com/systemverilog/systemverilog-deep-copy/

딥 카피는 얇은 카피와 달리 모든 클래스 멤버와 중첩된 클래스 멤버를 복사

모든 클래스 속성이 새 핸들에 복사되고 새 핸들이 반환

### Deep Copy:

```
class address_range;
  bit [31:0] s_addr;
  bit [31:0] e_addr;

//copy method
function address_range copy;
  copy = new();
  copy.s_addr = this.s_addr;
  copy.e_addr = this.e_addr;
  return copy;
endfunction
endclass
```

```
class packet;
  //class properties
  bit [31:0] addr;
  bit [31:0] data;
  address_range ad_r;

//constructor
function new();
  //creating object
  ad_r = new();
endfunction

//copy method
function packet copy();
  copy = new();
  copy.addr = this.addr;
  copy.data = this.data;
  copy.ad_r = ad_r.copy;
  return copy;
endfunction
endclass
```

```
//declare the handle's
packet pkt_1;
packet pkt_2;

//construct the object
pkt_1 = new();

//Deep copy,
pkt_2 = pkt_1.copy();
```

memory

memory

pkt\_1

pkt\_1.ad\_r

User has to write the copy method for deep copy.

On calling the copy method, new memory will be allocated and the variable values will be copied to new object and also it call's the copy method of handle inside the object and returns the new object handle.

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```
1 class first;
2   int data = 12;
3
4   function first copy();
5     copy = new(); //Copy 라는 객체를 생성하고
6     copy.data = data; //Copy 객체에 data 라는 멤버 복사
7   endfunction
8
9 endclass
10
11 class second;
12   int ds = 34;
13
14   first f1; // class handle
15
16   function new(); //호출되면 텍스트 추가 (클래스 안에 클래스 만들기)
17     f1 = new(); //Creating object
18   endfunction
19
20   function second copy();
21     copy = new();
22     copy.ds = ds;
23     copy.f1 = f1.copy; //f1의 copy 객체를 복사
24   endfunction
25
26 endclass
27
28 module tb;
29
30   second s1, s2;
31
32   initial begin
33     s1 = new();
34     s2 = new();
35
36     s1.ds = 45;
37
38     s2 = s1.copy(); //s1의 copy 객체를 s2에 복사 (DeepCopy)
39     $display("Value of s2 : %0d", s2.ds);
40
41     s2.ds = 78;
42     $display("Value of s1 : %0d", s1.ds); //s2객체에 값을 넣어도 s1에 반영이 안됨
43
44     s2.f1.data = 98;
45     $display("Value of s1 : %0d", s2.f1.data); //
46   end
47
48 endmodule
```

```
CPU time: .067 seconds to compile
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/14_Deep_Copy$ vcs -l vcs.log -sverilog -kdb -debug_access=all deep_copy.sv

Warning-[LINUX_KERNEL] Unsupported Linux kernel
Linux kernel '5.15.0-79-generic' is not supported.
Supported versions are 2.4+ or 2.6+.

Chronologic VCS (TM)
Version 0-2018.09-SP2-Full64 -- Sun Aug 27 04:01:17 2023
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This program is proprietary and confidential information of Synopsys Inc.
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controlling such use and disclosure.

Parsing design file 'deep_copy.sv'
Top Level Modules:
  tb
No Timescale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc0.so pre_vcsobj.*.so share_vcsobj.*.so
ld -shared -Bsymbolic -o ./../simv.daidir/_csrc0.so obj/anc0w.d.o
rm -f _csrc0.so
if [ -x ./simv ]; then chmod -x ./simv; fi
g++ -o ./simv -no-pie -Wl,-no-as-needed -Wl,-rpath-link=./ -Wl,-rpath=$ORIGIN/simv.daidir -Wl,-rpath=./simv.daidir -Wl,-rpath=$ORIGIN/simv.daidir/scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,-no-as-needed -dynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib -l378.archive.1.so_prev.archive.1.so_csrc0.so SBLIO_csrc0.so repats_wop.o repats.o rnar.nd.o rnar.lvs.o rnar.lvs.o.0.0.o -lirsoft.rt.stubs -lvsim -lerrorinf -lsgnallloc -lvfs -lvcsnew -lslmprofile -linclnative /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs.tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive -vcs.pli.stub.o /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_0-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread

./simv up to date
CPU time: .148 seconds to compile + .115 seconds to elab + .204 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/14_Deep_Copy$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version 0-2018.09-SP2-Full64; Runtime version 0-2018.09-SP2-Full64; Aug 27 04:01:2023
Value of s2 : 45
Value of s1 : 45
Value of s1 : 98

VCS Simulation Report
Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Sun Aug 27 04:01:19 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/14_Deep_Copy$
```



