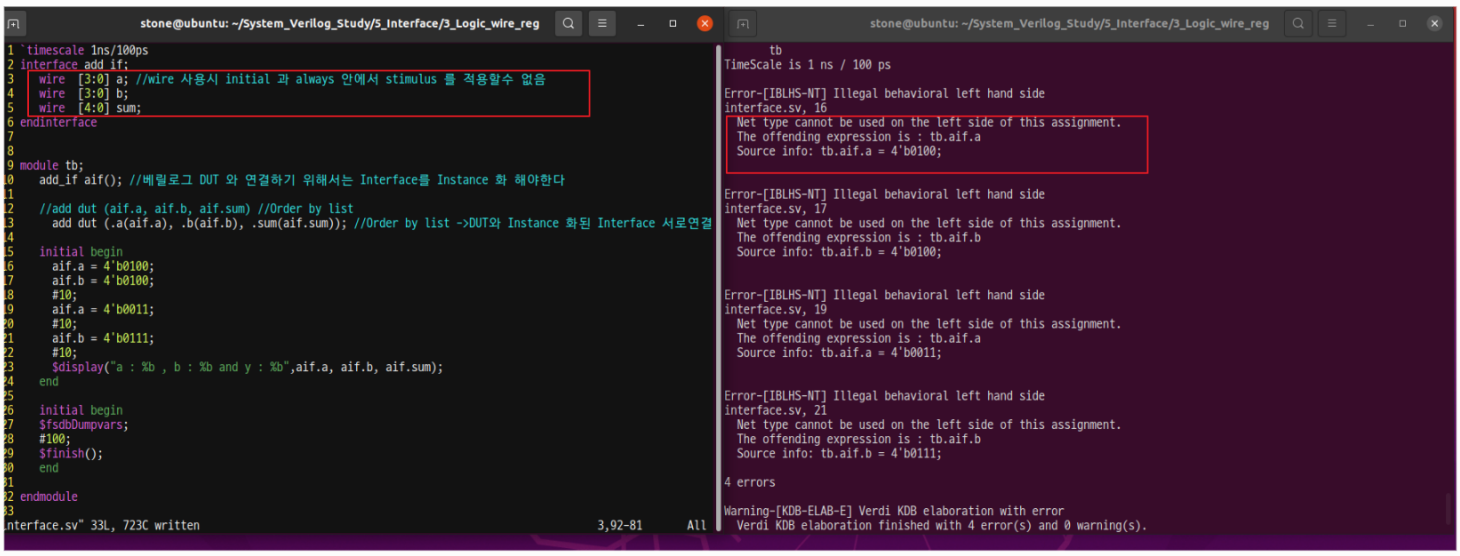
stone@ubuntu: ~/System_Verilog_Study/5_Interface/3_Logic_wire_reg
`timescale 1ns/100ps
interface add_if;
wire [3:0] a; //wire 사용시 initial 과 always 안에서 stimulus 를 적용할수 없음
wire [3:0] b;
wire [4:0] sum;
endinterface
module tb;
add_if aif(); //베릴로그 DUT 와 연결하기 위해서는 Interface를 Instance 화 해야한다
//add dut (aif.a, aif.b, aif.sum) //Order by list
add dut (.a(aif.a), .b(aif.b), .sum(aif.sum)); //Order by list ->DUT와 Instance 화된 Interface 서로연결
initial begin
aif.a = 4'b0100;
aif.b = 4'b0100;
#10;
aif.a = 4'b0011;
#10;
aif.b = 4'b0111;
#10;
$display("a : %b , b : %b and y : %b",aif.a, aif.b, aif.sum);
end
initial begin
$fsdbDumpvars;
#100;
$finish();
end
endmodule
nterface.sv" 33L, 723C written
3,92-81 All
stone@ubuntu: ~/System_Verilog_Study/5_Interface/3_Logic_wire_reg
tb
TimeScale is 1 ns / 100 ps
Error-[IBLHS-NT] Illegal behavioral left hand side
interface.sv, 16
Net type cannot be used on the left side of this assignment.
The offending expression is : tb.aif.a
Source info: tb.aif.a = 4'b0100;
Error-[IBLHS-NT] Illegal behavioral left hand side
interface.sv, 17
Net type cannot be used on the left side of this assignment.
The offending expression is : tb.aif.b
Source info: tb.aif.b = 4'b0100;
Error-[IBLHS-NT] Illegal behavioral left hand side
interface.sv, 19
Net type cannot be used on the left side of this assignment.
The offending expression is : tb.aif.a
Source info: tb.aif.a = 4'b0011;
Error-[IBLHS-NT] Illegal behavioral left hand side
interface.sv, 21
Net type cannot be used on the left side of this assignment.
The offending expression is : tb.aif.b
Source info: tb.aif.b = 4'b0111;
4 errors
Warning-[KDB-ELAB-E] Verdi KDB elaboration with error
Verdi KDB elaboration finished with 4 error(s) and 0 warning(s).