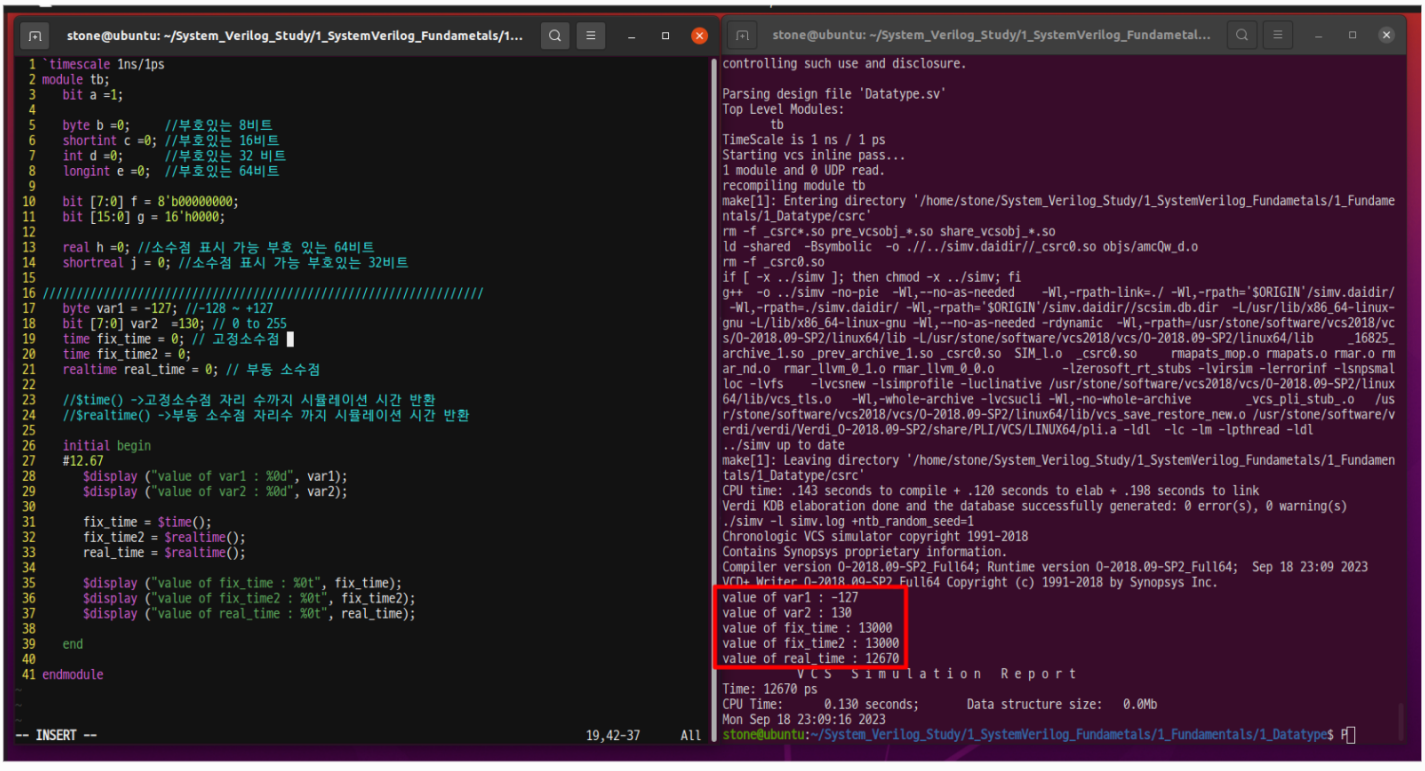


```
1  `timescale 1ns/1ps
2  module tb;
3     bit a =1;
4
5     byte b =0;      //부호있는 8비트
6     shortint c =0; //부호있는 16비트
7     int d =0;       //부호있는 32 비트
8     longint e =0;  //부호있는 64비트
9
10    bit [7:0] f = 8'b00000000;
11    bit [15:0] g = 16'h0000;
12
13    real h =0; //소수점 표시 가능 부호 있는 64비트
14    shortreal j = 0; //소수점 표시 가능 부호있는 32비트
15
16 ////////////////////////////////////////////////////////////////
17    byte var1 = -127; //-128 ~ +127
18    bit [7:0] var2  =130; // 0 to 255
19    time fix_time = 0; // 고정소수점
20    time fix_time2 = 0;
21    realtime real_time = 0; // 부동 소수점
22
23    //$time() ->고정소수점 자리 수까지 시뮬레이션 시간 반환
24    //$realtime() ->부동 소수점 자리수 까지 시뮬레이션 시간 반환
25
26    initial begin
27    #12.67
28       $display ("value of var1 : %0d", var1);
29       $display ("value of var2 : %0d", var2);
30
31       fix_time = $time();
32       fix_time2 = $realtime();
33       real_time = $realtime();
34
35       $display ("value of fix_time : %0t", fix_time);
36       $display ("value of fix_time2 : %0t", fix_time2);
37       $display ("value of real_time : %0t", real_time);
38
39    end
40
41 endmodule
```

```
controlling such use and disclosure.

Parsing design file 'Datatype.sv'
Top Level Modules:
       tb
TimeScale is 1 ns / 1 ps
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/1_Datatype/csrc'
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib     _16825_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o   _csrc0.so     rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/1_Datatype/csrc'
CPU time: .143 seconds to compile + .120 seconds to elab + .198 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
./simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep 18 23:09 2023
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
value of var1 : -127
value of var2 : 130
value of fix_time : 13000
value of fix_time2 : 13000
value of real_time : 12670
                V C S  S i m u l a t i o n  R e p o r t
Time: 12670 ps
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Mon Sep 18 23:09:16 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/1_Datatype$
```