```systemverilog
class generator;

  randc bit [3:0] raddr, waddr;
  rand bit wr;
  rand bit oe;

  constraint wr_c {
    wr dist {0:= 50, 1 := 50};
  }

  constraint oe_c {
    oe dist {1:= 50, 0 := 50};
  }

  constraint wr_oe_c {
    ( wr == 1 ) -> (oe == 0);
  }


endclass

module tb;

  generator g;

  initial begin
    g = new();

    g.wr_oe_c.constraint_mode(0); ///1 -> 제약조건 동작 // 0-> 제약조건 동작 안함
      $display("Constraint Status oe_c : %0d",g.wr_oe_c.constraint_mode());
    for (int i = 0; i<20 ; i++) begin
      assert(g.randomize()) else $display("Randomization Failed");
      $display("Value of wr : %0b ¦ oe : %0b ¦ ", g.wr, g.oe);
    end

  end

endmodule
```

rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.d
dir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir/scsim.db.dir -L/usr/lib/x86
4-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/softw
e/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux
/lib   _34239_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so   rmapats_mop
 rmapats.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o   -lzerosoft_rt_stubs -lv
sim -lerrorinf -lsnpsmalloc -lvfs   -lvcsnew -lsimprofile -luclinative /usr/stone/software/v
2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-arc
ve   _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_sa
_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.
-ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .149 seconds to compile + .117 seconds to elab + .201 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/11_turn_on_off_constraint$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 4 05:38 20
Constraint Status oe_c : 0
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 0 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 0 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 0 ¦ oe : 0 ¦
Value of wr : 0 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 0 ¦
Value of wr : 0 ¦ oe : 0 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 0 ¦ oe : 1 ¦
Value of wr : 0 ¦ oe : 0 ¦
Value of wr : 0 ¦ oe : 0 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 1 ¦
Value of wr : 1 ¦ oe : 0 ¦
Value of wr : 1 ¦ oe : 1 ¦
         V C S   S i m u l a t i o n   R e p o r t
Time: 0