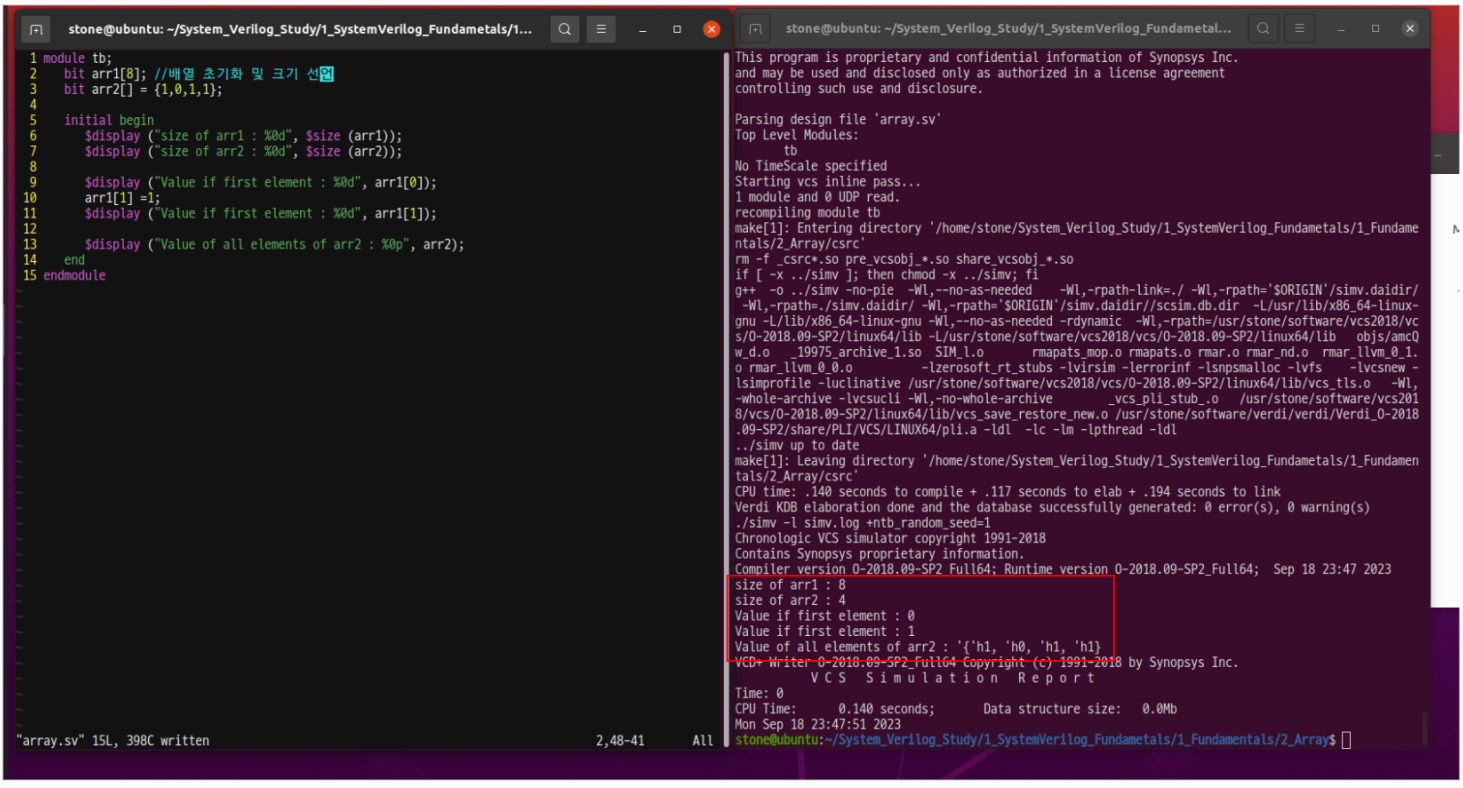
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametals/1...
1 module tb;
2 bit arr1[8]; //배열 초기화 및 크기 선언
3 bit arr2[] = {1,0,1,1};
4
5 initial begin
6 $display ("size of arr1 : %0d", $size (arr1));
7 $display ("size of arr2 : %0d", $size (arr2));
8
9 $display ("Value if first element : %0d", arr1[0]);
10 arr1[1] =1;
11 $display ("Value if first element : %0d", arr1[1]);
12
13 $display ("Value of all elements of arr2 : %0p", arr2);
14 end
15 endmodule
"array.sv" 15L, 398C written
2,48-41
All
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametal...
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Parsing design file 'array.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/2_Array/csrc'
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib objs/amcQw_d.o _19975_archive_1.so SIM_l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/2_Array/csrc'
CPU time: .140 seconds to compile + .117 seconds to elab + .194 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
./simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 18 23:47 2023
size of arr1 : 8
size of arr2 : 4
Value if first element : 0
Value if first element : 1
Value of all elements of arr2 : '{'h1, 'h0, 'h1, 'h1}
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Mon Sep 18 23:47:51 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/2_Array$