stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/11_Cop...

```
1 class first;
2
3    int data;
4
5 endclass
6
7 module tb;
8
9    first f1;
10   first p1;
11
12   initial begin
13      f1 = new(); //생성자
14
15      f1.data = 24;  // processing
16
17      p1 = new f1;   // f1객체의 데이터멤버를 p1 으로 복사
18
19      $display ("Value of data member : %0d", p1.data);
20   end
21
22 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/11_Copying_Object

```
Parsing design file 'copying_object.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib   o
bjs/amcQw_d.o   _20148_archive_1.so  SIM_l.o       rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar
_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs
  -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vc
s_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive         _vcs_pli_stub_.o   /usr/stone
/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/
verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .137 seconds to compile + .114 seconds to elab + .185 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/11_Copying_Object$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 26 02:04 2023
Value of data member : 24
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Sat Aug 26 02:04:40 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/11_Copying_Object$
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/11_Co...

```
1 class first;
2
3    int data;
4
5 endclass
6
7 module tb;
8
9    first f1;
10   first p1;
11
12   initial begin
13      f1 = new(); //생성자
14
15      f1.data = 24;  // processing
16
17      p1 = new f1;   // f1의 데이터멤버를 p1 으로 복사
18
19      $display ("Value of data member : %0d", p1.data);
20
21      p1.data = 12;
22
23      $display ("Vlaue of data member : %0d", f1.data);  //p1의 데이터 멤버의 값을
   변경해도 f1의 데이터 값은 변경되지 않음, 단순히 복사본만 얻음
24    end
25
26 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/11_Copying_Object

```
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib
 _22207_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o rmapats.o
 rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrori
nf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-201
8.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive         _vcs_p
li_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /us
r/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthr
ead -ldl
../simv up to date
CPU time: .139 seconds to compile + .116 seconds to elab + .193 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/11_Copying_Object$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Aug 26 02:15 2023
Value of data member : 24
Vlaue of data member : 24
                 V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Sat Aug 26 02:15:42 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/11_Copying_Object$
```