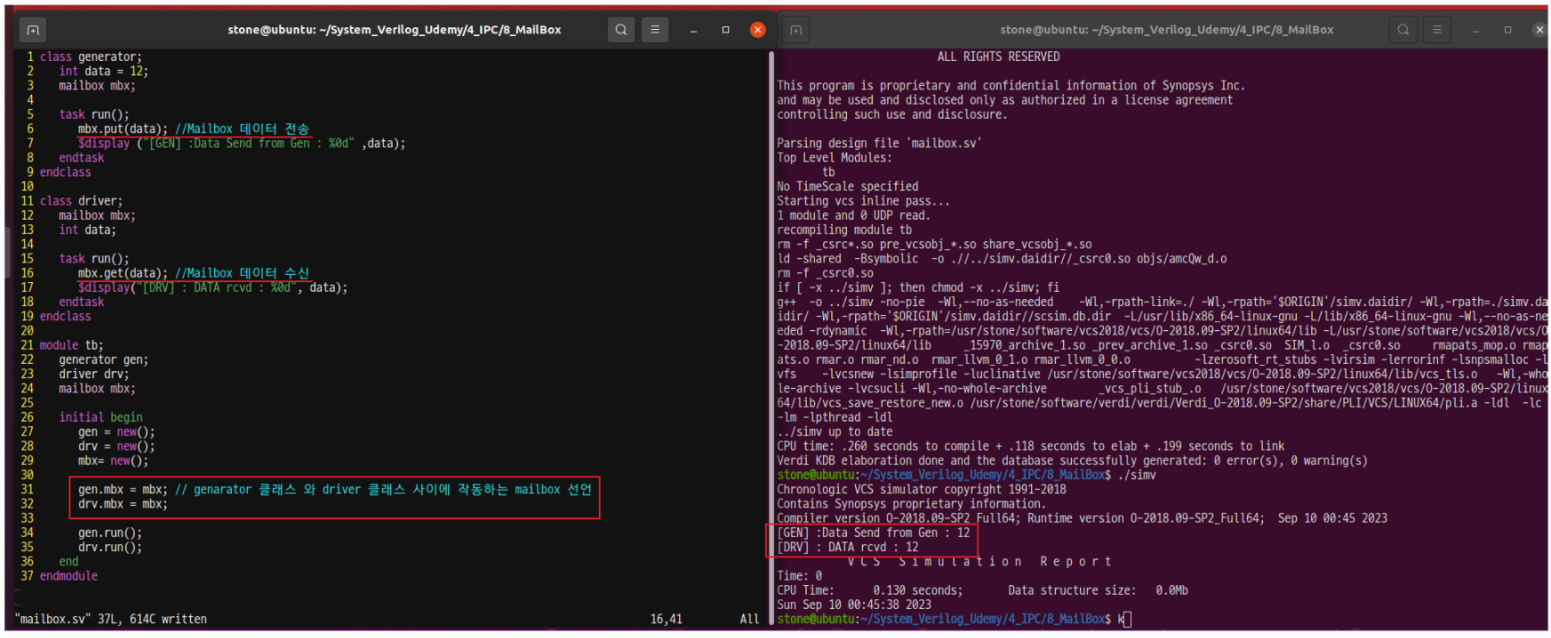
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/8_MailBox
class generator;
int data = 12;
mailbox mbx;
task run();
mbx.put(data); //Mailbox 데이터 전송
$display ("[GEN] :Data Send from Gen : %0d" ,data);
endtask
endclass
class driver;
mailbox mbx;
int data;
task run();
mbx.get(data); //Mailbox 데이터 수신
$display("[DRV] : DATA rcvd : %0d", data);
endtask
endclass
module tb;
generator gen;
driver drv;
mailbox mbx;
initial begin
gen = new();
drv = new();
mbx= new();
gen.mbx = mbx; // genarator 클래스 와 driver 클래스 사이에 작동하는 mailbox 선언
drv.mbx = mbx;
gen.run();
drv.run();
end
endmodule
"mailbox.sv" 37L, 614C written
16,41
All
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/8_MailBox
ALL RIGHTS RESERVED
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Parsing design file 'mailbox.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.da
idir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-ne
eded -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O
-2018.09-SP2/linux64/lib _15970_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmap
ats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -l
vfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-who
le-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux
64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc
-lm -lpthread -ldl
../simv up to date
CPU time: .260 seconds to compile + .118 seconds to elab + .199 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/8_MailBox$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 10 00:45 2023
[GEN] :Data Send from Gen : 12
[DRV] : DATA rcvd : 12
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Sun Sep 10 00:45:38 2023
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/8_MailBox$ k