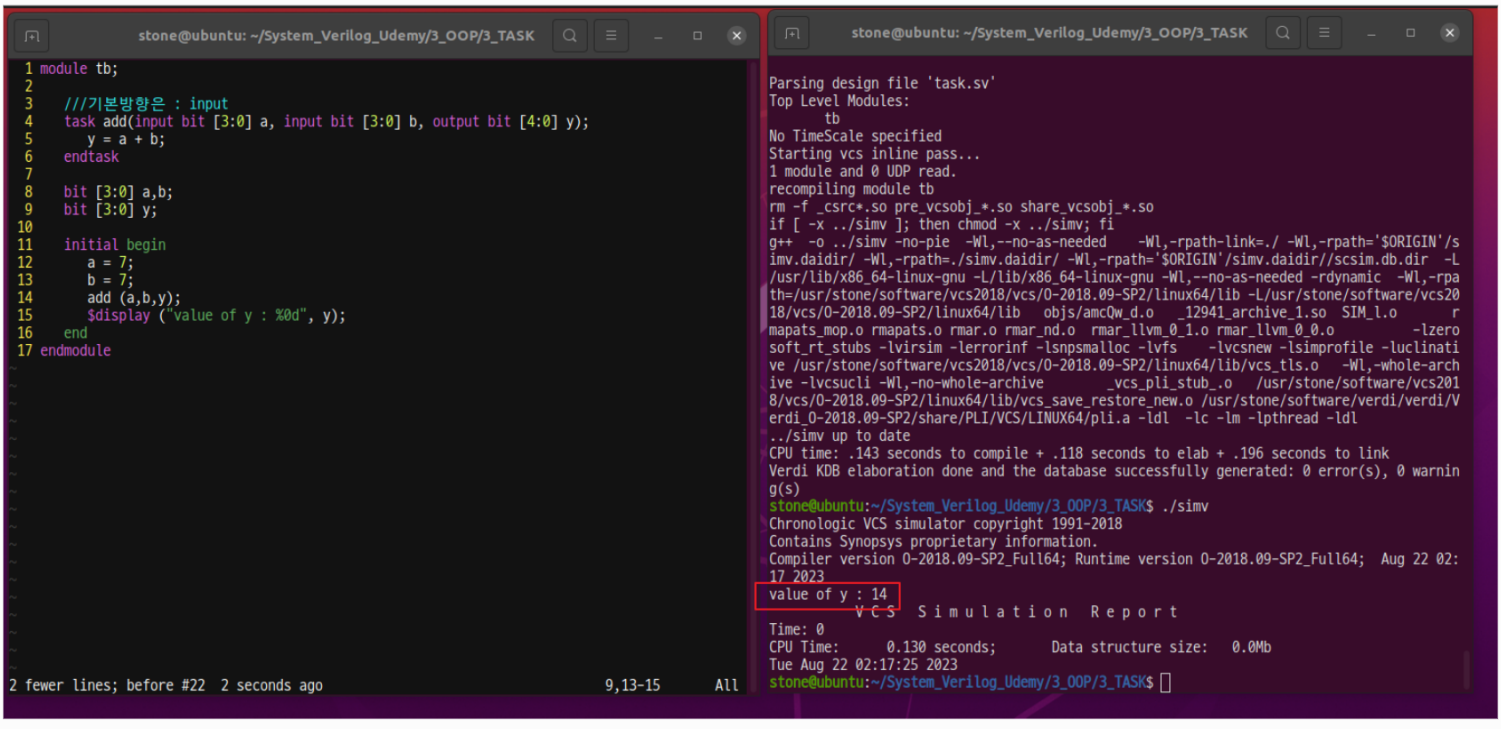
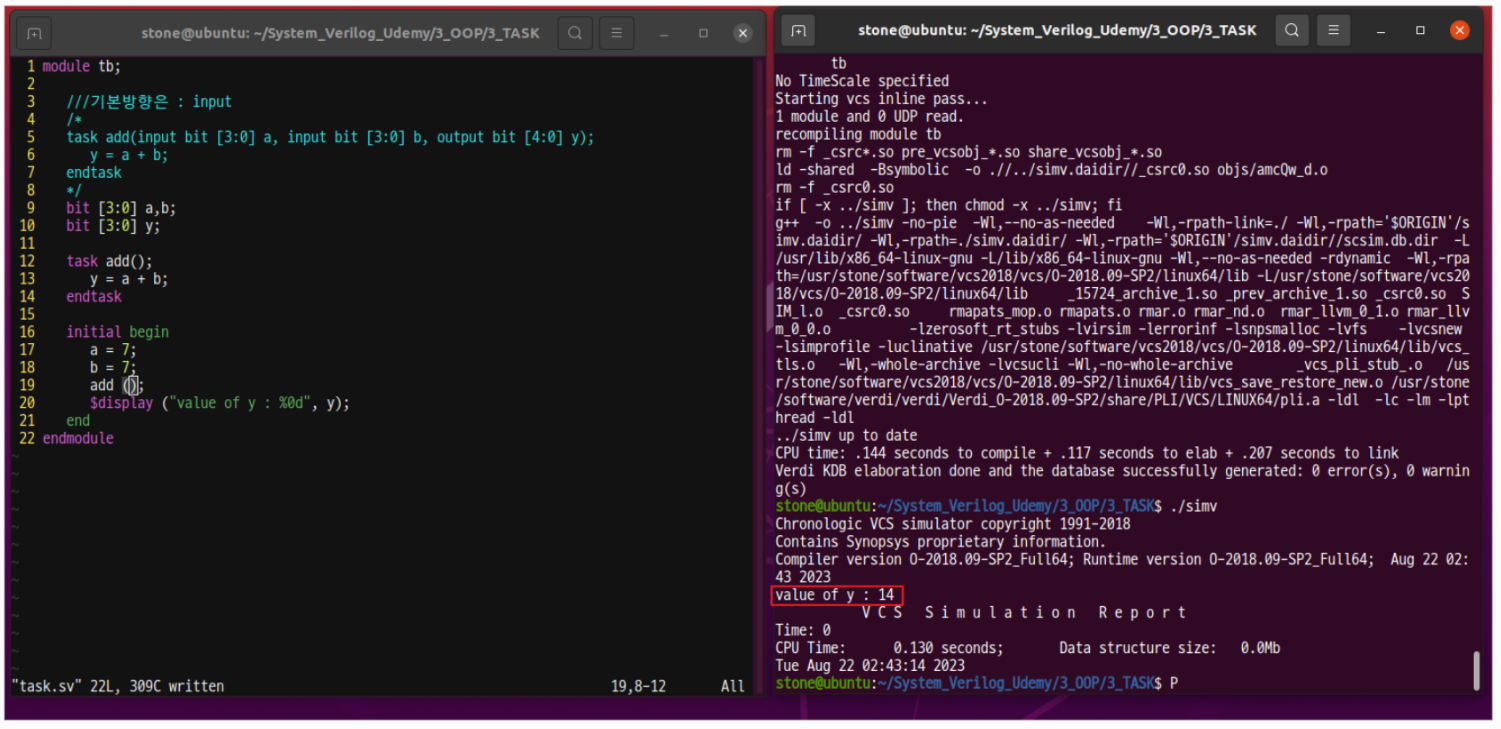
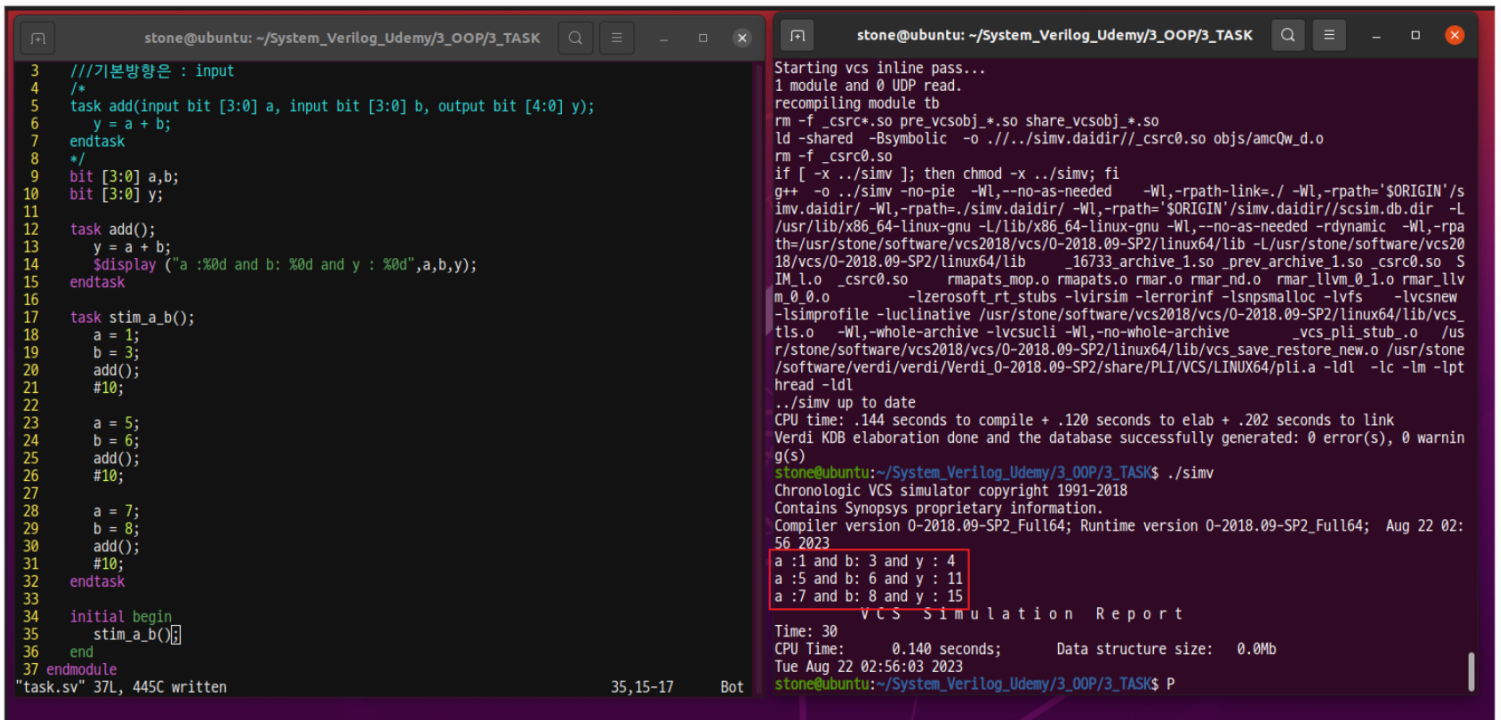
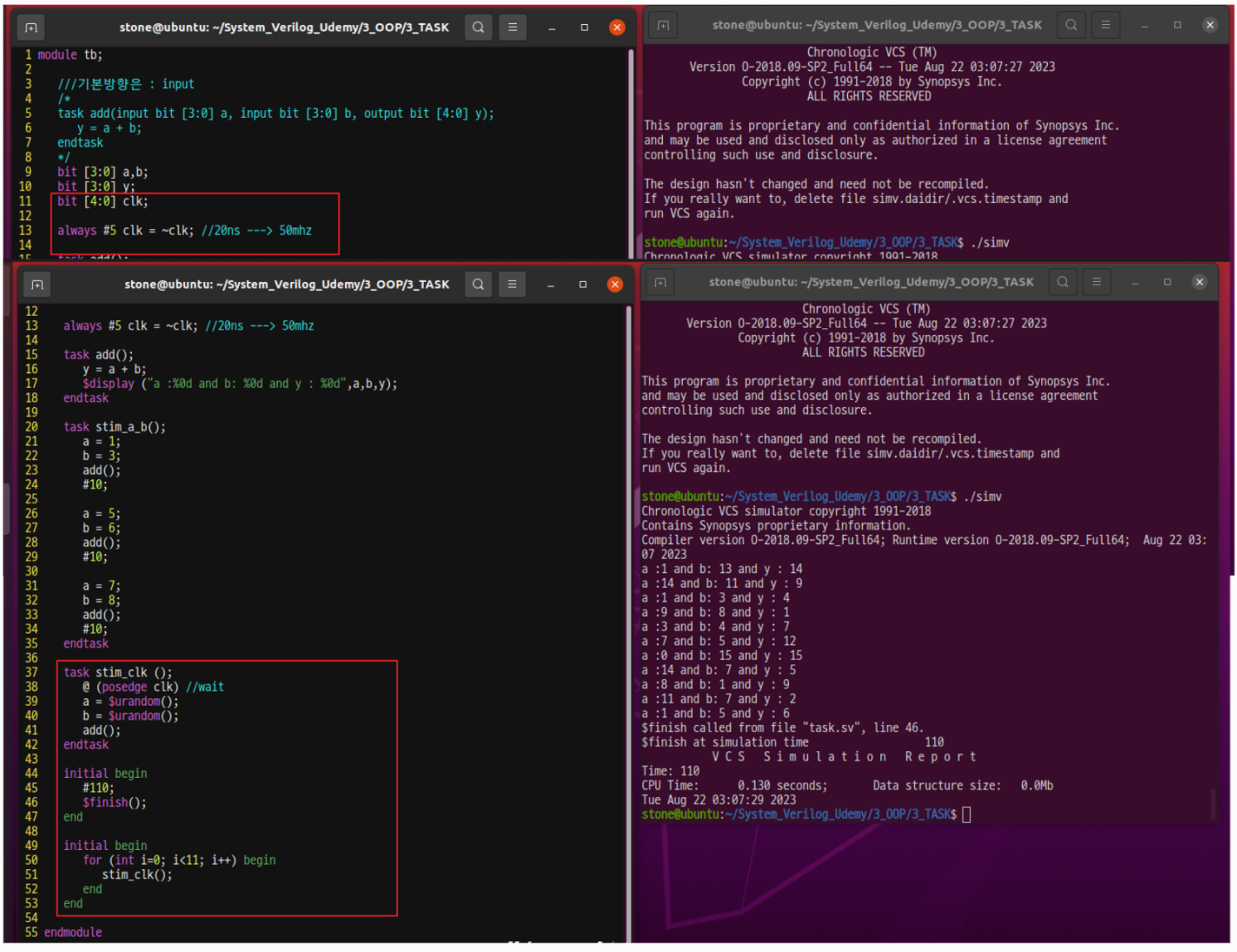

stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
1 module tb;
2
3 ///기본방향은 : input
4 task add(input bit [3:0] a, input bit [3:0] b, output bit [4:0] y);
5 y = a + b;
6 endtask
7
8 bit [3:0] a,b;
9 bit [3:0] y;
10
11 initial begin
12 a = 7;
13 b = 7;
14 add (a,b,y);
15 $display ("value of y : %0d", y);
16 end
17 endmodule
2 fewer lines; before #22 2 seconds ago 9,13-15 All
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
Parsing design file 'task.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib objs/amcQw_d.o _12941_archive_1.so SIM_l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .143 seconds to compile + .118 seconds to elab + .196 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 22 02:17 2023
value of y : 14
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Tue Aug 22 02:17:25 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
1 module tb;
2
3 ///기본방향은 : input
4 /*
5 task add(input bit [3:0] a, input bit [3:0] b, output bit [4:0] y);
6 y = a + b;
7 endtask
8 */
9 bit [3:0] a,b;
10 bit [3:0] y;
11
12 task add();
13 y = a + b;
14 endtask
15
16 initial begin
17 a = 7;
18 b = 7;
19 add ();
20 $display ("value of y : %0d", y);
21 end
22 endmodule
"task.sv" 22L, 309C written 19,8-12 All
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _15724_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .144 seconds to compile + .117 seconds to elab + .207 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 22 02:43 2023
value of y : 14
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Tue Aug 22 02:43:14 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$ P


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
3 ///기본방향은 : input
4 /*
5 task add(input bit [3:0] a, input bit [3:0] b, output bit [4:0] y);
6 y = a + b;
7 endtask
8 */
9 bit [3:0] a,b;
10 bit [3:0] y;
11
12 task add();
13 y = a + b;
14 $display ("a :%0d and b: %0d and y : %0d",a,b,y);
15 endtask
16
17 task stim_a_b();
18 a = 1;
19 b = 3;
20 add();
21 #10;
22
23 a = 5;
24 b = 6;
25 add();
26 #10;
27
28 a = 7;
29 b = 8;
30 add();
31 #10;
32 endtask
33
34 initial begin
35 stim_a_b();
36 end
37 endmodule
"task.sv" 37L, 445C written 35,15-17 Bot
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _16733_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .144 seconds to compile + .120 seconds to elab + .202 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 22 02:56 2023
a :1 and b: 3 and y : 4
a :5 and b: 6 and y : 11
a :7 and b: 8 and y : 15
V C S S i m u l a t i o n R e p o r t
Time: 30
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Tue Aug 22 02:56:03 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$ P


stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
module tb;
///기본방향은 : input
/*
task add(input bit [3:0] a, input bit [3:0] b, output bit [4:0] y);
y = a + b;
endtask
*/
bit [3:0] a,b;
bit [3:0] y;
bit [4:0] clk;
always #5 clk = ~clk; //20ns ---> 50mhz
task add();
y = a + b;
$display ("a :%0d and b: %0d and y : %0d",a,b,y);
endtask
task stim_a_b();
a = 1;
b = 3;
add();
#10;
a = 5;
b = 6;
add();
#10;
a = 7;
b = 8;
add();
#10;
endtask
task stim_clk ();
@ (posedge clk) //wait
a = $urandom();
b = $urandom();
add();
endtask
initial begin
#110;
$finish();
end
initial begin
for (int i=0; i<11; i++) begin
stim_clk();
end
end
endmodule
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/3_TASK
Chronologic VCS (TM)
Version O-2018.09-SP2_Full64 -- Tue Aug 22 03:07:27 2023
Copyright (c) 1991-2018 by Synopsys Inc.
ALL RIGHTS RESERVED
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
The design hasn't changed and need not be recompiled.
If you really want to, delete file simv.daidir/.vcs.timestamp and
run VCS again.
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 22 03:07 2023
a :1 and b: 13 and y : 14
a :14 and b: 11 and y : 9
a :1 and b: 3 and y : 4
a :9 and b: 8 and y : 1
a :3 and b: 4 and y : 7
a :7 and b: 5 and y : 12
a :0 and b: 15 and y : 15
a :14 and b: 7 and y : 5
a :8 and b: 1 and y : 9
a :11 and b: 7 and y : 2
a :1 and b: 5 and y : 6
$finish called from file "task.sv", line 46.
$finish at simulation time 110
VCS Simulation Report
Time: 110
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Tue Aug 22 03:07:29 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/3_TASK$