

add DUT 를 Monitor 와 Score board를 통한 검증

```
1 interface add_if;
2   logic [3:0] a;
3   logic [3:0] b;
4   logic [4:0] sum;
5   logic clk;
6 endinterface
7
8 class transaction;
9   randc bit [3:0] a;
10  randc bit [3:0] b;
11  bit [4:0] sum;
12
13  function void display();
14    $display("a : %0d, b : %0d, sum: %0d",a,b,sum);
15  endfunction
16 endclass
17
18 class monitor;
19   mailbox #(transaction) mbx;
20   transaction trans;
21   virtual add_if aif;
22
23   function new(mailbox #(transaction) mbx);
24     this.mbx = mbx;
25   endfunction
26
27   task run();
28     trans = new();
29     forever begin
30       repeat (2) @(posedge aif.clk); //2사이클 기다린후 (안정적인 결과를 얻기위해서추가)
31       trans.a = aif.a; //transaction 에 저장
32       trans.b = aif.b;
33       trans.sum = aif.sum;
34       $display("-----");
35       $display("Data sent to scoreboard");
36       trans.display();
37       mbx.put(trans); //Mailbox 에 전송
38     end
39   endtask
40 endclass
41
42 class scoreboard;
43   mailbox #(transaction) mbx;
44   transaction trans;
45   monitor mon;
46   function new(mailbox #(transaction) mbx);
47     this.mbx = mbx;
48   endfunction
49
50   task compare(input transaction trans); //a,b 의 값과 Sum의 값이 맞는지 확인
51     if((trans.sum) == (trans.a + trans.b))
52       $display("Sum result matched");
53     else
54       $error("result mismatched");
55   endtask
56
57   task run();
58     forever begin
59       mbx.get(trans);
60       $display("Data Receive From Monitor");
61       trans.display();
62       compare(trans); //compare 함수 호출
63     end
64   endtask
65 endclass
66 endclass
67
```

```
1 module add;
2   input [3:0] a;
3   input [3:0] b;
4   output reg [4:0] sum;
5   input clk;
6
7   always @(posedge clk) begin
8     sum <= a + b;
9   end
10 endmodule
11
12
```

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```
67 module tb;
68   add_if aif;
69   add_dut (.a(aif.a), .b(aif.b), .sum(aif.sum), .clk(aif.clk));
70   mailbox #(transaction) mbx;
71   scoreboard sco;
72   monitor mon;
73   initial begin
74     aif.clk = 0;
75   end
76
77   always #10 aif.clk = ~aif.clk;
78
79   initial begin
80     for(int i=0; i < 20; i++)begin
81       repeat(2)@(posedge aif.clk); //2사이클 딜레이
82       aif.a <= $urandom_range(0,15); //DUT 의 a,b, 포트에 Unsigned 값 0-15 무작위전송
83       aif.b <= $urandom_range(0,15);
84     end
85   end
86
87   initial begin
88     mbx = new();
89     sco = new(mbx);
90     mon = new(mbx);
91     mon.aif = aif;
92   end
93
94   initial begin
95     fork
96       mon.run();
97     sco.run();
98   end
99   join
100
101 end
102
103 initial begin
104   $dumpvars; //Veril 디버깅 파일 생성
105   #40;
106   $finish();
107 end
108 endmodule
```

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