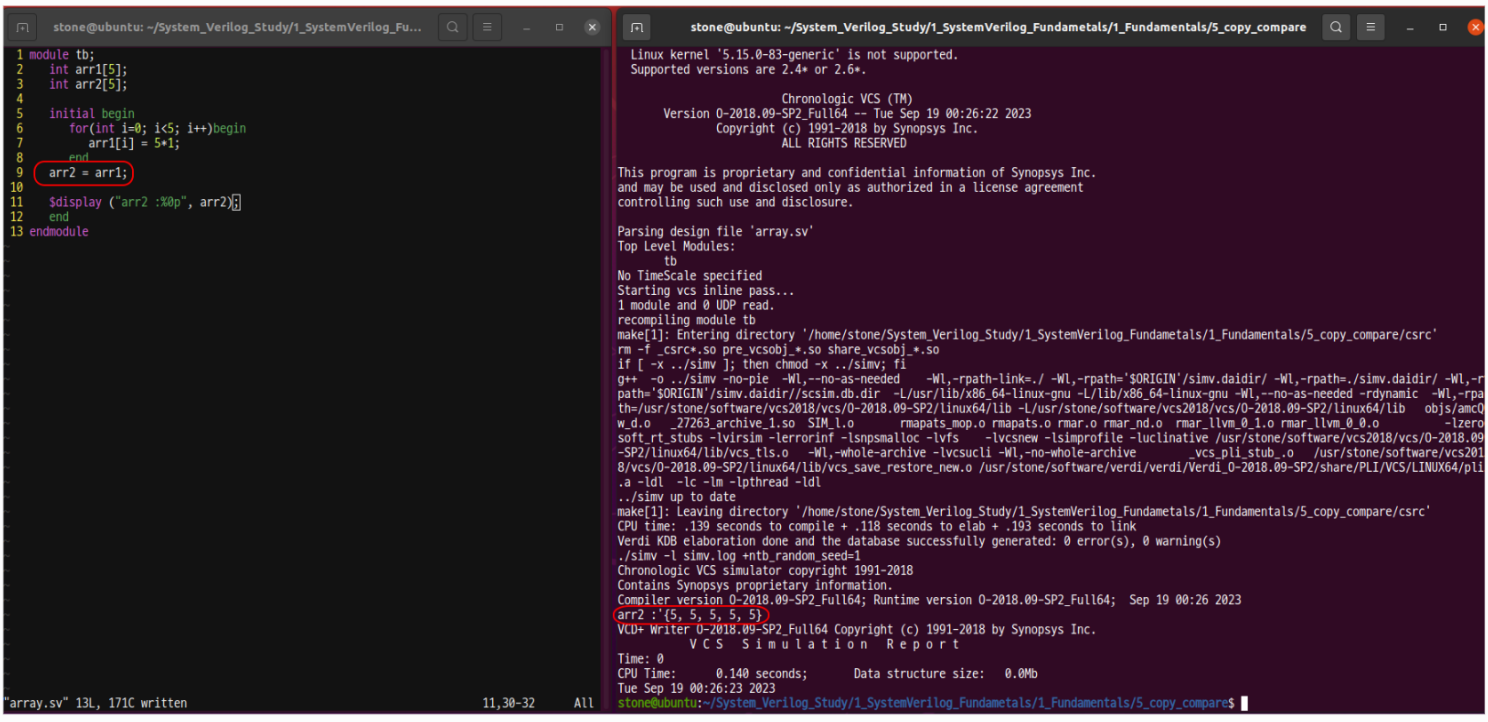
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fu...
1 module tb;
2 int arr1[5];
3 int arr2[5];
4
5 initial begin
6 for(int i=0; i<5; i++)begin
7 arr1[i] = 5*1;
8 end
9 arr2 = arr1;
10
11 $display ("arr2 :%0p", arr2);
12 end
13 endmodule
"array.sv" 13L, 171C written
11,30-32 All
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare
Linux kernel '5.15.0-83-generic' is not supported.
Supported versions are 2.4* or 2.6*.
Chronologic VCS (TM)
Version O-2018.09-SP2_Full64 -- Tue Sep 19 00:26:22 2023
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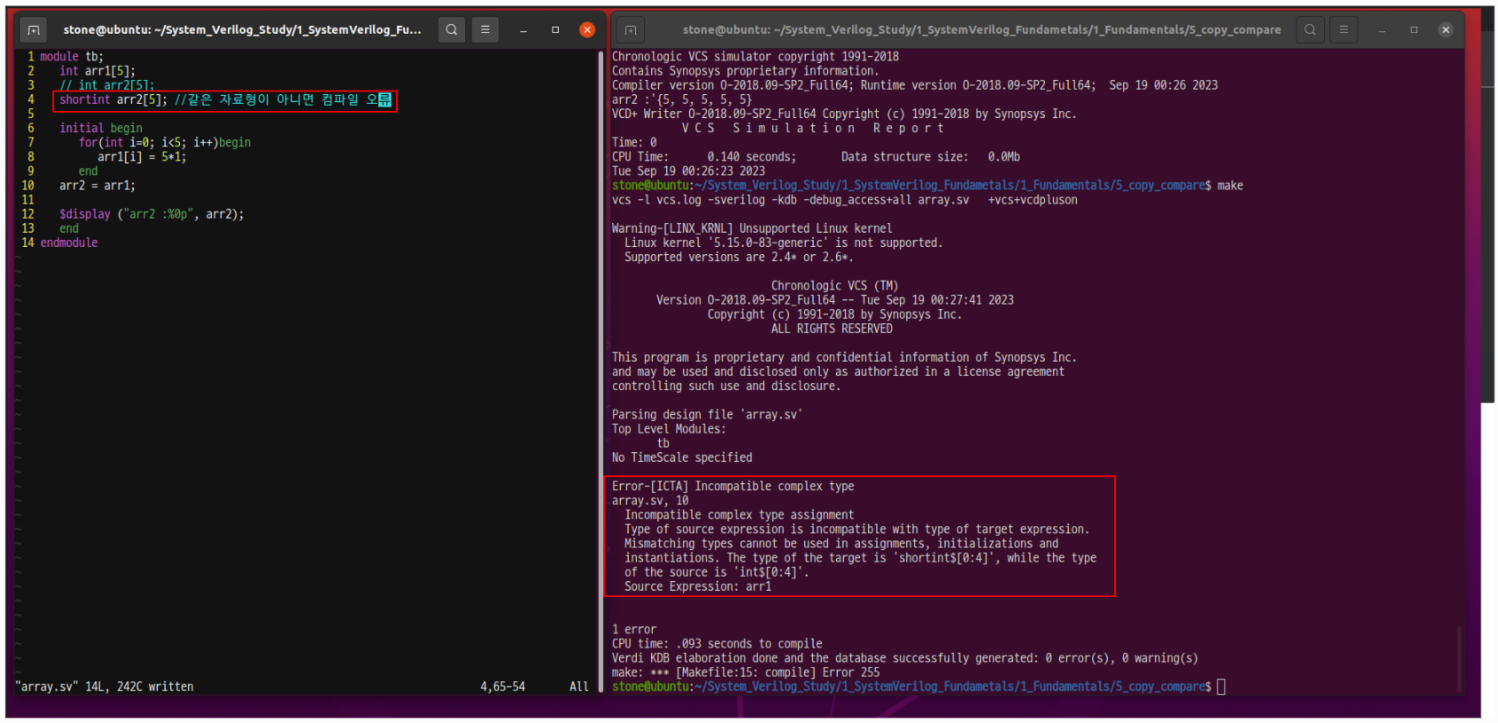
controlling such use and disclosure.
Parsing design file 'array.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare/csrc'
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib objs/amcQw_d.o _27263_archive_1.so SIM_l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare/csrc'
CPU time: .139 seconds to compile + .118 seconds to elab + .193 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
./simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 19 00:26 2023
arr2 :'{5, 5, 5, 5, 5}
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Tue Sep 19 00:26:23 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare$


stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fu...
1 module tb;
2 int arr1[5];
3 // int arr2[5];
4 shortint arr2[5]; //같은 자료형이 아니면 컴파일 오류
5
6 initial begin
7 for(int i=0; i<5; i++)begin
8 arr1[i] = 5*1;
9 end
10 arr2 = arr1;
11
12 $display ("arr2 :%0p", arr2);
13 end
14 endmodule
"array.sv" 14L, 242C written
4,65-54 All
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare
Chronologic VCS simulator copyright 1991-2018
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Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 19 00:26 2023
arr2 :'{5, 5, 5, 5, 5}
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Tue Sep 19 00:26:23 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare$ make
vcs -l vcs.log -sverilog -kdb -debug_access+all array.sv +vcs+vcdpluson
Warning-[LINX_KRNL] Unsupported Linux kernel
Linux kernel '5.15.0-83-generic' is not supported.
Supported versions are 2.4* or 2.6*.
Chronologic VCS (TM)
Version O-2018.09-SP2_Full64 -- Tue Sep 19 00:27:41 2023
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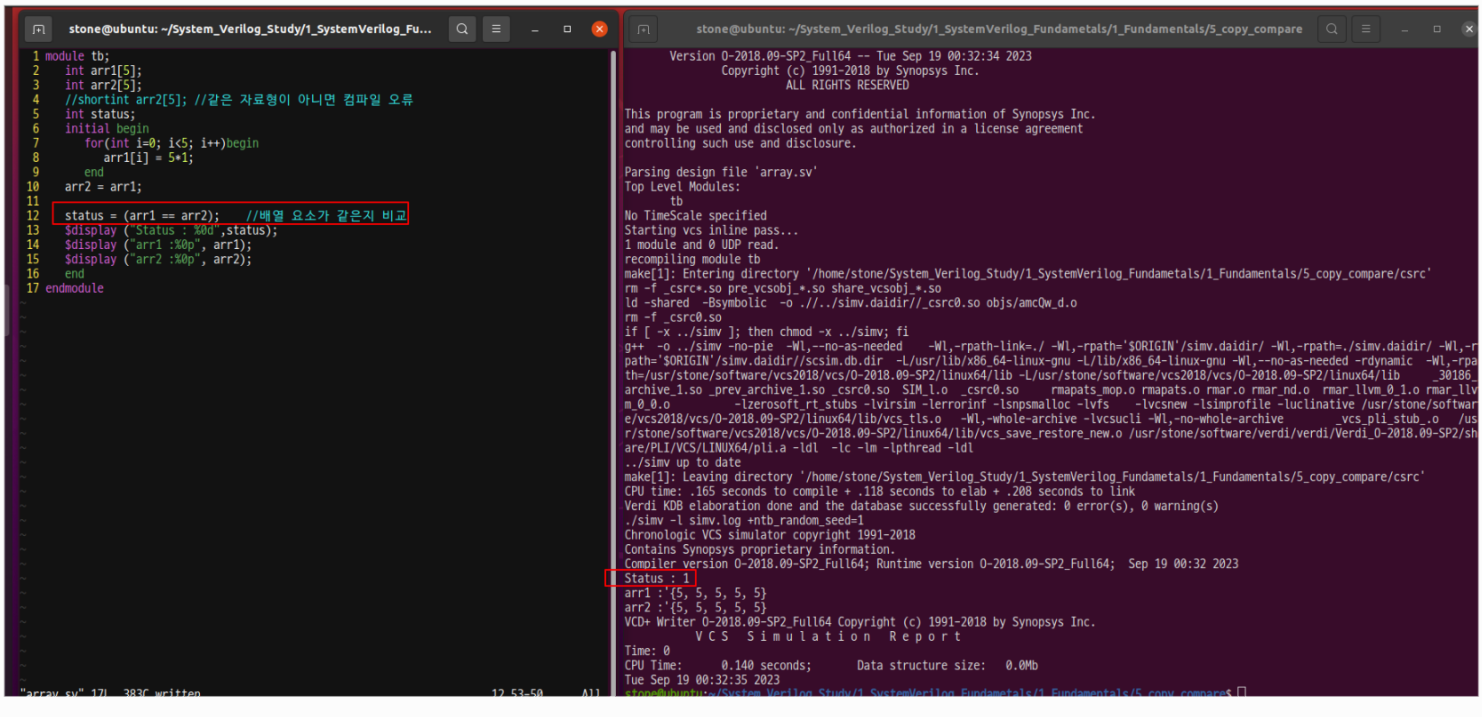
Parsing design file 'array.sv'
Top Level Modules:
tb
No TimeScale specified
Error-[ICTA] Incompatible complex type
array.sv, 10
Incompatible complex type assignment
Type of source expression is incompatible with type of target expression.
Mismatching types cannot be used in assignments, initializations and
instantiations. The type of the target is 'shortint$[0:4]', while the type
of the source is 'int$[0:4]'.
Source Expression: arr1
1 error
CPU time: .093 seconds to compile
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
make: *** [Makefile:15: compile] Error 255
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare$


stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fu...
1 module tb;
2 int arr1[5];
3 int arr2[5];
4 //shortint arr2[5]; //같은 자료형이 아니면 컴파일 오류
5 int status;
6 initial begin
7 for(int i=0; i<5; i++)begin
8 arr1[i] = 5*1;
9 end
10 arr2 = arr1;
11
12 status = (arr1 == arr2); //배열 요소가 같은지 비교
13 $display ("Status : %0d",status);
14 $display ("arr1 :%0p", arr1);
15 $display ("arr2 :%0p", arr2);
16 end
17 endmodule
"array.sv" 17L, 383C written
12,53-50 All
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare
Version O-2018.09-SP2_Full64 -- Tue Sep 19 00:32:34 2023
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Parsing design file 'array.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare/csrc'
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _30186_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/5_copy_compare/csrc'
CPU time: .165 seconds to compile + .118 seconds to elab + .208 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
./simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
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Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 19 00:32 2023
Status : 1
arr1 :'{5, 5, 5, 5, 5}
arr2 :'{5, 5, 5, 5, 5}
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Tue Sep 19 00:32:35 2023