```
Supported versions are 2.4* or 2.6*.
                                                                                                                                                                                                                                               Chronologic VCS (TM)
Version 0-2018.09-5P2_Full64 -- Sat Aug 26 00:02:46 2023
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ALL RIGHTS RESERVED
 8 class second;
9 first
                                                                                                                                                                                                                               This program is proprietary and confidential information of Synopsys Inc. and may be used and disclosed only as authorized in a license agreement controlling such use and disclosure.
           function new();
  f1 = new();
endfunction
                                                                                                                                                                                                                              Parsing design file 'class_in_class.sv'
Top Level Modules:
tb
No TimeScale specified
                                                                                                                                                                                                                              Error-[SV-ICVA] Illegal class variable access class in class.sv, 23
Local member 'data' of class 'first' is not visible to scope 'tb'.
Please make sure that the above member is accessed only from its own class properties as it is declared as local.
17 module tb:
             second s;
            initial begin
s = new(); //생성자
$display ("Value of data : %9d", s.f1.data);
s.f1.display();// 클래스 안의 함수 접근
                                                                                                                                                                                                                              Error-[SV-ICVA] Illegal class variable access class_in_class.sv, 26
Local member 'data' of class 'first' is not visible to scope 'tb'.
Please make sure that the above member is accessed only from its own class properties as it is declared as local.
                    s.fl.data = 43; //first 클래스안의 data 멤버 값 변경s.fl.display();
      endmodule
                                                                                                                                                                                                                              2 errors
CPU time: .094 seconds to compile
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
class_in_class.sv" 29L, 529C written
                                                                                                                                                                          2.64-55
                                                                                                                                                                                                            All
                                                                                                                                                                                                                                  stone@ubuntu: -/System_Verilog_Udemy/3_OOP/10_Scope_of_Data_... 🔾 🗏 – 🗆
  1 class first;
2 local int data=20; //local 은 해당데이터를 해당클래스 내부로만 제한시킴
3 task display();
4 $display ("Value of data : %%d",data);
                                                                                                                                                                                                                              if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,--rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir
/ -Wl,-rpath-./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/Lib/x86_64-li
nux-gnu -L/lib/x86_64-li
nux-gnu -L/lib/x86_95-P2/linux64/lib
- lvcsnew -Lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vc
- lvcsnew -Lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs
- stls.o - Wl,-whole-archive -Lvcsucli -Wl,-no-whole-archive - vcs.pli-stub. o /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/
verdi/Verdi_0-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
             task set (input int data); //local 변수의 값을 변경 시키기 위한 함수
this.data =data;
               function int get ();
return data;
endfunction
                                                                        //local 변수를 반환하는 함수
                                                                                                                                                                                                                               Verui/Verui_ Calais Strip
../simv up to date
CPU time: .140 seconds to compile + .114 seconds to elab + .187 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
.stone@uhuntu:~/System Verilog_Udemy/3_00P/10_Scope_of_Data_member$ ./simv
                                                                                                                                                                                                                              Chronologic VCS simulator copyright 1991-2018
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Compiler version 0-2018.09-SP2_Full64; Runtime version 0-2018.09-SP2_Full64; Aug 26 00:24 2023
Value of Data : 123
V C S S im u l a t i o n R e p o r t
Time: 0
CPULTime: 0 120 seconds: Data structure size: 0 0Mb
             function new();
  f1 = new();
endfunction
```

접근이 제한된 local 데이터멤버에 접근할지 상기와 같이 Class 내부에 local 데이터에 접근할수 있는 Task와 Fuction 선언

23 endclass module tb; second s:

initial begin s = new(); //생성자 s.fl.set(123); //first class 의 local 변수 변경[] Sdisplay ('Value of Data : %80', s.fl.get());;

CPU Time: 0.130 seconds; Sat Aug 26 00:24:38 2023

CPU Time: 0.130 seconds; Sat Aug 26 00:31:05 2023

Data structure size: 0.0Mb

Data structure size: 0.0Mb

Stone@ubuntu:-/System_Verilog_Udemy/3_00P/10_Scope_of_Data_member\$./simv
Chronologic VCS simulator copyright 1991-2018
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Compiler version 0-2018.09-SP2_Full64; Runtime version 0-2018.09-SP2_Full64; Aug 26 00:31 2023
Value of Data : 123
V C S S i m u l a t i o n R e p o r t
Time: 0
CUP Time: 0 130 compiler

'System_Verilog_Udemy/3_00P/10_Scope_of_Data_member\$