

The image shows a Verilog development environment with two main windows. The top-left window displays the Verilog source code for an interface and a testbench. The top-right window shows a module definition. The bottom window displays a waveform viewer.

**Verilog Source Code (Left Window):**

```
1 timescale 1ns/100ps
2 interface add_if;
3   logic [3:0] a;
4   logic [3:0] b;
5   logic [4:0] sum;
6 endinterface
7
8 module tb;
9   add_if aif(); //배열로그 DUT 와 연결하기 위해서는 Interface를 Instance 화 해야한다
10
11   //add_dut (aif.a, aif.b, aif.sum) //Order by list
12   add_dut (.a(aif.a), .b(aif.b), .sum(aif.sum)); //Order by list ->DUT와 Instance 화된 Interface 서로연결
13
14
15 initial begin
16   aif.a = 4'b0100;
17   aif.b = 4'b0100;
18   #10;
19   aif.a = 4'b0011;
20   #10;
21   aif.b = 4'b0111;
22   #10;
23   $display("a : %b , b : %b and y : %b",aif.a, aif.b, aif.sum);
24 end
25
26 initial begin
27   $fsdbDumpvars;
28   #100;
29   $finish();
30 end
31 endmodule
32
33 fewer lines; before #1 3 seconds ago
```

**Module Definition (Right Window):**

```
1 module add(
2   input [3:0] a,
3   input [3:0] b,
4   output [4:0] sum
5 );
6
7 assign sum = a + b;
8
9 endmodule
```

**Waveform Viewer (Bottom Window):**

The waveform viewer shows the signals `a`, `b`, and `sum` over time. The signals are 4-bit and 5-bit wide respectively. The waveform shows the values of `a` and `b` changing at 10ns intervals, and the resulting `sum` value.

Time (ns)	a [3:0]	b [3:0]	sum [4:0]
0	0100	0100	0100
10	0011	0100	0111
20	0011	0111	1010