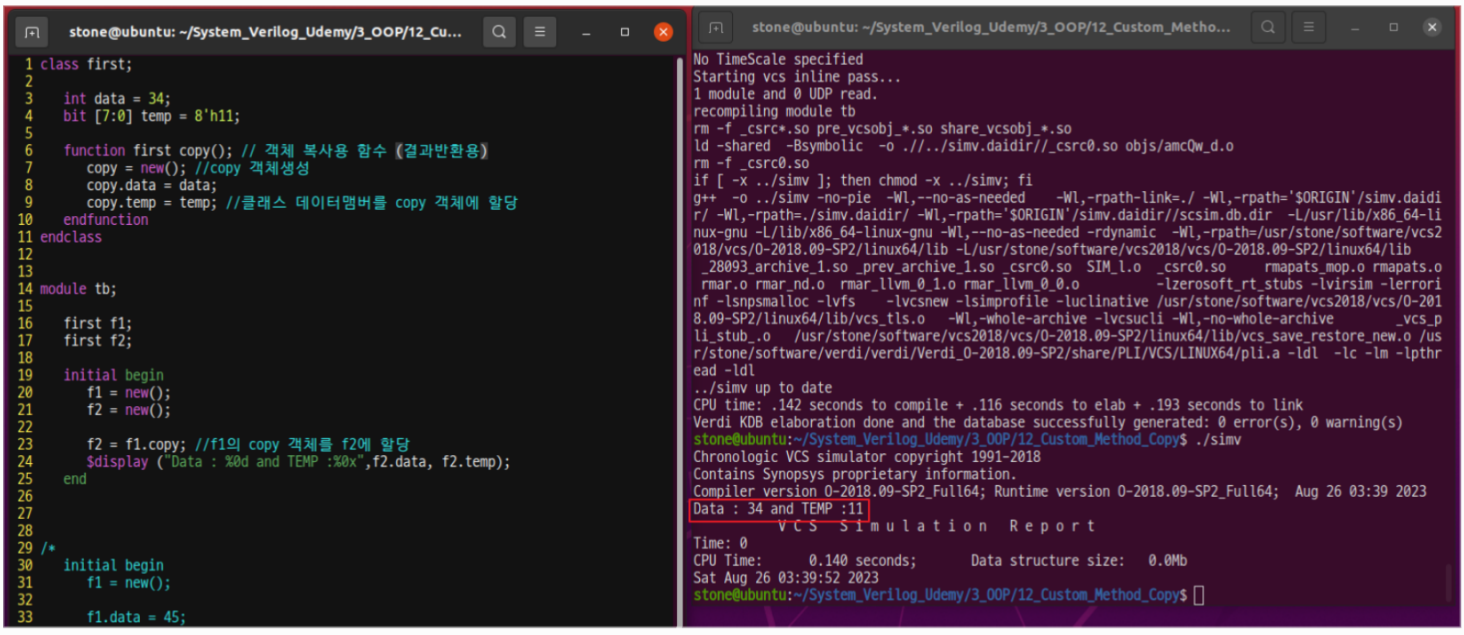
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/12_Cu...
1 class first;
2
3 int data = 34;
4 bit [7:0] temp = 8'h11;
5
6 function first copy(); // 객체 복사용 함수 (결과반환용)
7 copy = new(); //copy 객체생성
8 copy.data = data;
9 copy.temp = temp; //클래스 데이터맴버를 copy 객체에 할당
10 endfunction
11 endclass
12
13
14 module tb;
15
16 first f1;
17 first f2;
18
19 initial begin
20 f1 = new();
21 f2 = new();
22
23 f2 = f1.copy; //f1의 copy 객체를 f2에 할당
24 $display ("Data : %0d and TEMP :%0x",f2.data, f2.temp);
25 end
26
27
28
29 /*
30 initial begin
31 f1 = new();
32
33 f1.data = 45;
stone@ubuntu: ~/System_Verilog_Udemy/3_OOP/12_Custom_Metho...
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidi
r/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-li
nux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2
018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib
_28093_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o
rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrori
nf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-201
8.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_p
li_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /us
r/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthr
ead -ldl
../simv up to date
CPU time: .142 seconds to compile + .116 seconds to elab + .193 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/12_Custom_Method_Copy$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 26 03:39 2023
Data : 34 and TEMP :11
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Sat Aug 26 03:39:52 2023
stone@ubuntu:~/System_Verilog_Udemy/3_OOP/12_Custom_Method_Copy$