

```
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fu...
1 // Code your testbench here
2 // or browse Examples
3 module tb;
4
5   int arr[10]; //0-9
6   int i = 0;
7
8
9   initial begin
10
11     for(i= 0; i< 10; i++) begin //기본 반복문
12       arr[i] = i;
13     end
14
15
16     $display("arr : %0p", arr);
17
18   end
19 end
20
21
22
23 /*
24 initial begin
25
26   foreach(arr[j]) begin //0---9
27     arr[j] = 5;
28     $display("%0d", arr[j]);
29   end
30
31 end
32 */
33 /*
34 initial begin
35
36   repeat(10) begin
37     arr[i] = i;
38     i++;
39   end
40
41   $display("arr : %0p",arr);
42
43 end
44 */
```

```
Chronologic VCS (TM)
Version 0-2018.09-SP2-Full64 -- Tue Sep 19 00:07:38 2023
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controlling such use and disclosure.

Parsing design file 'array.sv'
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array/csrc'
rm -f _csrc*.so pre_vcsobj.*.so share_vcsobj.*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=../ -Wl,-rpath=$ORIGIN/./simv.daidir/ -Wl,-rpath=../simv.daidir/ -Wl,-rpath=$ORIGIN/./simv.daidir/scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib objs/amc0.w.d.o _23888.archive.1.so SIM.l.o rmapats.mop.o rmapats.o rmar.o rmar.nd.o rmar.llvm.0.1.o rmar.llvm.0.0.o -lzero soft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinate /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs.tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs.pli.stub.o /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_0-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array/csrc'

CPU time: .136 seconds to compile + .117 seconds to elab + .191 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
../simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version 0-2018.09-SP2-Full64; Runtime version 0-2018.09-SP2-Full64; Sep 19 00:07:2023
arr : {0, 1, 2, 3, 4, 5, 6, 7, 8, 9}
VCD+ Writer 0-2018.09-SP2-Full64 Copyright (c) 1991-2018 by Synopsys Inc.
VCS Simulation Report
Time: 0
CPU Time: 0.150 seconds; Data structure size: 0.0Mb
Tue Sep 19 00:07:39 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array$
```

```
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4
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12       arr[j] = 5;
13       $display("%0d", arr[j]);
14     end
15   end
16 end
17
18
19
20 /*
21 initial begin
22
23   for(i= 0; i< 10; i++) begin //기본 반복문
24     arr[i] = i;
25   end
26
27   $display("arr : %0p", arr);
28
29 end
30 */
31
32 /*
33 initial begin
34
35   repeat(10) begin
36     arr[i] = i;
37     i++;
38   end
39
40   $display("arr : %0p",arr);
41
42 end
43 */
44 array.sv 50L, 557C written
```

```
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array/csrc'
rm -f _csrc*.so pre_vcsobj.*.so share_vcsobj.*.so
ld -shared -Bsymbolic -o ../simv.daidir/_csrc0.so objs/amc0w.d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=../ -Wl,-rpath=$ORIGIN/./simv.daidir/ -Wl,-rpath=../simv.daidir/ -Wl,-rpath=$ORIGIN/./simv.daidir/scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib _24789.archive.1.so _prev_archive.1.so _csrc0.so SIM.l.o _csrc0.so rmapats.mop.o rmapats.o rmar.o rmar.nd.o rmar.llvm.0.1.o rmar.llvm.0.0.o -lzero soft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinate /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs.tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs.pli.stub.o /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_0-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array/csrc'

CPU time: .148 seconds to compile + .117 seconds to elab + .197 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
../simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version 0-2018.09-SP2-Full64; Runtime version 0-2018.09-SP2-Full64; Sep 19 00:14:2023
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5
VCD+ Writer 0-2018.09-SP2-Full64 Copyright (c) 1991-2018 by Synopsys Inc.
VCS Simulation Report
Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Tue Sep 19 00:14:13 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array$
```

stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fu...

```
1 // Code your testbench here
2 // or browse Examples
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4
5 int arr[10]; //0-9
6 int i = 0;
7
8
9 initial begin
10
11     repeat(10) begin //10번 반복
12         arr[i] = i;
13         i++;
14     end
15
16     $display("arr : %0p", arr);
17
18 end
19
20
21 /*
22 initial begin
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24     foreach(arr[j]) begin //0---9 //배열요소 반복문
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29 end
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36         arr[i] = i;
37     end
38
39
40     $display("arr : %0p", arr);
41
42
43 end
44 */

```

array.v" 49L, 555C written8,1Top

stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiti...

```
Version 0-2018.09-SP2_Full64 -- Tue Sep 19 00:18:29 2023
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No TimeScale specified
Starting vcs inline pass...
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make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array/csrc'
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o ../simv.daidir/_csrc0.so obj$amc0w_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=../ -Wl,-rpath='$(ORIGIN)/simv.daidir/' -Wl,-rpath=../simv.daidir/ -Wl,-rpath='$(ORIGIN)/simv.daidir/$sim.db.dir' -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib_25836.archive_1.so -prev_archive_1.so _csrc0.so SIM_1.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar.nd.o rmar.llvm.o rmar.llv.m.o_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinate /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs.tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs.pli_stub.o /usr/stone/software/vcs2018/vcs/0-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_0-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array/csrc'

CPU time: .166 seconds to compile + .119 seconds to elab + .206 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
../simv -l simv.log +ntb_random_seed=1
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Compiler version 0-2018.09-SP2_Full64; Runtime version 0-2018.09-SP2_Full64; Sep 19 00:18 2023
arr : {0, 1, 2, 3, 4, 5, 6, 7, 8, 9}
VCD+ writer 0-2018.09-SP2_Full64 copyright (c) 1991-2018 by Synopsys Inc.
VCS Simulation Report

Time: 0
CPU Time: 0.130 seconds; Data structure size: 0.0Mb
Tue Sep 19 00:18:30 2023

```

stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundamentals/1_Fundamentals/4_Loops_repetiion_array\$