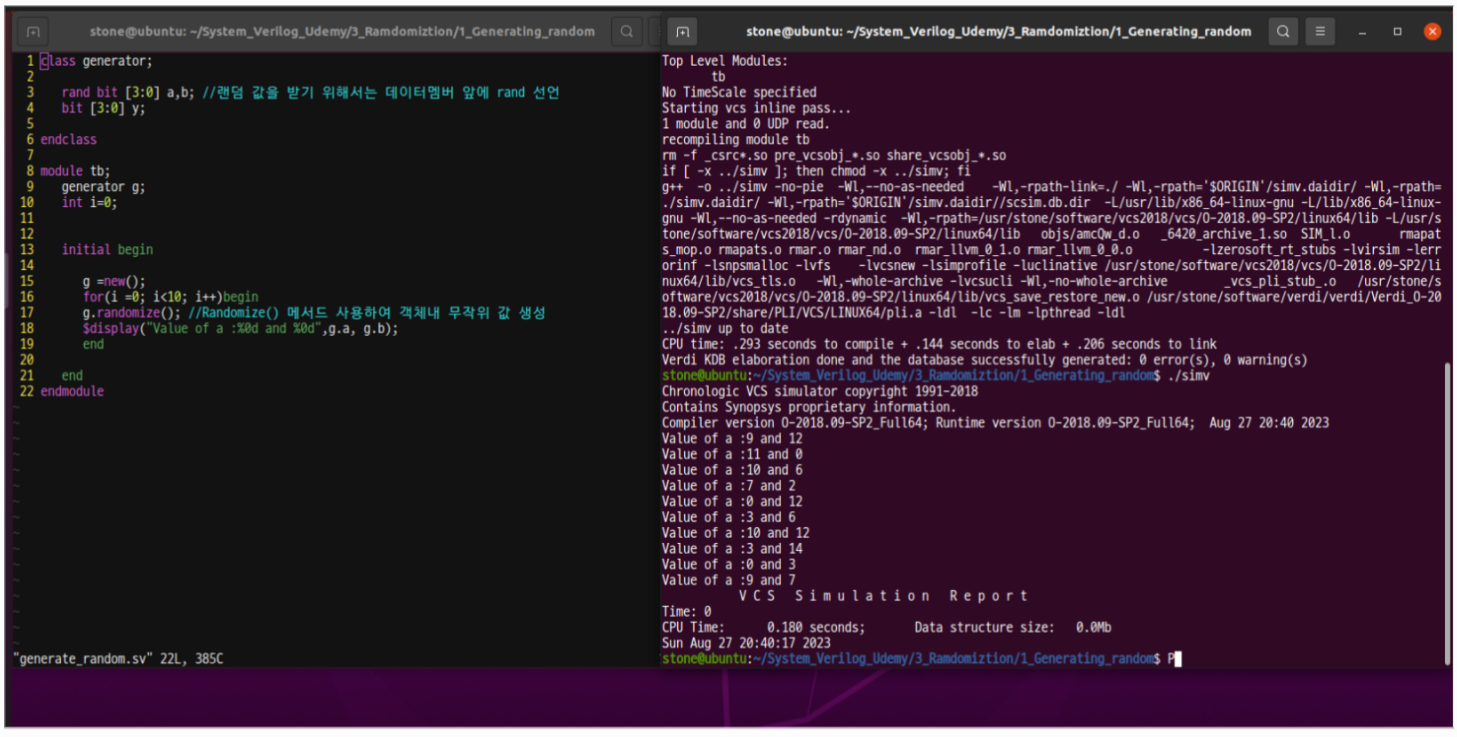
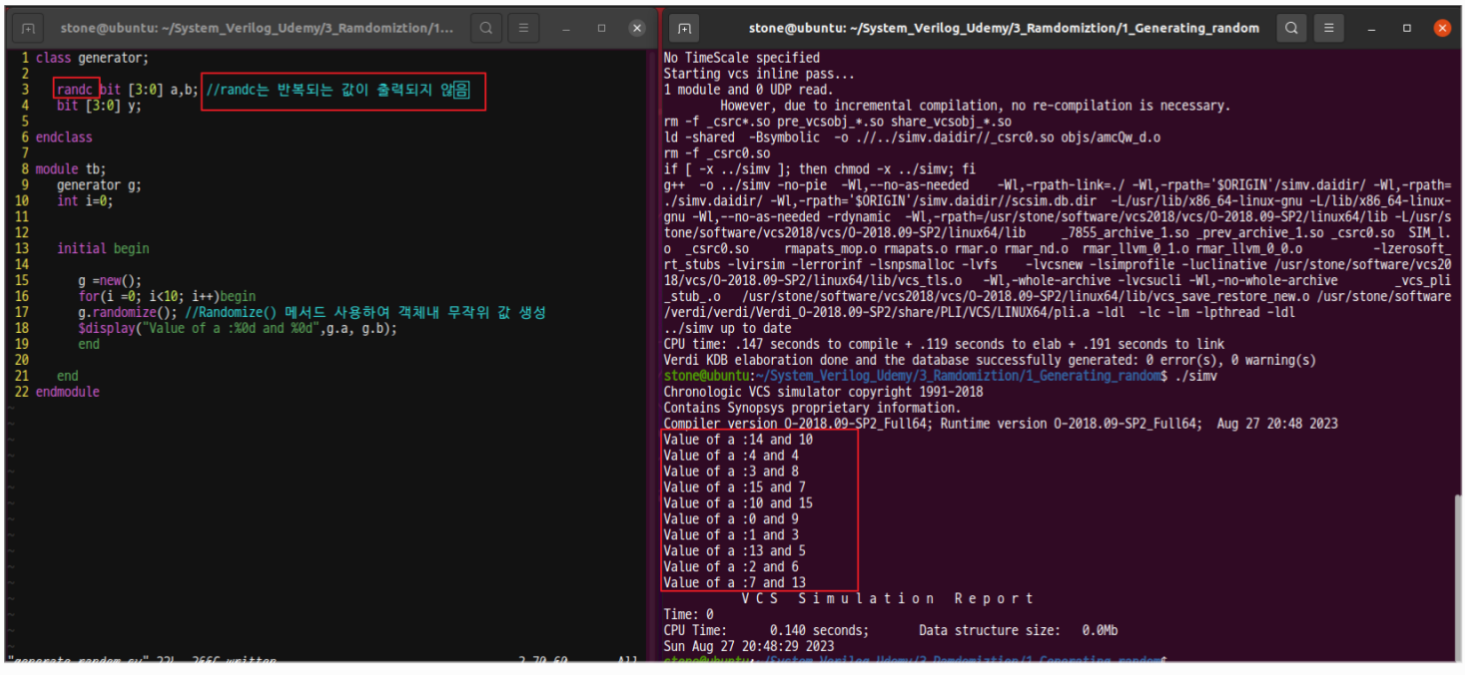

stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/1_Generating_random
1 class generator;
2
3 rand bit [3:0] a,b; //랜덤 값을 받기 위해서는 데이터멤버 앞에 rand 선언
4 bit [3:0] y;
5
6 endclass
7
8 module tb;
9 generator g;
10 int i=0;
11
12
13 initial begin
14
15 g =new();
16 for(i =0; i<10; i++)begin
17 g.randomize(); //Randomize() 메서드 사용하여 객체내 무작위 값 생성
18 $display("Value of a :%0d and %0d",g.a, g.b);
19 end
20
21 end
22 endmodule
"generate_random.sv" 22L, 385C
stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/1_Generating_random
Top Level Modules:
tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib objs/amcQw_d.o _6420_archive_1.so SIM_l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .293 seconds to compile + .144 seconds to elab + .206 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/1_Generating_random$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 27 20:40 2023
Value of a :9 and 12
Value of a :11 and 0
Value of a :10 and 6
Value of a :7 and 2
Value of a :0 and 12
Value of a :3 and 6
Value of a :10 and 12
Value of a :3 and 14
Value of a :0 and 3
Value of a :9 and 7
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.180 seconds; Data structure size: 0.0Mb
Sun Aug 27 20:40:17 2023
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/1_Generating_random$


stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/1...
1 class generator;
2
3 randc bit [3:0] a,b; //randc는 반복되는 값이 출력되지 않음
4 bit [3:0] y;
5
6 endclass
7
8 module tb;
9 generator g;
10 int i=0;
11
12
13 initial begin
14
15 g =new();
16 for(i =0; i<10; i++)begin
17 g.randomize(); //Randomize() 메서드 사용하여 객체내 무작위 값 생성
18 $display("Value of a :%0d and %0d",g.a, g.b);
19 end
20
21 end
22 endmodule
stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/1_Generating_random
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
However, due to incremental compilation, no re-compilation is necessary.
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _7855_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .147 seconds to compile + .119 seconds to elab + .191 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/1_Generating_random$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Aug 27 20:48 2023
Value of a :14 and 10
Value of a :4 and 4
Value of a :3 and 8
Value of a :15 and 7
Value of a :10 and 15
Value of a :0 and 9
Value of a :1 and 3
Value of a :13 and 5
Value of a :2 and 6
Value of a :7 and 13
V C S S i m u l a t i o n R e p o r t
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Sun Aug 27 20:48:29 2023