

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/6_Add_generator_pt1
1 //Transaction시 중요사항
2 //1. Generator custom Constructor에 Transaction Constructor를추가
3 //2. Transaction의 Deep Copy를 Generator 와 driver 사이에 전송
4 class transaction;
5     randc bit [3:0] a;
6     randc bit [3:0] b;
7
8     function void display ();
9         $display (" a : %0d b : %0d",a,b);
10    endfunction
11
12    function transaction copy(); //deep copy
13        copy = new();
14        copy.a = this.a;
15        copy.b = this.b;
16    endfunction
17 endclass
18
19
20 class generator;
21     transaction trans;
22     mailbox #(transaction) mbx;
23     int i=0;
24
25     function new(mailbox #(transaction) mbx);
26         this.mbx = mbx;
27         trans = new(); //Mailbox 를 통해서 객체 생성
28     endfunction
29
30     task run();
31         for (i=0; i<20; i++) begin
32             trans.randomize();
33             if (trans.randomize) begin
34                 trans.display();
35                 mbx.put(trans.copy); //copy 한 객체들을 mailbox로 전송
36                 $display ("Data sent to driver");
37             end
38             else
39                 $display ("Randomize Failed");
40             end
41         endtask
42     endclass
43
44 module tb;
45     generator gen;
46     mailbox #(transaction) mbx;
47
48     initial begin
49         mbx = new();
50         gen= new(mbx);
51         gen.run();
52     end
53 endmodule
```

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/6_Add_generator_pt1
a : 13 b : 5
Data sent to driver
a : 7 b : 13
Data sent to driver
a : 6 b : 0
Data sent to driver
a : 11 b : 14
Data sent to driver
a : 9 b : 2
Data sent to driver
a : 4 b : 0
Data sent to driver
a : 6 b : 4
Data sent to driver
a : 13 b : 3
Data sent to driver
a : 14 b : 6
Data sent to driver
a : 9 b : 2
Data sent to driver
a : 10 b : 12
Data sent to driver
a : 7 b : 10
Data sent to driver
a : 8 b : 13
Data sent to driver
a : 14 b : 2
Data sent to driver
a : 8 b : 1
Data sent to driver
a : 11 b : 8
Data sent to driver
a : 13 b : 14
Data sent to driver
VCS Simulation Report
Time: 0
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Tue Sep 12 04:23:12 2023
stone@ubuntu:~/System_Verilog_Study/5_Interface/6_Add_generator_pt1$
```