```
class generator;

  randc bit [3:0] a,b;
  bit [3:0] y;

  int min;
  int max;

  function new(input int min_val, input int max_val); //pre-randomize
    this.min = min_val;
    this.max = max_val;
  endfunction

  constraint data {
    a inside {[min:max]};
    b inside {[min:max]};
  }

  function void post_randomize(); //post-randomize
    $display("Value of a :%0d and b: %0d", a,b);
  endfunction



endclass


module tb;

  int i =0;
  generator g;

  initial begin
    g = new(3,8); //객체생성시 인수 값전달

    for(i = 0; i<10;i++)begin
      g.randomize();
      #10;
    end
```

```
Parsing design file 'Pre_Post_Randomization.sv'
Top Level Modules:
       tb
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared  -Bsymbolic  -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.dai
dir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_6
4-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic  -Wl,-rpath=/usr/stone/softwar
e/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64
/lib     _15822_archive_1.so _prev_archive_1.so _csrc0.so  SIM_l.o  _csrc0.so     rmapats_mop.o
 rmapats.o rmar.o rmar_nd.o  rmar_llvm_0_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvir
sim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs
2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archi
ve        _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save
_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a
-ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .147 seconds to compile + .117 seconds to elab + .195 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/6_Pre_Post_Randomization$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  4 02:57 2023
Value of a :8 and b: 7
Value of a :3 and b: 6
Value of a :6 and b: 5
Value of a :7 and b: 3
Value of a :5 and b: 4
Value of a :4 and b: 8
Value of a :7 and b: 7
Value of a :8 and b: 4
Value of a :3 and b: 5
Value of a :6 and b: 8
```