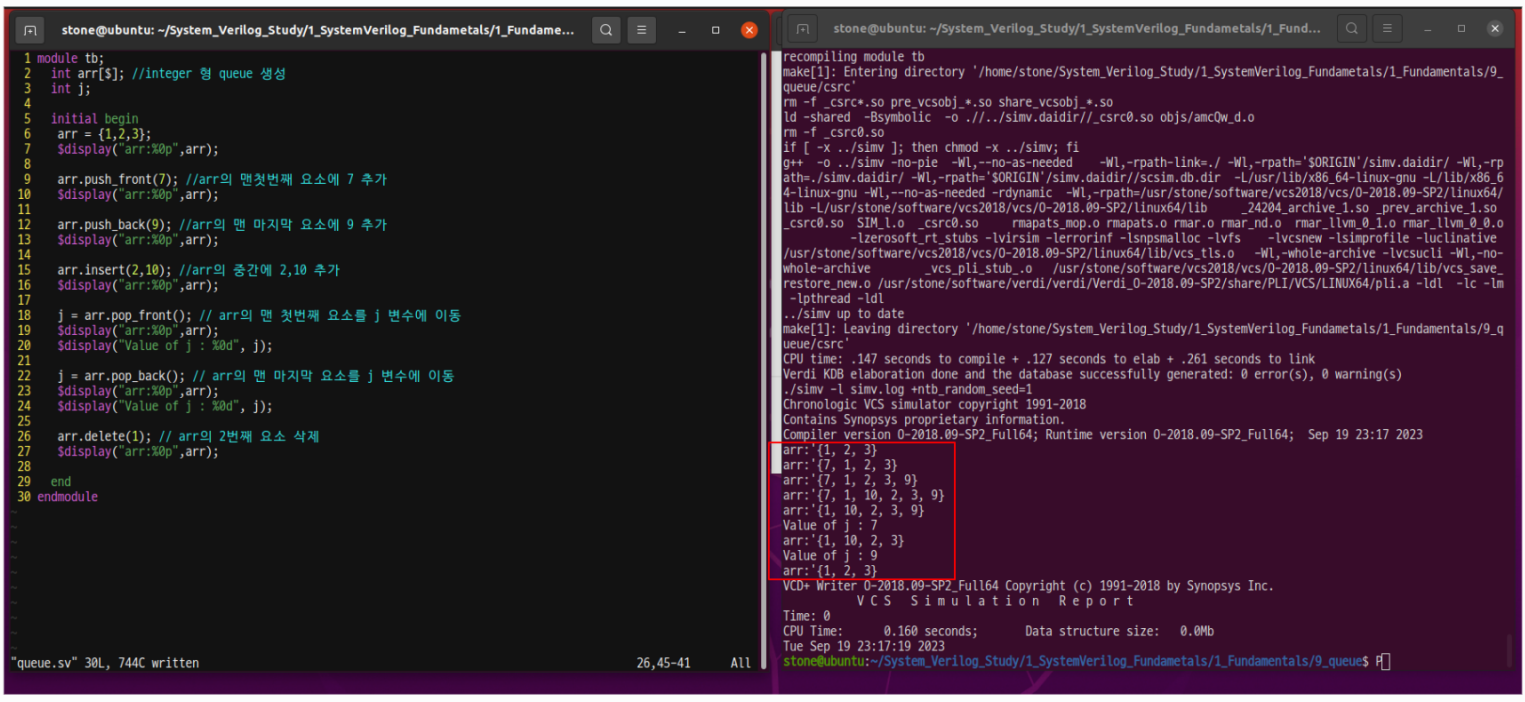
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundame...
1 module tb;
2 int arr[$]; //integer 형 queue 생성
3 int j;
4
5 initial begin
6 arr = {1,2,3};
7 $display("arr:%0p",arr);
8
9 arr.push_front(7); //arr의 맨첫번째 요소에 7 추가
10 $display("arr:%0p",arr);
11
12 arr.push_back(9); //arr의 맨 마지막 요소에 9 추가
13 $display("arr:%0p",arr);
14
15 arr.insert(2,10); //arr의 중간에 2,10 추가
16 $display("arr:%0p",arr);
17
18 j = arr.pop_front(); // arr의 맨 첫번째 요소를 j 변수에 이동
19 $display("arr:%0p",arr);
20 $display("Value of j : %0d", j);
21
22 j = arr.pop_back(); // arr의 맨 마지막 요소를 j 변수에 이동
23 $display("arr:%0p",arr);
24 $display("Value of j : %0d", j);
25
26 arr.delete(1); // arr의 2번째 요소 삭제
27 $display("arr:%0p",arr);
28
29 end
30 endmodule
"queue.sv" 30L, 744C written
26,45-41 All
stone@ubuntu: ~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fund...
recompiling module tb
make[1]: Entering directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/9_queue/csrc'
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -shared -Bsymbolic -o .//../simv.daidir//_csrc0.so objs/amcQw_d.o
rm -f _csrc0.so
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -no-pie -Wl,--no-as-needed -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _24204_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
make[1]: Leaving directory '/home/stone/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/9_queue/csrc'
CPU time: .147 seconds to compile + .127 seconds to elab + .261 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
./simv -l simv.log +ntb_random_seed=1
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 19 23:17 2023
arr:'{1, 2, 3}
arr:'{7, 1, 2, 3}
arr:'{7, 1, 2, 3, 9}
arr:'{7, 1, 10, 2, 3, 9}
arr:'{1, 10, 2, 3, 9}
Value of j : 7
arr:'{1, 10, 2, 3}
Value of j : 9
arr:'{1, 2, 3}
VCD+ Writer O-2018.09-SP2_Full64 Copyright (c) 1991-2018 by Synopsys Inc.
V C S Simulation Report
Time: 0
CPU Time: 0.160 seconds; Data structure size: 0.0Mb
Tue Sep 19 23:17:19 2023
stone@ubuntu:~/System_Verilog_Study/1_SystemVerilog_Fundametals/1_Fundamentals/9_queue$