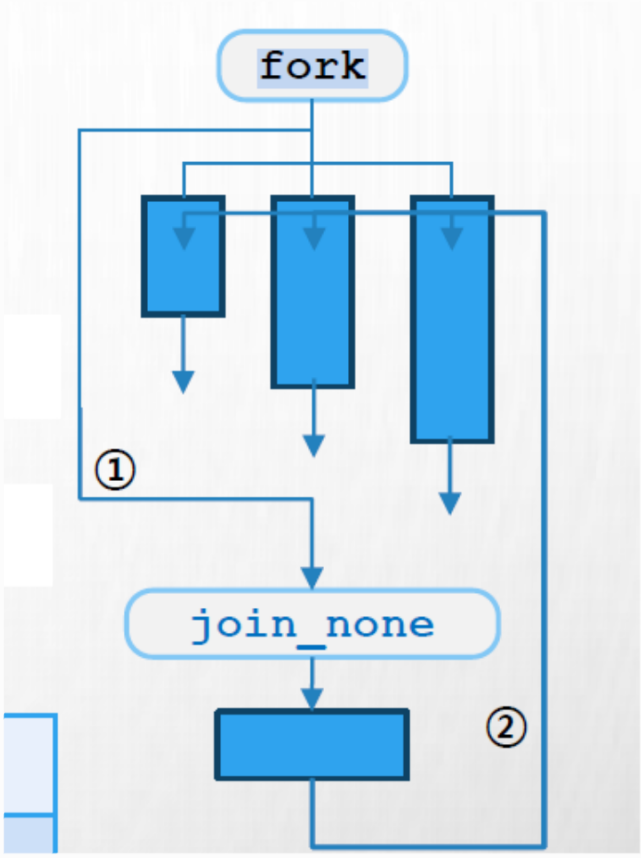
stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/6_fork_join_none

```
module tb;

    task first();
      $display("Task 1 Started at %0t",$time);
    #20;
      $display("Task 1 Completed at %0t",$time);
  endtask



  task second();
    $display("Task 2 Started at %0t",$time);
    #30;
   $display("Task 2 Completed at %0t",$time);
  endtask



  task third();
    $display("Reached next to Join at %0t",$time);
  endtask

 initial begin


  fork

    first();
    second();

  join_none


  third(); //third 가 먼저 실행되고 이후 fork join_none 구문 실행



 end
 endmodule
```

stone@ubuntu: ~/System_Verilog_Udemy/4_IPC/6_fork_join_none

```
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                           ALL RIGHTS RESERVED

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controlling such use and disclosure.

Parsing design file 'fork_join_none.sv'
Top Level Modules:
       tb

No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module tb
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
g++  -o ../simv -no-pie  -Wl,--no-as-needed    -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl,-rpath=./simv.daidi
r/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir  -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -
rdynamic  -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-
SP2/linux64/lib   objs/amcQw_d.o   _42573_archive_1.so  SIM_l.o       rmapats_mop.o rmapats.o rmar.o rmar_nd.o  rmar_llvm_0
_1.o rmar_llvm_0_0.o          -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs    -lvcsnew -lsimprofile -luclinat
ive /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o   -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archiv
e         _vcs_pli_stub_.o   /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/sof
tware/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl  -lc -lm -lpthread -ldl
../simv up to date
CPU time: .139 seconds to compile + .114 seconds to elab + .188 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/4_IPC/6_fork_join_none$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64;  Sep  8 07:03 2023
Reached next to Join at 0
Task 1 Started at 0
Task 2 Started at 0
Task 1 Completed at 20
Task 2 Completed at 30
           V C S   S i m u l a t i o n   R e p o r t
Time: 30
CPU Time:      0.130 seconds;       Data structure size:   0.0Mb
Fri Sep  8 07:03:01 2023
```