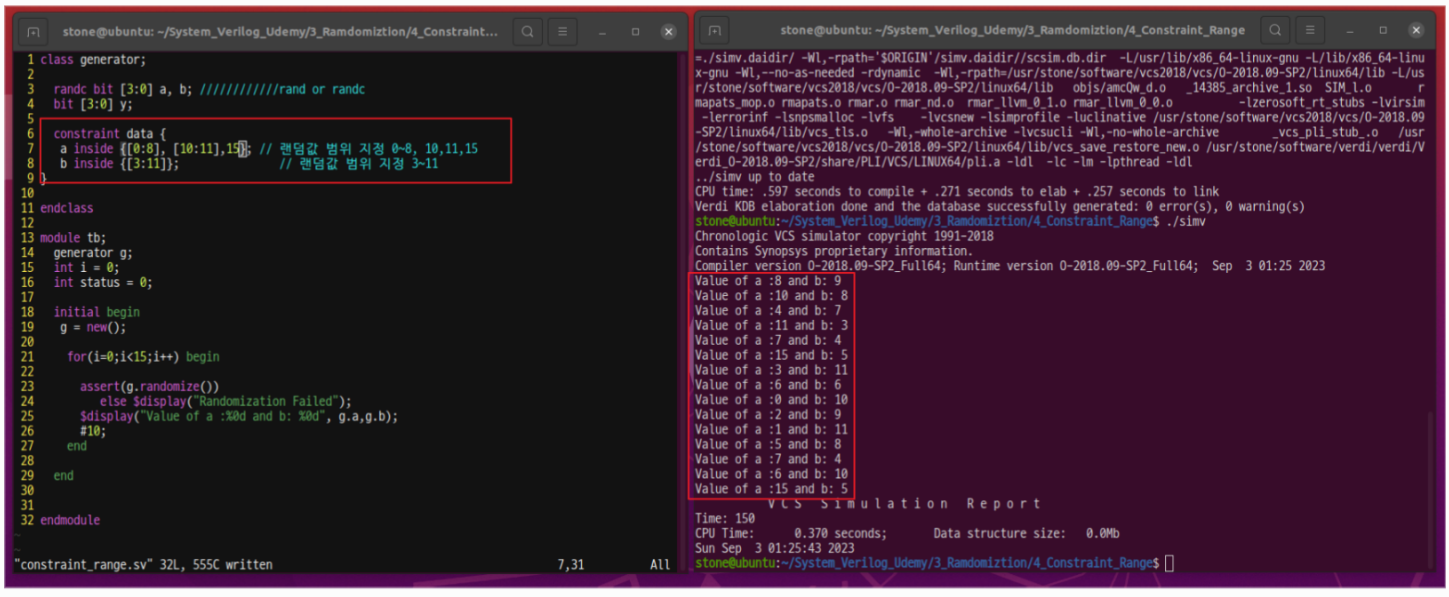
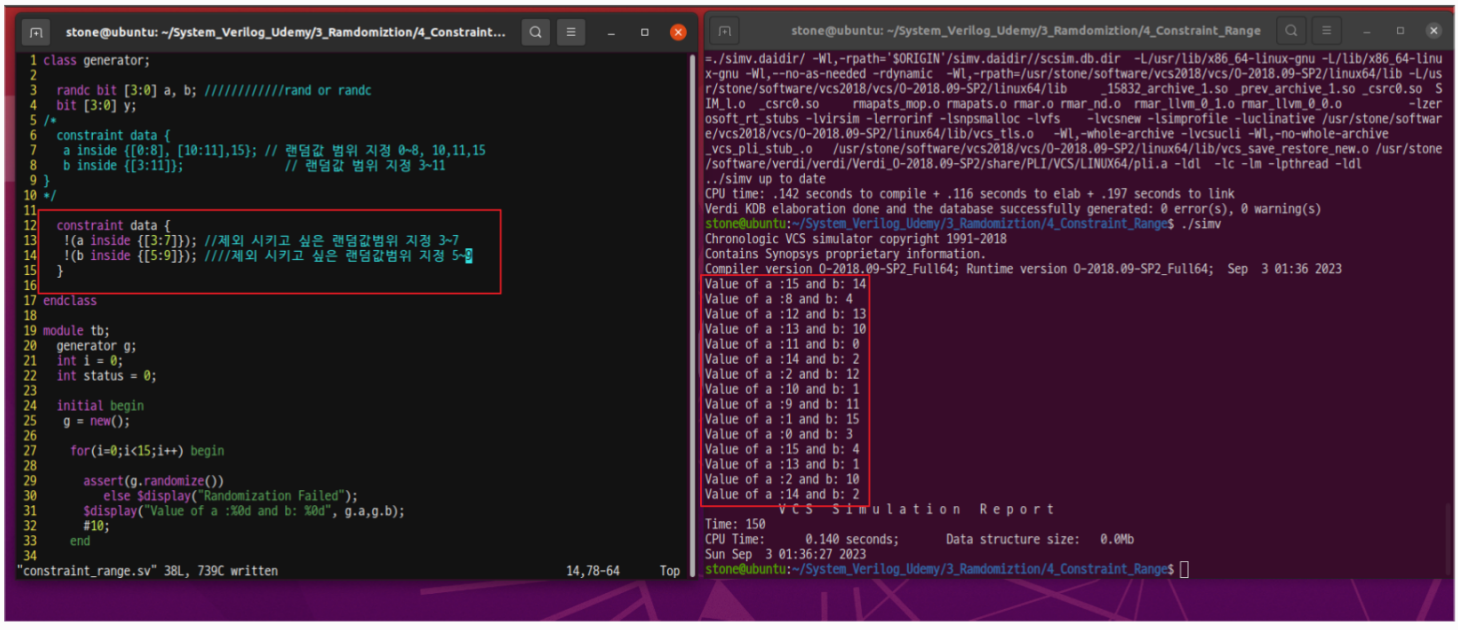

stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint...
1 class generator;
2
3 randc bit [3:0] a, b; ////////////rand or randc
4 bit [3:0] y;
5
6 constraint data {
7 a inside {[0:8], [10:11],15}; // 랜덤값 범위 지정 0~8, 10,11,15
8 b inside {[3:11]}; // 랜덤값 범위 지정 3~11
9 }
10
11 endclass
12
13 module tb;
14 generator g;
15 int i = 0;
16 int status = 0;
17
18 initial begin
19 g = new();
20
21 for(i=0;i<15;i++) begin
22
23 assert(g.randomize())
24 else $display("Randomization Failed");
25 $display("Value of a :%0d and b: %0d", g.a,g.b);
26 #10;
27 end
28
29 end
30
31
32 endmodule
"constraint_range.sv" 32L, 555C written 7,31 All
stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint_Range
=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib objs/amcQw_d.o _14385_archive_1.so SIM_l.o rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .597 seconds to compile + .271 seconds to elab + .257 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint_Range$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 3 01:25 2023
Value of a :8 and b: 9
Value of a :10 and b: 8
Value of a :4 and b: 7
Value of a :11 and b: 3
Value of a :7 and b: 4
Value of a :15 and b: 5
Value of a :3 and b: 11
Value of a :6 and b: 6
Value of a :0 and b: 10
Value of a :2 and b: 9
Value of a :1 and b: 11
Value of a :5 and b: 8
Value of a :7 and b: 4
Value of a :6 and b: 10
Value of a :15 and b: 5
V C S S i m u l a t i o n R e p o r t
Time: 150
CPU Time: 0.370 seconds; Data structure size: 0.0Mb
Sun Sep 3 01:25:43 2023
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint_Range$


stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint...
1 class generator;
2
3 randc bit [3:0] a, b; ////////////rand or randc
4 bit [3:0] y;
5 /*
6 constraint data {
7 a inside {[0:8], [10:11],15}; // 랜덤값 범위 지정 0~8, 10,11,15
8 b inside {[3:11]}; // 랜덤값 범위 지정 3~11
9 }
10 */
11
12 constraint data {
13 !(a inside {[3:7]}); //제외 시키고 싶은 랜덤값범위 지정 3~7
14 !(b inside {[5:9]}); ////제외 시키고 싶은 랜덤값범위 지정 5~9
15 }
16
17 endclass
18
19 module tb;
20 generator g;
21 int i = 0;
22 int status = 0;
23
24 initial begin
25 g = new();
26
27 for(i=0;i<15;i++) begin
28
29 assert(g.randomize())
30 else $display("Randomization Failed");
31 $display("Value of a :%0d and b: %0d", g.a,g.b);
32 #10;
33 end
34
"constraint_range.sv" 38L, 739C written 14,78-64 Top
stone@ubuntu: ~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint_Range
=./simv.daidir/ -Wl,-rpath='$ORIGIN'/simv.daidir//scsim.db.dir -L/usr/lib/x86_64-linux-gnu -L/lib/x86_64-linux-gnu -Wl,--no-as-needed -rdynamic -Wl,-rpath=/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib -L/usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib _15832_archive_1.so _prev_archive_1.so _csrc0.so SIM_l.o _csrc0.so rmapats_mop.o rmapats.o rmar.o rmar_nd.o rmar_llvm_0_1.o rmar_llvm_0_0.o -lzerosoft_rt_stubs -lvirsim -lerrorinf -lsnpsmalloc -lvfs -lvcsnew -lsimprofile -luclinative /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_tls.o -Wl,-whole-archive -lvcsucli -Wl,-no-whole-archive _vcs_pli_stub_.o /usr/stone/software/vcs2018/vcs/O-2018.09-SP2/linux64/lib/vcs_save_restore_new.o /usr/stone/software/verdi/verdi/Verdi_O-2018.09-SP2/share/PLI/VCS/LINUX64/pli.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .142 seconds to compile + .116 seconds to elab + .197 seconds to link
Verdi KDB elaboration done and the database successfully generated: 0 error(s), 0 warning(s)
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint_Range$ ./simv
Chronologic VCS simulator copyright 1991-2018
Contains Synopsys proprietary information.
Compiler version O-2018.09-SP2_Full64; Runtime version O-2018.09-SP2_Full64; Sep 3 01:36 2023
Value of a :15 and b: 14
Value of a :8 and b: 4
Value of a :12 and b: 13
Value of a :13 and b: 10
Value of a :11 and b: 0
Value of a :14 and b: 2
Value of a :2 and b: 12
Value of a :10 and b: 1
Value of a :9 and b: 11
Value of a :1 and b: 15
Value of a :0 and b: 3
Value of a :15 and b: 4
Value of a :13 and b: 1
Value of a :2 and b: 10
Value of a :14 and b: 2
V C S S i m u l a t i o n R e p o r t
Time: 150
CPU Time: 0.140 seconds; Data structure size: 0.0Mb
Sun Sep 3 01:36:27 2023
stone@ubuntu:~/System_Verilog_Udemy/3_Ramdomiztion/4_Constraint_Range$