

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/10_Monitor_Scoreboard
1 interface add_if;
2 logic [3:0] a;
3 logic [3:0] b;
4 logic [4:0] sum;
5 logic clk;
6 endinterface
7
8 class transaction;
9 randc bit [3:0] a;
10 randc bit [3:0] b;
11 bit [4:0] sum;
12
13 function void display();
14 $display("a : %0d, b : %0d, sum: %0d",a,b,sum);
15 endfunction
16 endclass
17
18 class monitor; //DUT에서 들어온 값을 transaction 및 Mailbox에 전송
19 mailbox #(transaction) mbx;
20 transaction trans;
21 virtual add_if aif;
22
23 function new (mailbox #(transaction) mbx);
24 this.mbx = mbx;
25 endfunction
26
27 task run();
28 trans = new();
29 forever begin
30   @(posedge aif.clk); //인터페이스 상송 Edge
31   trans.a = aif.a; //인터페이스로부터 들어 온 값들 transaction 에 저장
32   trans.b = aif.b;
33   trans.sum = aif.sum;
34   $display("Data sent to scoreboard");
35   trans.display();
36   mbx.put(trans); //Mailbox 에 전송
37 end
38 endtask
39 endclass
40
41 class scoreboard; //Monitor로부터 값수신
42 mailbox #(transaction) mbx;
43 transaction trans;
44 monitor mon;
45 function new(mailbox #(transaction) mbx);
46 this.mbx = mbx;
47 endfunction
48
49 task run();
50 forever begin
51   trans = mbx.get(trans);
52   $display("Data Receive From Monitor");
53   trans.display();
54   #70;
55 end
56 endtask
57 endclass
```

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/10_Monitor_Scoreboard
1 module add(
2 input [3:0] a,
3 input [3:0] b,
4 output reg [4:0] sum,
5 input clk
6 );
7
8 always @(posedge clk) begin
9   sum <= a + b;
10 end
11
12 endmodule
```

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/10_Monitor_Scoreboard
a : 0, b: 0, sum: 0
Data Receive From Monitor
a : 0, b: 0, sum: 0
Data sent to scoreboard
a : 1, b: 13, sum: 0
Data Receive From Monitor
a : 1, b: 13, sum: 0
Data sent to scoreboard
a : 14, b: 11, sum: 14
Data Receive From Monitor
a : 14, b: 11, sum: 14
Data sent to scoreboard
a : 1, b: 3, sum: 25
Data Receive From Monitor
a : 1, b: 3, sum: 25
Data sent to scoreboard
a : 9, b: 8, sum: 4
Data Receive From Monitor
a : 9, b: 8, sum: 4
Data sent to scoreboard
a : 3, b: 4, sum: 17
Data Receive From Monitor
a : 3, b: 4, sum: 17
Data sent to scoreboard
a : 7, b: 5, sum: 7
Data Receive From Monitor
a : 7, b: 5, sum: 7
Data sent to scoreboard
a : 0, b: 15, sum: 12
Data Receive From Monitor
a : 0, b: 15, sum: 12
Data sent to scoreboard
a : 14, b: 7, sum: 15
Data Receive From Monitor
```

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/10_Monitor_Scoreboard
56 endtask
57 endclass
58
59 module tb;
60 add_if aif();
61 add_dut (.a(aif.a), .b(aif.b), .sum(aif.sum), .clk(aif.clk));
62 mailbox #(transaction) mbx;
63 scoreboard sco;
64 monitor mon;
65 initial begin
66   aif.clk = 0;
67 end
68
69 always #10 aif.clk = ~aif.clk;
70
71 initial begin
72   for(int i=0; i < 20; i++)begin
73     @(posedge aif.clk);
74     aif.a <= $urandom_range(0,15); //DUT 의 a,b, 포트에 Unsigned 값 0-15 무작위전송
75     aif.b <= $urandom_range(0,15);
76   end
77 end
78
79 initial begin
80   mbx = new();
81   sco = new(sco);
82   mon = new(mon);
83   mon.aif = aif; //테스트bench 인터페이스와 monitor 연결
84 end
85
86 initial begin
87   fork
88     mon.run();
89     sco.run();
90   join
91 end
92
93 initial begin
94   $fsdbDumpvars; //Veril 디버깅 파일 생성
95   #400;
96   $finish();
97 end
98
99 endmodule
```

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/10_Monitor_Scoreboard
1 module add(
2 input [3:0] a,
3 input [3:0] b,
4 output reg [4:0] sum,
5 input clk
6 );
7
8 always @(posedge clk) begin
9   sum <= a + b;
10 end
11
12 endmodule
```

```
stone@ubuntu: ~/System_Verilog_Study/5_Interface/10_Monitor_Scoreboard
a : 11, b: 7, sum: 9
Data Receive From Monitor
a : 11, b: 7, sum: 9
Data sent to scoreboard
a : 1, b: 5, sum: 18
Data Receive From Monitor
a : 1, b: 5, sum: 18
Data sent to scoreboard
a : 6, b: 0, sum: 6
Data Receive From Monitor
a : 6, b: 0, sum: 6
Data sent to scoreboard
a : 1, b: 2, sum: 6
Data Receive From Monitor
a : 1, b: 2, sum: 6
Data sent to scoreboard
a : 8, b: 12, sum: 3
Data Receive From Monitor
a : 8, b: 12, sum: 3
Data sent to scoreboard
a : 7, b: 9, sum: 20
Data Receive From Monitor
a : 7, b: 9, sum: 20
Data sent to scoreboard
a : 12, b: 12, sum: 16
Data Receive From Monitor
a : 12, b: 12, sum: 16
Data sent to scoreboard
a : 8, b: 7, sum: 24
Data Receive From Monitor
a : 8, b: 7, sum: 24
Data sent to scoreboard
a : 7, b: 15, sum: 15
Data Receive From Monitor
```