Opcode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
NOP	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0x0000 R0 0x
ADD	0	0	0	1	Rd			X	X	X	Rs1			Rs2			0x1
SUB	0	0	1	0	Rd			X	X	X	Rs1			Rs2			0x2
MUL	0	0	1	1	Rd			X	X	X	Rs1			Rs2			0x3
DIV	0	1	0	0	Rd			X	X	X	Rs1			Rs2			0x4
AND	0	1	0	1	Rd			X	X	X	Rs1			Rs2			0x5
OR	0	1	1	0	Rd			X	X	X	Rs1			Rs2			0x6
NOT	0	1	1	1	Rd			X	X	X	Rs1		X	X	X		0x7
MV	1	0	0	0	Rd						Immediate[8:0]						0x8
LW	1	0	0	1	Rd			X	X	X	Rs		X	X	X		0x9
SW	1	0	1	0	Rd			X	X	X	Rs		X	X	X		0xA
BZ	1	0	1	1	Imm [8:3]						Rs		Imm [2:0]				0xB
BNZ	1	1	0	0	Imm [8:3]						Rs		Imm [2:0]				0xC
JMP	1	1	0	1	Immediate [11:0]												0xD

Memory Address	Instruction	Opcode	Rd	Rs1/Immediate	Rs2	Instruction from Announcment
0x0002	0x8E0A	MV	R7	d10		
0X0004	0x8D08	MV	R6	d8		
0x0006	0x8C02	MV	R5	d2		
0x0008	0x8020	MV	R0	0x20		
0x000A	0x8300	MV	R1	0x100		
0x000C	0x8402	MV	R2	0x002		
0x000E	0x8800	MV	R4	0x000		
0x0010	0x3001	MUL	R0	R0	R1	
0x0012	0xA038	SW	R0	R7		Load [12], 10
0x0014	0x1002	ADD	R0	R0	R2	
0x0016	0xA028	SW	R0	R6		Load [13], 8
0x0018	0x1002	ADD	R0	R0	R2	
0x001A	0xA026	SW	R0	R5		Load [14], 2
0x001C	0x1604	ADD	R3	R0	R4	
0x001E	0x8201	MV	R1	0x001		
0x0020		LOOP				
0x0022	0x2E39	SUB	R7	R7	R1	DEC RC
0x0024	0x1DE5	ADD	R6	R6	R5	ADD RA RB
0x0026	0xC1EE	BNZ	R7	LOOP		JNZ Loop
0x0028	0x9D28	LW	R6	R3		SW [14], RA