# Placekiq™

RF Transceiver • Low SWaP

## HARDWARE USER MANUAL

V1.0 - NOVEMBER 10, 2020

# CHANGELOG

| Revision | Date | Description | Author |
|---|---|---|---|
| 0.2 | 2014-06-16 | Initial version | Barry L |
| 0.3 | 2016-02-04 | Changing NAV engine in uBlox module | Barry L |
| 0.4 | 2019-02-11 | Updated to reflect changes in firmware version 2.0: Deprecated read/write of DACENABLE parameter; user REFSEL for all options. Added STORE command. Updated URLs | Barry L |
| 0.5 | 2019-08-12 | Updated sections 8.6 and 8.7, added section 12 | Barry L |
| 0.6 | 2019-10-03 | Updated section 12, added section 13 | Barry L |
| 1.0 | 2020-11-10 | Format conversion and cleanup | Barry L |

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# INTRODUCTION

This document provides an overview of Epiq Solutions' Placekiq [2], a MiniPCIe card with a uBlox® LEA-6T GPS module, four 40MHz reference outputs, four PPS outputs and a USB interfaces to a host. The following topics will be discussed:

- Overview of the Placekiq hardware interfaces
- Placekiq usage/integration options

All documentation and support for Placekiq is provided through Epiq Solutions' support website [2], which can be found at:

https://www.epiqsolutions.com/support

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

# LEGAL CONSIDERATIONS

**The Placekiq is distributed all over the world. Each country has its own laws governing reception and transmission of radio frequencies. The user of the Placekiq and associated software is solely responsible for ensuring that it is used in a manner consistent with the laws of the jurisdiction in which it is used.**

# PROPER CARE AND HANDLING

The Placekiq unit is fully tested by Epiq Solutions before shipment, and is guaranteed functional at the time it is received by the customer, and ONLY AT THAT TIME. Improper use of the Placekiq unit can cause it to become non-functional. In particular, a list of actions that may cause damage to the hardware include the following:

- Handling the unit without proper static precautions (ESD protection) when the housing is removed or opened up
- Inserting or removing Placekiq from a host system when power is applied to the host system
- Connecting a transmitter to the GPS_IN port without proper attenuation – A max input of -10 dBm is recommended

The above list is not comprehensive, and experience with the appropriate measures for handling electronic devices is required.

# INTRODUCTION

This guide provides an overview of the Placekiq hardware platform, associated capabilities, and basic usage. This includes the following:

- System level block diagram of the platform
- Overview of the externally accessible hardware ports
- Powering the system up and down

All documentation and support for Placekiq is provided through Epiq Solutions' support website [8], which can be found at:

https://www.epiqsolutions.com/support

Please note that it is necessary to register prior to accessing the relevant information for your purchase.

# REFERENCES


1. Placekiq Product Page

   https://epiqsolutions.com/rf-transceiver/sidekiq/#placekiq

2. Epiq Solutions Support Page

   https://support.epiqsolutions.com

3. uBlox LEA-6T Data Sheet

   http://www.u-blox.com/images/downloads/Product*Docs/LEA-6*DataSheet_%28GPS.G6-HW-09004%29.pdf

4. uBlox Receiver Description Protocol Specification

   http://www.u-blox.com/images/downloads/Product*Docs/u-blox6*ReceiverDescriptionProtocolSpec_%28GPS.G6-SW-10018%29.pdf

5. ADF4002 Data Sheet

   http://www.analog.com/static/imported-files/data_sheets/ADF4002.pdf

# TERMS AND DEFINITIONS

| Term | Definition |
|---|---|
| U.FL | Miniature RF connector manufactured by Hirose |
| W.FL | Micro-Miniature RF connector manufactured by Hirose |
| dB | Decibel |
| ESD | ElectroStatic Discharge |
| PPS | Pulse Per Second |
| GPS | Global Positioning System |
| UART | Universal Asynchronous Receiver Transmitter |
| MHz | Megahertz |
| LED | Light Emitting Diode |
| MHz | Megahertz |
| PC | Personal Computer |
| RF | Radio Frequency |
| RX | Receive |
| TX | Transmit |
| SDR | Software Defined Radio |
| NMEA | National Marine Electronics Association |
| DAC | Digital to Analog Converter |
| PLL | Phase-locked Loop |
| TCVCXO | Temperature compensated voltage controlled crystal oscillator |

# SYSTEM OVERVIEW

Placekiq is a GPS receiver and GPS disciplined 40 MHz reference oscillator a MiniPCIe form factor. It is ideally suited to provide the references for up to four Sidekiq SDR cards. The features of the platform include the following:

- NMEA sentences providing GPS location and heading information
- Four GPS disciplined 40 MHz signals
- Four GPS locked PPS signals
- Support for locking 40 MHz signals to an externally provided 10 MHz reference
- Support for tuning the 40 MHz oscillator with on-board DAC
- Support for using an external PPS to drive the four PPS signals
- Dimensions: 30mm x 51mm x 5mm
- Weight: 6 grams
- Power: <0.4 W

A block diagram of Placekiq is shown in Figure 1

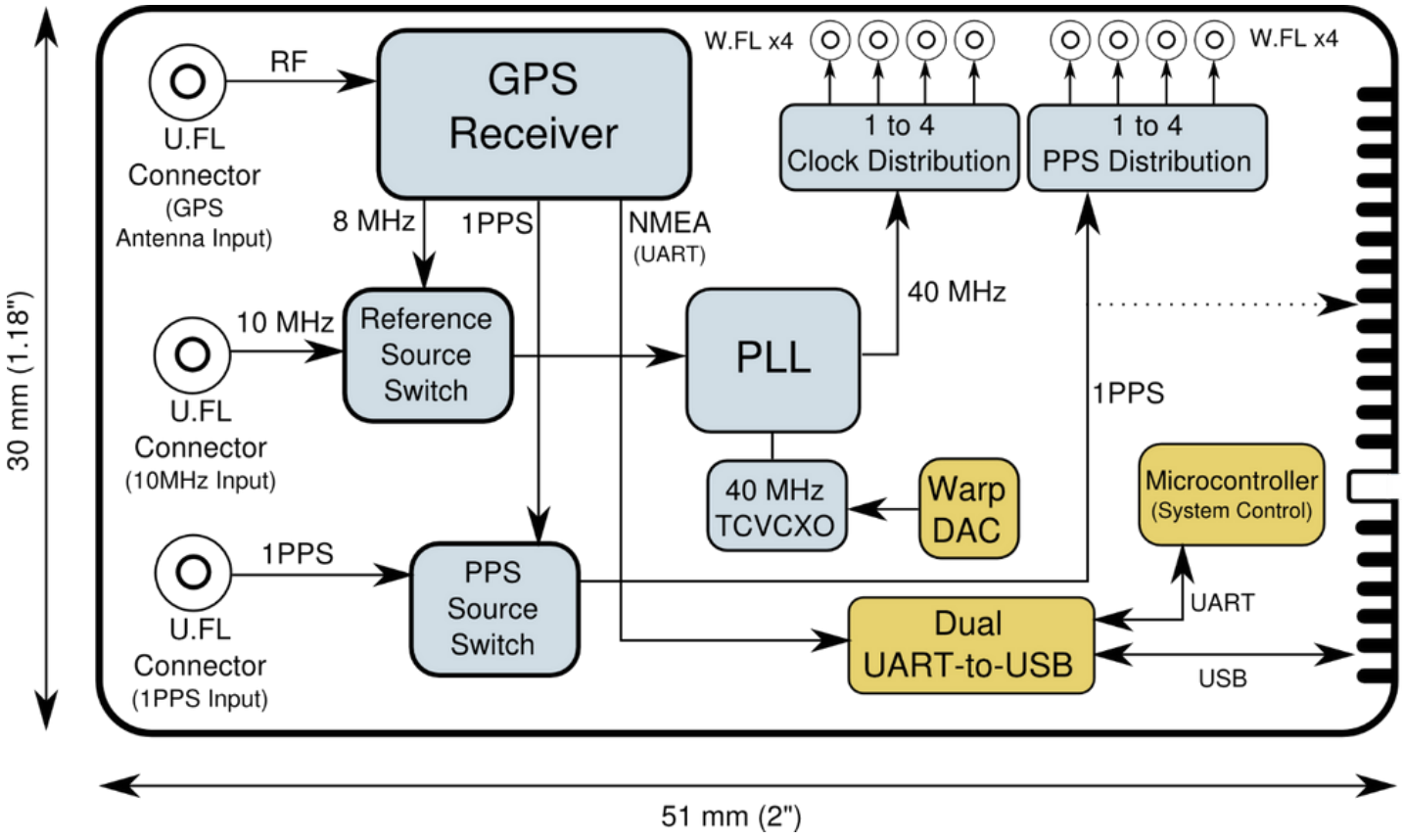


***Figure 1:*** *Block Diagram of the Placekiq MiniPCIe card*

# HARDWARE INTERFACES

Placekiq provides a variety of different hardware interfaces for use by an end user. Each of these hardware interfaces is shown in Figure 2, and defined below.

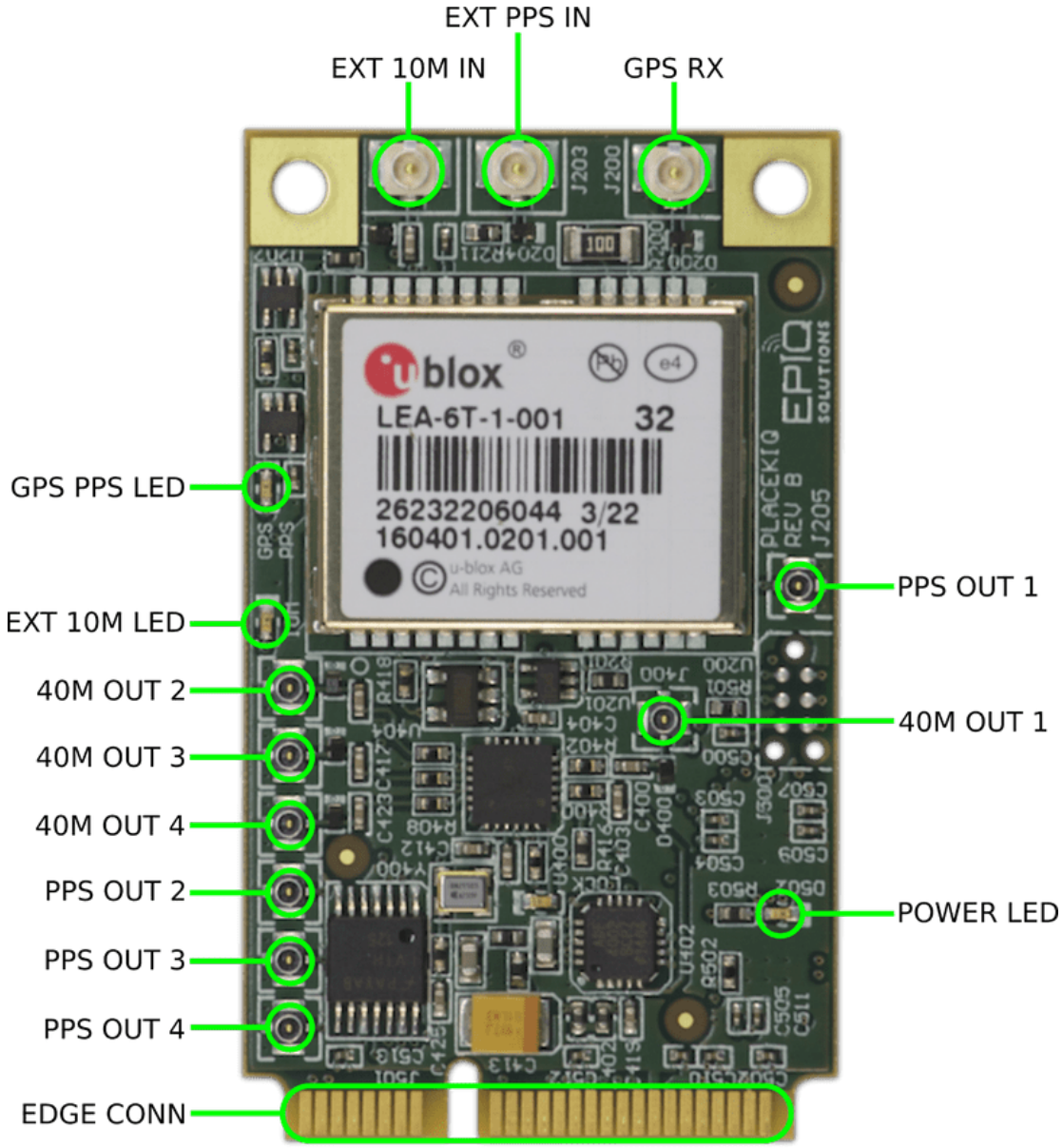


***Figure 2:*** *External Hardware Interfaces to Placekiq*

## GPS RX (J200)

The GPS RX interface is a U.FL jack connector that provides the RF input path to the GPS receiver on Placekiq. There is a 3.3V nominal bias on the center conductor of J200 to provide power to an active GPS antenna, however passive antennas will work as well. In the case of an electrical short to ground at the antenna, the GPS module will detect this and remove the bias. It then periodically attempts to re-establish the antenna power supply. Shorting the antenna will not cause damage to the device.

## EXT PPS IN (J203)

The External 1PPS input interface is a U.FL jack connector that allows for user to provide an external 1PPS signal to drive the four PPS outputs on Placekiq. This input expects 0V to 3.3V logic (Vin_high min = 2.3V, Vin_low max = 1V), but is tolerant of signals up to 5.5V.

## EXT 10M IN (J300)

The External 10 MHz input interface is a U.FL jack connector that allows for users to provide their own 10 MHz reference to the on-board 40 MHz phase-locked loop. The nominal input power to this interface is 0dBm into 50 Ohms, however, the PLL will typically lock to signals as low as -6dBm. There is an LED indicator which will illuminate when there is sufficient power at this interface (see below).

## GPS PPS LED (D201)

The GPS PPS LED will illuminate while there is a logic high on the GPS PPS output. This LED will be constantly illuminated when there is no GPS lock. Once a GPS lock is obtained, the GPS PPS LED will blink once per second at 50% duty cycle along with the GPS PPS signal.

## EXT 10M LED (D302)

The External 10 MHz Present LED illuminates when there is a 10 MHz signal greater than approximately -6dBm present at the External 10 MHz input connector (J300). The status of this LED can also be queried via the Control Interface.

## OUT 1-4 40M (J400, J401, J402, J403)

The 40 MHz Output W.FL jack connectors provide the 40 MHz signal from the on-board PLL. The power level at each of these connectors is 0dBm +/- 2dB. This signal can either be: a) GPS disciplined, b) locked to a user-provide external 10 MHz refernce or c) free running DAC warpable. The default reference for the 40 MHz PLL is the GPS module; however this is software selectable via the Control Interface.

## PPS OUT 1-4 (J201, J202, J204, J205)

The PPS Output W.FL jack connectors provide a 1 PPS signal toggling between 0V and 3.3V. When driven from the on-board GPS module locked GPS, the PPS signal at these connectors is locked to GPS. These signals can also be driven from the External 1PPS Input. The default driving source for these inputs is the on-board GPS modules; however this is software selectable via the Control Interface.

## EDGE CONN

The MiniPCIe Edge Connector is used to route various signals between the MiniPCIe host system and the Placekiq card. A complete table enumerating the pins and their usage on Placekiq is shown in Table 2 below.

| Pin # | MiniPCIe Pin Name | Description as used in Placekiq | | Pin # | MiniPCIe Pin Name | Description as used in Placekiq |
|---|---|---|---|---|---|---|
| 1 | WAKE# | Unused (floating) | | 27 | GND | Ground |
| 2 | +3.3Vaux | +3.3V supply | | 28 | 1.5V | Unused (floating) |
| 3 | COEX1 | Unused (floating) | | 29 | GND | Ground |
| 4 | GND | Ground | | 30 | SMB_CLK | SCL to on-board AVR Microcontroller (currently unused) |
| 5 | COEX2 | Unused (floating) | | 31 | PETn0 | Unused (floating) |
| 6 | 1.5V | Unused (floating) | | 32 | SMB_DATA | SDA to on-board AVR Microcontroller (currently unused) |
| 7 | CLKREQ# | Unused (floating) | | 33 | PETp0 | Unused (floating) |
| 8 | UIM_PWR | Unused (floating) | | 34 | GND | Ground |
| 9 | GND | Unused (floating) | | 35 | GND | Ground |
| 10 | UIM_DATA | Unused (floating) | | 36 | USB_D- | USB D- to CP2105 USB to Dual UART IC |
| 11 | REFCLK- | Unused (floating) | | 37 | GND | Ground |
| 12 | UIM_CLK | Unused (floating) | | 38 | USB_D+ | USB D+ to CP2105 USB to Dual UART IC |
| 13 | REFCLK+ | Unused (floating) | | 39 | +3.3Vaux | +3.3V supply |
| 14 | UIM_RESET | Unused (floating) | | 40 | GND | Ground |
| 15 | GND | Unused (floating) | | 41 | +3.3Vaux | +3.3V supply |

| | | | | | | |
|---|---|---|---|---|---|---|
| 16 | UIM_SPU | Unused (floating) | | 42 | LED_WWAN# | Unused (floating) |
| 17 | UIM_IC_DM | Unused (floating) | | 43 | GND | Ground |
| 18 | GND | Ground | | 44 | LED_WLAN# | Unused (floating) |
| 19 | UIM_IC_DP | Unused (floating)O | | 45 | RESERVED4 | Unused (floating) |
| 20 | W_DISABLE1# | Unused (floating) | | 46 | LED_WPAN# | Unused (floating) |
| 21 | GND | Unused (floating) | | 47 | RESERVED3 | Unused (floating) |
| 22 | PERST_ | Unused (floating) | | 48 | 1.5V | Unused (floating) |
| 23 | PERn0 | Unused (floating) | | 49 | RESERVED2 | Resistor selectable PPS signal by removing R206 and placing it at R212 (backside). This action will remove PPS signal at PPS Output 1. Default is unused (floating). |
| 24 | +3.3Vaux | +3.3V supply | | 50 | GND | Ground |
| 25 | PERp0 | Unused (floating) | | 51 | W_DISABLE2# | Unused (floating) |
| 26 | GND | Ground | | 52 | +3.3Vaux | +3.3V supply |

***Table 2:*** *Placekiq MiniPCIe edge connector pinout*

# BASIC USAGE IN A HOST SYSTEM

## HOST SYSTEM COMPATIBILITY

From a hardware perspective, Placekiq is compatible with any host system that provides a standards-compliant MiniPCIe card slot. However, there are several points to note regarding the usage of Placekiq in different host system. The following section provides an overview of these details.

### BIOS COMPATIBILITY

Different host systems enforce different rules regarding which MiniPCIe cards are considered to be compatible with their platform In some cases, such as laptops manufactured by Lenovo [3], the BIOS of the computer will probe the MiniPCIe slots to identify the type/manufacturer of the card installed at power-up. If the detected card is not in a pre-defined “white list” of compatible cards, the host system will not continue booting up. Other laptops, such as those manufactured by Dell, Inc. [4], have no such restrictions. It is recommended that the end user verify whether or not their intended host system imposes any limitations regarding compatible cards. Note: this only applies to internal MiniPCIe cards. Using Placekiq in an external MiniPCIe-to-Expresscard adapter, or an internal MiniPCIe-to-PCIe adapter does not present any issues.

### OPERATING SYSTEM COMPATIBILITY

Linux is the only operating system that is currently supported. Various kernel versions have been tested starting at Linux version 3.0. Placekiq has been tested both in x86-based Linux systems as well as ARM-based Linux systems. Kernel versions prior to 3.0 (i.e., 2.6+) may also be supported. The Placekiq utilizes cp210x driver to present two serial interfaces, one for command and control (typically at /dev/ttyUSB0) and the other for the GPS NMEA stream (typically at /dev/ttyUSB1).

Alternate operating systems, such as Windows, may also be supported in the future. Please contact Epiq Solutions for details.

### SIGNALING INTERFACES

Placekiq is intended to operate in host systems that provide a full-featured MiniPCIe interface, however only the USB interface is required.

## SYSTEM INTERFACE OPTIONS

Placekiq can be interfaced to a host system through different electrical/physical interfaces. The following sections provide details of several potential options. *Note: Placekiq should never be inserted into or removed from a host system with power applied to the host system. This could permanently damage the card. The one exception to this is when using Placekiq with an Expresscard adapter.*

### MINIPCIE SLOT

The most common method for interfacing Placekiq to a host system, such as a laptop or an embedded single board computer, is through a built-in MiniPCIe slot in the host system. This provides the most compact interfacing option from a size perspective, though may require some level of dis-assembly of the host system to access the card slot. Typical MiniPCIe slots provide both a x1 PCIe interface as well as a USB 2.0 high speed interface. Placekiq uses only the USB interface. Consult the host system documentation to confirm the available signaling options.

### EXPRESSCARD SLOT

Many laptops provide an external Expresscard [5] slot to allow a user to interface peripherals to their host system. Standards-compliant Expresscard slots provide both a x1 PCIe interface as well as a USB 2.0 high speed interface to the host. Placekiq can be used with an Expresscard-to-MiniPCIe adapter, and thus supports the typical hot-swap facility provided by Expresscard slots.

## PROPER DETECTION OF PLACEKIQ IN A HOST SYSTEM

A properly configured Linux host system (with the necessary cp210x driver installed) will allow Placekiq to enumerate on the USB bus and present two serial port interfaces. The enumeration on the USB bus can be verified by executing the command *“lsusb”* to confirm the presence of Placekiq. The execution of lsusb will provide a listing of all USB devices currently enumerated in the system, with output similar to the following when Placekiq is detected:

...

Bus 004 Device 001: ID 1d6b:0003 Linux Foundation 3.0 root hub
**Bus 001 Device 003: ID 10c4:ea70 Cygnal Integrated Products, Inc.**
Bus 001 Device 004: ID 1bcf:2895 Sunplus Innovation Technology Inc.

...

Depending on the verbosity level of the USB bus in the kernel, there may be additional messages contained in the kernel log indicating that the cp210x driver successfully attached to the USB ports. Running “dmesg” should produce an output similar to:

```
...

[5.121920] usb 1-1.3: New USB device found, idVendor=10c4, idProduct=ea70
[5.121928] usb 1-1.3: New USB device strings: Mfr=1, Product=2, SerialNumber=5
[5.121931] usb 1-1.3: Product: CP2105 Dual USB to UART Bridge Controller
[5.121935] usb 1-1.3: Manufacturer: Silicon Labs
...
[5.122715] cp210x 1-1.3:1.0: cp210x converter detected
...
[5.627928] usb 1-1.3: cp210x converter now attached to ttyUSB0
[5.628021] usb 1-1.3: cp210x converter now attached to ttyUSB1
...
```

From this point, Placekiq can be configured through the */dev/ttyUSB0* port, and the NMEA stream can be read from the */dev/ttyUSB1* port.

# SERIAL PORT INTERFACES

There are two serial port interfaces to Placekiq—the Control interface and the GPS interface.

## CONTROL INTERFACE

The control interface operates at 9600 baud/8-N-1 (8 data bits, no stop bits, 1 parity bit).

The commands supported are HELP, READ, WRITE, and STORE.

The READ/WRITE commands have the following general structure:

<READ | WRITE> <PARAMETER> <VALUE (if WRITE)>

The STORE command is used to set default values in the EEPROM.

### HELP COMMAND

Sending the help command will produce a list of available commands.

```
> help
ACK
***Placekiq command set:***
read, write, store, help

***Read/Write parameters:***
VERSION (sw version)
ADF4002 (adf4002 regs)
LD (lock detect)
REF (ref detect)
CLKWARP (vcxo tune dac)
PPSSEL (pps select control)
REFSEL (ref select control, 0=GPS,1=Ext,2=DAC)
SERIAL (serial #)
HWREV (hardware revision)
>
```

### READ/WRITE COMMAND PARAMETERS

### VERSION (read)

Queries the firmware version currently loaded on Placekiq.

Example:

```
> READ VERSION
ACK
Placekiq v2.0.0
```

### LD (read)

This commands queries the state of the lock detect in the 40 MHz PLL. Returns 1 if locked, 0 if unlocked.

Example:

```
> READ LD
ACK
1
```

#### REF (read)

Detects the presence of an external 10 MHz reference signal to the 40MHz PLL. Returns 1 if present, 0 otherwise.

Example:

```
> READ REF
ACK
0
>
```

### SERIAL (read)

Returns the serial number of Placekiq.

Example:

```
> READ SERIAL
ACK
45
>
```

### HWREV (read)

Returns the hardware revision of Placekiq.

Example:

```
> READ HWREV
ACK
1
>
```

### REFSEL (read/write)

Sets the clock reference. The reference may be selected as one of two inputs to the 40 MHz PLL, or the onboard DAC may be used to warp a TCVCXO.

The PLL source can either be the GPS disciplined 10 MHz (0) or an external 10 MHz provided at J300 (1). The DAC may be enabled by setting REFSEL as 2, which automatically will disable the

PLL. Similarly, by setting REFSEL to 0 for GPS or 1 for external 10 MHz, the DAC will be disabled.

The default value from the factory for REFSEL is 0. The STORE command may be used to set a different default value.

Read example:

```
> READ REFSEL
ACK
0
>
```

Write example:

```
> WRITE REFSEL 1
ACK
>
```

### PPSSEL (read/write)

Selects the driving source for the four PPS output W.FL connectors. This can either be the GPS module, or an external PPS source provided at J203. Set to 0 for GPS or 1 for external PPS. The default value from the factory for PPSSEL is 0. The STORE command may be used to set a different default value.

Read example:

```
> READ PPSSEL
ACK
0
>
```

Write example:

```
> WRITE PPSSEL 1
ACK
>
```

### DACENABLE (deprecated)

*The DACENABLE command has been deprecated as of firmware version 2.0.0. See the REFSEL parameter.*

### CLKWARP (read/write)

This command controls the 12-bit DAC driving the control voltage pin for the 40MHz TCVCXO. The voltage range of the DAC is 0 to 3V. The tuning sensitivity of the TCVCXO is 100 Hz/V. This means that the DAC provides roughly 73 mHz of tuning resolution over about 200 Hz. However, this tuning sensitivity is only guaranteed between 0.4V (DAC=682) and 2.4V (DAC=3413).

NOTE: if the DAC is not enabled, writing CLKWARP will cache the value written to be applied when the DAC is enabled. If the DAC is enabled, the new value is written immediately to the DAC hardware.

Read example:

```
>READ CLKWARP
ACK
2048
>
```

Write example:

```
> WRITE CLKWARP 2048
ACK
>
```

### ADF4002 (write)

This command is used for configuring the ADF4002 which is the PLL IC that is used for the 40 MHz reference. In most cases, users will simply write the REFSEL parameter to select between using the PLL and the DAC. However it is possible, for example, to write a predefined set of values to either a) tell the PLL to use a 10 MHz reference to produce 40 MHz, or b) disable the PLL in order to use the DAC warping capability. The default configuration is for the ADF4002 to be locked to 10 MHz.

Advanced users can use this interface to configure the PLL IC for a custom configuration. For example, the ADF4002 can be configured to lock to, say, 1, 2, 4 or 8 MHz instead of 10 MHz. For custom configurations refer to the ADF4002 data sheet [8].

Example:

```
> WRITE ADF4002 1F8092
ACK
>
```

### DAC Warping the Clock

In order to use the DAC to warp the clock, the PLL IC must be disabled. Otherwise the PLL will correct the DAC voltage at the TCVCXO control line, making it appear not to work. When using the REFSEL parameter to enable the DAC, the PLL is automatically disabled.

The following commands will the PLL IC and set the DAC to 2048.

```
> WRITE REFSEL 2    // enables the DAC
ACK
>
```

```
> WRITE CLKWARP 2048    // sets the DAC value to mid-range
ACK
>
```

### Reconfiguring the PLL IC to lock to 10 MHz

From the factory, on power up, the PLL IC is already configured to lock to 10 MHz. However, if the user has configured Placekiq to warp the clock with the DAC as shown in the previous section and they want to return to the default configuration without power cycling, the DAC needs to be disabled and the PLL IC registers need to be programmed with the correct values. Use the following commands.

```
> WRITE REFSEL 0    // disables the DAC
ACK
>
```

### STORE COMMAND

The STORE command may be used to modify the default power-up settings. The following parameters are configurable:

| Parameter | Factory Default |
|---|---|
| REFSEL | 0 – GPS Disciplined 10MHz |
| PPSSEL | 0 – GPS Module 1PPS |
| CLKWARP | 2048 |

Table Power-up defaults

Any of the parameters in Table may be modified at runtime so that the STORE command will set new power-up defaults. For example, to configure Placekiq to use an external 10MHz clock source at power-up, without the need to send commands after booting, use the following commands.

```
> WRITE REFSEL 1    // configure external 10MHz references
ACK
>
```

```
> STORE             // write current REFSEL, PPSSEL, and CLKWARP values to EEPROM
ACK
>
```

NOTE: to restore the factory settings, it is necessary to use the WRITE command to set each value to the factory default value, and then issue the STORE command.

## GPS INTERFACE

The GPS interface is a direct serial port to the uBlox LEA-6-T GPS module [8]. NMEA sentences can be seen at this port without any user configuration and this is sufficient for most use-cases.

There are some use cases where a user may need to alter the default configuration of the GPS module. For instance, the default configuration assumes that Placekiq is relatively stationary. If, however, Placekiq is to be used on some mobile platform, the GPS module will need to be set to a different mode in order to provide accurate location and heading information. The manufacturer of the GPS module, uBlox, provides a well-defined communication protocol for this purpose. Users are referred to the uBlox6 Receiver Description Protocol Specification [8] for interacting directly with the uBlox module. However, what follows are a couple examples of some common commands that users would likely need to use to configure the GPS engine.

### GPS NAVIGATION ENGINE SETTINGS

The uBlox module navigation engine can be optimized for timing and lock capabilities depending on the nature of the platform. The default configuration of Placekiq assumes a relatively stationary platform. However, for moving platforms, the navigation engine setting will need to be re-configured. The navigation engine settings are accessed in the CFG-NAV5 register in the uBlox. Refer to page 117 of the uBlox6 Receiver Description Protocol Specification [4], page 1 for a detailed description of each of the dynamic model settings.

| Byte Offset | Name | Type | Value | Description |
|---|---|---|---|---|
| 0 | Mask | 2 Bytes | 0x0001 | Ensures only the dynModel is changed |
| 2 | dynModel | 1 Byte | 0x02 (default) | 0 – Portable<br>2 – Stationary<br>3 – Pedestrian<br>4 – Automotive<br>5 – Sea<br>6 – Airborne <1g Accel<br>7 – Airborne <2g Accel<br>8 – Airborne <4g Accel |
| 3 | Don’t care | Byte | Don’t care | |
| … | … | … | … | |
| 32 | Don’t care | Byte | Don’t care | |

***Table 4:*** *CFG-NAV5 uBlox register*

### SAVE CONFIGURATION TO NON-VOLATILE MEMORY

Any configuration changes made to the uBlox module will not persist after a power cycle, unless the uBlox is commanded to save its configuration into non-volatile memory. This is accomplished by writing to the uBlox CFG-CFG register. The table below shows the values to be written to the CFG-CFG register in order to ensure the current configuration of the uBlox module persists after a power cycle.

| Byte Offset | Name | Type | Value | Description |
|---|---|---|---|---|
| 0 | clearMask | 4 Bytes | 0x00000000 | Mask with configuration sub-sections to clear |
| 4 | saveMask | 4 Bytes | 0x00000018 | Mask with configuration sub-sections to Save |
| 8 | loadMask | 4 Bytes | 0x00000000 | Mask with configuration sub-sections to Load |
| 12 | deviceMask | 1 Byte | 0x12 | Selects the devices for this command |

***Table 5:*** *CFG-CFG settings to save to SPI flash*

# MECHANICAL OUTLINE

A dimensioned mechanical drawing of Placekiq is shown in Figure 4. In addition, a 3D model (in STP format) is also available. Please contact Epiq Solutions for this model.

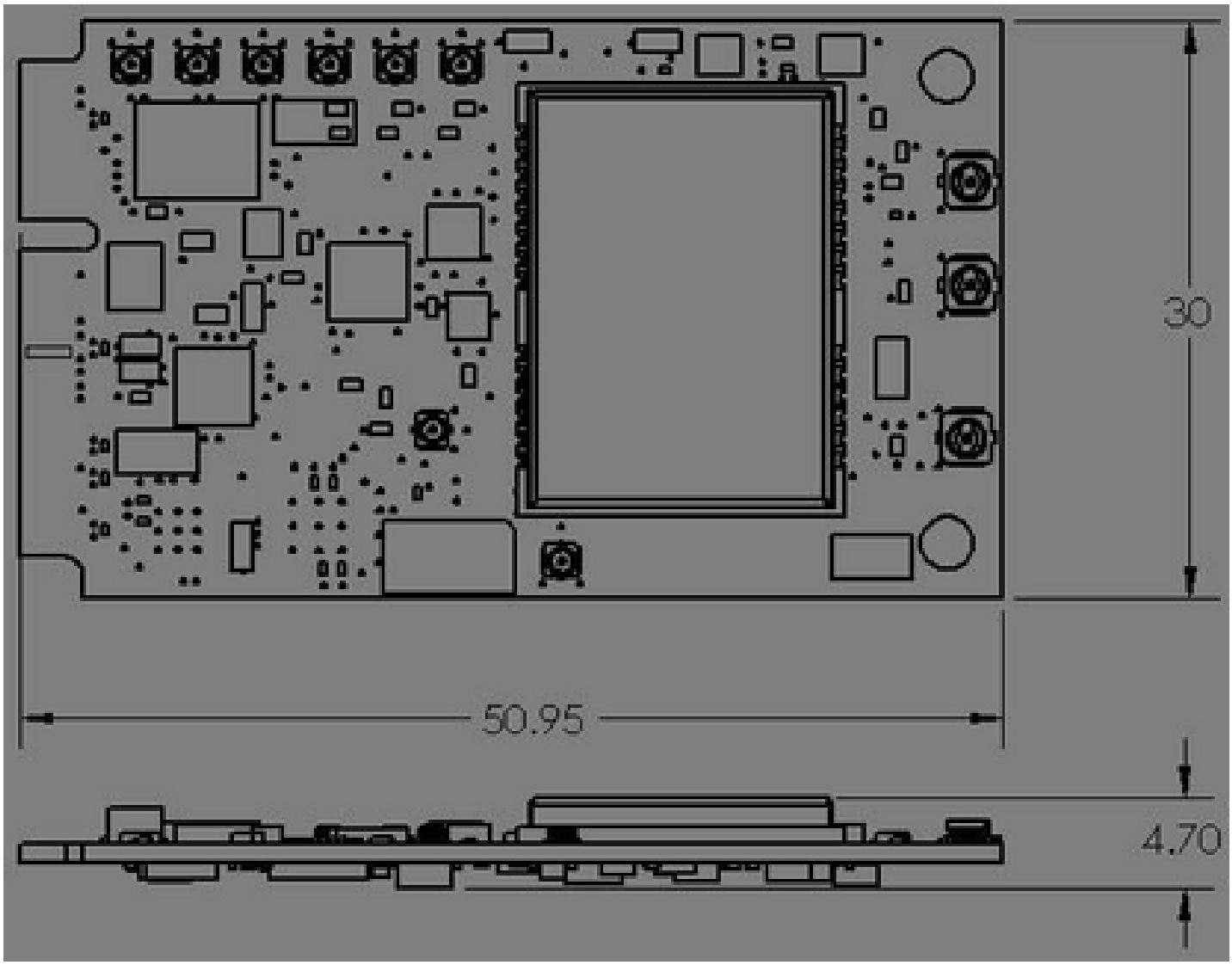


***Figure 3:*** *Mechanical Outline Placekiq MiniPCIe card*

# STATEMENT OF VOLATILITY

| | |
|---|---|
| **Model** | Placekiq |
| **Part Number** | ES010-101 |
| **Manufacturer** | Epiq Solutions |
| **Address** | 3740 Industrial Avenue<br>Rolling Meadows, IL 60008 |
| | |

***Table 6:*** *Model, Part Number, and Manufacturer Info*

| Memory Type | Memory Size | User Modifiable | Purpose | Process to Clear |
|---|---|---|---|---|
| SRAM | 2 KB | No | Microcontroller memory | Power-off |

***Table 7:*** *Placekiq Volatile Memory*

| Memory Type | Memory Size | User Modifiable | Removable | Purpose | Process to Clear |
|---|---|---|---|---|---|
| Flash | 1 Mbit | Yes | No | Holds GPS module firmware and configuration data | Must be returned to factory to be cleared |
| Flash | 32 KB | No | No | Microcontroller firmware | Must be returned to factory to be cleared |
| EEPROM | 16 KB | Yes | No | Contains product information for identifying the device (part#, serial#). Microcontroller configuration data | Product info data is read-only and must be returned to factory to be cleared. Configuration data cleared via usb port interface. |

***Table 8:*** *Placekiq Non-Volatile Memory*

# FAILURE RATE & MTBF

Listed below is the Failure Rate and MTBF for the ES010-101 Placekiq Circuit Card Assembly.

The calculations are derived from Relyence Reliability Software and based off a fixed, ground, controlled operating environment with an ambient temperature of 25°C.

| | |
|---|---|
| **Part Number** | ES010-101 |
| **Description** | Placekiq Circuit Card Assembly |
| **Failure Rate (fpmh)** | 0.086484 |
| **MTBF (hours)** | 11,562,794.52 |
| **Calculation Model** | Telcordia Issue 4 |
| **Operating Environment** | Fixed/Ground/Controlled |
| **Ambient Temperature** | 25°C |

***Table 9:*** *Placekiq Failure Rate & MTBF*