BIRLA INSTITUTE OF TECHNOLOGY & SCIENCE, PILANI

I Semester 2016-2017

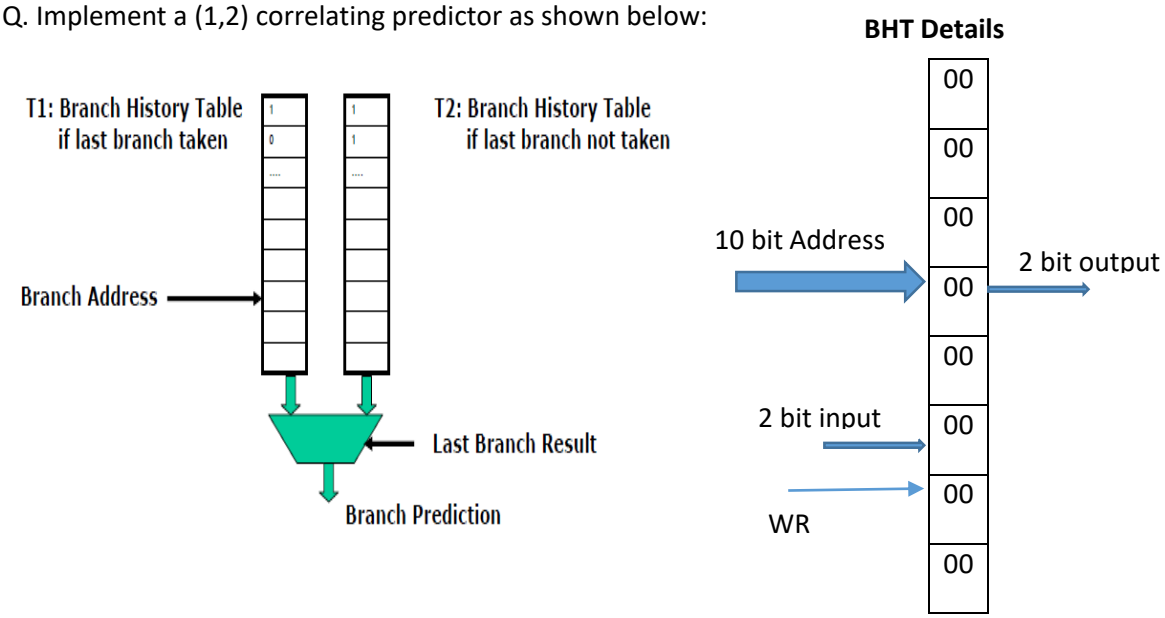
CS F342 Computer Architecture

Lab Exam

Date: 13/11/2016 **TIME: 90 Minutes** **MM: 33**

INSTRUCTIONS: (i) Create a folder on desktop, rename it to your IDNO. (ii) Rename the project with your IDNO (iii) Write your IDNO and name in .v file. *Write all modules in a single .v file.* Put this .v file in the folder you created on desktop.

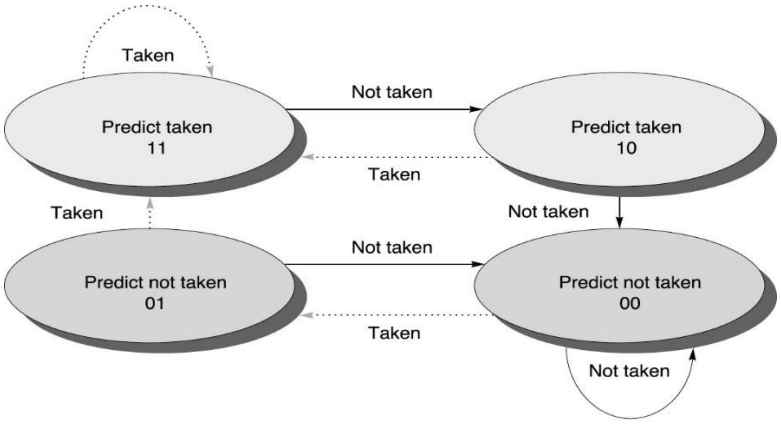
Q. Implement a (1,2) correlating predictor as shown below:



The predictor consists of two Branch History tables. The BHTs have 1K entries each. Each entry in BHTs is of two bits. Implement the above circuit in following modules:

1. **BHT:** This module describes an individual BHT. A BHT has 1024 entries of 2 bit each. BHT is indexed by 10-bit branch address (A9-A0) and has two-bit output (D1-D0). It has two-bit data input (I1-I0) and a write control signal (WR) used to update any 2-bit entry in BHT.
2. **MUX1:** This MUX has two 2-bit inputs and one 2-bit output (O1-O0). It also has a one bit select line (S). The select line of MUX is set based on the actual outcome of previous branch (1 if branch was taken and 0 if branch is not taken).

The two bits of an entry of BHT are modified as shown in the state diagram below:



Assume that ‘Taken’ is represented by binary ‘1’ and ‘Not Taken’ by ‘0’. Write a module named ‘**PREDICTOR**’ to implement the above FSM. The input to this module is the actual branch outcome represented by ‘X’ which determines the state transitions and a two-bit output (corresponding to the state bits (N1-N0). These output bits are used to update the BHT entries.

Write a module ‘**INTG**’ which integrates all above modules into a working circuit.

Write a test bench which shows the prediction made for a branch at address ‘0011110000’ which is executed five times with actual outcomes as NT,T,T,T,NT. Assume all entries of the BHTs are initialized to ‘00’ and the select line of MUX is also initialized to NT (0).