Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Test-1 (20th February 2018)

Duration: 25 minutes **Marks: 5 Marks**

---

1. Design and implement a sequence generator (operates on rising edge of clock and has a synchronous active high reset) to generate a 4-bit grey code (output in two successive clock cycles should differ only in one-bit position) as the output. You can use behavioral modeling style. Also provide a suitable test bench. The Test Bench should cover the following cases
    1. A test case to check if the reset is synchronous or not.
    2. Terminate the sequence in between.
    3. Complete sequence for at-least 3 complete cycles.

******