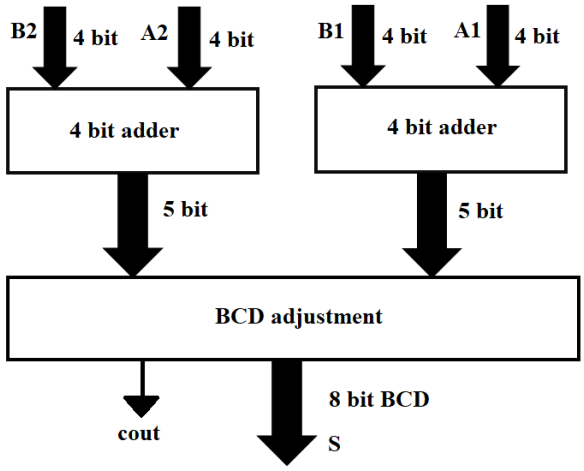
Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Test-2 (27th February 2018)

Duration: 35 minutes **Marks: 5 Marks**

A BCD adder is to be designed to add two digit BCD numbers ***A*** and ***B***. Assume that at any given time the input is a valid BCD number. The sum is a two digit BCD number ***S*** and a 1-bit carry ***cout***.

Implement a BCD adder as per the following architecture.

1. 4-bit adder should be implemented using a single assign statement.
2. BCD adjustment unit should be implemented using data flow modeling.



Implement the following using Verilog HDL. Provide a suitable test bench for the module. Include the following cases in your test bench:

A = 8'h 25, B = 8'h 52
A = 8'h 99, B = 8'h 88
A = 8'h 93, B = 8'h 12

NOTE: When you submit the file make sure that you save it with the name ***bcd_adder_your_first_name.v***

Example: If your name is Rahul Saraswat, name the file as ***bcd_adder_rahul.v*** also include name and ID No. in the first two lines (comment these lines) of your code.

****** End of Paper******