

Dat	e	Expected	Task	Time Spent	Note
	29/09/2019	0:00:00		0:00:00	
	30/09/2019	0:30:00	Meeting	0:30:00	Initial Meeting, explanation of project and initial work
	02/10/2019	2:30:00			
	02/10/2019	-0:30:00	Research	3:00:00	Read Papers over summer
	03/10/2019	0:30:00			
	03/10/2019	-0:30:00	First Submission	1:00:00	Drafted 2 Sections
	04/10/2019	0:30:00			
	04/10/2019	-3:30:00	Required Libraries	4:00:00	Got ParMetis/ PT-Scotch Sources, Intel Compiler, cuda. Need to build still.
	06/10/2019	-1:30:00			
	06/10/2019	-4:00:00	First Submission	2:30:00	Gantt Diagram
	10/10/2019	0:00:00			
	10/10/2019	-3:30:00	First Submission	3:30:00	Draft and submission
	11/10/2019	-2:30:00			
	11/10/2019	-4:30:00	Required Libraries	2:00:00	Build Libraries and OP2
	12/10/2019	-3:30:00			
	12/10/2019	-5:30:00	Research	2:00:00	Reading papers
	14/10/2019	-3:30:00			
	14/10/2019	-6:30:00	Required Libraries	3:00:00	Intel Load Libraries. Matlap eq. Octane to generate meshes. Managed to build and run airfoil_seq, however the numbers don't seem to be correct.
	17/10/2019	-3:30:00			
	17/10/2019	-4:00:00	Meeting	0:30:00	Skype Meeting, covered issues, next steps (rebase)
	23/10/2019	2:00:00			
	23/10/2019	-2:00:00	Familiarity Work	04:00:00	Rebase op2, run seq (test PASSED). run mpi found issues.
	24/10/2019	-1:00:00			
	24/10/2019	-1:30:00	Meeting	0:30:00	Set Timetable for rest of term, resolved issues with Scotch, discussed location for my implementation
	05/11/2019	10:30:00	oanig	0.00.00	
	30 2010	. 0.00.00			cuda tutorial, reading exising translator python
	05/11/2019	6:00:00	Research	4:30:00	
	06/11/2019	7:00:00			

				Created remote git branch, set deadline for progress report draft. Discussed progress. Also discussed code guidelines - git clang
06/11/2019	6:30:00	Meeting	0:30:00	
13/11/2019	13:30:00			
13/11/2019	7:30:00	Implementation	6:00:00	Re-did rebase, fixed conflicts. Fixed Makefile for scotch references, and LD_LIBRARY_PATH for HDF5 .so file
13/11/2019	5:30:00	Research	2:00:00	Determining values and origin of paramters to back-end gen functions.
14/11/2019	6:30:00	, , , , , , , , , , , , , , , , , , , ,		and the second s
14/11/2019	6:00:00	Meeting	0:30:00	
19/11/2019	11:00:00			
19/11/2019	7:30:00	Implementation	3:30:00	Code reading, updated seq_jit with new kernel value initialisation, modified op2.py to call new cuda_jit function
20/11/2019	8:30:00			
20/11/2019	4:30:00	First Submission	4:00:00	Begin Progress report, git cleanup
21/11/2019	5:30:00			
21/11/2019	5:00:00	Meeting	0:30:00	Discuss Progress Report draft
21/11/2019	3:30:00	First Submission	1:30:00	Additions discussed in meeting
21/11/2019	1:30:00	Research	2:00:00	Looked into enqueue_kernel to see how lazy ex is done, also header file creation.
22/11/2019	2:30:00			
22/11/2019	1:45:00	Research	0:45:00	Realised constants are defined by input, understand jit purpose now
22/11/2019	0:00:00	First Submission	1:45:00	Create Flow chart to explain JIT + write explanation
23/11/2019	1:00:00			
23/11/2019	0:00:00	First Submission	1:00:00	Finish Flow chart boxes, wording alterations
27/11/2019	4:00:00			
27/11/2019	1:45:00	Research	2:15:00	Investigate cuda seq generation in existing source, and halo message passing in papers/online. https://www.oerc.ox.ac.uk/sites/default/files/uploads/profile-pages/Gihan/JPDC-OP2.pdf
29/11/2019	3:45:00			
29/11/2019	3:25:00	Meeting	0:20:00	Discussed atomics flag in cuda aot codegen, doesn't change because the choice of codepath is hard coded to not be colouring
03/12/2019	7:25:00	Meeting	0.20.00	now.
03/12/2019	4:25:00	Implementation	3:00:00	Removed seq codegen and copied jit_include and user_function into file. Soa is Struct of Arrays, and can be forced in type declaration, meaning indicies need to include a "stride".
04/12/2019	5:25:00			
				Continued cuda jit codegen into kernel function files (completed), still errors when building with make - may need to look at const
04/12/2019	-1:35:00	Implementation	7:00:00	file generation
05/12/2019	-0:35:00			
05/12/2019	-0:45:00	Meeting	0.10.00	Discussed progress with cuda jit, and benchmarking/next steps
16/01/2020	41:15:00	wieeung	0.10.00	benomial king/next steps
16/01/2020	39:15:00	Implementation	2.00.00	Makefile, fix cuda function call
16/01/2020	38:15:00	Required Libraries		Update cuda driver
20/01/2020	42:15:00	Required Libraties	1.00.00	opuato oudu diivoi
20/01/2020	38:55:00	Implementation	3:20:00	Fixing bugs and small mistakes, investigate const for cuda
21/01/2020	39:55:00			

21/01/2020 31:55:00 Implementation 4:30:00 Implementation 4:30:	21/01/2020	36:25:00	Implementation	3:30:00	consts with dim1 seem to work using preprocessor #define. multi dim consts tho
2/101/2020 31:55:00 Implementation 4:30:00 memory?					in adt_calc on iteration 235 tho and result
Cuda kernels failing to run. Caused by reclase failing to run. Caused by reclase functions having the same name it seems although unsure exactly why. Restructured oxegen to replace func name of the seems although unsure exactly why. Restructured oxegen to replace func name of the seems although unsure exactly why. Restructured oxegen to replace func name of the seems although unsure exactly why. Restructured oxegen to replace func name of the seems although unsure exactly why. Restructured oxegen to replace func name of the seems although unsure exactly why. Restructured oxegen to replace function and oxegen to the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly why. Restructured oxegen to receive the seems although unsure exactly which is a construction of the seems of	21/01/2020	31:55:00	Implementation	4:30:00	
	22/01/2020	32:55:00			
22/01/2020 27/00:00 Implementation 2:25:00 completes ~2s slower than act compiled :/ 27/01/2020 32:00:00 Implementation 1:00:00 Re-added kernel timers and updated Makefile 1:00:00 with JITANon-JIT option Discussed completed work, and next steps: Volume translation, Orac Benchmark, Loop 0:30:00 Tiling paper Attempted Orac run, encountered issue with Cuda module. Chiror has docs on this but 0:30:00 Completed and gained access to Cambridge Requested for Volan but founds some for MG, and identified issue with translating. No input data for Volan but founds some for MG, and identified issue with rull pointer in Discussed progress, HPC systems access and term pian. Mgist need to impenent Discussed progress, HPC systems access and term pian. Mgist need to impenent Discussed progress, HPC systems access and term pian. Mgist need to impenent Discussed progress, HPC systems access, and term pian. Mgist need to impenent Discussed progress, HPC systems access, and t	22/01/2020	29:25:00	Implementation	3:30:00	rec/base functions having the same name it seems although unsure exactly why. Restructured codegen to replace func name with name_rec: resolved decided to break array constants into elements and define? should discuss
Re-added kernel timers and updated Makefile 1:00:00 with JIT/Non-JIT option 31:00:00 35:00:00 35:00:00 35:00:00 Discussed completed work, and next steps: Vola translation, Orac Benchmark, Loop 0:30:00 Tiling paper Attempted Orac run, encountered issue with Cuda module. Chiron has docs on this but 0:30:00 discontinued 0:3	22/01/2020	27:00:00	Implementation	2:25:00	
27/01/2020 31:00:00 Implementation 1:00:00 with JIT/Non-JIT option	27/01/2020	32:00:00			
Discussed completed work, and next steps:	27/01/2020	31:00:00	Implementation	1:00:00	
Note	31/01/2020	35:00:00			
Cuda module. Chiron has docs on this but	31/01/2020	34:30:00	Meeting	0:30:00	Volna translation, Orac Benchmark, Loop Tiling paper
Requested and gained access to Cambridge Requested and gained access to Cambridge HPC cluster. No password? Need to speak to O:5/02/2020 38:30:00 Benchmarking O:30:00 Gihan about this Cloned Volna and MG-CFD for translating. No input data for Volna but found some for MG, and identified issue with translator (#includes going after use defined func). Still seems to be issue with null pointer in O:5/02/2020 36:30:00 Implementation 3:00:00 comput_step_factor : 30 Discussed progress, HPC systems access and term plan. Might need to implement O:30:00 Colouring for K80s (Kepler) O:7/02/2020 37:00:00 Reeting O:30:00 Colouring for K80s (Kepler) O:7/02/2020 36:10:00 Benchmarking O:50:00 Supplimentary tool Colouring for K80s (Kepler) O:50:00 Colour	21/01/2020	24.00.00	Donahmarkina	0.30.00	Cuda module. Chiron has docs on this but
Requested and gained access to Cambridge HPC cluster. No password? Need to speak to Gihan about this Cloned Volna and MG-CFD for translating. No input data for Volna but found some for MG, and identified issue with translator (#includes going after user defined func). Still seems to be issue with uplointer in 05/02/2020 35:30:00 Implementation 3:00:00 compute_step_factor: 30			Denominarking	0.30.00	discontinued
HPC cluster. No password? Need to speak to	03/02/2020	39.00.00			Requested and gained access to Cambridge
input data for Volna but found some for MG, and identified issue with translator (#includes going after user defined func). Still seems to be issue with null pointer in office issue with null pointer is null pointer in office is null pointer in o	05/02/2020	38:30:00	Benchmarking	0:30:00	HPC cluster. No password? Need to speak to
Discussed progress, HPC systems access and term plan. Might need to implement	05/02/2020	25:20:00	Implementation	2.00.00	input data for Volna but found some for MG, and identified issue with translator (#includes going after user defined func). Still seems to be issue with null pointer in
Discussed progress, HPC systems access and term plan. Might need to implement 0:30:00 colouring for K80s (Kepler)			implementation	3.00.00	compute_step_lactor . 30
Meeting O:30:00 Meeting O:30:00 Colouring for K80s (Kepler)	06/02/2020	30.30.00			Discussed progress HPC systems access
12/02/2020 37:00:00 Emailed cam hpc about access. Attempted to generate Volna input data, but issues with ogenerate Volna input data, but issues with supplied to generate Volna input data, but issues with supplied to generate Volna input data, but issues with ogenerate Volna input data, but issues with supplied to supplied variable varia	06/02/2020	36:00:00	Meeting	0:30:00	and term plan. Might need to implement
O7/02/2020 36:10:00 Benchmarking O:50:00 Supplimentary tool	07/02/2020	37:00:00			G () ,
12/02/2020					generate Volna input data, but issues with
Attempting Cam system access, managed to compile but running with slurm indicates an account issue 13/02/2020 41:10:00 Modify Makefile to allow JIT and non-JIT Binaries without rebuilding for comparison Ran Generated code on Gihan's machine for benchmarking. Observed consistant 6s time 0:30:00 lost to compilation 18/02/2020 45:10:00 Added timer wrapper around compilation for comparison. Read about NVRTC - should definitely mention if not implement. Wrestled some more with CAM HPC and managed to 18/02/2020 43:40:00 Benchmarking 2:30:00 submit the jobs. No results yet however Got results from Cam system. Unable to build mpi_seq version of OP2 though			Benchmarking	0:50:00	supplimentary tool
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19/02/2020 41:10:00 Benchmarking 2:30:00 mpi_seq version of OP2 though	19/02/2020	43:40:00			
	19/02/2020	41:10:00	Benchmarking	2:30:00	

			Disussed next steps, set next meeting for
21/02/2020	42:40:00	Meeting	0:30:00 preliminary slides for presentation.
29/02/2020	50:40:00		
			Get parallel libs onto Cam system, to compile gen_seq OP2, run mpi_genseq airfoil for jit
29/02/2020	47:40:00	Benchmarking	3:00:00 comparison
29/02/2020	45:10:00	Presentation	2:30:00 Colour scheme, basic structure
01/03/2020	46:10:00		
01/03/2020	44:10:00	Presentation	2:00:00
03/03/2020	46:10:00		
03/03/2020	45:40:00	Meeting	0:30:00 Discussed slides, changes to be made
04/03/2020	46:40:00		
04/03/2020	43:10:00	Presentation	3:30:00 Re-ordered slides,
04/03/2020	42:40:00	Benchmarking	0:30:00 Get Machine specs
04/03/2020	41:10:00	Presentation	1:30:00 Making diagrams
05/03/2020	42:10:00		
05/03/2020	41:40:00	Meeting	0:30:00 Discussed Final slides.
08/03/2020	44:40:00		
08/03/2020	42:40:00	Presentation	2:00:00 Tweaking and Finalising
10/03/2020	44:40:00		
10/03/2020	43:10:00	Presentation	1:30:00 Finalising and giving Presentation
20/03/2020	53:10:00		
20/03/2020	52:10:00	Report	1:00:00 Structure
22/03/2020	54:10:00		
22/03/2020	52:40:00	Report	1:30:00 Intro and Background first draft
22/03/2020	51:40:00	Report	1:00:00 Intro redraft, Background & Motivations
23/03/2020	52:40:00		
23/03/2020	50:10:00	Report	2:30:00 Specification section first draft
24/03/2020	51:10:00		
24/03/2020	48:40:00	Report	2:30:00 Implementation section and tweeks
24/03/2020	46:40:00	Report	2:00:00 Implementation started codeGen breakdown
25/03/2020	47:40:00		
25/03/2020	46:10:00	Report	1:30:00 Continue codegen explanation
25/03/2020	43:40:00	Report	2:30:00 Continue codegen explanation
26/03/2020	44:40:00		
00/00/0000	40:40.00	D	Continue codegen explanation: Host Function
26/03/2020	42:10:00	Report	2:30:00 Differences
27/03/2020	43:10:00	D (0.00.00 Finishing Laws Start Law II
27/03/2020	41:10:00	Report	2:00:00 Finishing kernel file code gen section
27/03/2020	38:40:00	Report	Finished Kernel File section, some tweaks 2:30:00 and a long time on one figure
29/03/2020	40:40:00		5
29/03/2020	38:40:00	Report	2:00:00 Tweaking figures, User Function section
			Adding support for variable index for array
29/03/2020	37:10:00	Implementation	1:30:00 constant
30/03/2020	38:10:00		
30/03/2020	36:40:00	Report	1:30:00 Tweaks and redrafting
31/03/2020	37:40:00		
31/03/2020	34:40:00	Report	3:00:00 Redrafting, and Master Kernels File section
01/04/2020	35:40:00		
01/04/2020	34:10:00	Report	Master Kernels File Section, started Makefile 1:30:00 section, fixed small bug Started Testing section, tested with inneand
01/04/2020	32:10:00	Report	Started Testing section, tested wth icpc and 2:00:00 working on gcc
04/04/2020	35:10:00		, ,
04/04/2020	33:40:00	Report	1:30:00 Wrote up Testing Plan, made Figures

04/04/2020	32:10:00	Report	1:30:00 Writing testing results started
04/04/2020	31:10:00	Report	1:00:00 Testing results codegen done
06/04/2020	33:10:00		
06/04/2020	30:10:00	Report	3:00:00 Finished testing section
07/04/2020	31:10:00		
07/04/2020	29:25:00	Report	1:45:00 Benchmarking section done, started results
08/04/2020	30:25:00		
08/04/2020	29:10:00	Report	Finished Benchmarking, start going from start 1:15:00 throguh research
09/04/2020	30:10:00		
09/04/2020	27:40:00	Report	2:30:00 Started Research Section
11/04/2020	29:40:00		
11/04/2020	28:10:00	Report	Wrote more research section, discovered 1:30:00 issue with SoA codegen
11/04/2020	26:10:00	Implementation	Fixed SoA codgen, attempted to add further optimisation by declaring but proved to be an 2:00:00 overcomplication
11/04/2020	25:40:00	Report	0:30:00 Started CUDA research section
12/04/2020	26:40:00	Νέροιτ	0.30.00 Glatted CODA research section
12/04/2020	24:55:00	Report	1:45:00 Cuda Research Section progress
15/04/2020	27:55:00	Report	1.43.00 Guda Nesearch Section progress
15/04/2020	26:25:00	Donart	1:30:00 Related Work research section
		Report	1.50.00 Related Work research section
16/04/2020	27:25:00	Danart	0.45:00 Evaluation started
16/04/2020	25:10:00	Report	2:15:00 Evaluation started