Attribution & Literature

- We will only be scratching the surface of DSP in this course
- For further details, please see published literature by Valentin Jordanov. A select listing of relevant papers:
  - Jordanov_DSP_MovingAverage_IEEE_1993.pdf
  - Jordanov_Filters_NIMA345_1994.pdf
  - Jordanov_Deconvolution_NIMA351_1994.pdf
  - Jordanov_DSP_Realtime_NIMA353_1994.pdf
  - Jordanov_PSD_IEEE_1995.pdf
  - Jordanov_DSP_Compact_NIMA380_1996.pdf
  - Jordanov_ShapingWeights_NIMA505_2003.pdf
  - Jordanov_PeakDetect_IEEE_2003.pdf
  - Jordanov_DSP_Realtime_NIMA652_2011.pdf
  - Jordanov_Exponential_NIMA670_2012.pdf
- Material for next 3 lectures derived from material from DSP short course led by V. Jordanov

General Considerations

- Random nature of radioactive detector events → different analysis techniques compared to those used in telecommunications, speech, imaging, etc.
    - Anti-aliasing less important for radiation detection than in other applications
    - Emphasis on real-time processing: typically design and analyze digital shapers in discrete **time domain**
        - Most DSP textbooks and other literature focus on analysis in the **frequency domain**, where the mathematics of convolution are simplified
- Real-time operation is absolutely necessary for radiation measurement applications
    - Rate considerations from detector physics
    - Avoid bottlenecking at the DSP component

Digital Vs. Analog Processing

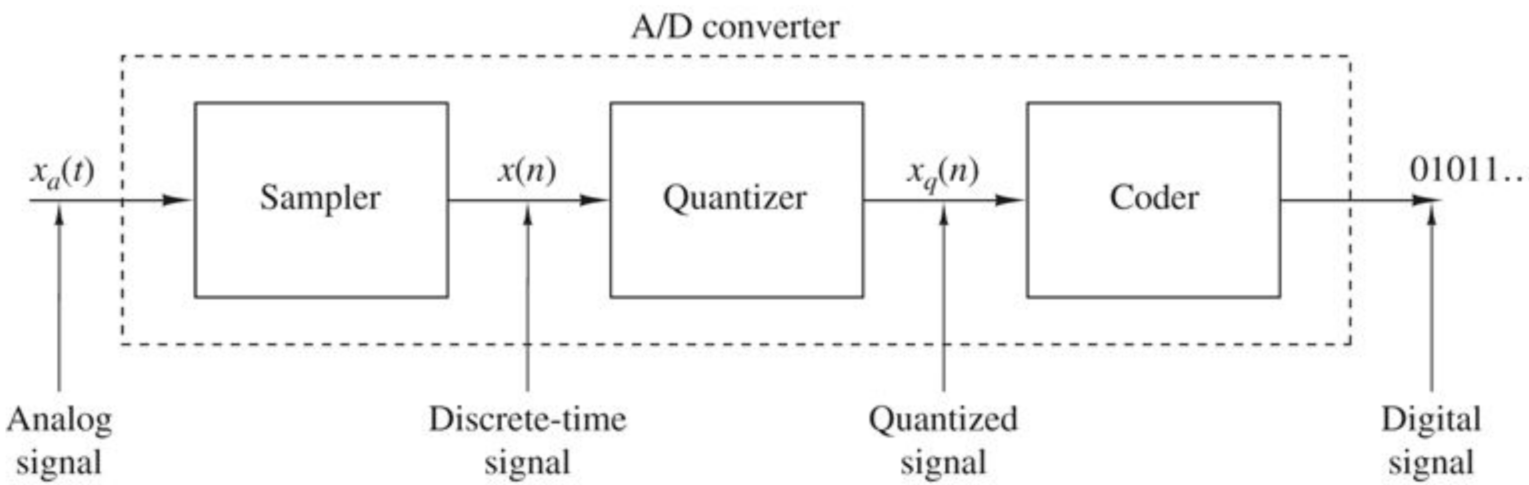
- Digital Signal Processing
  - **Flexibility**
    - complex math & logic operations and higher-order filter designs
    - Reprogrammable functionality (system flexibility)
    - Online & Offline processing - robust evaluation and quicker design revisions
  - No tuning of analog components during production/operation (improved reliability and reduced cost)
  - Improved version control, reproducibility, and distributability of digital designs
- Analog Signal Processing
  - High-frequency applications
  - High-density applications (multi-channel systems): optimized solutions for specific applications (ASICs)
  - Potentially reduced cost for single (specific) application

From Analog To Digital

- Leverage rapid advances in digital technology driven by industry (computing & communications, etc)
  - Miniaturization, speed, power consumption, etc.
  - Cost per functionality decreases much more rapidly in digital domain than in analog
- Benefits of VLSI downscaling
  - Digital ckts not subject to analog noise (after conversion)
  - Shrinking feature size → greater functionality per Si area
  - Amenable to automated design and testing
  - “Arbitrary” precision
  - Inexpensive storage

Analog to Digital Conversion

- Convert continuous signal to digital signal
  - Bridge between continuous and discrete time domains
- Analog-to-Digital Converter (ADC) → accepts analog input signal (often voltage) and produces corresponding digital code at output
- ADC incorporates sampling circuit, digitizer, encoder, etc.

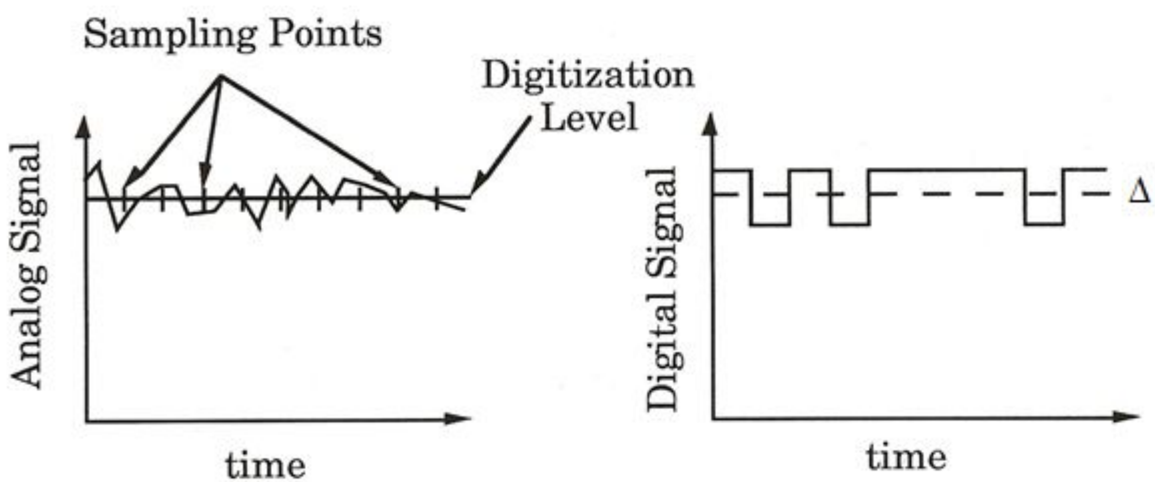


For a review of ADC architectures for RD&M, see Knoll Ch. 17

Quantization of Sampled Signals

- Quantization Error (Q.E.) or noise is introduced by digitization process
  - Assume set of values I within one quantization step with mean m_I and D to be the width of the step so that all (equally probable) analog values from m_I -1/2 D to m_I +1/2 D are converted into the value m_I by the ADC:

$$\boxed{\sigma_{\Delta}^{2} = \frac{1}{\Delta} \int_{\mu_I - \Delta/2}^{\mu_I + \Delta/2} \left[I - \mu_I \right]^2 dI = \frac{\Delta^2}{12}}$$



$$\Delta = \frac{x_{max} - x_{min}}{N - 1}$$

$V_{max} = x_{max}$-x_{min}: Maximum signal range

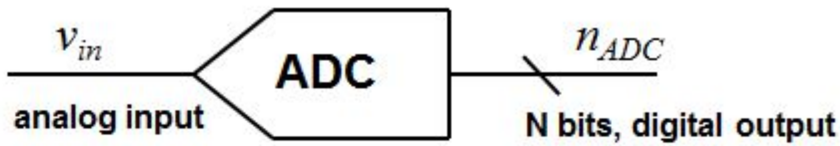
N: # of quantization levels

- Theoretically, quantization of analog signal **always** results in a loss of information
  - Overcome in practice by ensuring QE < other sources of noise (e.g. electronic noise)

Dynamic Range & Noise

- Expresses range of input signal values that can be resolved
- Given by the ratio of the noise floor to the maximum signal that can be expressed
  - Often presented in units of dB
  - E.g. 16-bit ADC with ±5V input range: $20\log_{10}(2^{16}) = 96$ dB
    - Assumes noise floor == Q.E., If noise floor is higher, dynamic range reduced
  - Subject to ADC offset
    - If only positive polarity signals from previous example → halve dynamic range (48 dB)
- If noise floor is greater than QE, effective resolution of ADC is reduced
  - Effective Number of Bits (ENOB): $N - \log_2(RMS_{noise}/\Delta E_{step})$
  - E.g. 14-bit ADC w/ 10V input range → 0.6 mV | if $RMS_{noise} = 1.2$ mV $\rightarrow 14 - \log_2(1.2/0.6) =$ **13 effective bits!**

ADC Basics



$N \quad$ = number of bits of resolution in ADC

n_{ADC} = converted code $0 \le n_{ADC} \le 2^{N-1})$

v_{in} = sampled input voltage

V_{+REF} = upper end of input voltage range

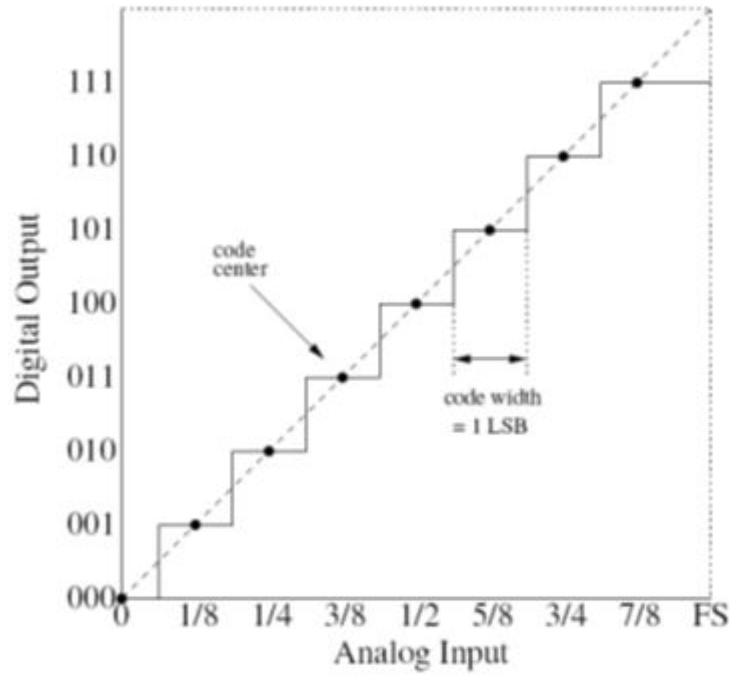
V_{-REF} = lower end of input voltage range

$FSR = Full - scale\ range$

$$n_{ADC} = INTEGER\left[\frac{(v_{in} - V_{-REF})(2^N - 1)}{V_{+REF} - V_{-REF}} + \frac{1}{2}\right]$$

if $V_{-REF} = 0$, and $FSR = V_{+REF}$

$$\boxed{n_{ADC} = INTEGER\left[\frac{v_{in}(2^N - 1)}{FSR} + \frac{1}{2}\right]}$$



n_{ADC} <u>rounded to nearest integer</u>

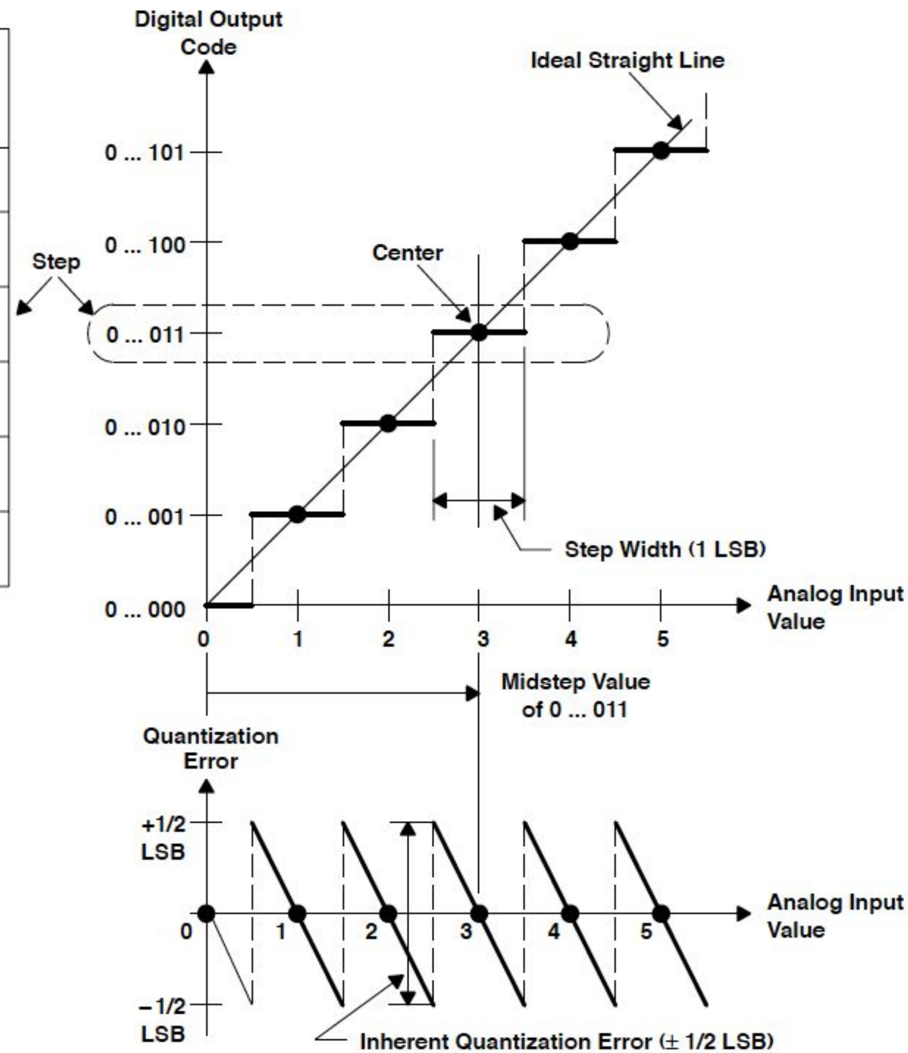
Ideal Conversion

- Ideal ADC transfer function
- Least-significant bit (LSB)
    - Width of single step: measure of converter resolution

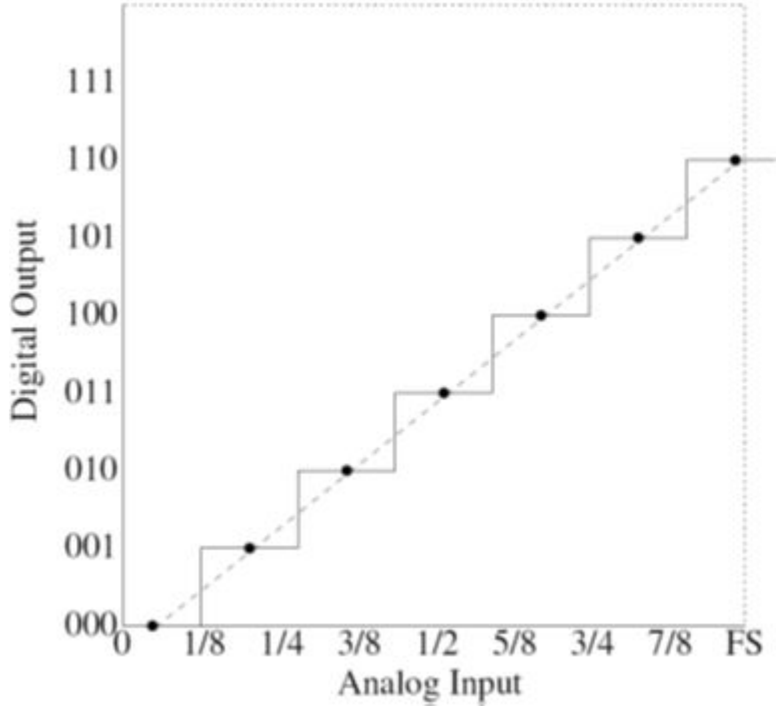
$$1 \text{ LSB} = \text{FSR} / (2^n - 1)$$

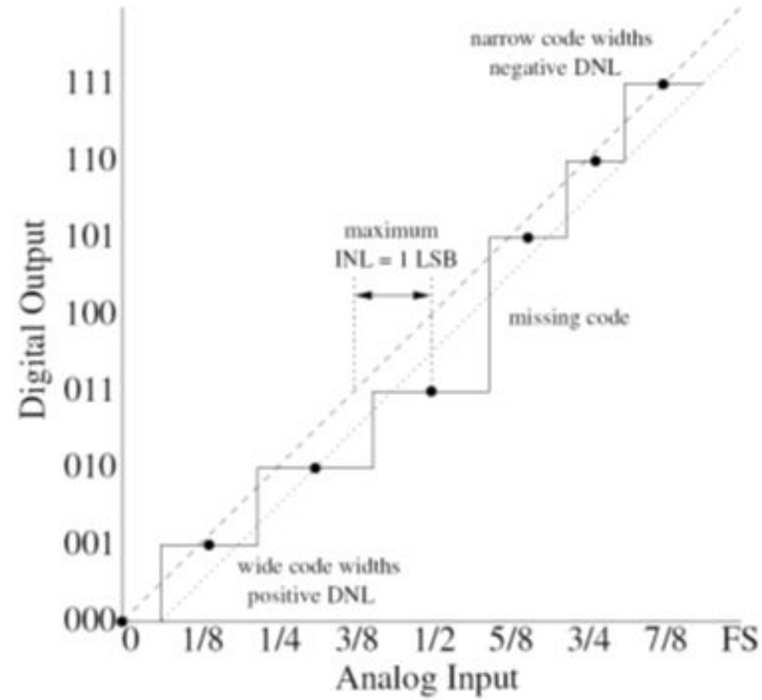
CONVERSION CODE

RANGE OF ANALOG INPUT VALUES	DIGITAL OUTPUT CODE
4.5 • 5.5	0 ... 101
3.5 • 4.5	0 ... 100
2.5 • 3.5	0 ... 011
1.5 • 2.5	0 ... 010
0.5 • 1.5	0 ... 001
0 • 0.5	0 ... 000



A/D Conversion Characteristics





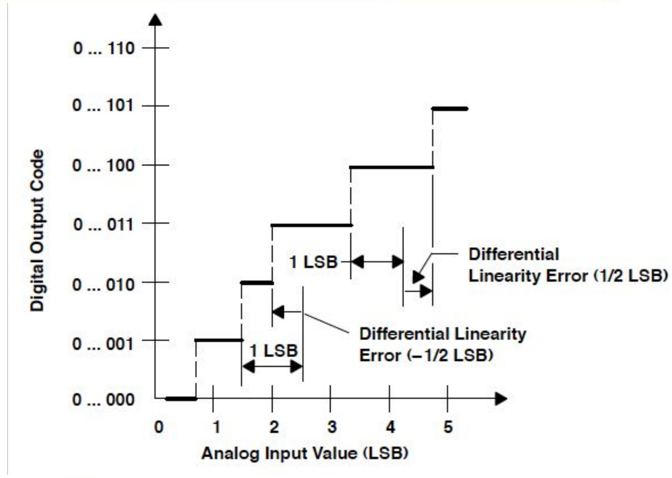
- DC Offset Error
- Gain Error
- Temperature/long-term drift

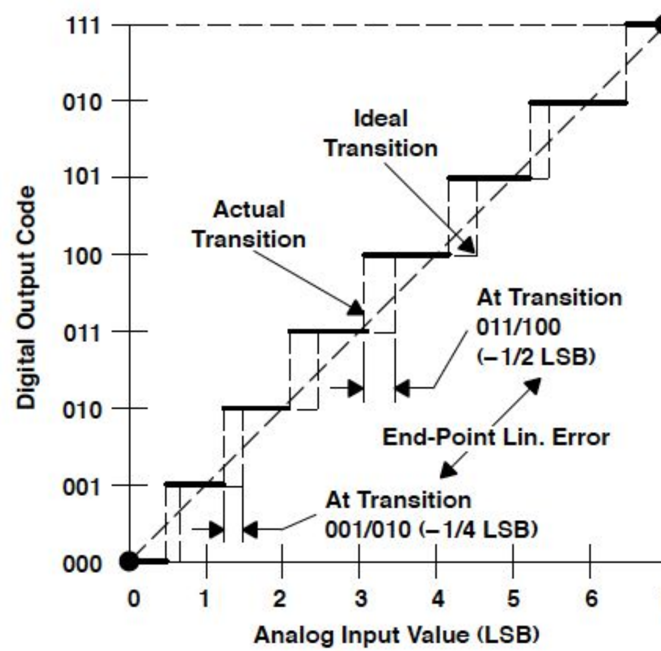
- Differential Nonlinearity (DNL)
- Integral Nonlinearity (INL)
- Non-monotonic conversion
- Missing Codes

➢ Conversion errors usually expressed in terms of least-significant bit (LSB)

ADC Nonlinearity

- **Differential Nonlinearity**
  - Difference between ideal step width (1 LSB) and actual step width
  - DNL[i] = (V[i+1] - V[i]) - 1 LSB
- **Integral Nonlinearity**
  - Deviation of ADC transfer function from a straight line
  - End-point linearity: straight line between V_{min} and V_{max}
  - INL[i] = (V[i] - V[0]) - ((i/N)*(V_{max} - V_{min}))
  - “Integral” nonlinearity → Accumulation of differential nonlinearities from 0th to ith step



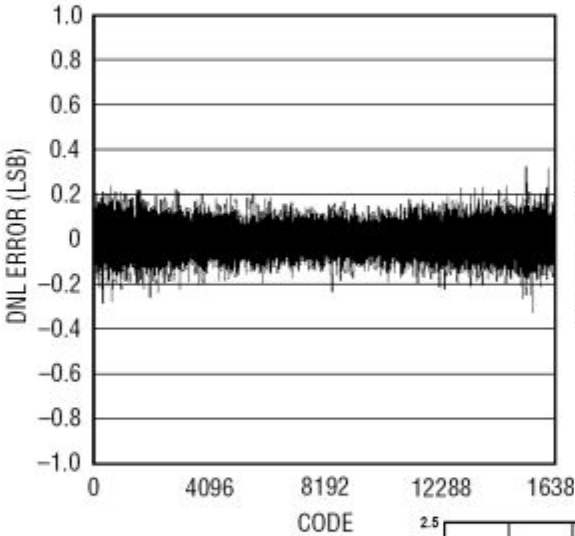


(a) ADC

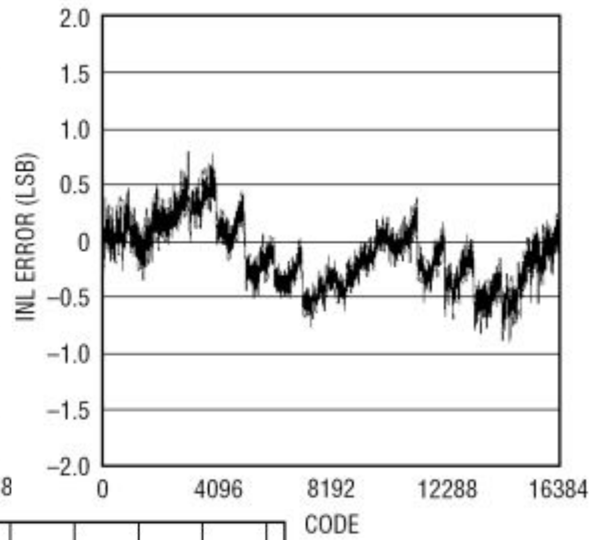
ADC Data Sheets

- ADC characterized by manufacturer
  - Select the right component for specific application!

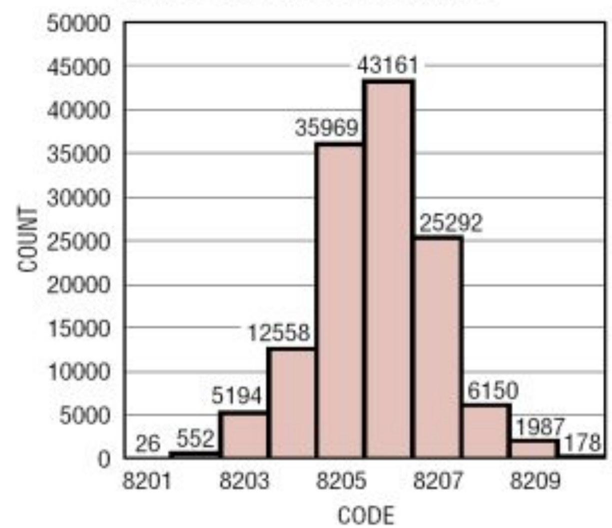
Typical DNL, 2V Range

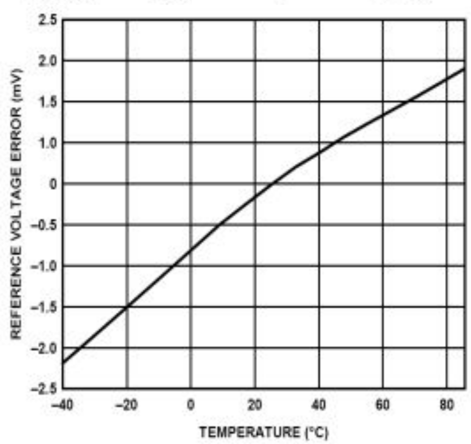


Typical INL, 2V Range



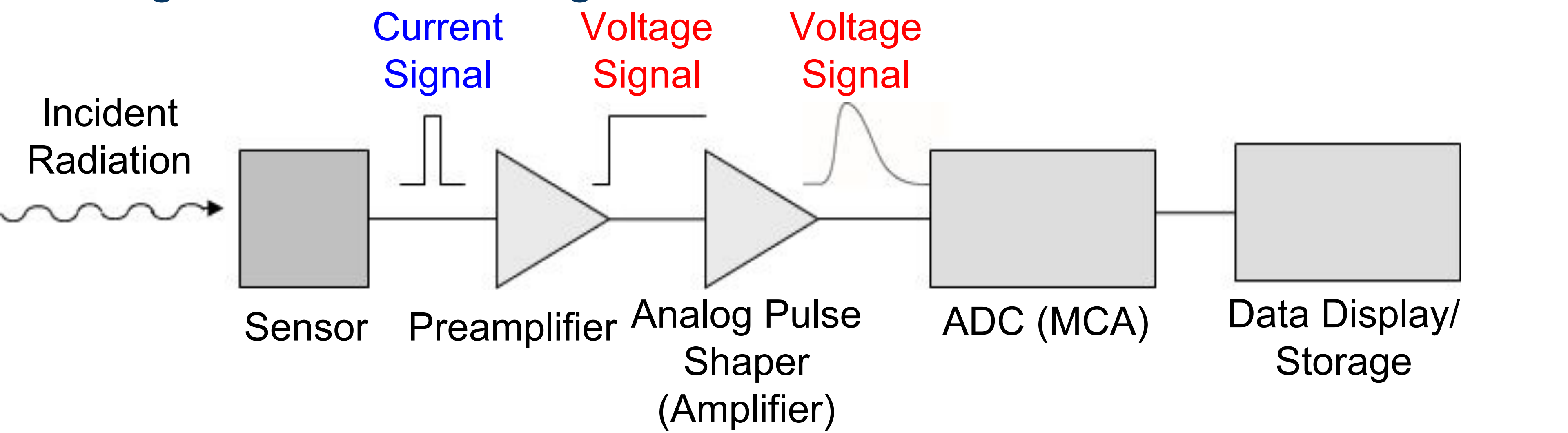
Grounded Input Histogram



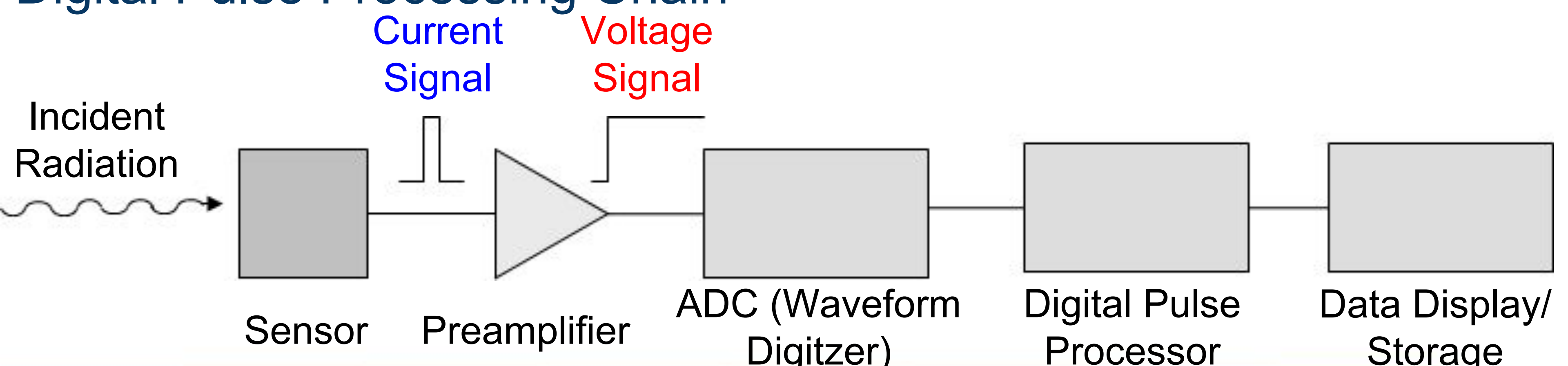


Spectroscopy Signal Processing Chain

Analog Pulse Processing Chain

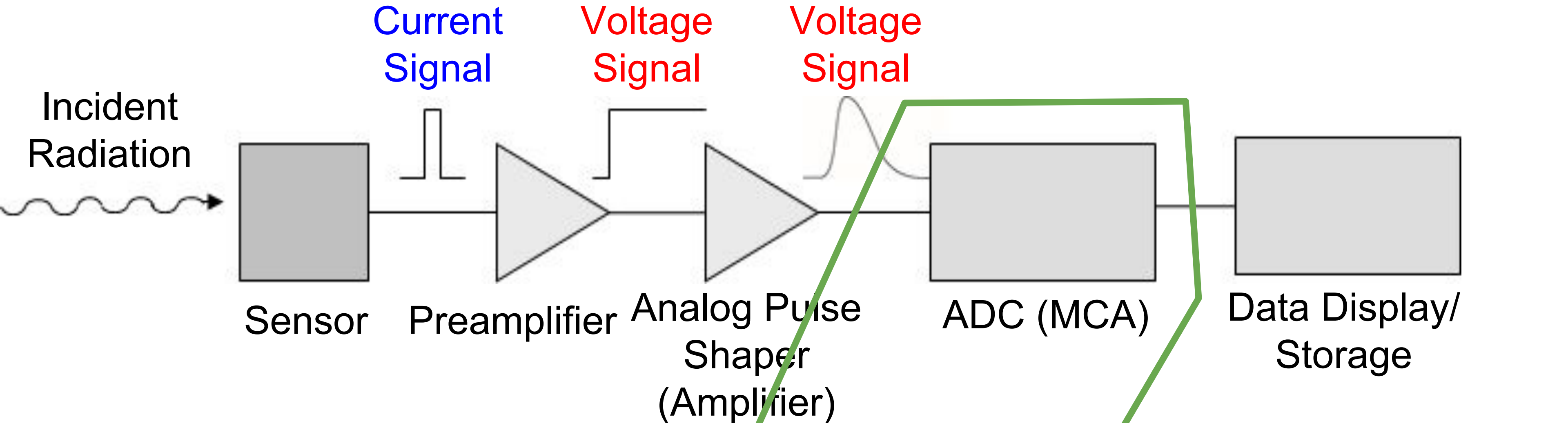


Digital Pulse Processing Chain

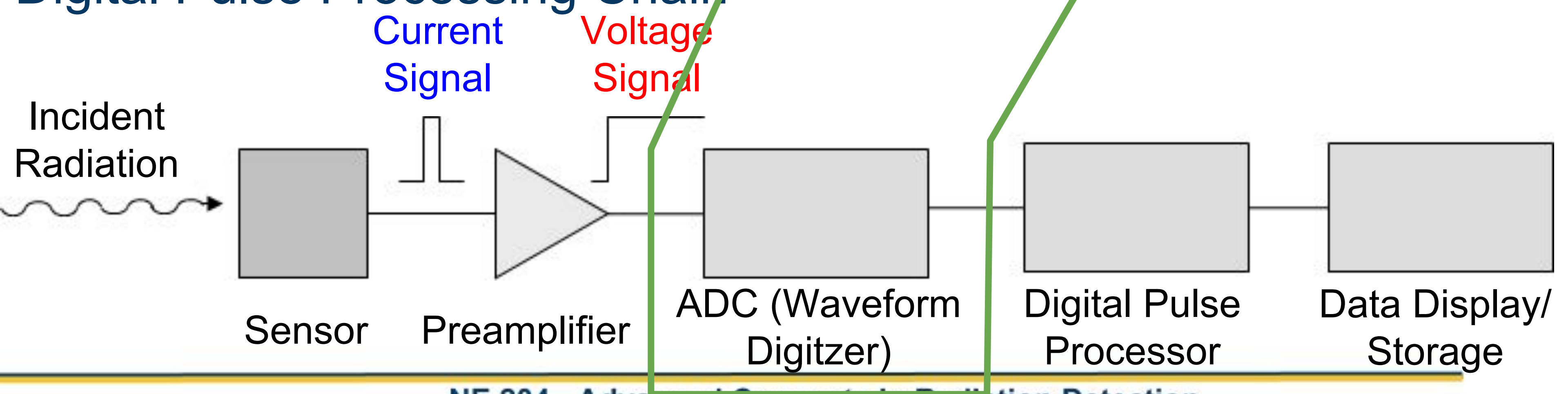


Spectroscopy Signal Processing Chain

Analog Pulse Processing Chain



Digital Pulse Processing Chain



Choosing the ADC to fit the Application

- ADC for multichannel analyzer
  - Goal: digitize pulse heights of shaped signals
    - Speed: dictated by count rate & shaping time
    - Linearity: INL must be minimized over whole range
    - Resolution: dictated by energy resolution of detector
  - Wilkinson, SAR (serial arch.) ADCs (see Knoll ch. 18)
- ADC for digital signal processing
  - Goal: Digitize signal from detector
    - Speed: dictated by timing/features of signals
    - Linearity: INL & DNL can lead to biases in signal shapes
    - Resolution: dictated by system noise (QE < other noise sources)
  - Flash, subranging (parallel arch.) ADCs (review Knoll ch. 17)

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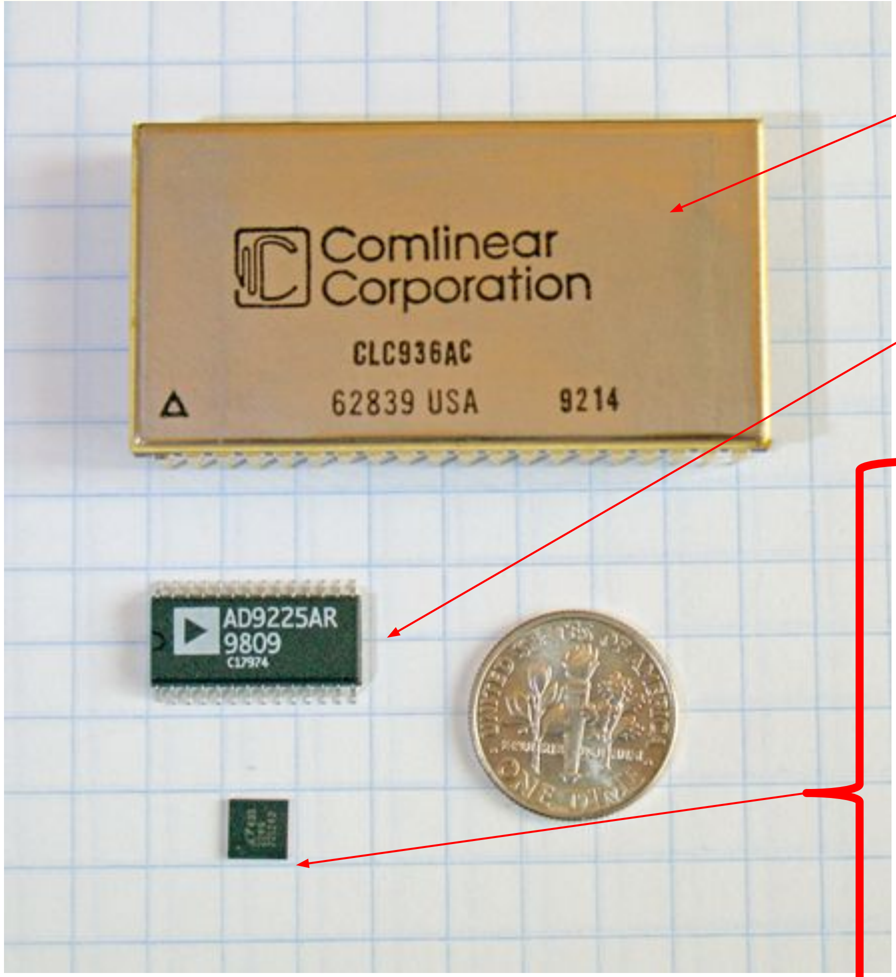
Fast ADC History



1992
12 bit, 20Msps, 4W, $750

1998
12 bit, 25Msps, 280mW, $30

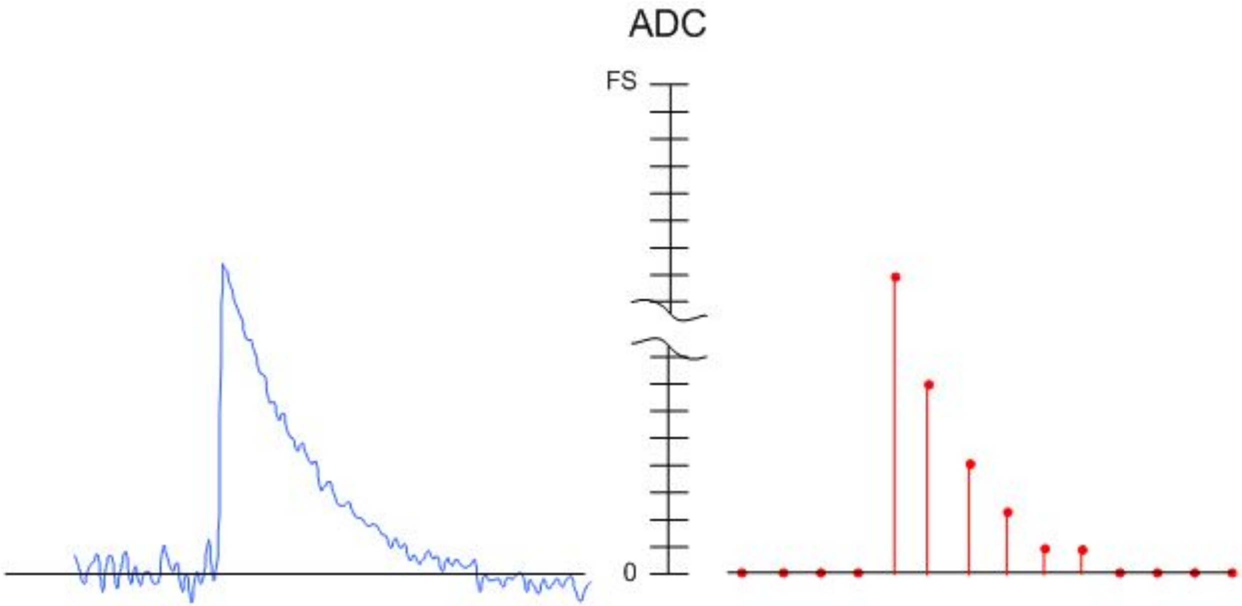
2004
14 bit, 80Msps, 220mW, $30

2008
16 bit, 105Msps, 900mW, $80

2013
16 bit, 125Msps, 750mW, $130 (2 Ch)
14 bit, 250Msps, 711mW, $130 (2 Ch)
12 bit, 500Msps, 650mW, $130 (1 Ch)

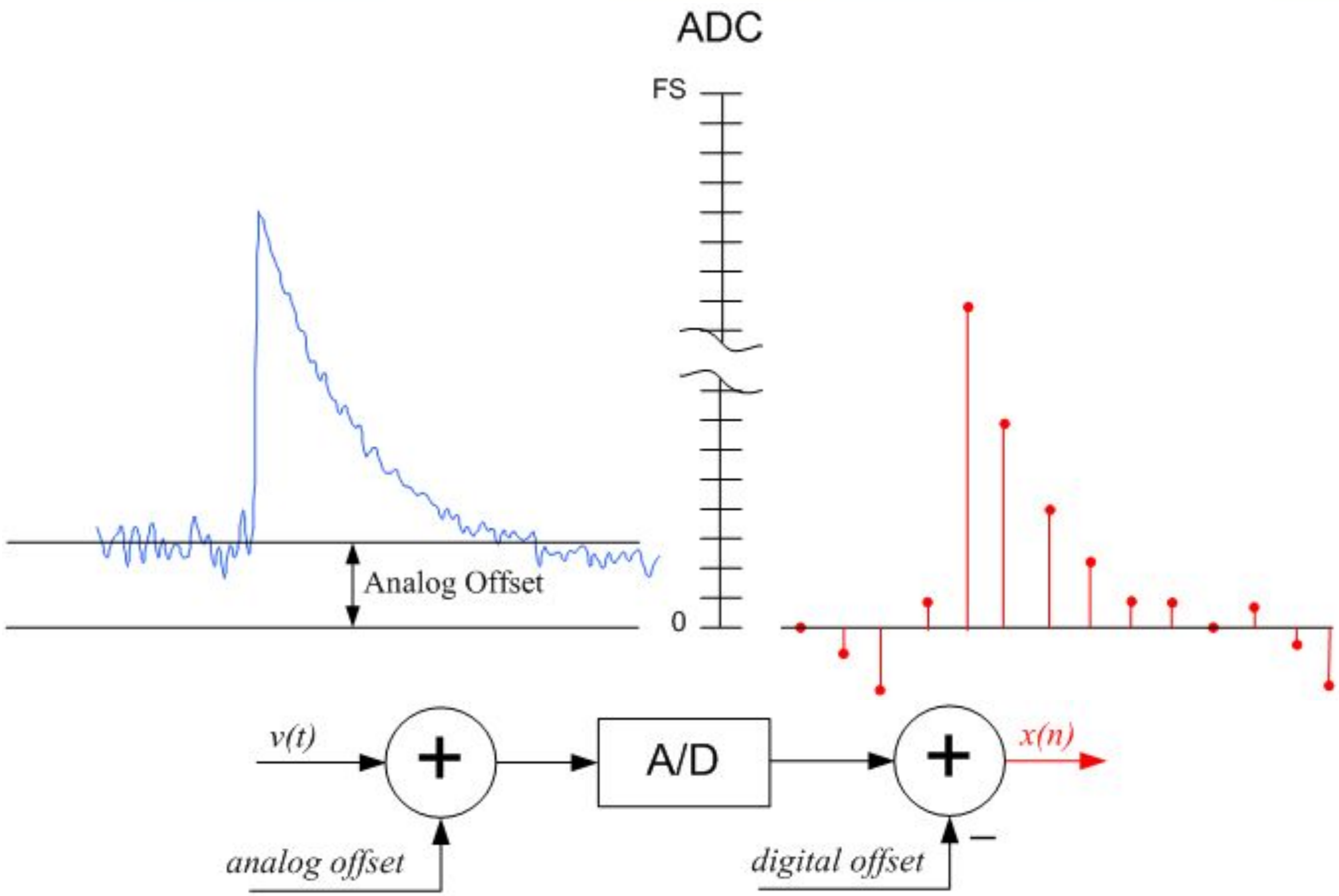
Today

Fast Digitization of Preamp Signals: Amplitude Considerations



- Want to maximize ADC range used for digitizing pulses
  - Must consider the baseline & negative excursions!

Fast Digitization of Preamp Signals: Amplitude Considerations



- Add offset in analog domain, subtract off in digital domain
  - Example: Bipolar pulses - what effect does this have on ADC resolution/dynamic range?

Fast Digitization of Preamp Signals: Timing Considerations

- **Phase Error**: Signal arrival time not synchronous with sampling
  - Depends on sampling time, ΔT!
    - ADC with sufficient resolution to minimize **Quantization Error**
    - ADC with sufficient sampling rate to minimize **Phase Error**