School of Engineering

Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

TITLE: *Analysis of reliability of Flip-Flop and latches under Transistor Aging Effects and variations in CMOS Technology*

PRESENTER: **Vikram G Rao**

TIME & DATE: **4 PM, November 15th, 2010** **LOCATION:** **SCI 256**

COMMITTEE CHAIR: **Dr. Hamid Mahmoodi**
COMMITTEE MEMBERS: **Dr. Hao Jiang**

ABSTRACT

According to Moore's Law, "the number of transistors on a chip double every two years." Thus the need for scaling transistors is always in the market. With the usage of High-K metal gate technology for the new scaled generation of CMOS technology, new reliability problems are surfacing. One of the major Reliability issues is the aging effect, referring to the degradation in performance of MOS devices over time. These issues include Positive Bias Temperature Instability (PBTI) and Negative Bias Temperature Instability (NBTI) affecting the NMOS and PMOS respectively.

As we know, Flip-Flop and Latches form the basic blocks of pipelined architectures. The timing characteristics of Flip-Flops often determine the frequency of operation of the circuit. The most important timing constraints we consider while designing a circuit using flip-flops are setup time, hold time and clock to output delay. In this project, we have analyzed and tested different Flip-Flop circuits for aging effects and evaluated their performance. It is observed that proper application of Dual Threshold voltage can reduce the impact of aging effects on Flip-Flop delays. More noticeably, in the case of Sense Amplifier Flip – Flop, Dual Threshold Voltage shows delay reduction over time by transistor aging.