TIME DEPENDENT BREAKDOWN OF GATE OXIDE AND PREDICTION OF OXIDE GATE LIFETIME

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In
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by

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San Francisco, California

May, 2012

CERTIFICATION OF APPROVAL

I certify that I have read *Time dependent Breakdown of Gate Oxide and Prediction of Oxide Gate lifetime* by Bin Wu, and that in my opinion this work meets the criteria for approving a written research paper submitted in partial fulfillment of the requirements for the degree: Masters of Science in Engineering: Embedded System.

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With the scaling of the CMOS technology and the associated gate oxide thickness, the reliability of the gate oxide has become a major barrier for reliable circuit design in nano-scale. The gate oxide breakdown caused by excessive electric field in the gate oxide causes increased gate leakage degrading the circuit performance. Models for predicting the Time to Dielectric Breakdown (TDDB) are valuable in designing reliable circuits. Our research objective is to develop a TDDB model that designers can use to predict the lifetime of a given circuit. We review several physical explanations and models that try to explain TDDB. The gate breakdown problem, according to recent experiments, could be divided into three phenomena. We test these assumptions under very thin oxide regime and compare results with the empirical data to check the validity of the models.

I certify the Abstract is a correct representation of the content of this research paper.

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Committee Chair Date

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I. INTRODUCTION

Although there is no universally approved model for the breakdown mechanism of gate oxide, factors that influence the process of breakdown, such as thickness of gate, stressed field strength, or voltage that influence the breakdown of gate oxide, could be studied by observation from experiment. Early researches [1] [2] based on experiment data tried to find the mathematic connection between these factors and the breakdown time, or known as the Time Dependent Dielectric Breakdown (TDDB). The observed models from different groups are quite different, due to different measuring ranges. Further researches and reports all tried to build a unified theory system to describe the TDDB behavior. However, confusion still exists, as more new theories [3][4][5]showed up and the situation becomes more complicated. A single model could not describe the TDDB of gate oxide in wide range of oxide thickness or stressed field strength. Multiple mechanisms play roles in yielding defection in oxide layer under different situations. Different mechanisms would dominate as the scenario varies in

the range of gate thickness, stressed field strength, and voltage. The prediction based on several mechanisms could give a more reasonable result.

Almost all the hypothetic models agree that the breakdown of gate is related to the defect, or called trap, yielding in the oxide layer. The mechanisms how are these traps yield in the oxide layer are still controversial. By analyzing suitable scenarios that each model fits, we could give a more accurate prediction for the lifetime of the gate oxide, in wide range of gate thickness and stressed voltage.

II. Breakdown of Oxide Gate

It is commonly accepted that the breakdown of gate oxide is due to degradation of SiO_2 and trap charges exist in the oxide layer. These defects could reduce the effective thickness of the gate and accelerate the degradation of the oxide gate. Once the degradation of the oxide layer reach a critical density, as shown in Fig 1, the breakdown would happen and the breakdown would induce large leakage current(SILC) though the gate.

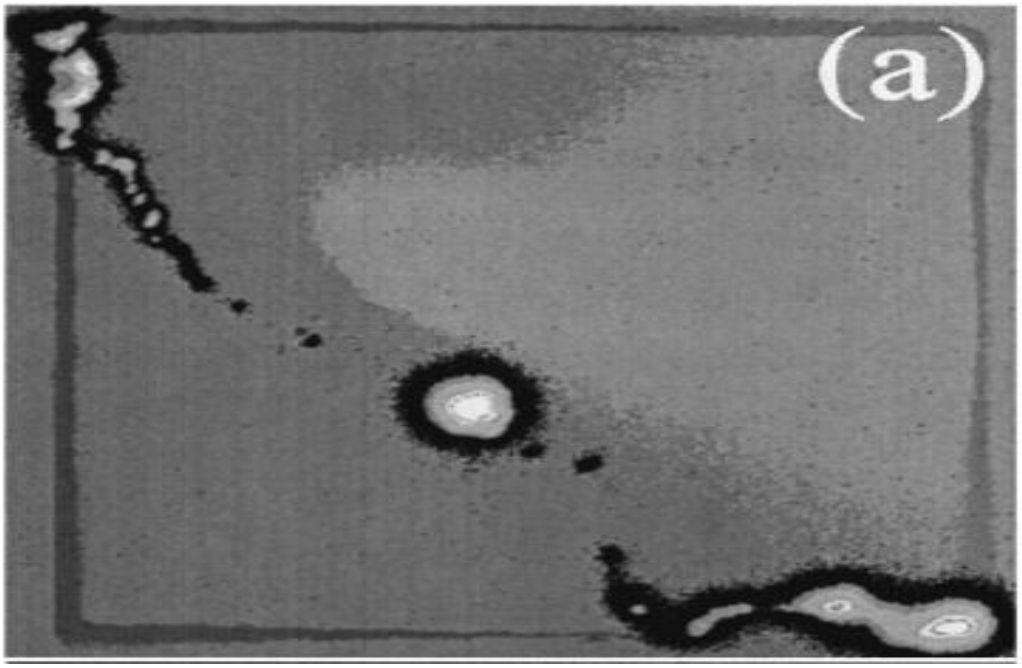

Fig.1 EMMI Image of the Gate after Oxide Breakdown [6]

The thickness of the gate, the stressed field strength and the voltage stressed on the gate could all influence the degradation speed of the gate oxide.

A. Physical explanation models for defect in Oxide layer

There are several hypothetical physical breakdown model based on the mathematic model. They all assume that the original structure of the oxide layer is damaged due to induced influence factor or the natural self character of the SiO2 material.

1) Anode Hole Injection(AHI) Model

Anode Hole Injection Model assume that the trap generated by tunneling current [7] [9]. The tunneling current could be induced by more than one mechanism, such as Fowler–Nordheim tunneling current and Direct tunneling current [8]. The high kinetic energy (> 8MV/cm) electrons

arriving at the gate might transfer their energy to those electrons deep in the valence band [10], this transmission of energy gives the electron in the valence a chance to reach the available conduction band edge of the anode. Once the electron reaches the conduction band and move freely, the electron will create a hot hole in oxide layer, which would induce more tunneling current. The 1/E model is believed to describe this breakdown mechanism [9].

2) Thermo chemical Model

Thermo chemical Model describes the self degrade thermo process that exists in all material. The Chemical Structure of SiO2 is shown in Fig. 2[10]. The angle between all O-Si linking bonds around the same Si atom is always 109 degree, which is stable. However the angle between two linking bonds that are from two different Si atoms could vary from 120 degree to 180 degree, which might be unstable, as the strength of the bond is severely week when the angle is above 150 degree [10]. The Si-O-Si bond could be

replaced with Si-Si bond, due to Oxygen Vacancy, as shown in Fig 3.

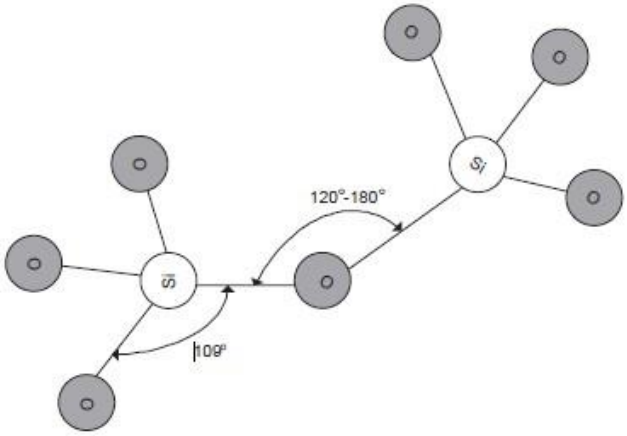

Fig.2 Chemical Structure of SiO_2 [10]

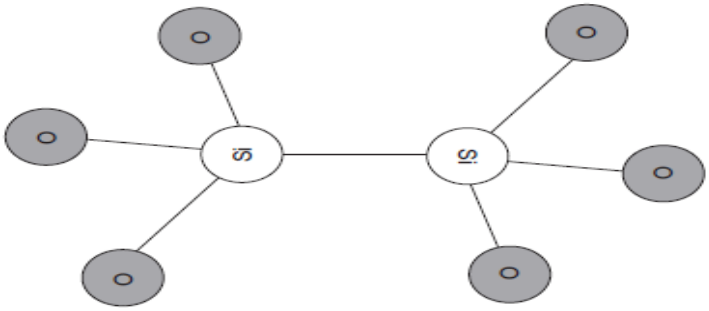

Fig.3 Oxygen Vacancy in SiO_2 [10]

The new Si-Si linking bond is a weak bond and the remaining polar Si-O bonds are going to heavily stain the Si-Si bond. The break of Si-Si bond is going to create a hole trap, which could eventually cause gate breakdown.

3) Hydrogen Release (HR) Model

Hydrogen Release (HR) Model is quite similar to the AHI model. In AHI model, the high energy electron transfers its energy to the electron in the oxide layer and creates trap holes. In HR model, the high energy electron breaks the Si-H bond at the interface [12], and this process will release protons (H^+) into the oxide layer and break the weak Si-Si linking bond:

(Si-Si) + H^+ → Si-H^++-Si [13].

The proton in the oxide layer is a trap as the proton could attract around electrons.

4) Channel Hot-Carriers

All the breakdown physical model mentioned above are going to happen as long as the gate is under stressed. The breakdown speed might also be influenced by many other factors. Hot carries yield by drain to source voltage could produce electron and hole pair; the electron could enter the gate due to the gate stressed voltage, which could yield more traps in the

gate oxide. Thus, the TDDB time could reduce due to the increase in the leakage current as shown in Fig 4.

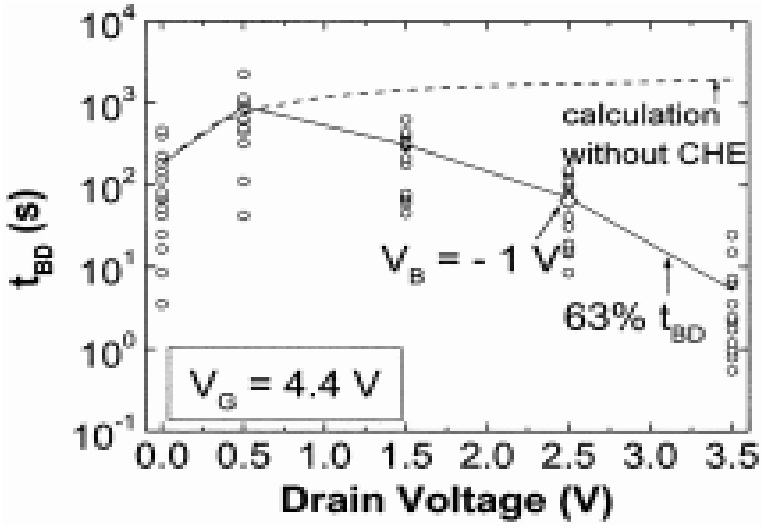

Fig.4 T_{BD} for all the stressed samples (open circles) and corresponding 63% value (solid line) as a function of V. For V = 4:4 V and V = V = 0. After the initial increase, due to the reduction in the effective stressed oxide area, a strong reduction is observed in the hot carrier regime. The dashed line shows the calculated t without considering CHC effects. Applying a negative V in the hot carrier regime does not significantly change the t value (open diamond). [14]

5) Other factors

It is important to point out that the physical models mentioned above and the mathematic model which is going to be introduced in the following section,

do have fitting oxide thickness boundary. If the thickness of the gate is too thick, the models may not fit [15]. The gate could also be influenced by other kinds of damage. For example, radiation could damage the oxide layer and reduce the TDDB time [16].

B. Mathematic models for breakdown

That this paper does not make direct connection between the physical explanations and mathematic models is due to several reasons. First, the data observed from experiments is not based on any physical explanation. Secondly, as the efficiency of degradation exist. There might be different efficiency for different types of degradation, so it is easy to isolate each physical explanation and mathematic model.

Although the theories that explain the TDDB behavior are controversial, the mathematic models observed from the experiment are solid. Large amounts of experiment data have been collected from last decade.

1) E model

E model describes the connection as between TDDB time and working electric field strength as TBD~exp($\gamma_E E_{ox}$). The E model is brought up by J.W. McPherson [2] in 1985 to describe the Thermo chemical Model. This model is believed to be quiet valid when the dielectric in stressed under low voltage.

2) 1/E model

1/E model describes the connection as between TDDB time and working electric field strength as TBD~exp (G/E_{ox}). The field acceleration factor (G) can be decomposed as the sum of two terms: $G=B + f(\Phi_p)$. 1/E model is brought up by Chenming Hu in 1998. [1] This model emphasizes on the Fowler-Nordheim current and the tunneling of it. 1/E model is believed to be responsible for the AHI model at first. However, recent reports also believe the HR model, the mechanism of which is similar to AHI, should be considered as part of the degradation that this model describes.

However, it is obvious that FN tunneling current would not dominate under all scenarios, as DT current will be a significant part of tunneling current when the gate oxide is thin and the stressed voltage is low. Chenming Hu himself later also notices this limitation of the model and later propose that a unified model which contains both E and 1/E model [7].

3) Physical based breakdown Model

Physical based breakdown Model [8] does not have a single concise equation to calculate the breakdown time as E and 1/E model. Voltage-Driven Acceleration Model divides the problems into at least two cases: DT current domain regime and FN current domain regime.

The principle equation for voltage-driven acceleration model is the widely motioned.

$$T_{BD} = \frac{N_{BD} * q}{J_{tunneling\_current} * \zeta} \quad (1)$$

Equation (1) means that the life time of gate oxide relies on the density of trapped holes, as we mentioned at the beginning of section II. Once the

density reaches a critical value, breakdown will happens.

What is different is that previous models always consider one breakdown mechanism and ignore that a unified model considering varieties of scenarios cannot rely on one single physical explanation, which means the leakage current equation may vary depending on working condition of the gate. Hence, the current density should consider another important difference for this model is that the N_{BD}, which is the critical defect density to cause breakdown, should not depend on the voltage stressed on the gate. This means the density that decides whether the breakdown happens or not should only be influenced by the physical parameters of the gate itself [8]. The variation of stressed voltage after the breakdown should not change the breakdown status of the gate.

The efficiency of the degradation is another important factor that depends on how we understand the breakdown happened. Previous report shows that the degradation efficiency is voltage dependent only. Part of the plot matches the power function of voltage perfectly. The author believes

that the range for the match to be valid is below 4V [8]. We think a boundary point of 3.5V is more practically accurate and theoretically meaningful, as 3.5V is also the boundary point between DT domain regime and FN domain regime. In the FN regime, the efficiency shows weaker dependence of voltage than in the DT regime. However, we think the efficiency still varies according to voltage.

III. Prediction of TDDB

The breakdown of gate is related to the defect yielding in the oxide layer. The prediction of lifetime of oxide gate could be calculated by equation (1). The following paragraph is going to explain how each part is calculated in detail.

A. Tunneling Current

The tunneling current is the current that tunnel through the gate when the gate is stressed under voltage. The tunneling current could be divided into two types of tunneling, Fowler–Nordheim tunneling (FN tunneling) and Direct tunneling (DT tunneling).

$$J_{tunneling\_current}=J_{FN}+J_{DT} \quad (2)$$

FN tunneling always exists if there is a voltage difference between the two sides of gate. DT tunneling current is not significant compared to FN tunneling current except low thickness range oxide gate under low voltage situation.

In the case of FN tunneling, electrons tunnel through a triangular potential barrier, whereas in the case of DT tunneling, electrons tunnel through a trapezoidal potential barrier. The tunneling probability of an electron depends on the thickness of the barrier, the barrier height, and the structure of the barrier [17].

1） Fowler–Nordheim tunneling (FN tunneling)

Fowler–Nordheim tunneling happens as the electrons from inverted surface tunnel into the conduction band of the oxide layer, as shown in Fig.5.

Ignoring the effect of finite temperature and image-force-induced barrier lowering, the FN tunneling current density is given by [18]:

$$J_{FN} = \frac{q^3 E_{ox}^2}{16\pi^2 \hbar \phi_{ox}} \exp\left(-\frac{4\sqrt{2m^*}\,\phi_{ox}^{3/2}}{3\hbar q E_{ox}}\right) \quad (3).$$

E_{ox} is the stressed field strength across the oxide layer. Φ_{ox} is barrier height for electrons in the conduction band; $m*$ is the effective mass of an electron in the conduction band of silicon. The FN current equation

represents the tunneling through the triangular potential barrier and is valid for $V_{ox} > \Phi_{ox}$, V_{ox} is the voltage drop across the oxide [9].

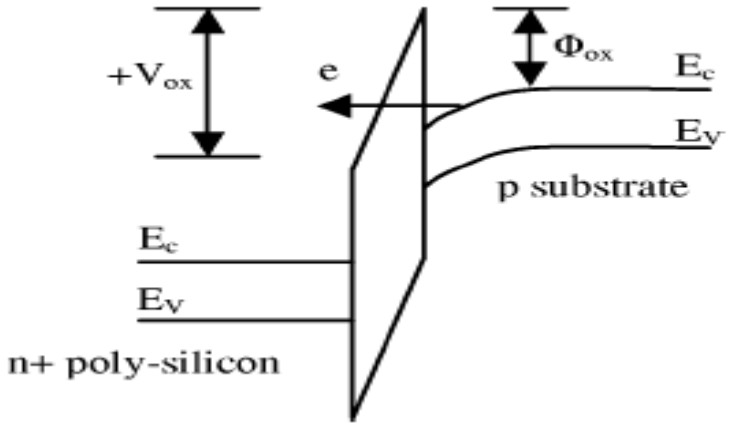

Fig.5 FN tunneling of electrons. [17]

2） Direct tunneling (DT tunneling)

In very thin oxide layers (less than 4 nm) case, electrons from the inverted silicon surface, instead of tunneling into the conduction band of SiO_2, directly tunnel to the gate through the forbidden energy gap of the SiO_2 layer [18]. The electrons tunnel through a trapezoidal potential barrier, as shown in Fig.6, instead of a triangular potential barrier in FN case [18]. The direct

tunneling current density equation is given by

$$J_{DT} = A^{*}E_{ox}^{2} * \exp\left\{ -\frac{B\left[1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{3/2}\right]}{E_{ox}} \right\} \quad (4).$$

A equals $q^3/16\pi^2\ \hbar\Phi_{ox}$ and B equals $4\sqrt{2m*}\Phi_{ox}^{3/2}/3\hbar q$. Φ_{ox} is barrier height for electrons. It is important to notice that the term $1\text{-}V_{ox}/\phi_{ox}$ are not in a valid definition range when the $V_{ox}>\phi_{ox}$. Hence, unlike the existence of FN tunneling in all stressed voltage range, DT tunneling does not exist when $V_{ox}>\phi_{ox}$. The calculation of tunneling current requires to consider both DT current and FN current, as Direct tunneling current is significant compared to FN current for low oxide thickness.

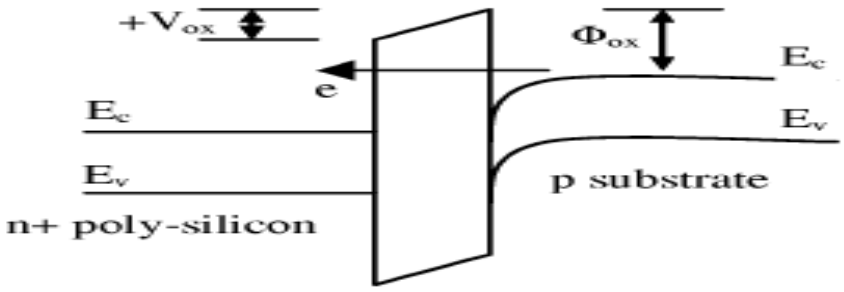

Fig.6 Direct tunneling of electrons. [17]

3） Barrier height and image-force-induced barrier lowering

Both Fowler–Nordheim tunneling and direct tunneling depend on the barrier height as we have discussed before. However, the barrier height does not only rely on the material of gate and the density of doping concentration of silicon, but also rely on the stressed electric field strength. Thus, the real barrier height should equals to the barrier height, without the influence of the stressed field, deducted by the barrier lowering, as shown by equation (5):

$$\phi = \phi_{ox} - \Delta\phi \quad (5).$$

Where $\Delta\phi$ is the barrier lowering called image-force-induced barrier lowering, and $\Delta\phi = \sqrt{\frac{q^3 \cdot E_{ox}}{4 \cdot \pi \cdot \varepsilon_{ox}}}$. The emission of electron from Si to SiO_2 will causes image charge at the oxide side of the Si–SiO_2 interface, and the charge will lower the barrier height [18].

B. Degrade Generation Efficiency

The degrade generation efficiency, as shown in Fig.8 could be calculated

based on raw Q_{BD} data, which is shown in Fig.7 [19]. The equation used is shown as following:

$$\zeta = \frac{e \cdot T_{ox}}{a_0^3 \cdot Q_{BD}} \exp\left\{ - \frac{1}{\beta} \cdot \mathrm{Ln}\left(\frac{A_{ox}}{a_0}\right)\right\} \quad (6).$$

Different mechanisms of degradation could be the best answer to explain why V^{38} function alone could not fit the entire graphic, as shown in Fig.8. Electronic excitation (EE) mechanism and vibration excitation (VE) mechanism are believed to play role under different electron energy level [19]. Jordi Suñé1 and Ernest Y. Wu conclude that at high electron energies (above 6.5eV), electronic excitation (EE) causes HR; at very low energies (< 2.5 eV) HR is controlled by vibration excitation (VE) and a transition from single-electron to multiple-electron mechanisms is reported, and between these extremes, the results are consistent with a cooperation of VE and EE mechanisms [19].

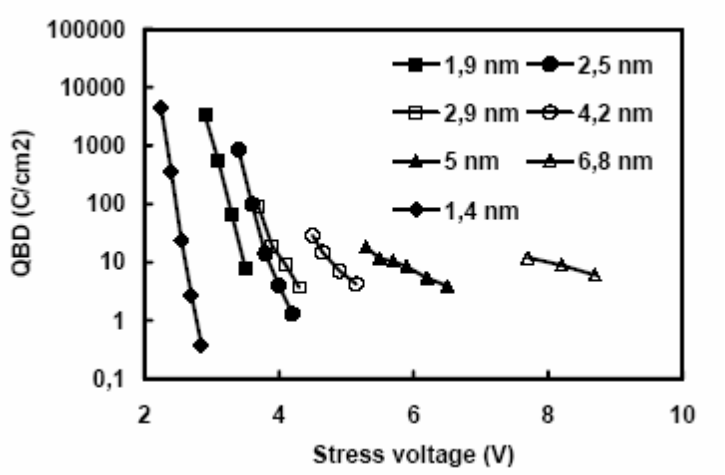

Fig.7 Mean charge to breakdown vs. stress voltage for NFETs with different TOX stressed under CVS at 140^0C [19].

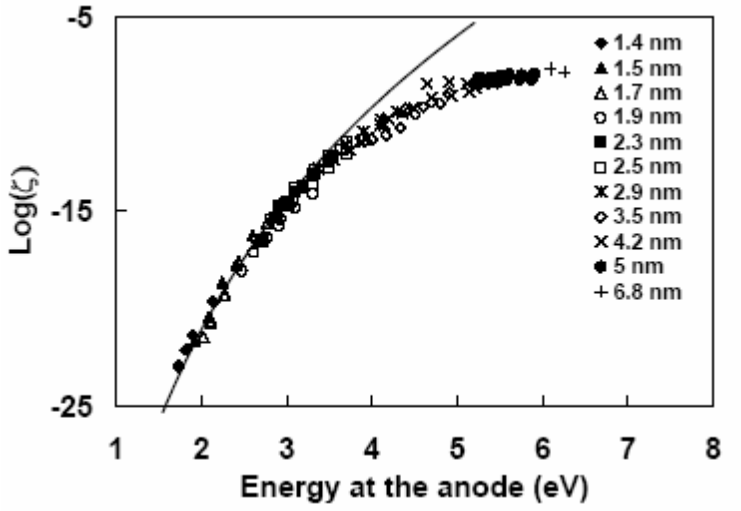

Fig.8 Defect generation efficiency calculated from the raw QBD data [19].

The original paper suggests using V^{38} function to plot the graphic below

4ev situation, and the graphic above that case should be considered as independent of V in order to match the final result, as both tunneling current and TDDB time shown a V^{30} connection in that voltage range [8]. So the red part of the efficiency plot should be calibrated to a segment that is in parallel with X-axis.

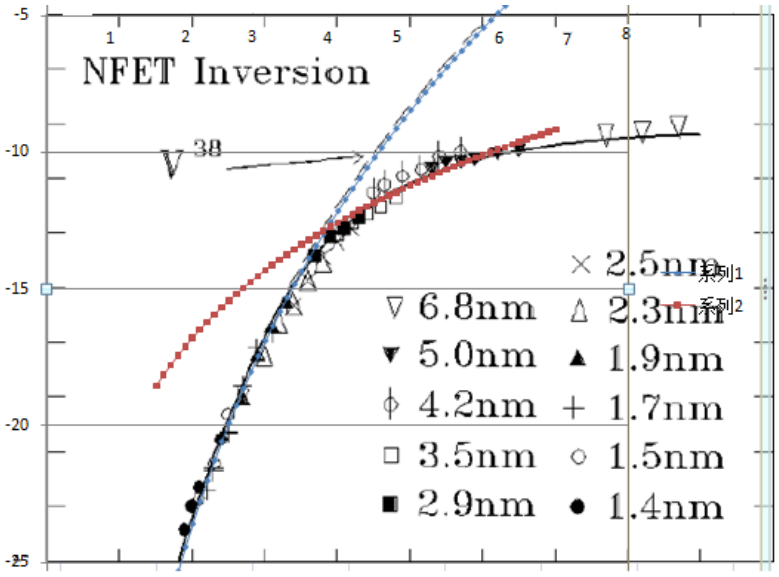

Fig.9 power V functions used to fit the degradation curve.

C. Critical Breakdown density

The break down density is a parameter that tries to describe the breakdown as a physical condition of the gate oxide layer, without involving stressed

voltage value. Since the breakdown density should be a value that is only related to its physical parameter area and thickness, the following equation is used to calculate the breakdown density:

$$N_{BD} = \frac{T_{OX}}{a_0} \exp\{-\frac{1}{\beta(T_{OX})} \cdot \mathrm{Ln}(\frac{A_{OX}}{a_0^2})\} \quad (7).$$

Equation 7, derived within the analytical version of the percolation model, makes the breakdown density depending on area and weibull slope. [20]

IV. Simulation Result

In this section, the simulation results of breakdown density, leakage current and TDDB lifetime are shown. The leakage current and TDDB life time are compared to measurement data.

A. Simulation Result of critical breakdown density

Fig.10 and Fig.11 are the simulation results of critical breakdown density based on Equation 7 in different scale. As shown in Fig.10 and Fig.11, the N_{BD} will increase drastically with the accumulation of thickness. Influence of the area is relatively smaller than the influence of the thickness.

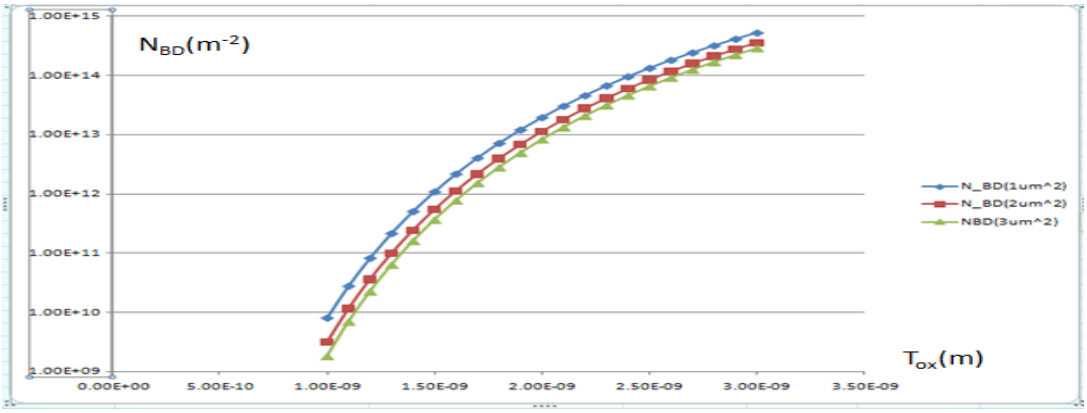

Fig.10 simulation result of breakdown density (N_{BD}) in log10 scale.

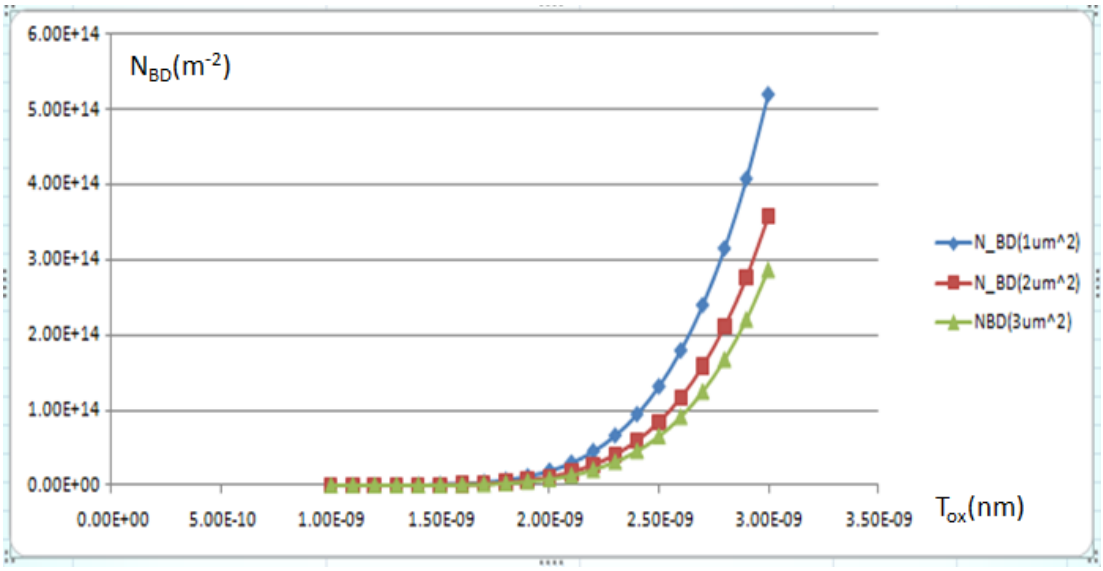

Fig.11 simulation result of breakdown density (N_{BD}) in regular scale.

B. Simulation Result of tunneling current.

Fig.12 and Fig.13 show the simulation current of gates of different thickness. Fig.14 is the measurement of actual leakage current. The simulation result is slightly smaller than the actual data, but the trend is the same. The leakage current increasing rate slow down as when the voltage reaches certain value.

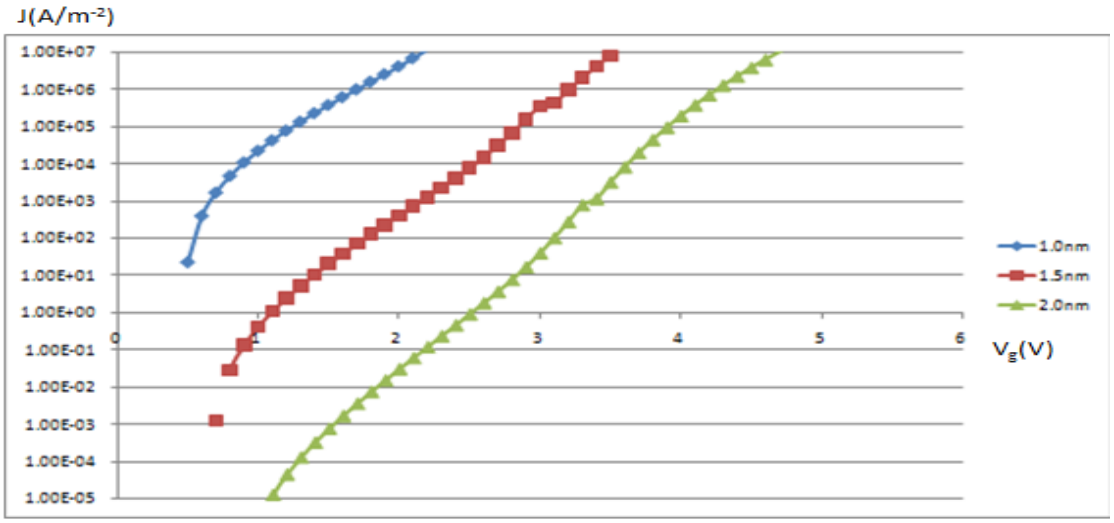

Fig.12 simulation result of leakage current under 1.0nm, 1.5nm and 2.0nm gate thickness situation in log10 scale.

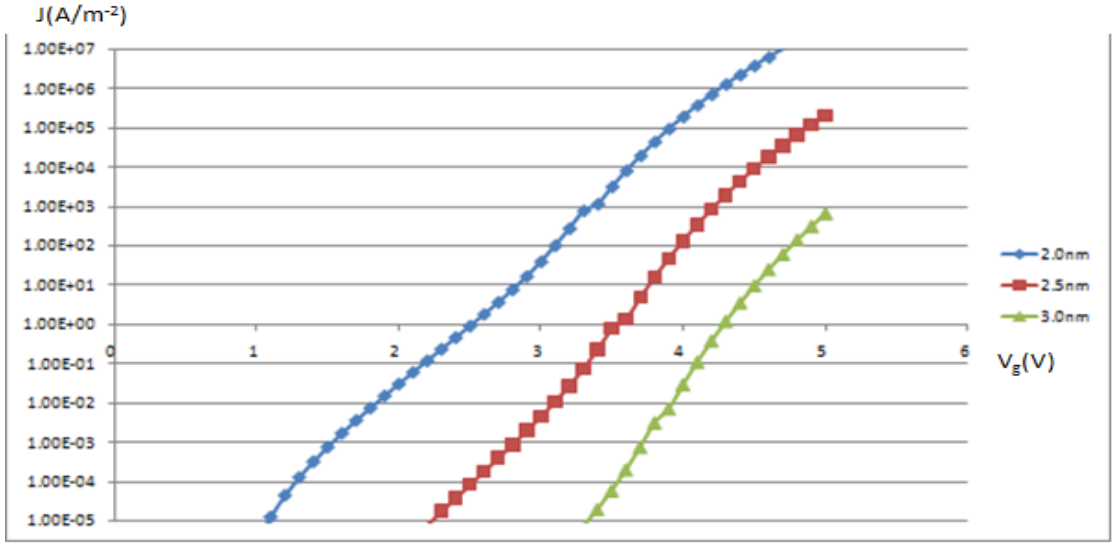

Fig.13 simulation result of leakage current under 2.0nm, 2.5nm and 3.0nm gate thickness situation in log10 scale.

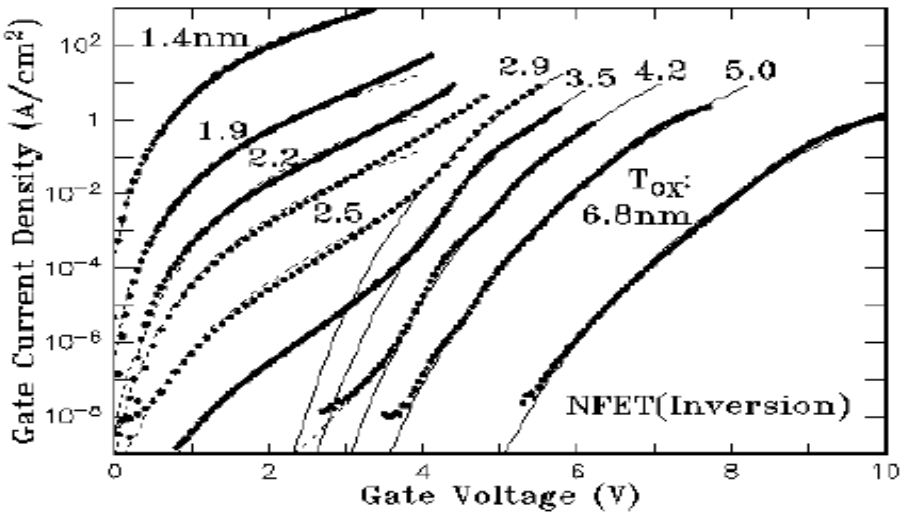

Fig. 14 Measured tunneling currents (solid dots) for a wide range of oxide thickness from 1.4nm to 6.8nm at 30℃ in n+-type polysilicon/NFET inversion. The solid and dashed lines represent the calculation using the FN expression and using the semi-classic approach [21] for DT currents, respectively. [8]

C. Simulation Result of TDDB time

Fig. 15 16 and 17 are the simulation result of TDDB time by using the Physical based breakdown Model.

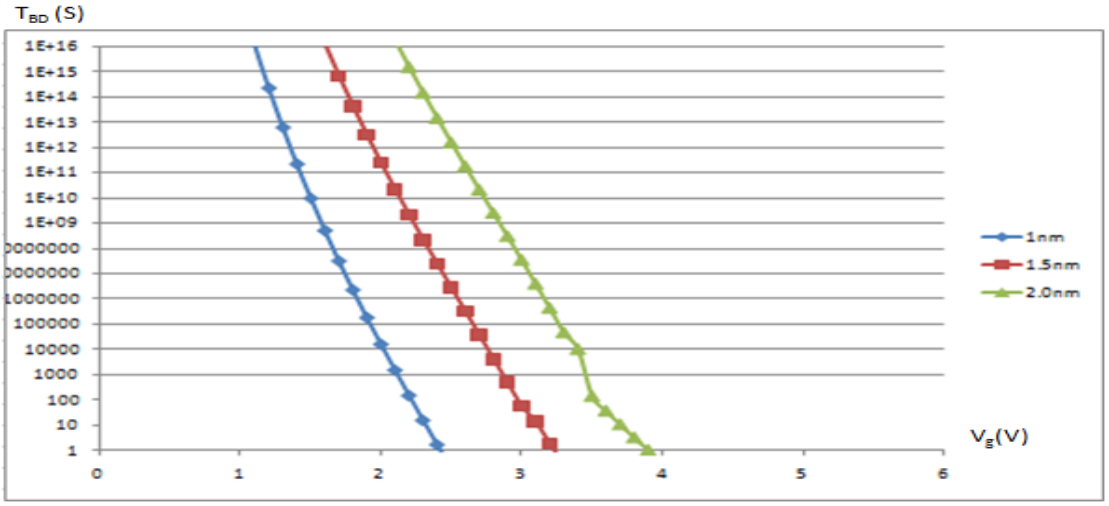

Fig.15 simulation result of TDDB lifetime under 1.0nm, 1.5nm and 2.0nm gate thickness situation in log10 scale.

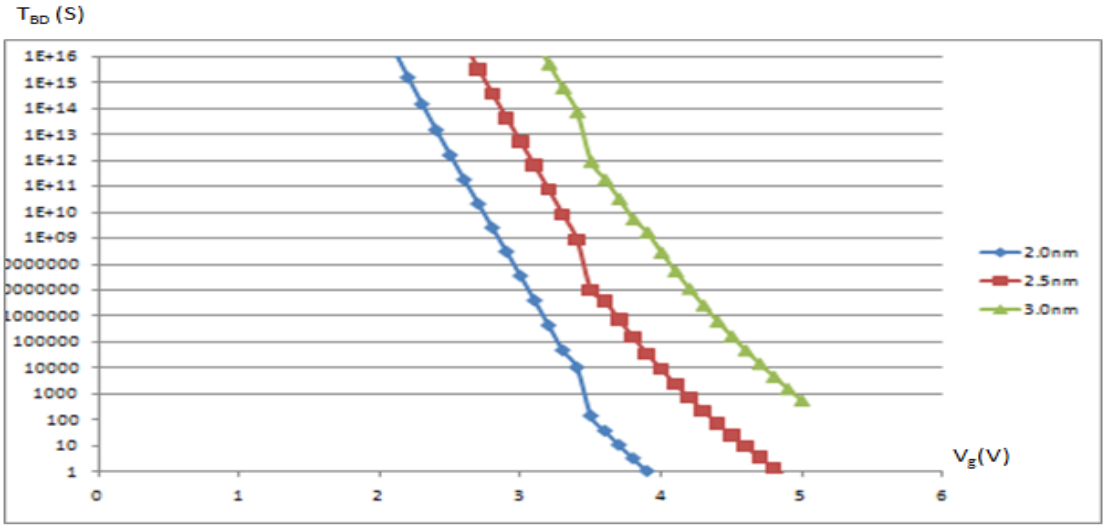

Fig.16 simulation result of TDDB lifetime under 2.0nm, 2.5nm and 3.0nm gate thickness situation in log10 scale.

Fig. 17, Fig.18 and Fig.19 could be linked together to see the difference between the simulation result and the actual experimental data. Similar liner connection could be concluded from the simulation result between 10^2 seconds and 10^6 seconds TDDB observation time zone.

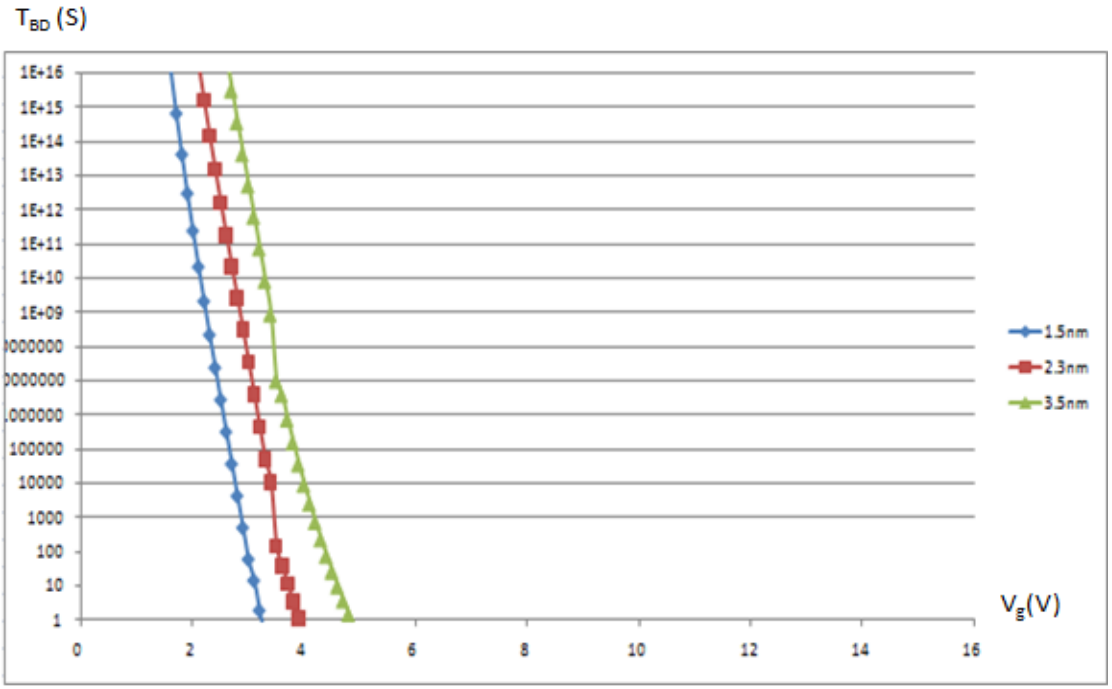

Fig.17 simulation result of TDDB lifetime under 1.5nm, 2.3nm and 3.5nm gate thickness situation in log10 scale

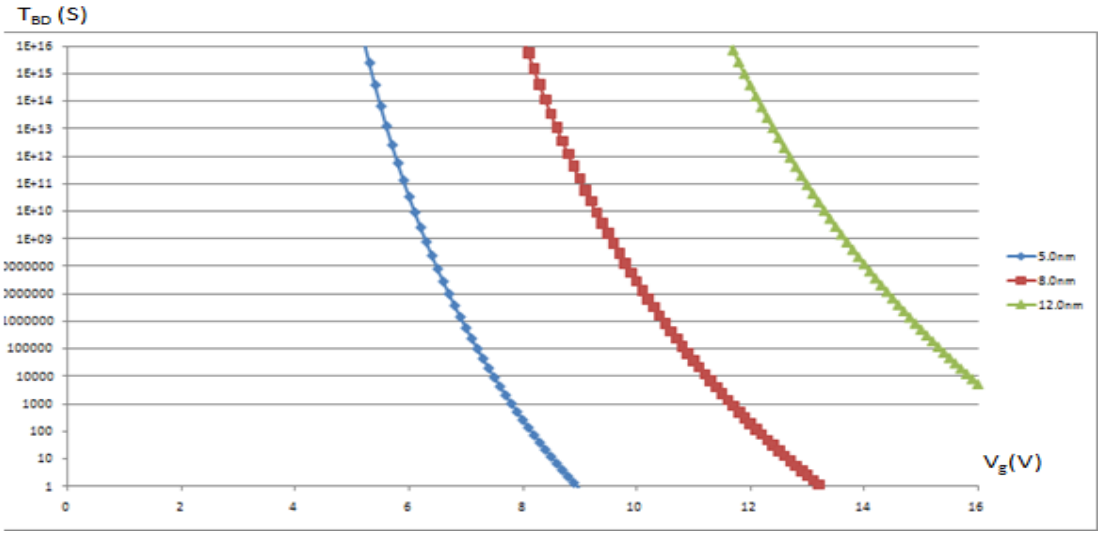

Fig.18 simulation result of TDDB lifetime under 5.0nm, 8.0nm and 12.0nm gate thickness situation in log10 scale

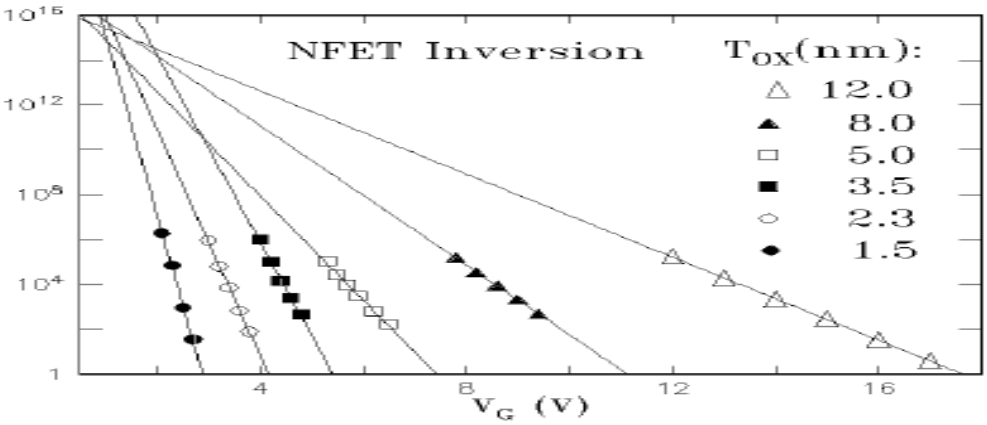

Fig.19 TBD data vs. gate voltages for NFET inversion mode at 140 ℃. The lines are from the least-square fit using TBD exponential law. All the TBD data plotted in Fig. 2 are scaled to the reference of 10-5cm^2. [8]

The log 10 scale of TDDB plot vs. Gate voltage almost shows a liner connection. This is probably due to that the observation time zone is too narrow to see the other nonlinear part of the graphic.

The simulation result is actually shifted towards right in voltage axis. This could be caused by the errors of calculating voltage stressed on the gate oxide layer and the mismatch in previous simulation of leakage current. The actual stressed voltage on the oxide layer might be smaller than calculation; and the leakage current should be bigger than calculation.

D. Simulation Result of threshold voltage vs. oxide thickness

The threshold voltage V_{th} of the gate is influenced by the thickness of the gate. The following equation is used to calculate the impact of the gate thickness on the threshold voltage:

$$V_t = V_{fb} + 2\psi_B + \frac{\sqrt{4*\varepsilon_{si}*q*N_a*\psi_B}}{C_{ox}} \quad (8)$$

V_{fb} and $2\psi_B$ are constant when the doping density (N_a) is fixed. V_{th} should have a liner connection with C_{ox}, which means V_{th} should also have a liner

connection with oxide thickness. The slope of the liner connection depends on the doping density of the body.

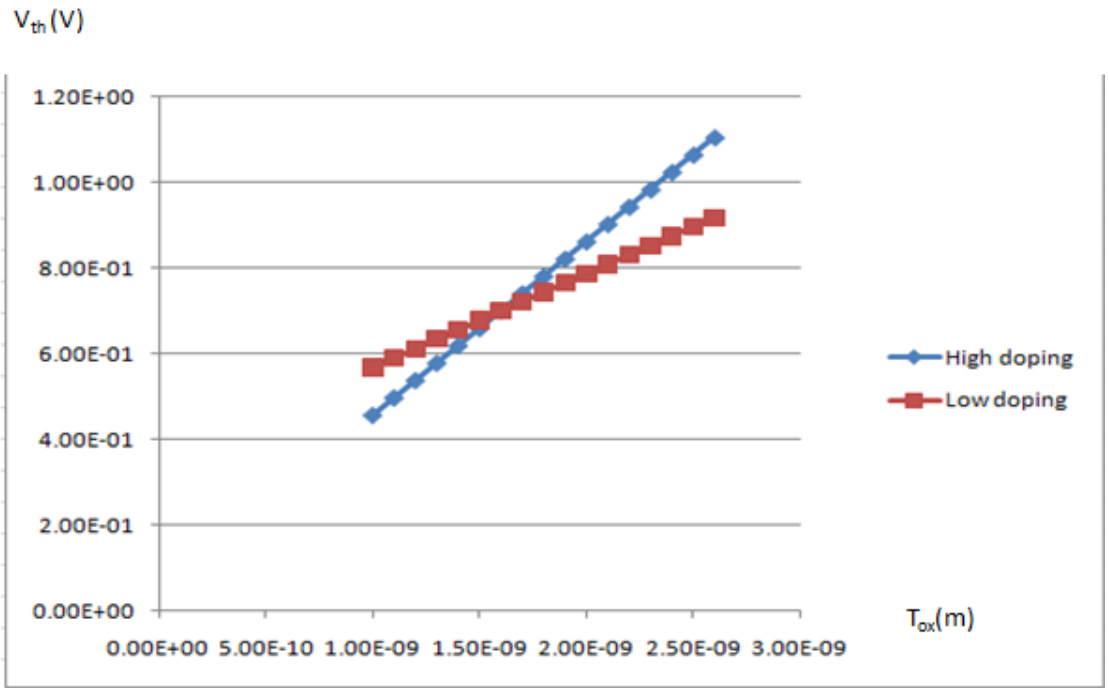

Fig.20 Threshold voltage vs. gate thickness under different doping density. The Vth0 is 0.7V under 32nm; and the default oxide thickness is 1.6nm.

As shown in Fig.20, the threshold voltage shows liner connection to the thickness. Thus, the delay trade off of decreasing oxide thickness also shows an approximate liner connection under thin oxide thickness.

V. Discussion

The reason of discussing soft breakdown is that soft breakdown process is closely connected to hard breakdown, and soft breakdown is inevitable for the current industry technology. High k material is also discussed here as high k material has been widely used already in the industry. Similar mechanism may happen in high K material TDDB.

A. Soft breakdown

As shown previously from Fig.15 to Fig.19, a proper choice of supply voltage, based on the circuit requirement of both lifetime and speed, is going to basically eliminate the influence of hard breakdown on the reliability in the design lifetime. However, the soft breakdown would happen eventually as stressed gate voltage always exists. Thus, the influence of soft breakdown cannot be ignored for the reliability of any design. Gate current increase is one of the most important changes of device after gate oxide breakdown

[23].The leakage current change vs. time could be expressed in the following equation[22][23]:

$$I_G(t) = I_0 \cdot \exp(t \cdot GR) \qquad (9)$$

The I_0 is the leakage current of oxide gate without any defect produced yet, and this initial leakage current could be obtained by using equation (2). GR is the gate current growing rate and it could be expressed as following [22]:

$$G_R = k_1 \cdot \exp(\beta V_g - \theta_1 \cdot T_{ox}) \quad (10)$$

K_1 could be calculated by the initial leakage current [22]. $\theta_1 = \ln\theta$, where θ is about 10/3. Depending on the change of current, the equivalent resistance can be obtained by using the leakage current and expressed in following equation [22]:

$$R_g(t) = \frac{V_{DD}}{I_0} \cdot \exp(- t \cdot GR) \qquad (11)$$

B. High-K material

The principle of the high K material break down, which is described by the Generated Subordinate Carrier Injection (GSCI) model, is similar to

conventional SiO_2 material. High energy electron or proton that tunnel (Frenkel-Poole tunneling or trap-assisted-tunneling) through the gate layer create defect in the layer.

The difference of conventional SiO_2 and high k material breakdown is that the structure difference of high k material gate and SiO_2, which may cause some difference in the breakdown modeling. First, the structure of high k gate is asymmetric in body-gate direction, thus the particle of the current causing trapping is different, which would result in different current value [24]. Secondly, breakdown is initiated in the interfacial layer and then followed by a correlated localized breakdown path in the high-K layer [25]. Previous studies suggest that the ultra-thin interfacial layer IL determines the high-K/IL stack breakdown and that the high-K layer has little impact on the breakdown statistics [25] [26]. Thus, the model used to describe high k is similar to the equation (1) that is for SiO_2. Based on the leakage current of high k gate and the mount of defect yielding in the gate, an accurate lifetime of high k gate could be maintained.

VI. Conclusion

For the conventional SiO_2 gate, the prediction of TDDB life time based on Physical based breakdown Model in log 10 scale shows similar liner connection vs. gate voltage in the 10^2-10^6 time window. Only a small part of the complete graphic could be observed in human lifetime, since 10 years only equal 10^9 second. The slope of such line is going to increase as the oxide thickness scales down, which means the reliability is more sensitive to voltage variances.

Such trend of reliability vs. voltage may give benefit to the use of several technologies. Multi supply voltage could face less trade off in achieving the same benefit of reliability compared to a regular design in non-performance required situation, as the gate oxide thickness almost shows linear connection to delay trade off under thin oxide thickness situation (3nm). Another technology may benefit from this trend is power gating. Power gating is initially designed for saving power, not for enhancing reliability. The margin of available voltage for old technology is quite wide. The

lifetime of circuit is long enough for high performance required when we increase the supply voltage. However, the reliability is more sensitive to the voltage as the technology scale down, and the increase of supply voltage for high performance would reduce the lifetime significantly. Thus, reducing the stressed time of gate by using power gating would ameliorate the reliability impact of increasing voltage.

The TDDB mechanism of high k and SiO_2 are similar and models for high k could be borrowed from SiO_2 based on the understanding of the physic mechanism.

Soft breakdown is a major issue for both high k and SiO_2 material. As the hard breakdown would be properly avoided by a careful choice of supply voltage, depending on both lifetime and speed requirement, soft breakdown is the major issue we need to worry about for the working condition of circuits in the future research.

Reference

[1] Lee, J.C. , Chen Ih-Chin , and Hu Chenming , “Modeling and Characterization of Gate Oxide Reliability,” IEEE Trans. Electron Devices, vol. 35, no. 12, pp. 2268–2278, Dec. 1988.

[2] J . W. McPherson and D. A. Baglee, “Acceleration factors for thin gate oxide stressing,” in Int. Rel. Phys. Symp., p. 1, 1985.

[3] E. Wu, A. Vayshenker, E. Nowak, J. Su ñé, R.-P. Vollertsen, W. Lai, and D. Harmon, “Experimental Evidence of TBD Power-law for Voltage acceleration Factors for Ultra-Thin Gate Oxide,” IEEE Trans. Electron Device. Vol.49, pp.2244-2253, 2002.

[4]. R. Duschl and R.-P. Vollertsen, “Voltage Acceleration of Oxide Breakdown in the sub-10nm Fowler-Nordheim and Direct Tunneling Regime,” IEEE International Integrated Reliability Workshop, Final Report, pp.44-48, 2005.

[5]. R.-P. Vollertsen, T. Pompl, R. Duschl, A. Kerber, M. Kerber, M. Röhner, and R. Schwab, “Long term gate dielectric stress – a timely method?”

Digest of the 2006 International Electron Device Meeting, pp. 747-750, 2006.

[6] S. Lombardo, F. Crupi, A. La Magna, and C. Spinella. “Electrical and thermal transiet during dielectric breakdown of thin oxides in metal-SiO2-silicon capacitors,” Journal of Applied Physics, 84(1):472 – 479, July 1998.

[7] Chenming Hu and Qiang Lu, ”A unified gate oxide reliability model”, In IEEE International Reliability Physics Symposium, pages 47 – 51, 1999.

[8] E. Wu, J. Sune, and R. P. Vollersten, “Comprehensive physics-based breakdown model for reliability assessment of oxides with thickness ranging from 1 nm up to 12 nm,” in Proc. 47th Annu. IEEE Int. Rel. Phys. Symp., 2009, pp. 708–717.

[9] Klaus F. Schuegraf and Chenming Hu, “Hole injection SiO2 breakdown model for very low voltage lifetime extrapolation.” IEEE Transaction on Electron Devices, 41(5):761 – 767, May 1994.

[10] Takayuki Tomita, Hiroto Utsunomiya, Yoshinari Kamakura, and Kenji

Taniguchi, “Hot hole induced breakdown of thin silicon films.” Applied Physics Letters, 71(25):3664 – 3666, December 1997.

[11] J.W. McPherson and H.C. Mogul. “Underlying physics of the thermochemical E model in describing low-field time-dependent dielectric breakdown in sio2 thin films.” Journal of Applied Physics, 84(3):1513 – 1523, August 1998.

[12] T. Pompl, H. Wurzer, M. Kerber, and I. Eisele. “Investigation of ultra-thin gate oxide reliability behavior by seperate characterization of soft breakdown and hard breakdown.” In IEEE International Reliability Physics Symposium, pages 40 – 47, 2000.

[13] Jordi Su˜n´e and Ernest Wu. “A new quantitative hydrogen-based model for ultra-thin oxide breakdown.” In Symposium on VLSI Technology, pages 97 – 98, 2001.

[14] Felice Crupi, Ben Kaczer, and Guido Groeseneken. “New insights into the relation between channel hot carrier degradatin and oxide breakdown in short channel nMOSFETs.” IEEE Electron Device Letters, 24(4):278 – 280,

April 2003.

[15] Slimane Oussalah and Boualem Djezzar, “Field Acceleration Model for TDDB: Still a Valid Tool to Study the Reliability of Thick SiO2-Based Dielectric Layers?”. IEEE Transactions on Electron Devices, Volume: 54, Issue: 7 On Page(s): 1713 - 1717, July 2007.

[16] A. Cester. “Wear-out and breakdown of ultra-thin gate oxides after irradiation.” Electronics Letters, 38(19):1137 – 1139, Sept. 2002.

[17] KAUSHIK ROY, SAIBAL MUKHOPADHYAY AND HAMID MAHMOODI-MEIMAND, “Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Sub micrometer CMOS Circuits”, Proceedings of the IEEE, Volume: 91, Issue: 2 On Page(s): 305 - 327, Feb 2003.

[18]--- , Fundamentals of Modern VLSI Devices. New York: Cambridge Univ. Press, 1998, ch. 2, pp. 95–97.

[19] J. Suñé and E. Wu, “Mechanisms of Hydrogen Release in the Breakdown of SiO2-based gate oxides,” Digest of the International Electron

Device Meeting, pp. 388-391, 2005.

[20] J. Suñé, "New Physics-Based Analytic Approach to the Thin Oxide Breakdown Statistics," IEEE Electron Device Lett., vol.22, p.296-298, 2001.

[21] W. Lee and C. Hu, "Modeling CMOS Tunneling Currents Through Ultrathin Gate Oxide Due to Conduction- and Valence- Band Electron and Hole Tunneling," IEEE Trans. Electron Devices, vol. 48, pp. 1366-1373, 2001.

[22] B. P. Linder, J. H. Stathis, D. J. Frank, S. Lombardo, and A. Vayshenker, "Growth and scaling of oxide conduction after breakdown," in IRPS, 2003, pp. 402–405.

[23] J. Qin, X. J. Li, and J. B. Bernstein, "SRAM Stability Analysis Considering Gate Oxide SBD, NBTI and HCI," in Proc. IEEE IIRW, Oct. 2007, pp. 33-37.

[24] Okada, K.; Mizubayashi, W.; Yasuda, N.; Satake, H.; Ota, H.; Kadoshima, M.; Tominaga, K.; Ogawa, A.; Iwamoto, K.; Horikawa, T.; Nabatame, T.; Toriumi, A. , "Model for Dielectric Breakdown Mechanism of HfA10x/Si02 Stacked Gate Dielectrics Dominated by the Generated Subordinate Carrier

Injection," Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International

[25] Mora, P. ; Monsieur, F. ; Rafik, M. ; Guarin, F. ; Yang, G. ; Roy, D. ; Chang, W.L. ; Stathis, J. "High-K gate stack breakdown statistics modeled by correlated interfacial layer and high-k breakdown path," Reliability Physics Symposium (IRPS), 2010 IEEE International, On Page(s): 364 - 368

[26] Kang, C.Y. ,SEMATECH, Austin, TX, Park, C.S. ; Heh, D. ; Young, C. ; Kirsch, P. ; Park, H.B. ; Choi, R. ; Bersuker, G. ; Yang, J.-W. ; Lee, B.H. ; Lichtenwalner, J. ; Jur, J.S. ; Kingon, A.I. ; Jammy, R, "Performance and Reliability Characteristics of the Band Edge High-k/Metal Gate nMOSFETs with La-doped Hf-Silicate Gate Dielectrics," Reliability Physics Symposium, 2008. IRPS 2008. IEEE International, Page(s): 663 - 664