ANALYSIS OF IMPACT OF TRANSISTOR AGING EFFECTS ON CLOCK SKEW IN NANO-SCALE CMOS

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CERTIFICATE OF APPROVAL

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ANALYSIS OF IMPACT OF TRANSISTOR AGING EFFECTS ON CLOCK SKEW IN NANO-SCALE CMOS

Mandeep Singh Randhawa

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Transistor aging effects in Nano-scale CMOS result in transistor performance degradation over the device life-time. The primary physical mechanism behind transistor aging is Bias Temperature Instability (BTI). Such transistor aging results in circuit performance degradation over time. In this research we are interested in analyzing the impact of the BTI aging effect on clock skew in on-chip clock distribution networks. Clock skew is an important parameter in the clock distribution. It is defined as the maximum time difference between the clock signals received at different end points of a clock distribution network on a chip. The reason for clock skew could be process variations, temperature, or capacitance differences across the clock network. Ideally the clock signal has to be fully synchronous everywhere on a chip (i.e. clock skew of zero), but in reality we get some limited clock skew in the order of a few Pico-Second. If clock skew becomes too high, it can result in timing errors in synchronous designs. In this research, we have analyzed and quantify the impact of transistor aging effects on clock skew. We have simulated an H-tree clock distribution network and analyzed how the transistor aging affects clock skew over a period of 2 years. Our results show that the V_t mismatch and low temperature mismatch induced clock skew reduces as a result of transistor aging over time, whereas capacitance mismatch and high temperature mismatch induced clock skew increases over time a result of transistor aging. In a 32nm technology node, the clock skew aging could be in the range of -26% to +36% depending on mismatch cause of clock skew.

I certify that the Abstract is a correct representation of the content of this thesis.

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Chair, Thesis Committee Date

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1. INTRODUCTION

Clock skew has emerged as a big performance limiting factor in sub 65nm technologies. Its cause could be process variation, temperature mismatch or capacitance mismatch. Moreover, due to transistor aging effects in Nano-scale, circuit delay will increase over lifetime. Aging also impacts the clock skew over lifetime.

Aging effect has become a critical issue as the size of transistors is scaling down. Bias Temperature Instability (BTI) effect can be further divided into NBTI and PBTI. NBTI effect degrades the performance of PMOS over time by increasing its threshold voltage. Similarly PBTI effect degrades the performance of NMOS. As the use of High K materials is increasing; PBTI effect is also increasing. In [5] and [6], authors have discussed how variability in process, temperature and power fluctuation could affect clock skew, whereas in our work we have incorporated the effect of aging along with temperature and capacitance mismatch. This is the first paper which has incorporated the effects of temperature and capacitance mismatch along with aging effects. We also used realistic temperature profile of a chip [3]; to calculate the effect of aging and performed simulations to obtain clock skew results over the 2-year period.

In this research we have simulated an H- tree clock distribution network in a predictive 32 nm technology [1]. The clock distributions network is a two-level H-tree as shown in Fig. 1. There is one H tree in the first level and 4 H-trees in the second level. A single H-tree has 6 buffers; therefore there are 30 buffers in the entire H-tree network. The buffers used in this H-tree network are CMOS inverters made using PMOS and NMOS transistors. The second level H-trees are situated at the four end nodes of the first level H-tree; they receive input from the end nodes of the first level H tree.

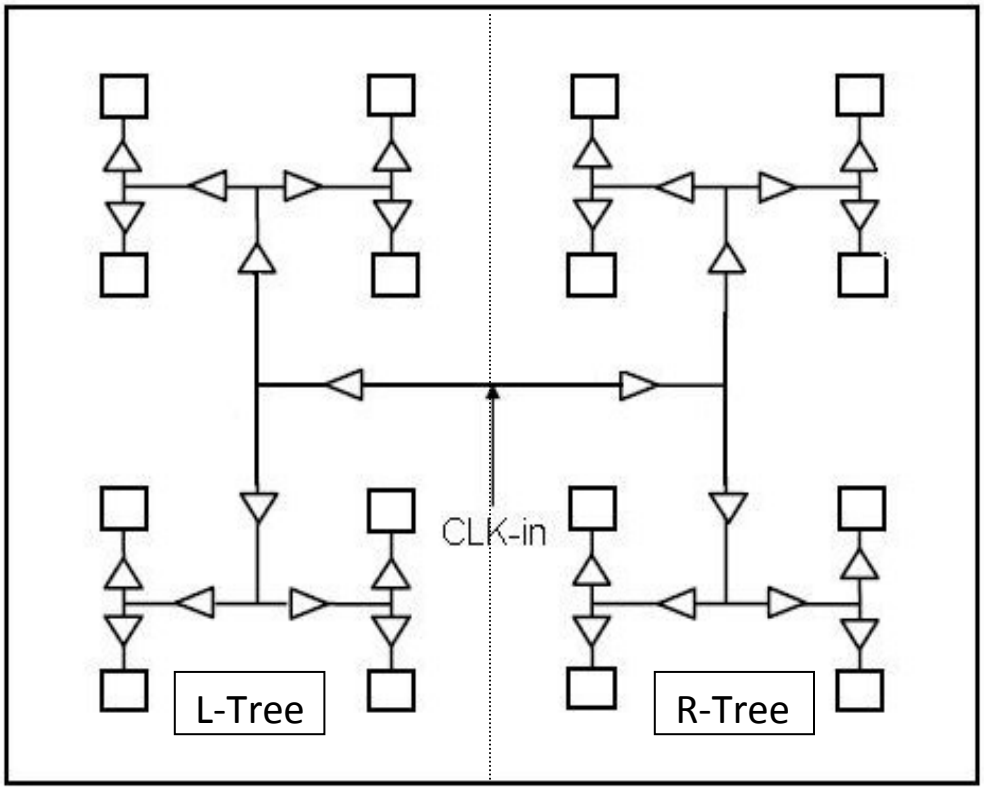

Fig. 1: 2-Level H-Tree

The contributions in this work are as follows:

- We have performed an analysis of combined effect of NBTI and PBTI on clock skew
- We have performed the clock skew aging analysis under V_t, temperature, and capacitive mismatch.

- We show that the clock skew reduces by transistor aging when the cause of mismatch is Vt or low temperature difference. We show that the clock skew increases by transistor aging when the cause of mismatch is capacitance or high temperature difference.
- We have performed clock skew aging analysis using a realistic temperature profile of a test chip.

2. BTI MODEL

High temperature and temperature stress on gate causes the threshold voltage to increase. This process is called Bias Temperature Instability (BTI). When Silicon oxide was used as gate material, major focus was on negative BTI (NBTI) which degrades the performance of PMOS. Nowadays when high K material is being used as gate material, positive BTI (PBTI) effect is growing significantly.

In our research, we have used a simplified BTI model discussed in [2]. In this model, V_t shift is calculated by the following equation:

$$\Delta V_t = K_v \cdot \beta^{0.25} \cdot t^{0.25} + \delta_v \qquad (1)$$

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}(V_{gs}-V_{th})} \cdot \exp\left(\frac{E_{ox}}{E_o}\right) \cdot \left[1-\frac{V_{ds}}{\alpha(V_{gs}-V_{th})}\right] \cdot \exp\left[\frac{-E_a}{kT}\right] \qquad (2)$$

$$E_{ox} = (V_{gs} - V_{th})/T_{ox} \qquad (3)$$

$$T_{ox} = EOT = (3.9/K)t_{hk} \qquad (4)$$

In the above equation K_v is the rate of generation of H^+ species, β represents the percentage of time the device is under stress, and t is time, which in our case is up to 2 years. Effective oxide thickness is represented by T_{ox}, K is the relative permittivity of the high K dielectric material, t_{hk} is the thickness of the high K dielectric. V_{gs} is the gate to source voltage, V_{th} is the threshold voltage, V_{ds} is the drain to source voltage, C_{ox} is the oxide capacitance per unit area, E_{ox} is the electric filed in the oxide, E_a is the activation energy, k is the Boltzmann constant and T is temperature. Rest of the parameters δ_v , A, E_o, α are constants taken from [2]. Fig. 2 below shows the percentage of NBTI induced V_t shift in high K dielectric 32 nm PMOS over a period of 2 years.

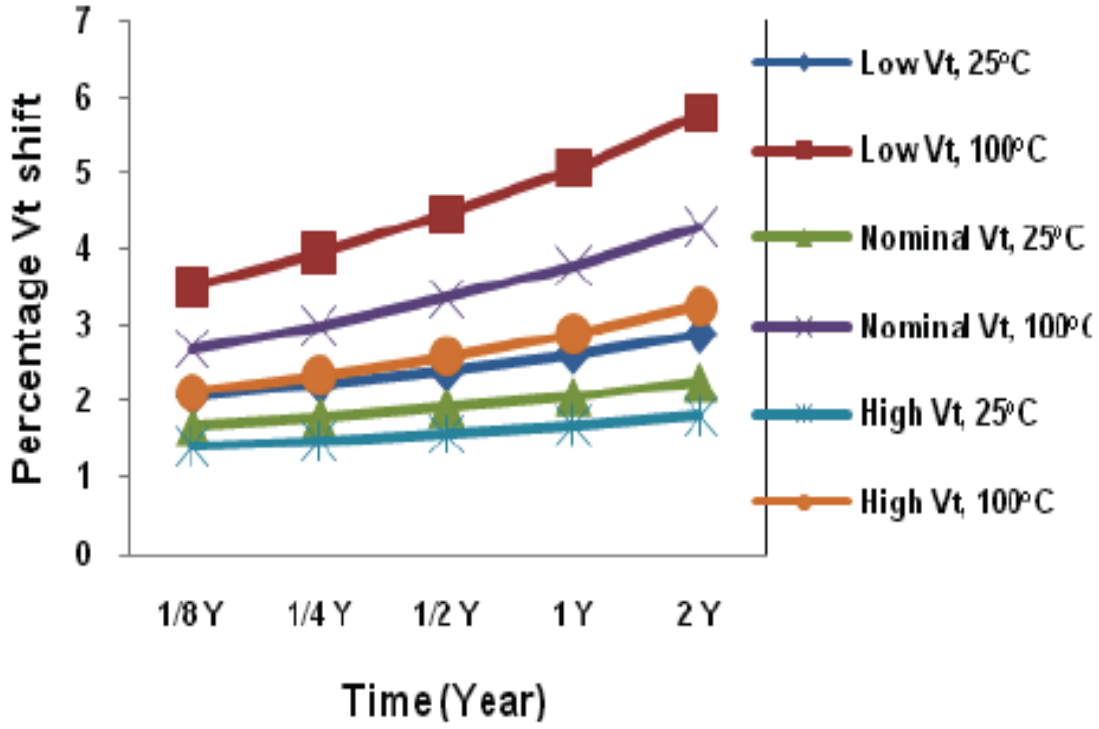

Fig. 2: Percentage of NBTI induced V_t shift in high K dielectric 32 nm PMOS

3. Aging of Clock Skew under V_t Mismatch

Clock skew is caused by mismatch in transistors and wires of H-Tree, such as V_t, temperature, and capacitance mismatch. In this section we focus on V_t mismatch and the impact of transistor aging. To simplify the mismatch analysis, we have divided the H-tree into two halves; namely the left half (L-Tree) and the right half (R-Tree), as shown in Fig. 1. The clock buffers in the L-Tree are assigned low V_t and the clock buffers in the R-Tree are given high V_t. The V_t mismatch of 50mV if applied between the L-Tree and R-Tree. The temperature of both sides is set at 100°C. In order to record the initial values of skew; Hspice simulation is run and the waveforms of final clock nodes are plotted. For waveforms, we carefully select the final node of H-tree that show maximum value of clock skew. For aged clock skew readings; we calculated the values of V_t shift (NBTI and PBTI) over a period of 2 years using the Eq. (1). It is evident from Eq. (2) and (3) that the value of V_t shift depends on initial V_t.

We estimate the Vt shift for each transistor considering its own initial V_t. This calculated value of V_t shift is applied to the H–tree to estimate clock skew after 2 years. Then the Hspice simulation is run again and results are recorded in the same way by plotting the clock signals showing maximum skew. A lower Vt transistor experiences more electric field stress (E_{ox} in Eq. (3)) and hence experiences more Vt shift compared to a high V_t transistor. Low V_t clock buffers show less delay compared to high V_t clock buffers. However, the low V_t transistors age at a faster rate than high V_t transistors, as predicted by Eq. 1, 2, and 3.

Hence, it is expected that the degree of mismatch between a low V_t and a high V_t transistor should reduce over time, resulting in less clock skew over time. This expectation is confirmed by the clock skew results shown in Fig. 3. In this case, the clock skew reduces by 7.5% over a 2-year lifetime.

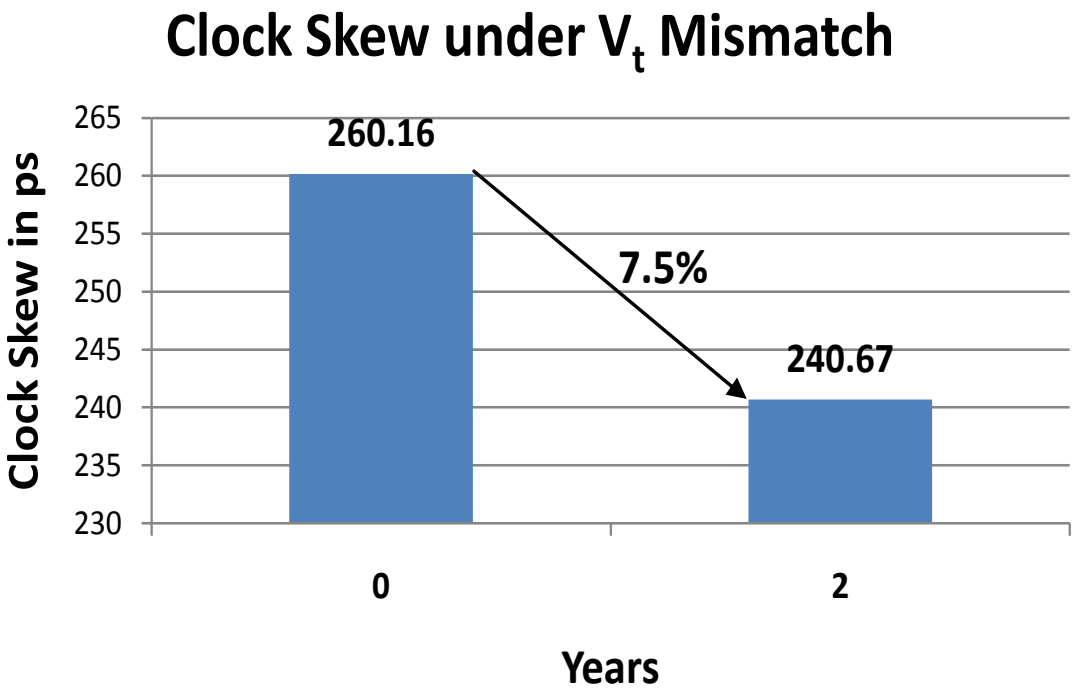

Fig. 3: Aging of clock skew with 50mV initial Vt mismatch

4. Aging of Clock Skew under Temperature Mismatch

In this section we focus on temperature mismatch and the impact of transistor aging. The L-Tree is assigned lower temperature and the R-Tree is assigned higher temperature. The temperature mismatches we have applied are +/- 10, +/-20 and +/-30 ℃. The chip temperature in case of 10 ℃ mismatch is set at 100 ℃ and therefore +/- 10 ℃ will correspond to 110 and 90 ℃ respectively. The assigned chip temperature for 20 ℃ mismatch is set at 90 ℃. Hence, +/- 20 mismatches will correspond to 110 and 70 ℃ respectively. For 30 ℃ mismatch, chip temperature is set at 80 ℃ and +/- 30 is used to assign the temperature of 50 ℃ to L-Tree side and 110 ℃ to R-Tree side of the H-tree. Temperature has a strong influence on the aging. The rate of aging is higher at higher temperatures as predicted by Eq. (2). We estimate the V_t shift for each transistor considering its own operating temperature.

It is observed that the clock skew increases by transistor aging under large temperature mismatch (20 and 30 ℃). The increase in clock skew over a 2-year period is 36% and 18.3%, for the 20 and 30 ℃ mismatch cases, respectively. The increased clock skew is due to uneven aging of the transistors in the L-Tree and R-Tree because of having different operating temperature. However, under low temperature mismatch of 10 ℃, the clock skew reduces over the 2 year lifetime by 26%. This is due to the fact that higher temperature lowers V_t but increases the rate of V_t increase caused by aging. For low temperature mismatch, the difference in the rate of V_t shift between the L-Tree and R-Tree results in a more balanced propagation delay through the H-tree over time, causing clock skew reduction. This effect is not observed when the temperature mismatch is too much. Fig. 4 shows the results of the above mentioned simulations.

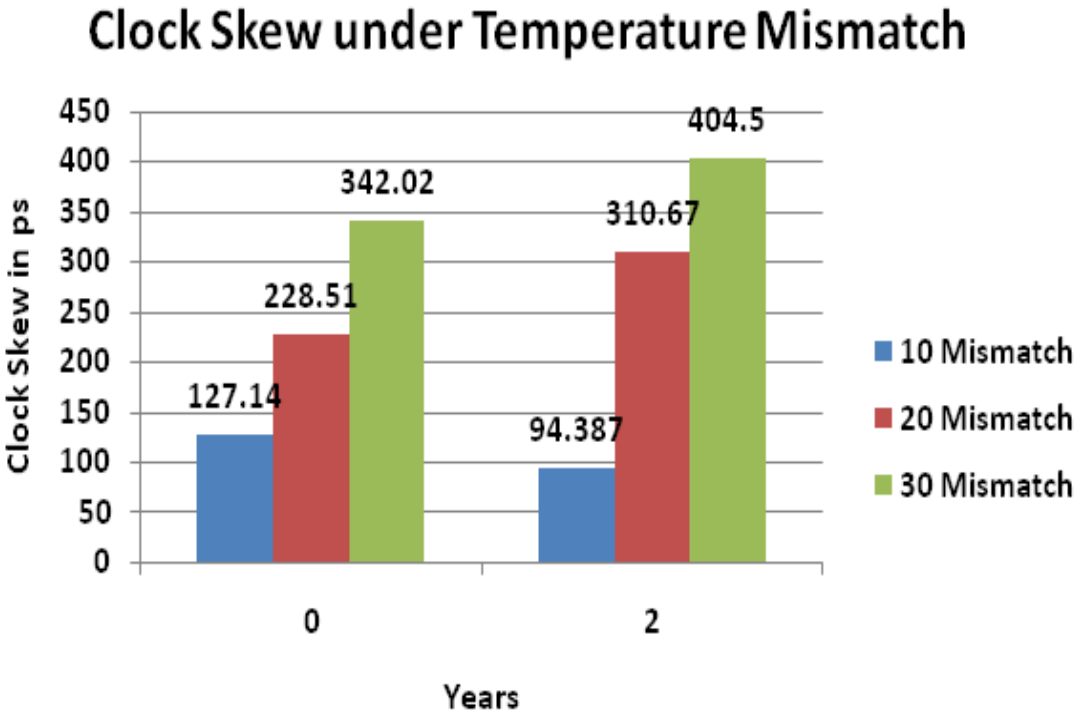

Fig 4: Aging of clock skew with 10, 20 and 30 °C temperature mismatch over a period of 2 years.

5. Aging of Clock Skew under Capacitance Mismatch

In this section, we investigate aging of clock skew caused by capacitance mismatch. For this purpose, we have used same V_t transistors on both sides of the H tree but we reduced the values of capacitances in the L-Tree side by 10%. Chip temperature is uniformly set at 100 °C and initial clock skew results are obtained by running Hspice simulation. In order to obtain the aged value of clock skew, we applied the estimated value of V_t shift to the H-Tree. Skew results are obtained by plotting clock signals showing maximum skew between the L-Tree and R-Tree side of the H-tree network. Fig. 5 shows the aging of the clock skew in this case. The results clearly indicate that even under capacitance mismatch, the magnitude of clock skew increases by 6.4% over a period of two years. This is despite the fact that in this case the aging of the transistors is uniform because they all have same V_t and operating at same temperature.

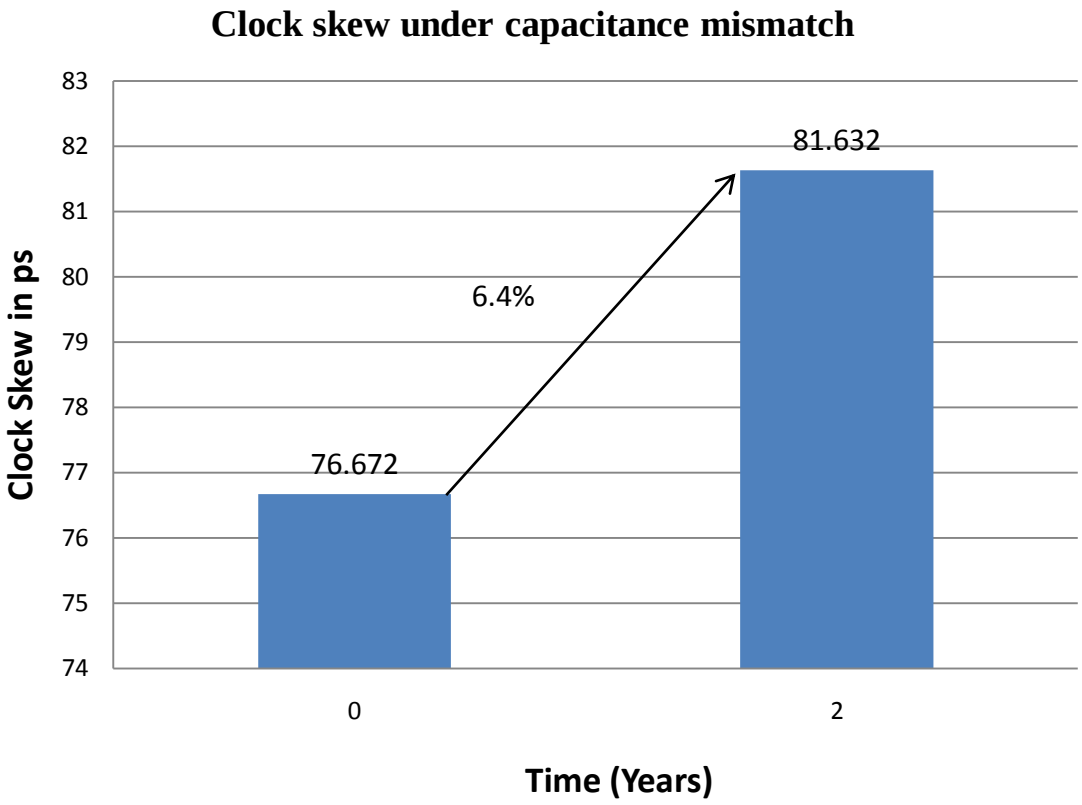

Fig. 5: Aging of clock skew with 10% capacitance mismatch.

6. Aging of Clock Skew under Realistic Temperature Profile

In order to consider more realistic mismatch scenarios, we have used the temperature profile of a chip as discussed in [3] and applied it to our H-tree network. Fig. 6 shows the spatial temperature profile used for this study. All transistors are given same V_t.

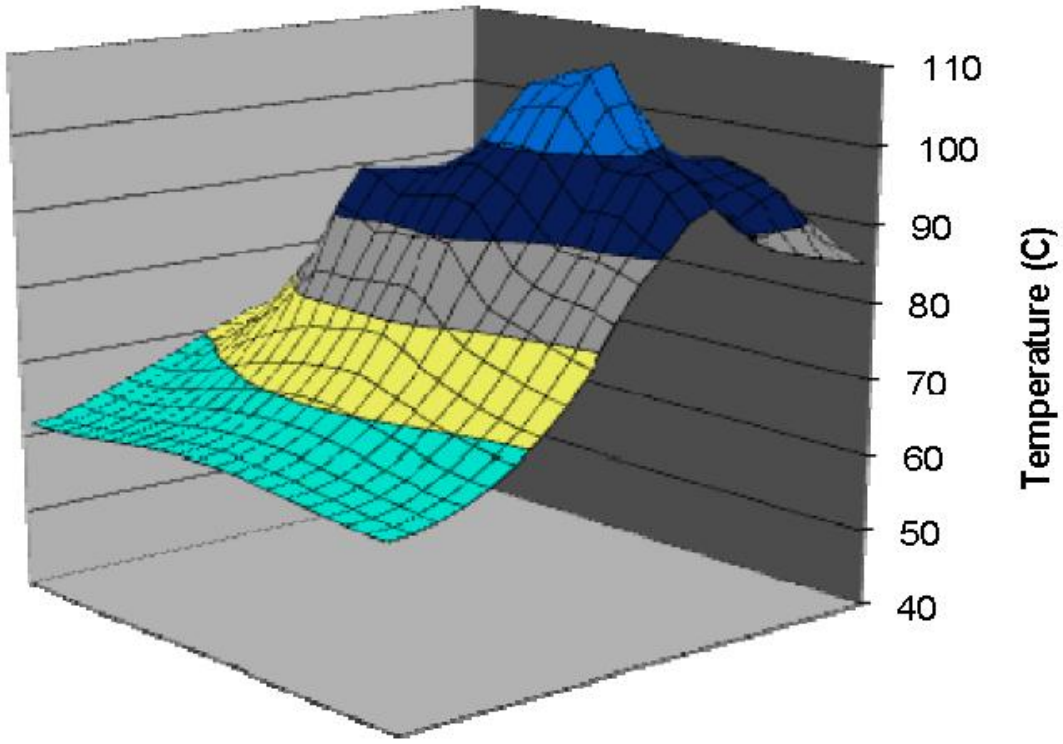

Fig. 6: Realistic chip temperature profile

In this case, every clock buffer in the H-tree is assigned a unique temperature obtained from the spatial temperature profile. Moreover, since each clock buffer is at a different temperature, the aging of each buffer will be different. The aging induced V_t shift is strongly temperature dependent as modeled by Eq. (2). We estimate the V_t shift of each transistor considering its own operating temperature. The initial clock skew is obtained by plotting waveforms from all the 16 end nodes of the H-tree and measuring the maximum skew. Then, the calculated values of V_t shift for 2-year lifetime are applied to individual buffers of the H-tree. Aged clock skew result is obtained by plotting 16 waveforms from all the end nodes of H tree network and measuring maximum skew. Fig. 7 below shows the increase in clock skew over a period of 2 years. The results indicate a significant increase of 18.68% over the period of 2 years. The results show that the aging increases the clock skew significantly.

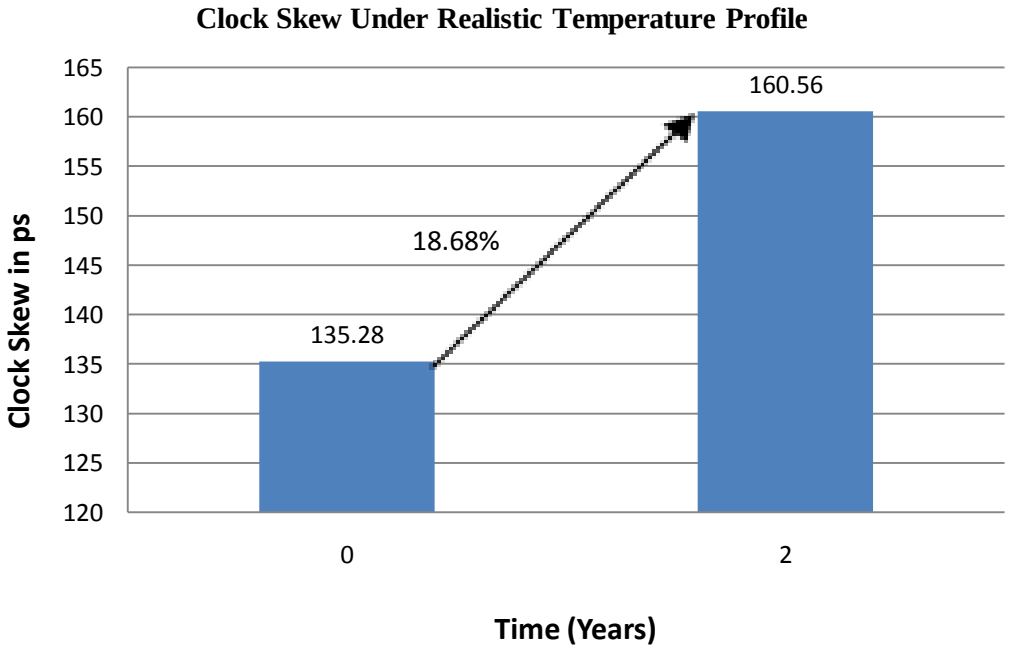

Fig. 7: Clock skew aging under realistic temperature profile.

7. CONCLUSION

In this research, we have analyzed how the magnitude clock skew varies under transistor aging effects over a period of 2 years. We have analyzed the clock skew aging under different scenarios of mismatch. It is observed that V_t mismatch and low-temperature mismatch induced clock skew reduced by transistor aging whereas the high temperature mismatch and capacitance mismatch induced clock skew increases over time by transistors aging. We have applied a realistic temperature profile of a chip into our clock tree and measured clock skew aging by applying aging to the clock buffers depending on their individual operating temperatures. The results show that clock skew is increasing over a period of two years. Results indicate that the best way to manage clock skew under transistor aging is to achieve a more uniform temperature profile for the chip. Under low temperature mismatch, it is possible that the clock skew may even reduce over lifetime.

8. REFERENCES

[1] Predictive Technology Models: http://ptm.asu.edu

[2] R. Vattikonda, W. Wang, Y. K. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," *Design Automation Conference, 2006 43rd ACM/IEEE* , vol., no., pp.1047-1052.

[3] Pei-Yu Huang, Chih-Kang Lin, Yu-Min Lee, Nat. Chiao Tung Univ., Hsinchu, Taiwan "Full chip thermal analysis for early design stage via Generalized Integral Transforms" Design Automation Conference, 2008. ASPDAC 2008, Asia and South Pacific.

[4] Pullela, S. Menezes, N. Omar, J. Pillage, L.T. "Skew and delay optimization for reliable buffered clock trees" Computer-Aided Design, 1993. ICCAD-93, Digest of Technical Papers, 1993 IEEE/ACM International Conference 1993.

[5] Hashimoto, M. Yamamoto, T. Onodera, H. Dept. of Communication & Computer Eng., Kyoto Univ., Japan "Statistical analysis of clock skew variation in H-tree structure" Quality of Electronic Design, 2005. ISQED 2005, Sixth International Symposium 2005.

[6] Narasimhan, Ashok; Sridhar, Ramalingam; Dept. of Computer Sci. & Eng., Buffalo Univ., NY "Impact of Variability on Clock Skew in H-tree Clock Networks" Quality Electronic Design, 2007, ISQED '07, 8th International Symposium 2007.