School of Engineering

Electrical and Computer Engineering

Master Oral Defense

Title: OPTIMIZATION OF SUPPLY VOLTAGE FOR MININUM ENERGY IN POWER GATED CIRCUITS IN NANO-SCALE CMOS

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Abstract:

Technology scaling according to Moore's law has resulted in the development of integrated chips; it has also posed several limitations in terms of power consumption and performance. Voltage scaling in particular has led to several tradeoffs. One of its tradeoffs is its effect on the power consumption. As the supply voltage (Vdd) is scaled down to voltage below the threshold voltage (Vt) value, the sub threshold leakage current (Ileak) increases and hence the static power dissipation increases. It has been noticed that, due to scaling, the static power is contributing to almost 40% of the total power consumption.

Power gating is one of the methods that can be employed in order to mitigate the risk of increasing leakage current. Dynamic power gating is a technique that can be used to dynamically turn the sleep transistor ON only for the time period the circuit performs the computation and immediately switches to OFF when the circuit is inactive. As the sleep transistor will be ON during the computation period, the leakage current is mitigated and hence overall power consumption is reduced. This research is performed inorder to determine an optimal value of supply voltage by performing dynamic powergating and voltage scaling to design a low power circuit.