Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

TITLE: *Analysis of Clock Skew under combined effects of Transistor Aging, Temperature and Capacitance mismatch in Nano-scale CMOS.*

PRESENTER: **Mandeep Randhawa**

TIME & DATE: **3.30 to 4.30pm, April 21st, 2010** **LOCATION:** **SCI 256**

COMMITTEE CHAIR: **Dr. Hamid Mahmoodi**
COMMITTEE MEMBERS: **Dr. Hao Jiang**

ABSTRACT

Transistor aging effects in Nano-scale CMOS result in transistor performance degradation over the device life-time. The primary physical mechanism behind transistor aging is Bias Temperature Instability (BTI). Such transistor aging results in circuit performance degradation over time. In this research we are interested in analyzing the impact of the BTI aging effect on clock skew in on-chip clock distribution networks. Clock skew is an important parameter in the clock distribution. It is defined as the maximum time difference between the clock signals received at different end points of a clock distribution network on a chip. The reason for clock skew could be process variations, temperature, or capacitance differences across the clock network. Ideally the clock signal has to be fully synchronous everywhere on a chip (i.e. clock skew of zero), but in reality we get some limited clock skew in the order of a few Pico-Seconds. If clock skew becomes too high, it can result in timing errors in synchronous designs. In this research, we have analyzed and quantify the impact of transistor aging effects on clock skew.

We have simulated an H-tree clock distribution network and analyzed how the transistor aging affects clock skew over a period of 2 years. Our results show that the V_t mismatch and low temperature mismatch induced clock skew reduces as a result of transistor aging over time, whereas capacitance mismatch and high temperature mismatch induced clock skew increases over time a result of transistor aging.