School of Engineering

Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

TITLE: ***Low Power Scanner for High-Density Electrode Array Neural Recording***

PRESENTER: **Eli Lyons**

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COMMITTEE CHAIR: **Dr. Hamid Mahmoodi**
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ABSTRACT

There is an increasing amount of interest in measuring signals from electrogenic cells, such as neurons or cardiomyocytes. A current trend is to increase the density of electrodes for higher resolution readings. Reading from all locations in a large electrode array, for example an array with 10,000 electrodes, leads to significant power consumption in interfacing ICs. Excessive power consumption not only reduces battery life in implantable applications, but also raises the temperature and damages biological cells. The primary goal of this research is to design a low power integrated system that can be used in vivo for scanning the electrode arrays. The design presented provides three main modes of operation implemented in a low power fashion. A model created in Python provides input vectors and output comparison for the verification process of the Auto Calibration mode. Clock Gating is applied to the design with a reduction of power in the gate level simulation of more than 70% for all three modes of operation. Further power savings are observed with the application of Power Gating.