

Hamid Mahmoodi

Assistant Professor

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EDUCATION

Purdue University, West Lafayette, IN

PhD in Electrical and Computer Engineering, Aug. 2005
Thesis: Low-Power, High-Performance, and Robust Circuit Design in Nanoscale CMOS
Advisor: Professor Kaushik Roy

University of Tehran, Tehran, Iran

M.S. in Electrical and Computer Engineering, Aug. 2000
Thesis: Low-Power Design of Digital Systems Based on Adiabatic Switching Principles
Advisor: Professor Ali Afzali-Kusha

Iran University of Science and Technology, Tehran, Iran

B.S. in Electrical Engineering (with honors), Aug. 1998

PROFESSIONAL EXPERIENCES

School of Engineering, San Francisco State University, San Francisco, CA

- Assistant Professor of Computer Engineering, Aug. 2005-present

NanoElectronics Research Laboratory, Purdue University, West Lafayette, IN

- Graduate Research Assistant, Feb. 2001-August 2005
- Supervisor: Professor Kaushik Roy
- Active PhD research on low-power and high-performance circuit design for nanoscale technologies (the research was mostly funded by SRC and DARPA), fabricated 5 chips, filed 5 patents, and published numerous conference and journal papers

IC Design Center, University of Tehran, Iran

- Graduate Research Assistant, Oct. 1999-Dec. 2000
- Supervisor: Professor Ali Afzali-Kusha
- Active M.S. Research on Low-Power Digital Design Based on Adiabatic Switching Principles, fabricated one chip and numerous published conference and journal papers

Electronic Research Center, Iran University of Science and Technology, Tehran, Iran

- Design engineer in Automation and Control Laboratory to design control systems using microcontrollers and Programmable Logic Controllers (PLCs), May 1998-Oct. 1999
- Translated (from English to Persian) and published a textbook on PLCs, entitled "Programmable Logic Controllers: Principles and Applications"
- Designed a microcontroller based digital control laboratory
- Designed a serial EPROM programmer and emulator
- Designed an educational system for the Z80 microprocessor

Advanced Electronic Research Center, Iran Electronic Industries Co., Tehran, Iran

- Research Engineer, Oct. 1998-Oct. 1999
- Research on Satellite Command and Data Handling Systems

AWARDS AND HONORS

- 2006 IEEE Circuits and Systems Society VLSI Transactions Best Paper Award
- SRC Technical Excellence Award, an award given by the Silicon Research Corporation (SRC) to our research team at Purdue University lead by Prof. Kaushik Roy for excellent research contributions, Oct. 2005
- Inclusion of biography in the 60th diamond edition of “Who’s Who in America”, Oct. 2005
- Certificate of successful completion of essential teaching seminar for engineering faculty, Sep. 2005
- Competent Toastmaster Award by Toastmasters International for completion of the toastmasters international communication and leadership program, Feb. 2005
- Best paper award in IEEE International Conference on Computer Design, Oct. 2004
- Ranked 5th in the national graduate schools entrance examination in Electrical Engineering, Iran, July 1998
- Distinguished student in the field of Electronics Engineering in the academic year 1997-98, Iran University of Science and Technology, Feb. 1998
- 3rd place prize in the contest for “Scientific and Practical Student Projects”, Iran University of Science and Technology, June 1997
- Distinguished student in the field of Electronics Engineering in the academic year 1996-97, Iran University of Science and Technology, Feb. 1997

PUBLICATIONS**Published Journal Papers (Refereed):**

1. Y. Wang, H. Mahmoodi, L-Y. Chiou, H. Choo, J. Park, W. Jeong, and K. Roy, “Energy-efficient Hardware Architecture and VLSI Implementation of a Polyphase Channelizer with Applications to Subband Adaptive Filtering,” accepted for *Journal of Signal Processing Systems*
2. S. Bhunia, H. Mahmoodi, A. Raychowdhury, and K. Roy, "Arbitrary Two-Pattern Delay Testing Using A Low-Overhead Supply Gating," *Journal of Electronic Testing Theory and Applications*, June 2008.
3. H. Mahmoodi, V. Mohan, M. Cooke, and K. Roy, “Ultra Low Power Clocking Scheme Using Energy Recovery and Clock Gating,” accepted for *IEEE Transactions on Very Large Scale Integration Systems*
4. K. Kim, H. Mahmoodi, and K. Roy, “A Low-Power SRAM Using Bit-Line Charge-Recycling,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 446-458, Feb. 2008
5. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Reduction of Parametric Failures in Sub-100-nm SRAM Array using Body Bias," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 1, pp. 174-183, Jan. 2008
6. A. Datta, A. Goel, T. Cakici, H. Mahmoodi, D. Lekshmanan, and K. Roy, “Modeling and Circuit Synthesis for Independently Controlled Double Gate FinFET Devices”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 11, pp. 1957-1966, Nov. 2007
7. S. Mukhopadhyay, K. Kim, H. Mahmoodi, and K. Roy, “Design of a Process Variation Tolerant Self-Repairing SRAM for Yield Enhancement in Nanoscaled

- CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1370-1382, June 2007
8. N. Banerjee, A. Raychowdhury, K. Roy, S. Bhunia, and H. Mahmoodi, "A Novel Low-Overhead Operand Isolation Technique for Low-Power Datapath Synthesis," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 14, no. 9, pp. 1034-1039, Sep. 2006
 9. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "A Novel High Performance and Robust Sense Amplifier Using Independent Gate Control in Sub-50nm Double-Gate MOSFET," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 14, no. 2, pp. 183-192, Feb. 2006
 10. Q. Chen, H. Mahmoodi, S. Bhunia, and K. Roy, "Efficient Testing of SRAM with Optimized March Sequences and a Novel DFT Technique for Emerging Failures due to Process Variations," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 13, no. 11, pp. 1286-1295, Nov. 2005
 11. H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of Delay Variations Due to Random-Dopant Fluctuations in Nanoscale CMOS Circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1787-1796, Sep. 2005
 12. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling of Failure Probability and Statistical Design of SRAM Array for Yield Enhancement in Nano-Scaled CMOS," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 24, no. 12, pp. 1859-1880, Dec. 2005
 13. S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "Low-Power Scan Design Using First Level Supply Gating," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 13, no. 3, pp. 384-395, Mar. 2005
 14. A. Agrawal, B. Paul, H. Mahmoodi, A. Datta, and K. Roy, "A Process-Tolerant Cache Architecture for Improved Yield in Nanoscale Technologies," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 13, no. 1, pp. 27-38, Jan. 2005 (**Best paper award**)
 15. H. Mahmoodi and K. Roy, "Diode-Footed Domino: A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style," *IEEE Transactions on Circuits and Systems I*, vol. 51, no. 3, pp. 495-503, Mar. 2004
 16. J. Park, W. Jeong, H. Mahmoodi, Y. Wang, H. Choo, and K. Roy "Computation Sharing Programmable FIR Filter for Low Power and High Performance Applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 2, pp. 348-357, Feb. 2004
 17. K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305-327, Feb. 2003
 18. K. Roy, S. Mukhopadhyay, and H. Mahmoodi, "Leakage current in deep-submicron CMOS circuits," *Journal of Circuits, Systems, and Computers*, vol. 11, no. 6, pp. 575-600, Dec. 2002
 19. H. Mahmoodi, A. Afzali-Kusha, and M. Nourani "An adiabatic carry-look ahead adder with efficient supply clock generator," *IEE Proceedings on Circuits, Devices and Systems*, vol. 148, no. 5, pp. 229-234, Oct 2001

Published Conference Papers (Refereed):

20. F. Moradi, D. T. Wisland, H. Mahmoodi, T. C. Vu, "New Subthreshold Design Concepts in 65nm CMOS Technology," accepted for *IEEE International Symposium on Quality Electronic Design*
21. F. Moradi, D. T. Wisland, H. Mahmoodi, and T. V. Cao "Ultra Low Power Full

- Adder Design in Subthreshold Region” Accepted for *International Conference on Microelectronics*, Dec. 2008
22. A. Jalali and H. Mahmoodi, “Virtual Age: Next Wave of Change in Society,” accepted for the *International Conference on e-Commerce, e-Administration, e-Society, and e-Education*, Jan. 2009, Singapore
 23. F. Moradi, D. T. Wisland, S. Aunet, H. Mahmoodi, T. V. Cao, “65nm Sub-Threshold 1T1SRAM for Ultra Low Voltage Applications,” *IEEE International Systems-On-Chip Conference*, pp. 113-118, Sep. 2008
 24. F. Moradi, D. T. Wisland, H. Mahmoodi, T. V. Cao, “High Speed and Leakage-Tolerant Domino Circuits for High Fan-in Applications in 70nm CMOS Technology,” *International Caribbean Conference on Device, Circuits, and Systems*, pp.1-5, April 2008
 25. F. Moradi, H. Mahmoodi, and H. Alimohammadi, “A Leakage-tolerant CMOS Comparator in Ultra Deep Submicron CMOS Technology,” *XXII Conference on Design of Circuits and Integrated Systems*, pp. 415-418, Nov. 2007
 26. S. Paul, S. Bhunia, and H. Mahmoodi, “Low-Overhead Design Technique for Calibration of Maximum Frequency at Multiple Operating Points,” *IEEE International Conference on Computer Aided Design*, pp. 401-404, Nov. 2007
 27. K. Kim, H. Mahmoodi, and K. Roy, “A Low-Power SRAM Using Bit-Line Charge-Recycling Technique,” *International Symposium on Low Power Electronic Design*, Aug. 2007
 28. V. Tirumalashetty and H. Mahmoodi, “Clock Gating and Negative Edge Triggering for Energy Recovery Clock,” *IEEE International Symposium on Circuits and Systems*, pp. 1141-1144, May 2007
 29. Rajani Kuchipudi and Hamid Mahmoodi, “Strain Silicon Optimization for Memory and Logic in Nano-Scale CMOS,” *IEEE International Symposium on Quality Electronic Design*, pp. 27-32, Mar. 2007
 30. J. Yeung and H. Mahmoodi, “Robust Sense Amplifier Design under Random Dopant Fluctuations in Nano-Scale CMOS Technologies,” *IEEE International Systems-On-Chip Conference*, pp. 261-264, Sep. 2006
 31. F. Moradi, A. Peiravi, and H. Mahmoodi “A Novel Leakage-Tolerant Domino Logic Circuit with Feedback from Footer Transistor in Ultra Deep Submicron CMOS,” *IEEE International Conference on Mixed Design of Integrated Circuits and Systems*, pp. 210-213, June 2006
 32. S. Mukhopadhyay, K. Kim, H. Mahmoodi, A. Datta, D. Park, and K. Roy, “Self-Repairing SRAM for Reducing parametric Failures in Nanoscaled Memory,” *Symposium on VLSI Circuits*, pp. 132-133, June. 2006
 33. N. Banerjee, K. Roy, H. Mahmoodi, and S. Bhunia, “Low Power Synthesis of Dynamic Logic Circuits Using Fine-Grained Clock Gating” *Design, Automation, and Test in Europe*, vol. 1, pp. 1 – 6, Mar. 2006
 34. K. Roy, H. Mahmoodi, S. Mukhopadhyay, H. Ananthan, A. Bansal, and T. Cakici, “Double-Gate SOI Devices for Low-Power and High-Performance Applications,” *International Conference on VLSI Design*, pp. 8, Jan. 2006
 35. A. Goel, S. Bhunia, H. Mahmoodi, and K. Roy, “Low-Overhead Design of Soft-Error-Tolerant Scan Flip-Flops with Enhanced-Scan Capability,” *Asia and South Pacific Design Automation Conference*, pp. 6, Jan. 2006
 36. K. Roy, H. Mahmoodi, S. Mukhopadhyay, H. Ananthan, A. Bansal, and T. Cakici, “Double-Gate SOI Devices for Low-Power and High-Performance Applications,” *IEEE/ACM International Conference on Computer Aided Design*, pp. 217-224, Nov. 2005

37. S. Mukhopadhyay, A. Raychowdhury, H. Mahmoodi, and K. Roy, "Leakage Current Based Stabilization Scheme for Robust Sense-Amplifier Design for Yield Enhancement in Nano-scale SRAM," *IEEE Asian Test Symposium*, pp. 176-181, Dec. 2005
38. T. Cakici, H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Independent Gate Skewed Logic in Double-Gate SOI Technology," *IEEE International SOI Conference*, pp. 83-84, Oct. 2005
39. N. Banerjee, A. Raychowdhury, S. Bhunia, H. Mahmoodi, and K. Roy, "Novel Low-Overhead Operand Isolation Techniques for Low-Power Datapath Synthesis," *IEEE International Conference on Computer Design*, pp. 206-211, Oct. 2005
40. S. Mukhopadhyay, K. Kang, H. Mahmoodi, and K. Roy, "Reliable and Self-Repairing SRAM in Nano-scale Technologies using Leakage and Delay Monitoring," *International Test Conference*, pp. 10, Nov. 2005
41. M. Meterelliyoz, H. Mahmoodi, and K. Roy, "A Leakage Control System for Thermal Stability during Burn-In Test," *International Test Conference*, pp. 10, Nov. 2005
42. Q. Chen, S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Process Variation Tolerant Online Current Monitor for Fault Immune Systems," *IEEE International On-Line Testing Symposium*, pp. 171-176, July 2005
43. S. Bhunia, N. Banerjee, Q. Chen, H. Mahmoodi, and K. Roy, "A Novel Synthesis Approach for Active Leakage Power Reduction Using Dynamic Supply Gating," *Design Automation Conference*, pp. 479-484, June 2005
44. M. Cooke, H. Mahmoodi, Q. Chen, and K. Roy, "Energy Recovery Clocked Dynamic Logic," *Great Lake Symposium on VLSI*, Apr. 2005
45. F. Moradi, H. Mahmoodi, and A. Peiravi "A High Speed and Leakage-Tolerant Domino Logic for High Fan-in Gates," *Great Lake Symposium on VLSI*, pp. 478-481, Apr. 2005
46. A. Ghadiri and H. Mahmoodi, "Pre-capturing Static Pulsed Flip-Flops," *IEEE International Symposium on Circuits and Systems*, pp. 2421-2424, May 2005
47. Q. Chen, H. Mahmoodi, S. Bhunia, and K. Roy, "Modeling and Testing of SRAM for New Failure Mechanisms due to Process Variations in Nanoscale CMOS," *IEEE VLSI Test Symposium*, pp. 292-297, May 2005
48. S. Bhunia, H. Mahmoodi, A. Raychowdhury, and K. Roy, "A Novel Low-overhead Delay Testing Technique for Arbitrary Two-Pattern Test Application," *Design, Automation, and Test in Europe*, pp. 1136-1141, Mar. 2005
49. S. Bhunia, H. Mahmoodi, and K. Roy, "Power Reduction in Test-Per-Scan BIST with Supply Gating and Efficient Scan Partitioning," *IEEE International Symposium on Quality Electronic Design*, pp. 453-458, Mar. 2005
50. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Design of High Performance Sense Amplifier Using Independent Gate Control in Sub-50nm Double-Gate MOSFET," *IEEE International Symposium on Quality Electronic Design*, pp. 490-495, Mar. 2005
51. F. Moradi, A. Peiravi, and H. Mahmoodi, "A New Leakage-Tolerant Design for High Fan-in Domino Gates," *International Conference on Microelectronics*, pp. 493-496, Dec. 2004
52. A. Ghadiri and H. Mahmoodi, "Dual-Edge Triggered Static Pulsed Flip-Flops," *International Conference on VLSI Design*, pp. 846-849, Jan. 2005
53. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Statistical Design and Optimization of SRAM Cell for Yield Enhancement," *IEEE/ACM International Conference on Computer Aided Design*, pp. 10-13, Nov. 2004
54. H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of Delay Variations Due to Random-Dopant Fluctuations in Nanoscaled CMOS Circuits," *IEEE Custom*

- Integrated Circuits Conference*, pp. 17-20, Oct. 2004
55. H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "High Performance and Low Power Domino Logic Using Independent Gate Control in Double-Gate SOI MOSFETs," *IEEE International SOI Conference*, pp. 67-68, Oct. 2004
56. S. Bhunia, H. Mahmoodi, D. Ghosh, S. Mukhopadhyay, and K. Roy, "A Novel Low-Power Scan Design Technique Using Supply Gating," *IEEE International Conference on Computer Design*, pp. 60-65, Oct. 2004 (**Best paper award**)
57. S. Bhunia, H. Mahmoodi, A. Raychowdhury, and K. Roy, "First Level Hold: A Novel Low-Overhead Delay Fault Testing Technique," *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pp. 314-315, Oct. 2004
58. S. Mukhopadhyay, H. Mahmoodi, and K. Roy, "Modeling and Estimation of Failure Probability due to Parameter Variations in Nanoscale SRAMs for Yield Enhancement," *Symposium on VLSI Circuits*, pp. 64-67, June 2004
59. H. Mahmoodi and K. Roy, "Data-Retention Flip-Flops for Power-Down Applications," *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 677-680, May 2004
60. H. Mahmoodi and K. Roy, "Dual-Edge Triggered Level Converting Flip-Flops," *IEEE International Symposium on Circuits and Systems*, vol. 2, pp. 661-664, May 2004
61. Y. Wang, H. Mahmoodi, L. Chiou, H. Choo, J. Park, W. Jeong, and K. Roy "Hardware Architecture and VLSI Implementation of a Low-Power High-Performance Polyphase Channelizer with Applications to Subband Adaptive Filtering," *IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. 5, pp. 97-100, May 2004
62. A. Ghadiri and H. Mahmoodi, "Comparative Energy and Delay of Energy Recovery and Square Wave Clock flip-Flops for High-Performance and Low-Power Applications," *International Conference on Microelectronics*, pp. 89-92, Dec. 2003
63. H. Mahmoodi and K. Roy, "A Leakage-Tolerant High Fan-in Dynamic Circuit Design Style," *IEEE International Systems-On-Chip Conference*, pp. 117-120, Sep. 2003
64. M. Cooke, H. Mahmoodi, and K. Roy, "Energy Recovery Clocking Scheme and Flip-Flops for Ultra Low-Energy Applications," *International Symposium on Low Power Electronic Design*, pp. 54-59, Aug. 2003
65. K. Roy, H. Mahmoodi, S. Mukhopadhyay, "Leakage control for Deep Submicron Circuits," *SPIE's First International Symposium on Microtechnologies for the New Millennium*, vol. 5117, pp. 135-146, May 2003
66. S. Mukhopadhyay, H. Mahmoodi, C. Neau, K. Roy, "Leakage in Nanometer Scale CMOS Circuits," *International Symposium on VLSI Technology, Systems, and Applications*, pp. 217-222, Apr. 2003
67. H. Mahmoodi and K. Roy, "Self-precharging flip-flop (SPFF): a new level converting flip-flop," *European Solid-State Circuits Conference*, pp. 407-410, Sep. 2002
68. J. Park, W. Jeong, H. Choo, H. Mahmoodi, Y. Wang, and K. Roy "High performance and low power FIR filter design based on sharing multiplication," *International Symposium on Low Power Electronic Design*, pp. 295-300, Aug. 2002
69. H. Mahmoodi and A. Afzali-Kusha, "Efficient Power Clock generation for Adiabatic Logic", *IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 642-645, May 2001
70. H. Mahmoodi and A. Afzali-Kusha, "Low-Power Low-Noise Adder Design with Pass-transistor Adiabatic Logic", *International Conference on Microelectronics*, pp. 61-64, Nov. 2000
71. H. Mahmoodi, A. Afzali-Kusha and M. Nourani, "Efficiency of Adiabatic Logic for

Low-Power, Low-Noise VLSI", *IEEE Midwest Symposium on Circuits and Systems*, vol. 1, pp. 324-327, Aug. 2000

Books:

1. A. Jalali and H. Mahmoodi, "Programmable Logic Controllers: Principles and Applications", Tehran: Iran University of Science and Technology Press, 1999

Miscellaneous:

1. H. Mahmoodi "Low Power, Robust, and High Performance Circuit Design in Nano-Scale CMOS," PhD Dissertation, Purdue University, Aug. 2005
2. K. Roy, H. Mahmoodi, and S. Mukhopadhyay, "Leakage Current in Scaled CMOS: Mechanisms and Reduction Techniques," the *SRC Cavin's Corner*, <http://www.src.org>, Aug. 2003
3. H. Mahmoodi "Low-Power Design of Digital Systems Based on Adiabatic Switching Principles," M.S. Thesis, University of Tehran, Sep. 2000

PATENTS

1. *Self Repairing Technique in Nano-Scale SRAM to Reduce Parametric Failures*, S. Mukhopadhyay, H. Mahmoodi, K. Kim, and K. Roy, Filed with Purdue Office of Technology Commercialization in Oct. 2005, Patent pending
2. *Sense Amplifier Circuit*, S. Mukhopadhyay, H. Mahmoodi, and K. Roy, Filed with Purdue Office of Technology Commercialization in Jul. 2005, Patent issued by the US Patent and Trademark Office under Patent No. 7,304,903 on Dec. 4, 2007
3. *Apparatus and Methods for Determining Memory Device Faults*, Q. Chen, H. Mahmoodi, S. Bhunia, and K. Roy, Filed with Purdue Office of Technology Commercialization in May 2005, Patent accepted by the US Patent and Trademark Office on Oct. 20, 2008
4. *Synthesis Approach for Active Leakage Power Reduction Using Dynamic Supply Gating*, S. Bhunia, N. Banerjee, H. Mahmoodi, Q. Chen, and K. Roy, Filed with Purdue Office of Technology Commercialization in May 2005, Patent pending
5. *Design and Delay Fault Testing Technique Using First Level Supply Gating*, S. Bhunia, H. Mahmoodi, S. Mukhopadhyay, and K. Roy, Filed with Purdue Office of Technology Commercialization in Aug. 2004, Patent issued by the US Patent and Trademark Office under Patent No. 7,319,343 on Jan. 15, 2008

GRANTS AND PROPOSALS**Funded Grants:**

1. CIS User grant from Stanford Nanofabrication Facility (\$5,000), Project: Non-Volatile memory on Flexible Substrate, Role: PI, Oct. 2008
2. Synopsys CAD Tools license donation, (\$3,000), Project: SFSU-Synopsys Collaboration, Role: PI, Sep. 2008
3. IBM 65nm CMOS Process Design Kit donation, Project: Fault Tolerant Computing Architecture for Nano-Scale CMOS, Role: PI, April 2008
4. SFSU mini-grant (\$5,000), Project: Low Power Design of Digital Systems Using Energy Recovery Clocking and Clock Gating, Role: PI, Nov. 2005

TEACHING EXPERIENCES/COURSE DEVELOPMENT

- Course taught at San Francisco State University: ENGR 356: Basic Computer Architecture, ENGR 357: Basic Digital Lab, ENGR 453: Digital IC Design, ENGR 691/692: Computer

Engineering Design Project II, ENGR 696/697: Engineering Design project, ENGR 848: Digital VLSI Design, ENGR 856: Nano-Scale Circuits and Systems, ENGR 897: Research, ENGR 898: Thesis, ENGR 899: Special Study

- New course development: ENGR 848: Digital VLSI Design, ENGR 856: Nano-Scale Circuits and Systems
- New lab development: VLSI Research Lab
- Attended the Essential Teaching Seminar, San Francisco State University, Sep. 2005
- Took an elective course on teaching: “Educational Methods in Engineering” at Purdue University
- Developed a multimedia based online tutorial to teach basics of soldering to engineering and technology students
- Attended the Teaching and Learning with Technology Conference, Purdue University, Apr. 2004

RESEARCH ADVISING EXPERIENCES

- Advising 5 graduate (M.S.) students in their thesis research at San Francisco State University
- Past graduate students advised in their research at San Francisco State University:
 1. Sussan Hashemi
 2. Vishy Mohan (currently with Energy Consulting Company)
 3. Zeeshan Ahmed (currently with Synopsys)
 4. Rajani Kuchipudi
 5. Joyce Yeung (currently with Qimonda AG)

REVIEWING ACTIVITIES

- Reviewing papers for the following journals and conferences:
 1. IEEE Journal of Solid-State Circuits (JSSC)
 2. IEEE Transactions on Very Large Scale Integration Systems (TVLSI)
 3. IEEE Transactions on Circuits and Systems I (TCAS)
 4. IEE Electronics Letters
 5. IEE Proceedings Circuits, Devices & Systems
 6. Symposium on VLSI Circuits
 7. IEEE Custom Integrated Circuit Conference (CICC)
 8. International Symposium on Quality Electronic Design (ISQED)
 9. International Symposium on Low Power Electronics and Design (ISLPED)
 10. Design Automation Conference (DAC)
 11. IEEE VLSI Test Symposium (VTS)
 12. Design, Automation, and Test in Europe (DATE)
 13. IEEE International Symposium on Circuits and Systems (ISCAS)
 14. International Conference on VLSI Design
- Served as a panelist to review proposals submitted in the Division of Electrical, communications and Cybersystems at NSF, May 2007

PROFESSIONAL MEMBERSHIPS

- Technical program committee member of *IEEE Custom Integrated Circuit Conference*, 2005-present
- Technical program committee member of *International Symposium on Quality Electronic Design*, 2006-present
- Graduate Faculty of Purdue University, Dec. 2005-present

- Member of the *Institute of Electrical and Electronics Engineers (IEEE)*, 2000- present
- Executive committee member of IEEE San Francisco Section, 2007-2008