

Electrical and Computer Engineering

Master Oral Defense

Title: WRITE SWITCHING CURRENT CONTROL TO REDUCE WRITE ENERGY FOR STT RAM

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Committee Chair: Dr. Hamid Mahmoodi

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Abstract:

The emerging application of The Spin Torque Transfer Random Access Memory (STT-RAM) has been gaining significant attentions from the semiconductor industry, since STT RAM is a fast, scalable, and long durable non volatile memory. However, one of the most challenges of STT-RAM is write operation taking more energy by using high switching current. This research tries to optimize write energy by controlling level of write switching currents which is divided into 6 levels since different switching currents needed for AP-P (1-0) or P-AP (0-1) phrases. Since AP-P phrase needs less switching current than P-AP, three low levels are used for AP-P phrase and three high levels for P-AP phrase. We start writing new bit value into STT-RAM by using the lowest switching current for a specific phrase, and increasing it into the next level if write is not successful. The STT RAM Cell Controller is designed using Verilog. System Verilog is used to design Random Test Bench that represents for write success probabilistic environment.