



Electrical and Computer Engineering

Master Oral Defense

**TITLE: Analysis of Performance Degradation
Of a circuit Due To Transistor Aging Effect in
Nano Scale**

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Time & Date: 3:00PM, December 13, 2012

Location: SCI - 110

Committee Chair: Dr. Hamid Mahmoodi

Committee Members: Dr. Hao Jiang

Abstract:

Scaling down the dimensions of Metal Oxide Semiconductors (MOS) to Nano-scale has resulted in degradation of transistor performance over the time period. All the Integrated Circuits (ICs) experience the degradation over the time period due to underlying transistors. In this research, analysis of transistor breakdown is performed through computer simulations using the Custom Designer SE tool to understand effects on circuit power and performance. To simulate the effect of transistor breakdown, the resistors are added to the output of NOT, NOR and NAND gates which are connected in series. The resistors are placed between the transistor terminals to model the breakdown. The values of the resistors represent the severity of breakdown; large resistors represent fresh transistors, whereas low resistors represent a fully broken transistor. This research aims to offer better insight into the impact of transistor breakdown and to improve IC design in Nano-scale.