School of Engineering

Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

Title: System Verilog Design Verification Tutorial

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Time & Date: August 16th, 2012**,** 10:00am **Location:** SCI 110

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ABSTRACT

The process of verification parallels the design creation process. A designer reads the hardware specification for a block, interprets the human language description, and creates the corresponding logic in a machine-readable form, usually RTL code written using Verilog or VHDL language. To do this, the user needs to understand the input format, the transformation function, and the format of the output. There is always ambiguity in this interpretation, perhaps because of ambiguities in the original document, missing details or conflicting descriptions. The SystemVerilog language provides three important benefits over Verilog such as (i) Explicit design intent (ii) Conciseness of expressions (iii) A high level of abstraction for design. These benefits of SystemVerilog enable you to rapidly develop your RTL code, easily maintain your code, and minimize the occurrence of situations where the RTL code simulates differently than the synthesized netlist. SystemVerilog allows you to design at a high level of abstraction. This results in improved code readability and portability. Advanced features such as interfaces, concise port naming, explicit hardware constructs, and special data types ease verification challenges.