School of Engineering

Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

TITLE: ***Reconfigurable FIR Filter Architecture for Reliable Computing in Nano Scale CMOS Technology***

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TIME & DATE: WEDNESDAY, MAY 9 2012, 2:00 PM **LOCATION: SCI 110**

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ABSTRACT
In the Nano scale CMOS technology, transistor scaling causes variations in process, voltage and temperature parameters which results in unreliable circuit operations. The inability of circuit to perform its intended functionality results in reliability issues in Nano scale CMOS technology. To deal with above challenges in nanotechnology the existing reliability enhancements methods are based on redundancy. Although exiting redundancy method increase reliability they consume more power and area without increasing system performance. The proposed research is to develop efficient techniques for reliability enhancement of digital circuits in nanotechnology. The proposed system uses three FIR modules running in parallel to improve system performance and maintain system output frequency. The proposed scheme has capacity to reconfigure itself to bypass faulty module while maintaining output frequency constant. In this scheme, the reconfigurable FIR filter architecture is designed in RTL using Verilog HDL and the design is verified using System Verilog Test bench. The design and verification of system is performed using Synopsys VCS tool. The result of reconfigurable architecture is verified using high level C reference model. The functional coverage report shows that system has tested with sufficient number of input stimulus with 100% verification goal. The result shows that system reconfigured itself correctly to provide better performance and reliability.