

Full Custom IC Design Flow Tutorial Using Synopsys Cosmos Tools

By

Eli Lyons

Vish Ganti

Hamid Mahmoodi

**Nano-Electronics & Computing Research Center
School of Engineering
San Francisco State University
San Francisco, CA
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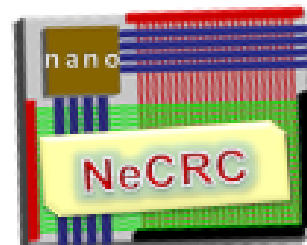


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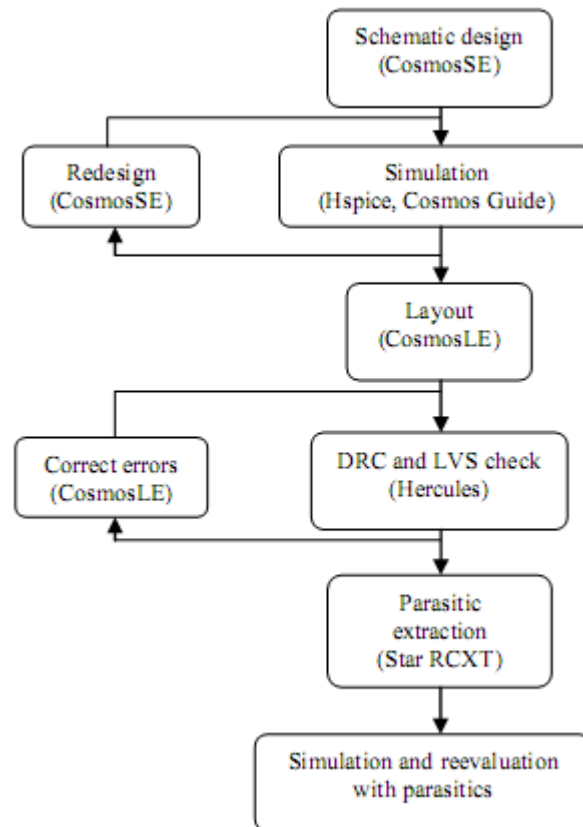
Introduction

This manual assumes you are able to do some basic things in a Linux environment such as create a folder, change directories....etc. If you want to learn how to use Linux here are many good tutorials available on the web, such as this one: <http://tldp.org/LDP/gs/node5.html>.

Figure I.1 shows the design flow this tutorial will be implementing. In the first three parts of this manual you will design and simulate a CMOS inverter using CosmosSE in conjunction with Hspice and CosmosScope to visually assemble the circuit schematic, simulate it, and view the output waveforms. For further help you are encouraged to go to “Help” in the menu bar of CosmosSE.

Starting in Part 4 you will use CosmosLE to create a layout, and use Hercules to run a design rule check (DRC) on the layout based on the technology process. You will also use Hercules to make sure our inverter layout matches our schematic by running a Layout Versus Schematic (LVS) check. Finally, you will use the inverter we create in a gate level design of a ring oscillator.

Fig. I.1: Custom design flow



Part 1. Setting up your workspace

The first step is to login. Please refer to the login tutorial if you are having trouble logging in or running the following commands. If you are using a Linux machine not connected to hafez.sfsu.edu try using the following command to ensure you can use x-server:

```
ssh -l username -X hafez.sfsu.edu
```

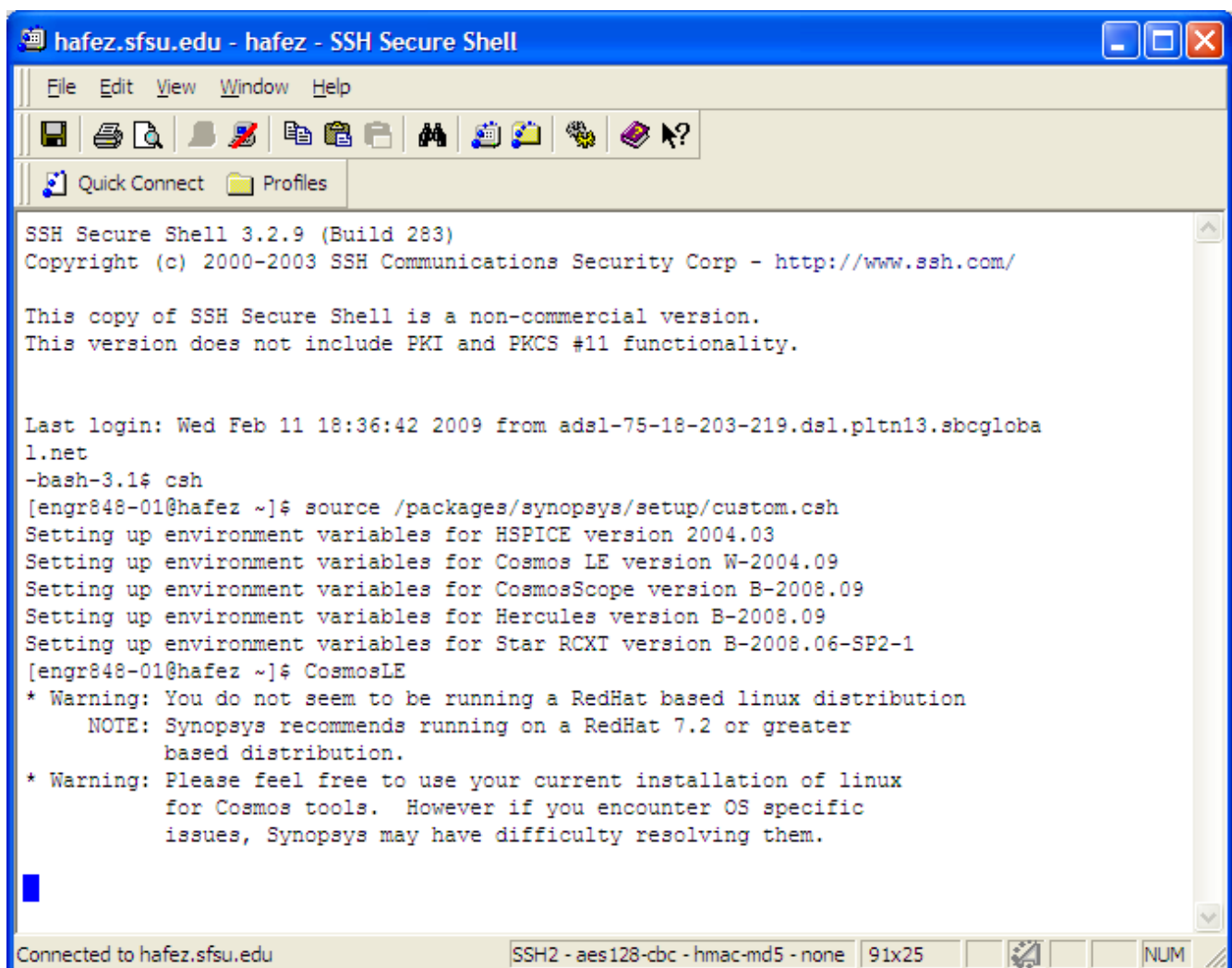
To setup all the software we will use the following commands in the shell window. These commands must be run every time you use the Synopsys software :

```
csh
```

```
source /packages/synopsys/setup/custom.csh
```

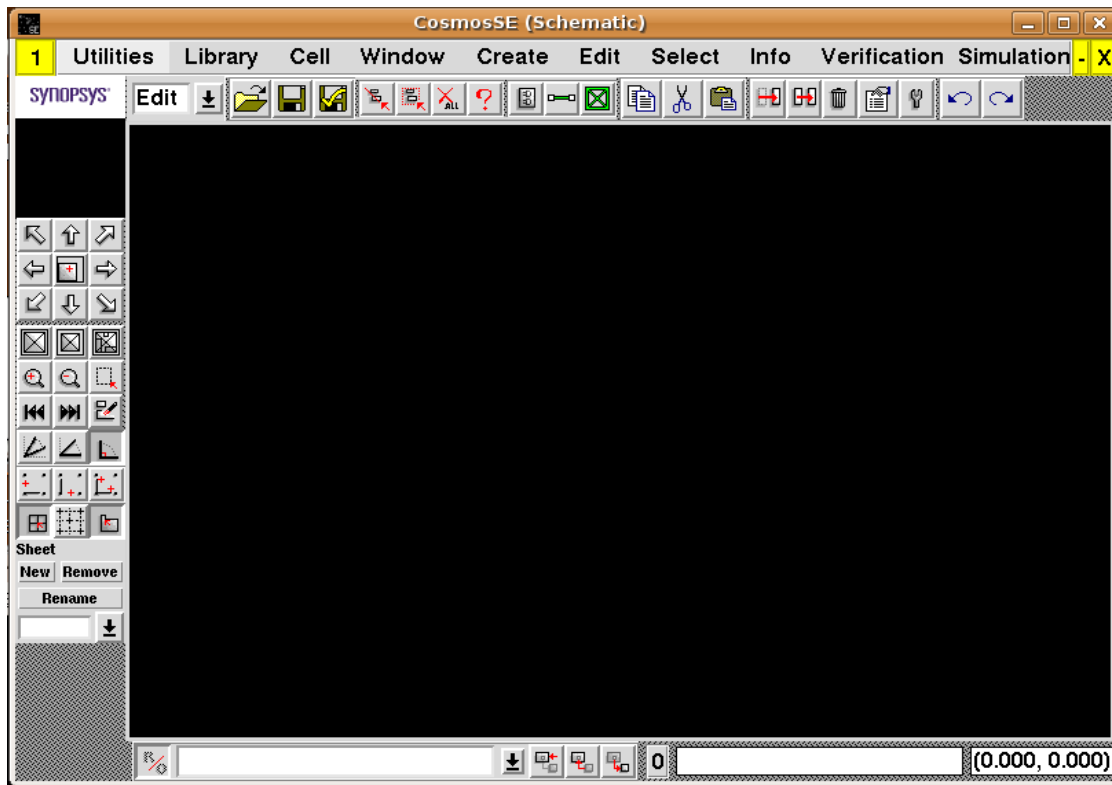
To run an instance of CosmosSE simply type “CosmosSE”. Your command window should look like the one shown in Fig. 1.1. Most likely you will also have the warnings shown, don't worry about them as long as CosmosSE opens.

Fig. 1.1: Shell commands



CosmosSE should open in a new window (Fig. 1.2).

Fig. 1.2: CosmosSE window



In the menu bar go to **Library>Create**. In the “Library Name” field enter “mylibrary” and in the “Tech File Name” field copy and paste this file directory in the field:

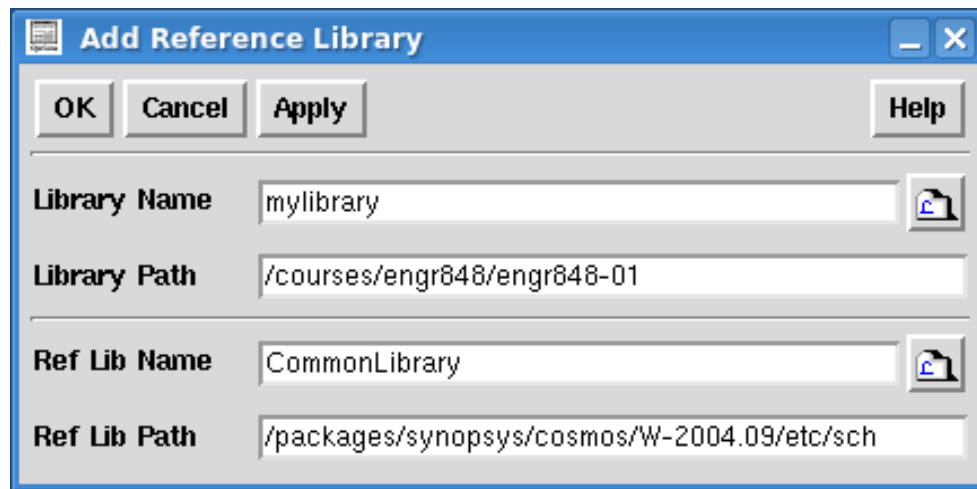
`/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/techfile/saed90nm_1p9m.tf`

Note that you could choose the technology file by clicking the open folder icon and browsing for it as well.

Click OK.

In the menu bar go to **Library>Add**.

Fig. 1.3: Add reference library

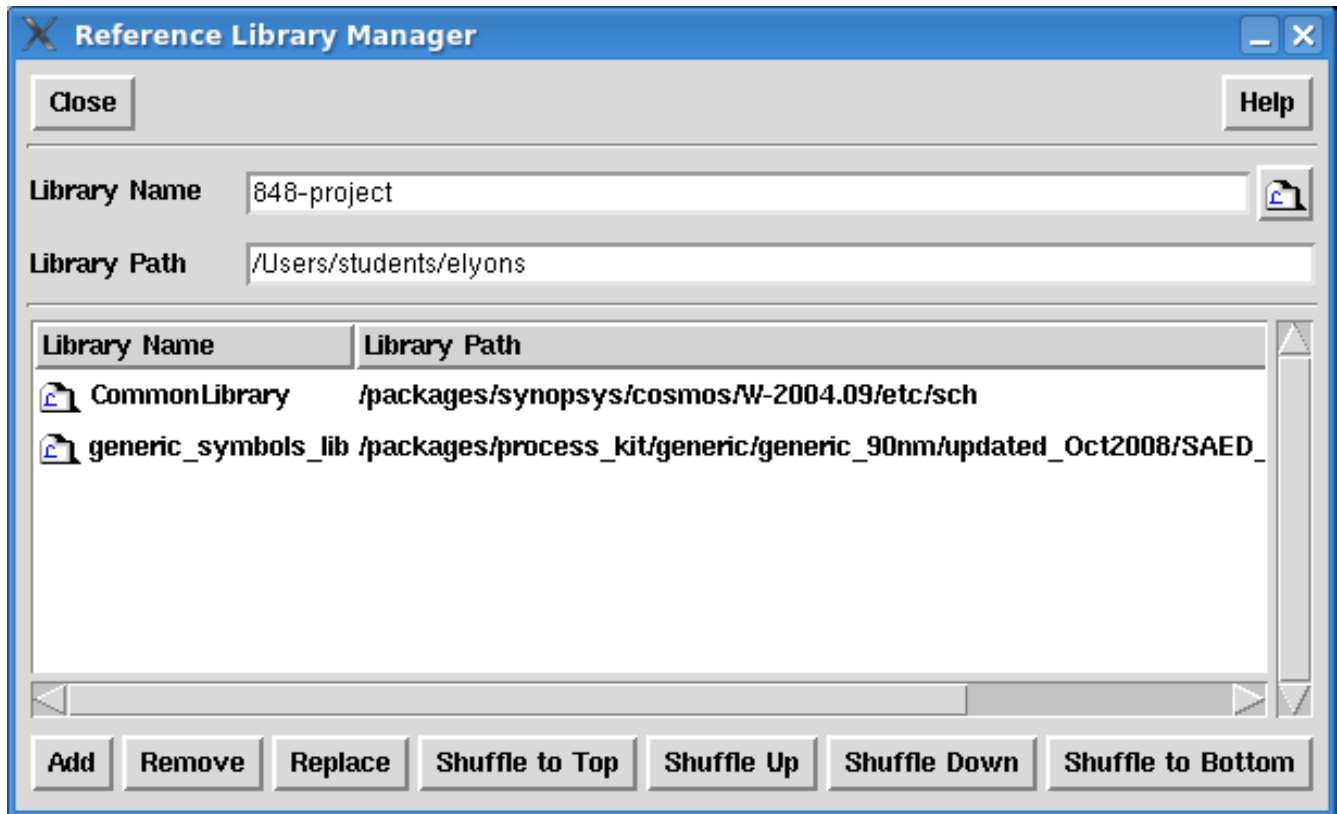


Again, you may click the folder icon on the right of the “Ref Lib Name” and select CommonLibrary in the directory /packages/synopsys/cosmos/W-2004.09/etc/sch or you can fill in the fields manually. When you are done click OK.

In the menu bar go to **Library>Manager**. Click “Add” and select “generic_symbols_lib” in the directory:

/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit

Fig. 1.4: Reference library manager



In the menu bar go to **Cell>Create**. Enter a name in the “Cell Name” field and click OK. At this point you have finished setting up your library. If you want to quit Cosmos at this time you can click the close window box in the Command window (Fig. 3.1). Follow the prompts to make sure you close Cosmos and save your work. **It is important to close Cosmos properly before you close your terminal connection as this can result in a lock being put on your cell (see troubleshooting).**

Part 2. Creating a schematic

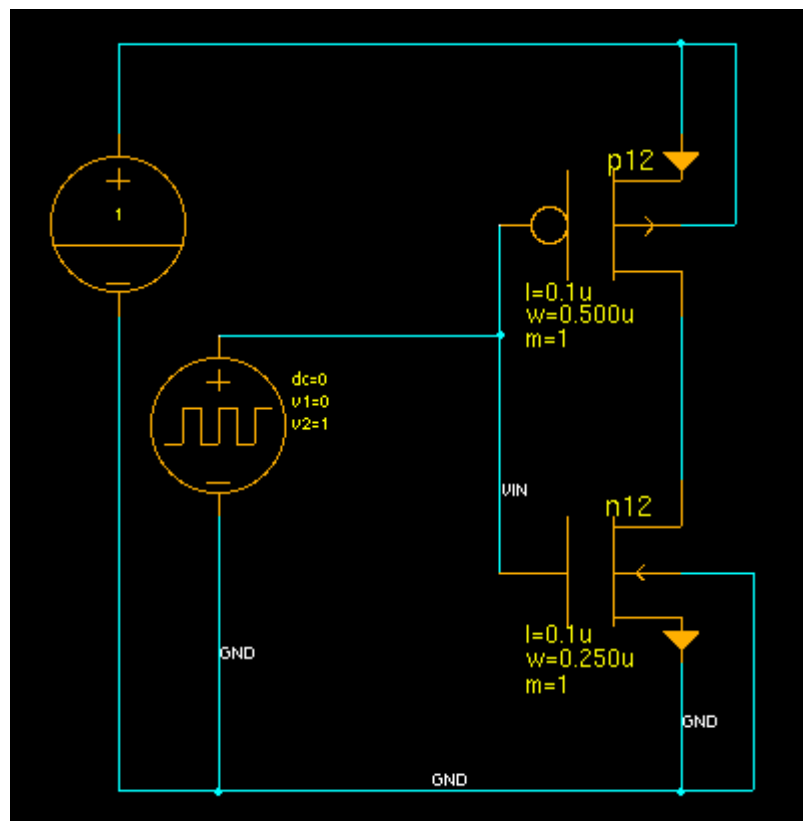
There are three ways to place components. Press <shift-i>, click the Create Instance icon in the edit toolbar, or go to **Create>Instance** in the menu bar. Select the cell instance part you want to place by clicking it once and then clicking inside the schematic.

Use g_nmos4t, g_pmos4t, c_vpulse and c-vgeneric for the inverter parts. To create wire move the mouse over a part terminal, hold down the right click button and select “Create Wire”. When you are finished your inverter should look like the schematic below. To edit the properties of your parts move the mouse over the part, right click and select “properties”. Change the properties to the values in the schematic below. In our case the process is a 0.90um process, so 0.1um is the minimum gate length. You can change the names of the nets by right clicking on the nets and selecting “attributes”. Change the names of the nets to VDD, VIN, VOUT and GND.

Important: You must specify a ground in your schematic, which is done by changing the attribute of your ground net to “GND” or “0”. This can be seen in the model below.

It should also be noted that the resolution in the layout editor is 5nm. Therefore, transistor dimensions should always be an integer factor of 5nm.

Fig. 2.1: Inverter schematic for simulation



Change the properties of the voltage pulse input to the values shown in Fig. 2.2.

Fig. 2.2: Properties of Voltage pulse



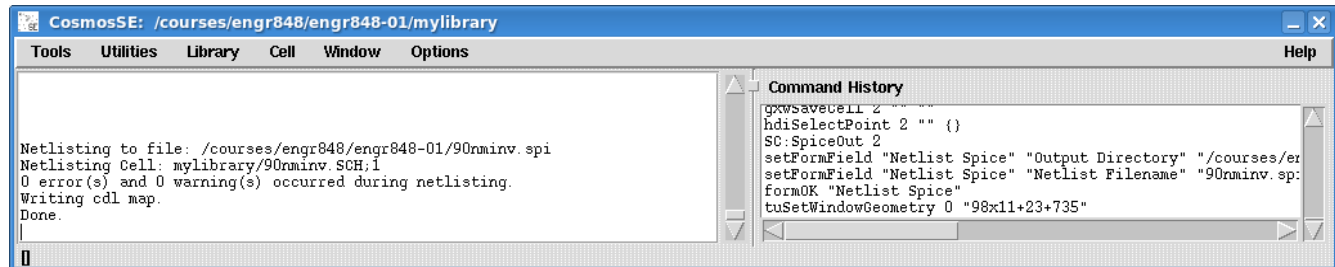
The 'Edit Properties' dialog box for a voltage pulse component. The 'Object' field shows 'Instance c_vpulse1 ID:2305'. The 'Find' button is next to it. The table below lists the properties and their values.

Name	Value	Vis	Lock
dc	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
v1	0	<input checked="" type="checkbox"/>	<input type="checkbox"/>
v2	1	<input checked="" type="checkbox"/>	<input type="checkbox"/>
tr	100ps	<input type="checkbox"/>	<input type="checkbox"/>
tf	100ps	<input type="checkbox"/>	<input type="checkbox"/>
td	100ps	<input type="checkbox"/>	<input type="checkbox"/>
pw	2n	<input type="checkbox"/>	<input type="checkbox"/>
per	4ns	<input type="checkbox"/>	<input type="checkbox"/>
device	vsources	<input type="checkbox"/>	<input type="checkbox"/>
spice_format	%ref{v} %port{p m} %prop{dc} PULS	<input type="checkbox"/>	<input type="checkbox"/>
		<input type="checkbox"/>	<input type="checkbox"/>

Part 3. Schematic Simulation

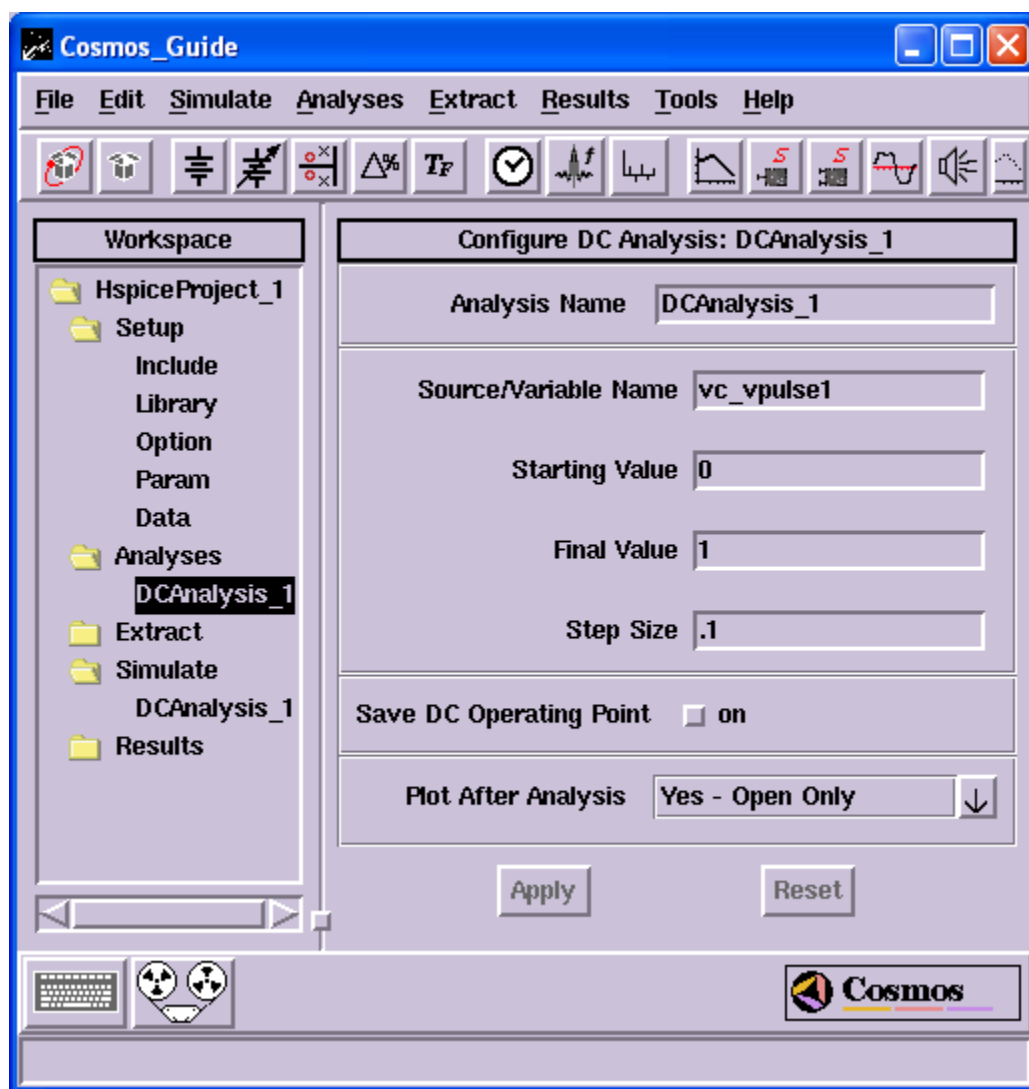
Before simulation you need to build your netlist by going to **Simulation>Spice** in the menu bar. The necessary fields should already be filled out. Click OK. You can make sure there were no errors by looking in the Cosmos command window.

Fig. 3.1: Cosmos command window



Next go to **Simulation>DC Sweep Analysis**. Cosmos Guide should open, if it does not run it is probably due to a poor internet connection. Enter the fields with the values shown below, notice that the source we are sweeping is `vc_vpulse1`. If you look at the attributes of input pulse in the schematic, the name is `c_vpulse1`, however in the netlist this is a voltage and we must make that clear by adding the “v” in front of the name in Cosmos Guide. Also take note that we have chosen to “Plot After Analysis”. Once all the fields have been filled out click “Apply”.

Fig. 3.2: DC analysis in Cosmos Guide



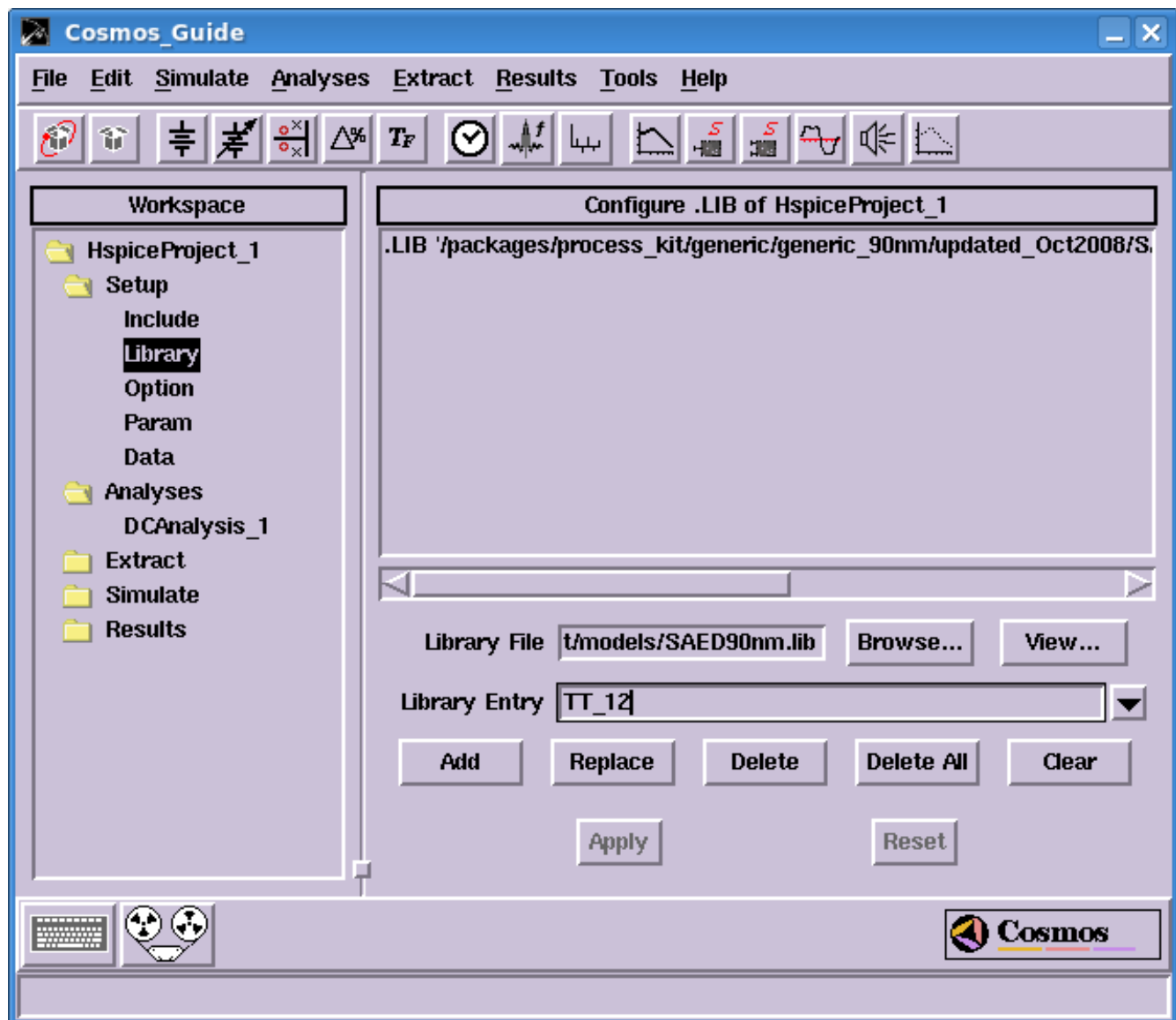
After you perform the DC sweep simulation we are setting up, you may want to re simulate using a smaller step size like 1m. Be careful because if you're step size is too small your simulation will require a large memory allocation, if the required allocation is too large it will result in an error.

Open “Setup” in “Workspace” on the left of Cosmos guide and select “Library”. Click “Browse” for a library file and select the “SAED90nm.lib” in the following directory:
/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/models/

In the Cosmos Guide you should see a drop down arrow next to “Library Entry” that allows you to select which model you want to use for the simulation. Choose “TT_12”, which simulates the model of a typical NMOS and typical PMOS. Click “Apply”. If the drop down arrow does not render properly in the GUI click inside the text field and use the keyboard arrows to select “TT_12”.

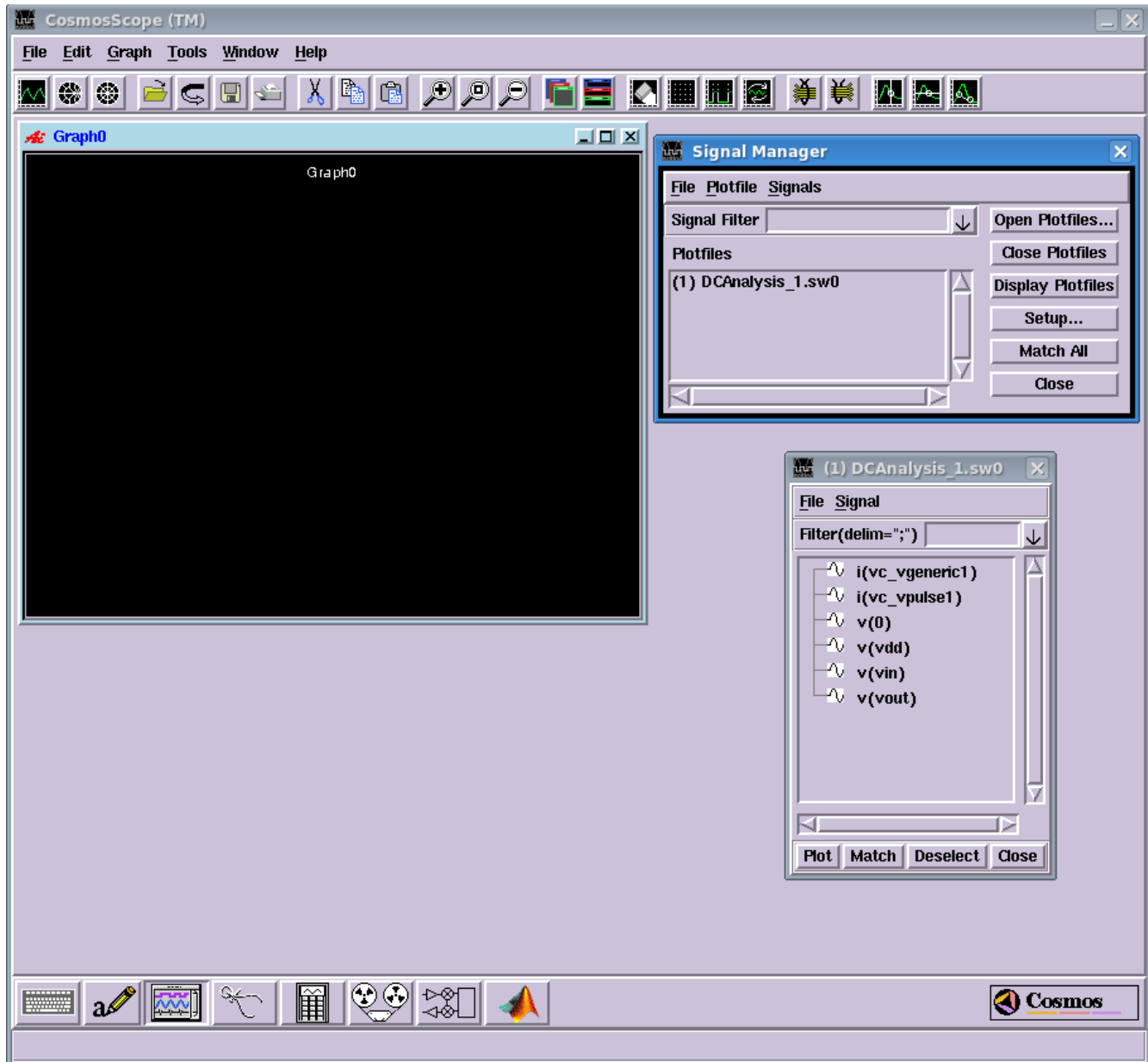
You probably noticed there are also entries for FF, SF...etc. These are models of fast NMOS and PMOS or one slow and one fast...etc. This library provides you with entries to simulate all combinations of the corners of the CMOS technology.

Fig. 3.3: Adding a library in Cosmos Guide



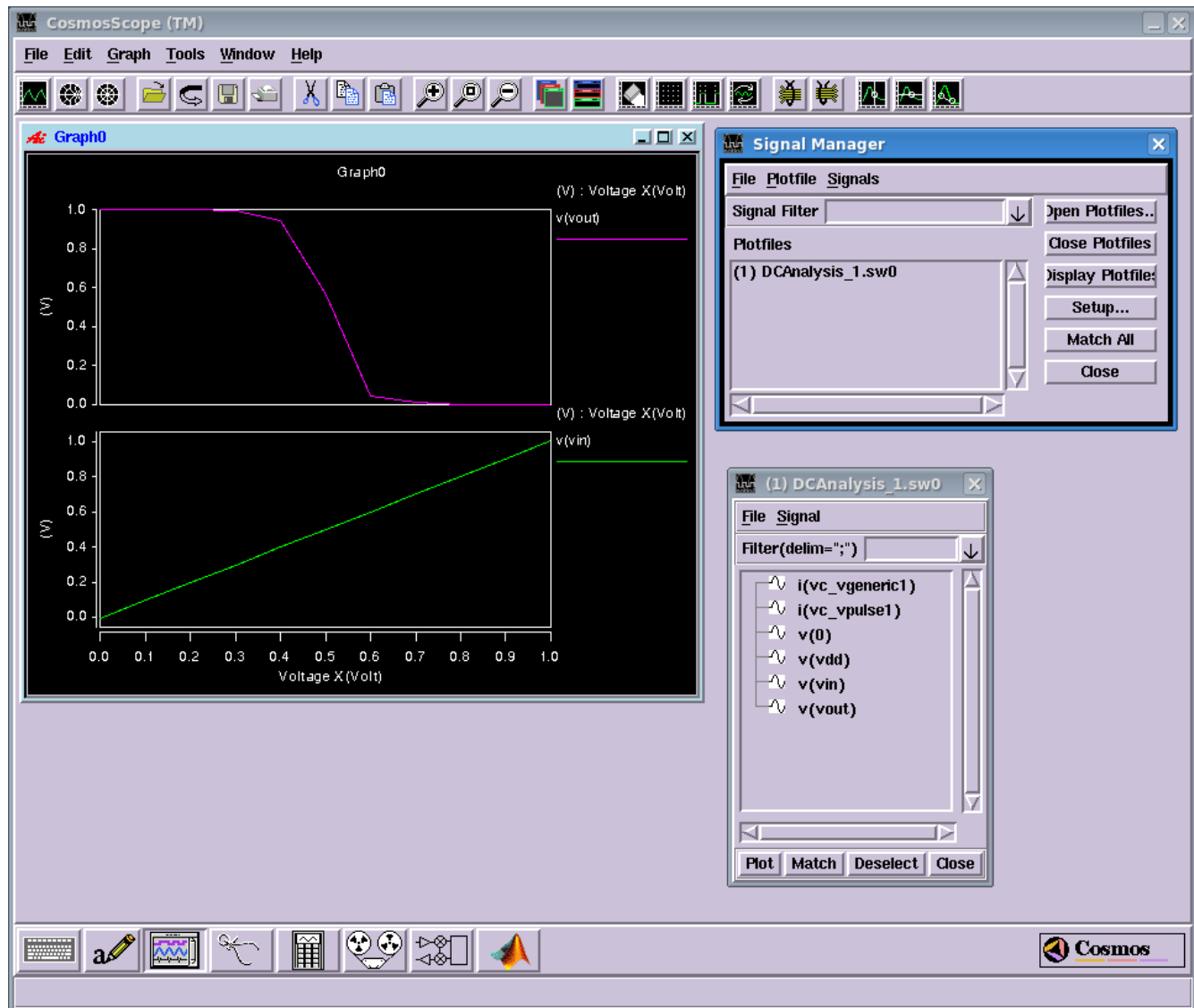
Go to **Simulate>Run All Projects>Serial**. The simulation should run and CosmosScope should open automatically. If your simulation ran without error you may want to save your simulation workspace by going back to the Cosmos Guide window and going to **File>Save**.

Fig. 3.4a: Cosmos Scope window



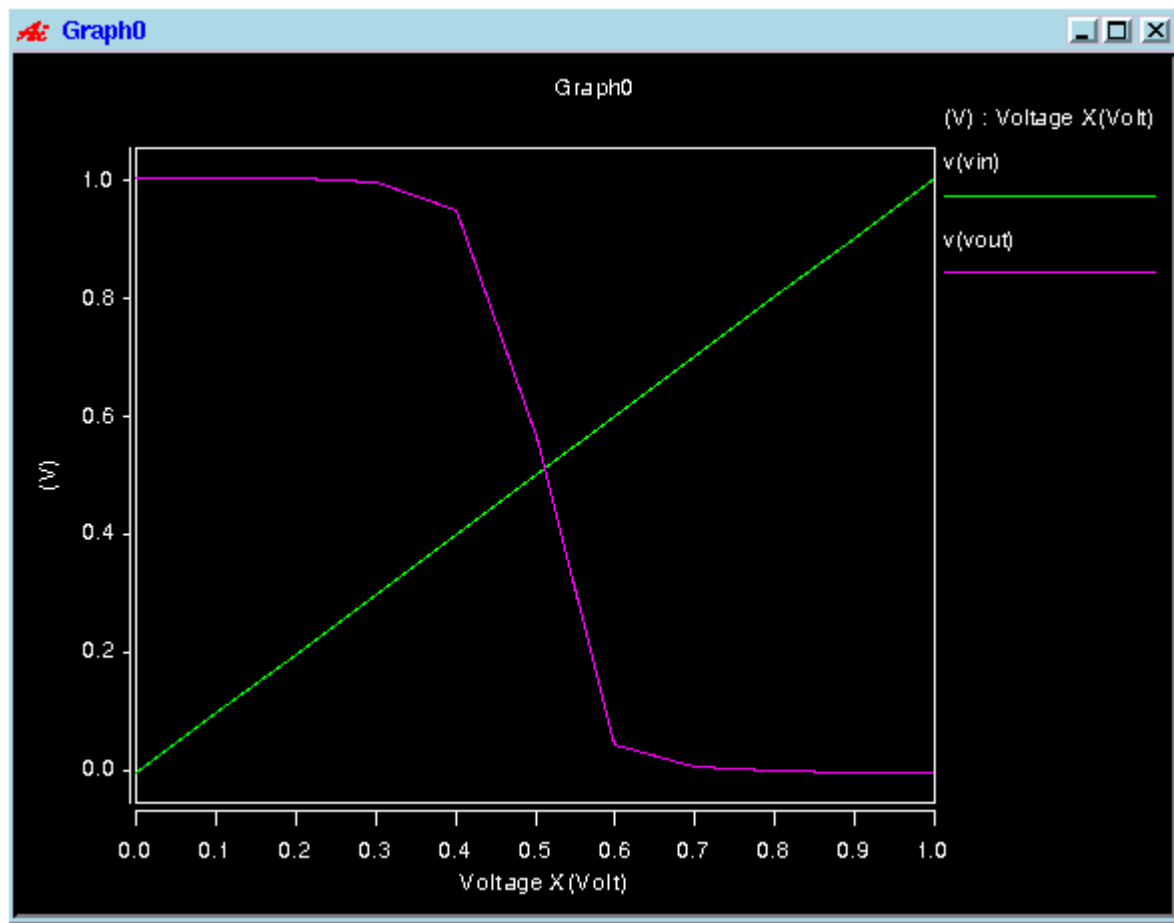
A signal manager window and the Plot File window will open up. In the Plot File window, plot $v(in)$ by double clicking $v(in)$, or by selecting $v(in)$ and clicking Plot. The input waveform of the inverter will open up. Now plot $v(out)$, the same way you plotted $v(in)$. This will open another graph with $v(out)$.

Fig. 3.4b: Graphs of V_{in} and V_{out}



Now to compare them on the same graph, simply click and drag the title “v(out)” from the top graph to the bottom graph where v(in) is plotted.

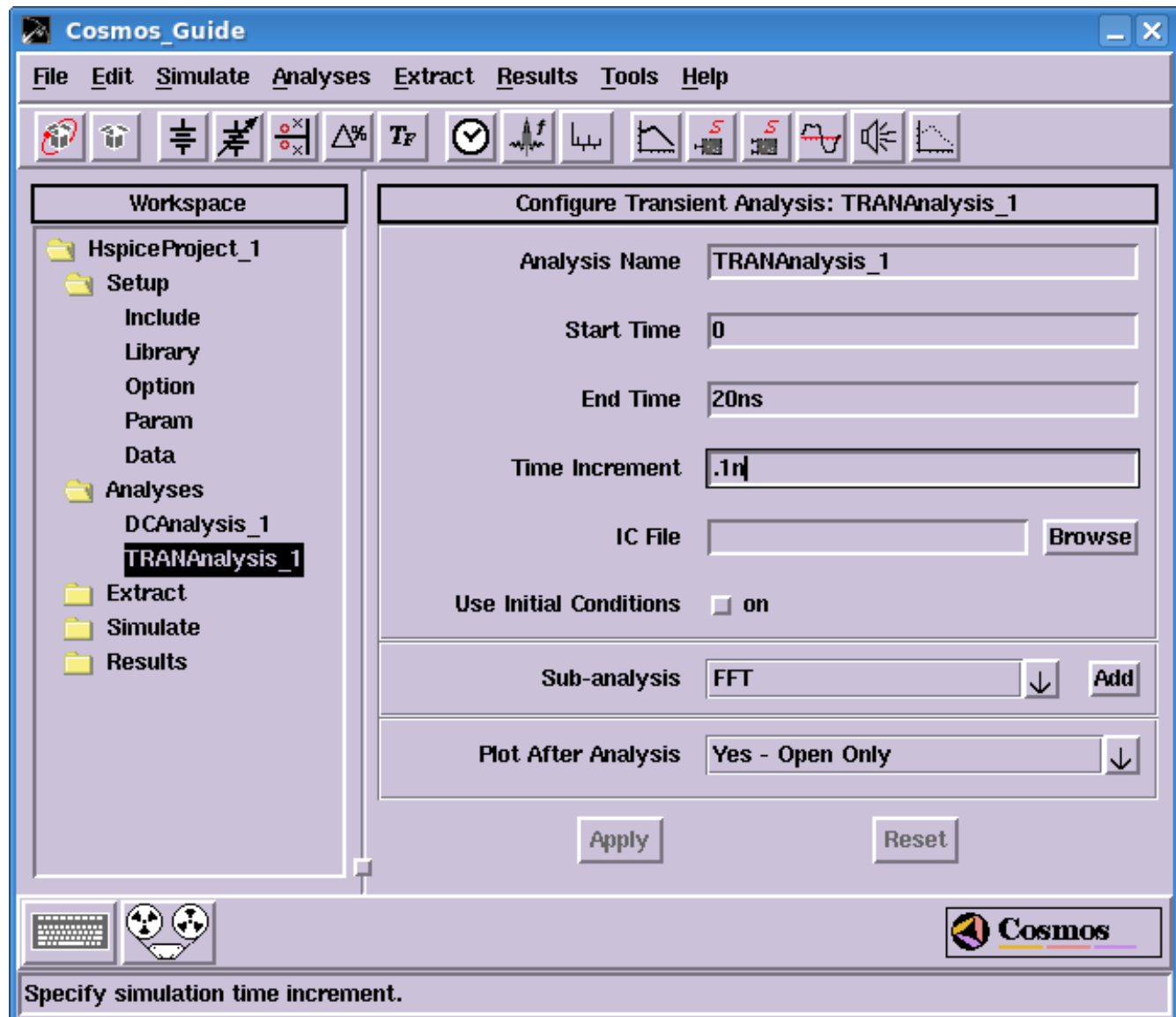
Fig. 3.4c: Vin and Vout graphed together



If you want to zoom in on a certain part of the plots, move your mouse cursor to the x- axis and click your starting point and drag it to your desired ending point. The graph will auto-adjust to your specified zoom length. To return to the default view, click on the magnifying glass with the square inside of it.

To simulate a transient response go to the Cosmos Guide window and go to **Analyses>Transient Analysis>Transient Analysis** or click the transient analysis icon which looks like a clock. In Fig. 3.5 a 0.1n time increment was used, however in many simulations you may want to use a smaller time increment, such as 1p.

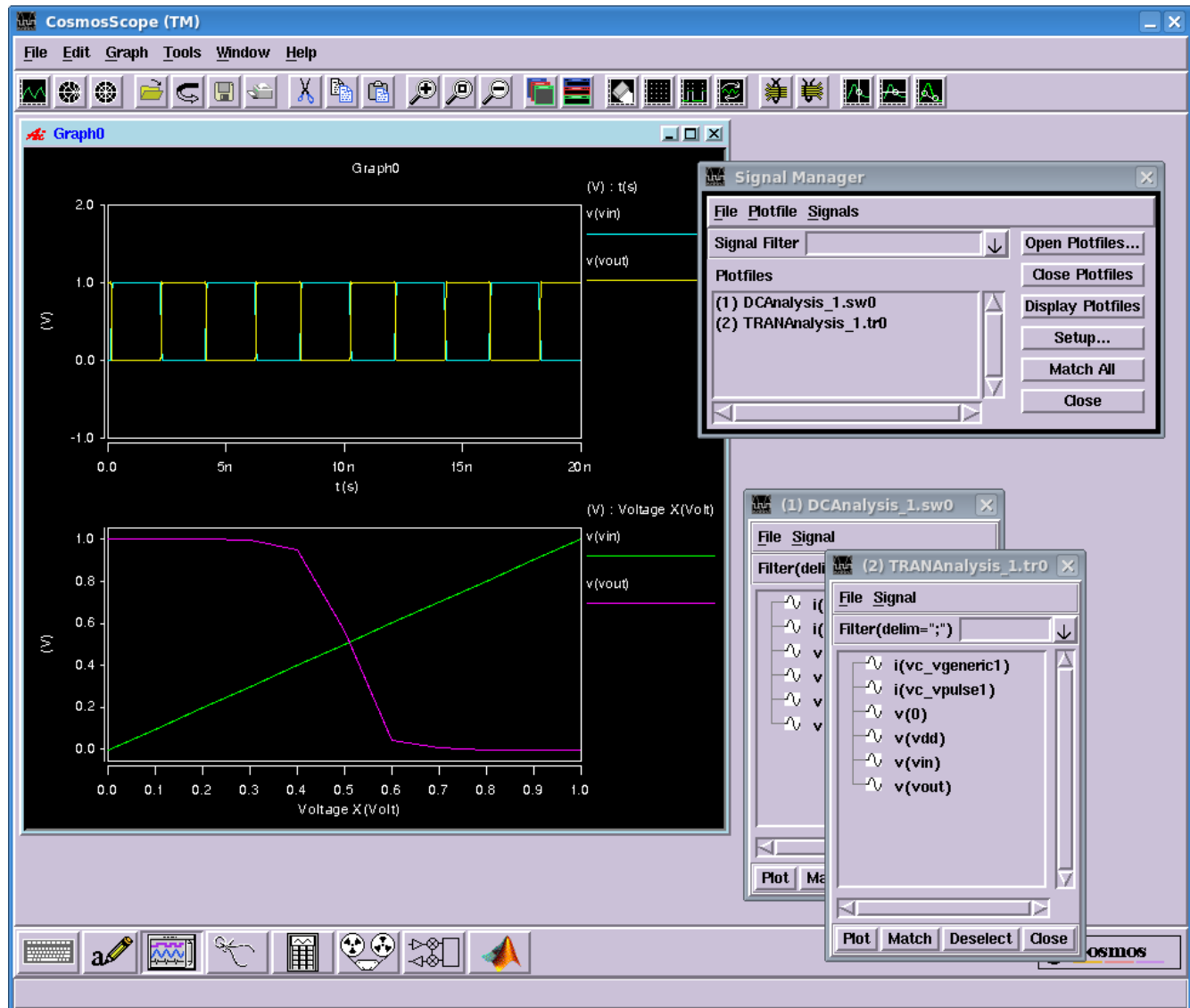
Fig. 3.5: Transient Analysis in Cosmos Guide



Go to **Analyses>Simulate>Run All Projects>Serial**. Following the same process for the voltage sweep graph, now we can see both the Transient plot and Voltage sweep plot.

On your own, explore the various measurement tools available in CosmosScope by going to **Tools>Measurement**. Click the arrow next to the “Measurement” field and browse the different tools. Try finding the delay between V_{in} and V_{out} by going to **Time Domain>Delay**.

Fig. 3.6: Simulation of both DC and Transient analysis

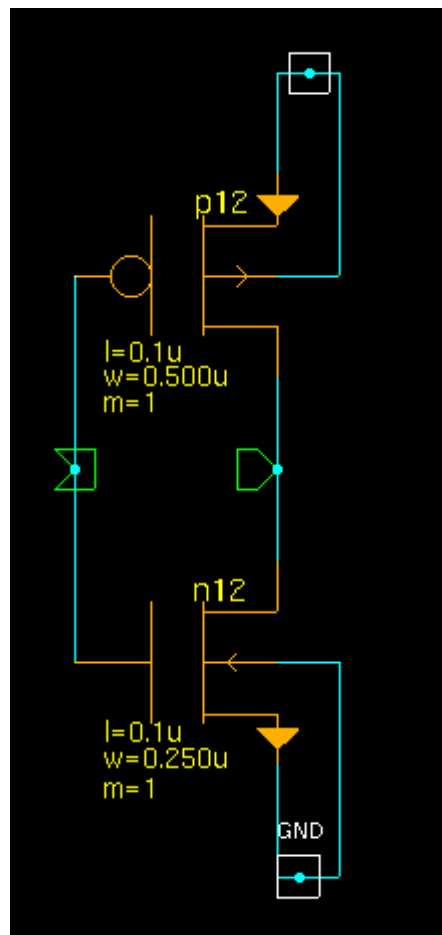


Now that we have simulated the inverter, we can see that it is working properly. Now close

Cosmos Guide and go back to the CosmosSE schematic window. Now we are going to make an actual physical layout for this inverter but before we do that we must modify the schematic. First delete the power sources since these will not appear on the layout we are going to make. Change the net named '0' to VSS. Now create a port by going to **Create>Connector** or click on the icon of a green box with a square in it. Place a port on the VDD net and and another on the VSS net. Now change the “Port Type” to Input and place it on the VIN net. Likewise choose “Port Type” to Output and place it on the VOUT net. Now your schematic should look similar to the one below.

Update the netlist by going to **Simulation>Spice**. Take note of the directory the spice netlist is being saved as it will be used later.

Fig. 3.7: Inverter schematic for use in higher level design



Part 4. Creating the Layout

To Draw a layout, its strongly recommended that you make yourself familiar with the Lambda Rules. This will help in reducing the layout design cycle time and debugging the errors identified by the Design Rules Check (DRC). You can find the guide with the rules for the 90nm technology we are using here:


/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/documentation/design_rules/general/SAED90DR01.doc

It is also suggested that you run the DRC throughout the layout process, instead of waiting until you have completed your layout to run it. This may help in finding errors you are making early on, and correct your mistake before you repeat throughout the layout.

Important: If you have errors in your DRC report look for the coordinates that are listed by each error. These will allow you to pinpoint where the error is on your layout.

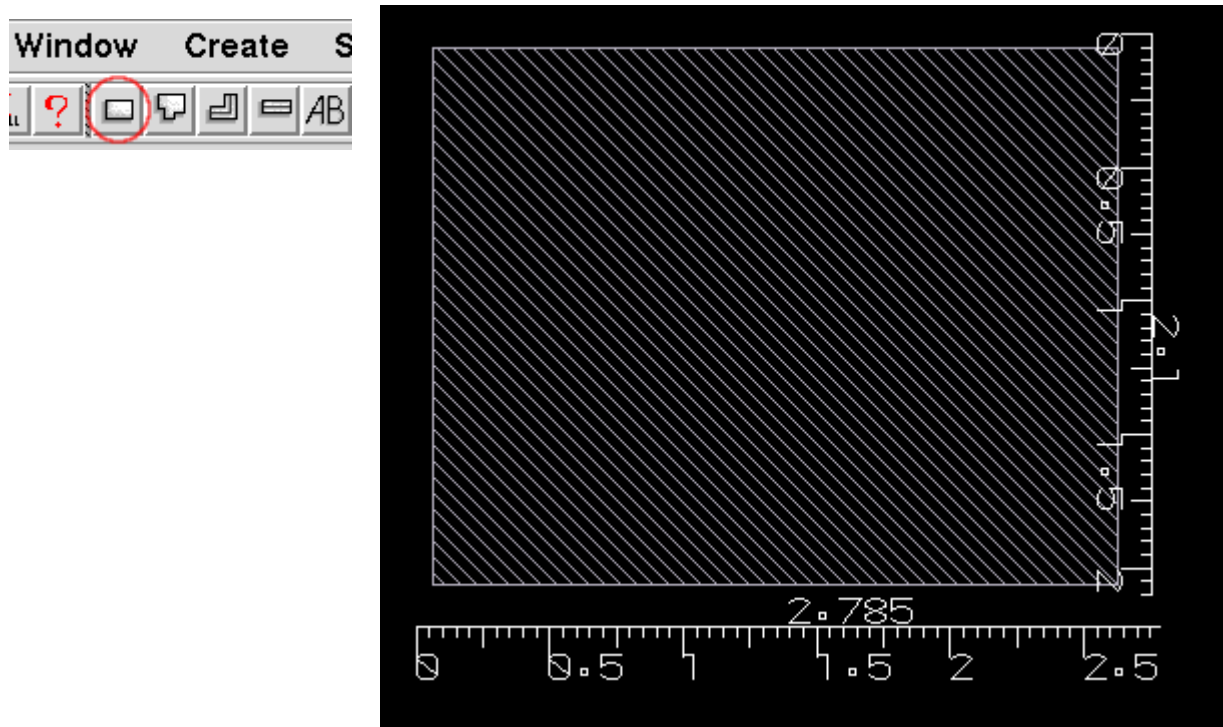
First, open CosmosLE. If your project library is already open in CosmosSE, go to Cell>Create. Make sure the cell is of type .CEL and the name of the cell is the same as the schematic cell you are making the layout of, in this case 90nminv. Click OK and CosmosLE and the new cell will open.

If you are starting from the terminal, make sure you run the custom.csh script as shown in Part 1. of this manual. Then enter CosmosLE to open the Cosmos layout editor. Open the library you created for this project, called mylibrary in this manual. Create a cell as instructed in the previous paragraph.

Go to **Window>Ruler**. Another window should pop up which has a “clear” button which you can use to clear your rulers. Click once to start drawing the ruler and again to end it. Draw two rulers about the lengths shown in figure 4.1. Select the NWELL layer  in the layers panel on the right and select “Create Rectangle” (Fig. 4.1).

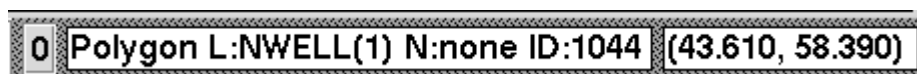
Draw a rectangle that fits approximately fits the dimensions of the rulers you set. You can always adjust the dimensions of this rectangle by first right clicking and selecting “Stretch” and then clicking the side you want to stretch.


Fig. 4.1: Drawing N-well



After you have created an N-well, move your mouse over it. Notice at the bottom there are two fields that tell you what layer you are on and the coordinates. This is useful information if you are having trouble figuring out what a layer is and when you are fixing errors found in DRC.

Fig. 4.2: Layer and coordinates



Now we are going to make diffusion areas for PMOS, NMOS and body connections. From our schematic we know that the width of the PMOS should be .500u and the width of NMOS is 0.250u. The location of the diffusion should be similar to the ones in figure 4.3. There are two horizontal diffusion areas that are the NMOS and PMOS devices, and two vertical rectangles that will be the body connections. Place rulers down to help you make sure the width of the diffusion areas for the NMOS and PMOS match our schematic area exactly. Select the “DIFF”  layer and again use the “Create

Rectangle” tool to draw the diffusion area. Use rulers to check the width of the rectangles. If the widths are different than the widths of the devices in the schematic, you will not pass LVS.

Fig. 4.3: Drawing diffusion areas

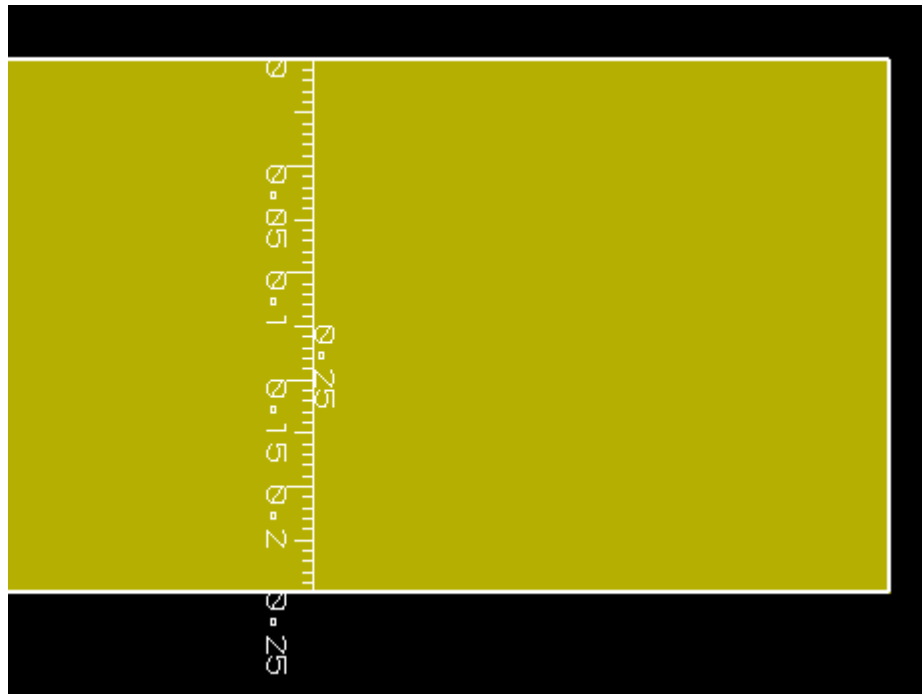
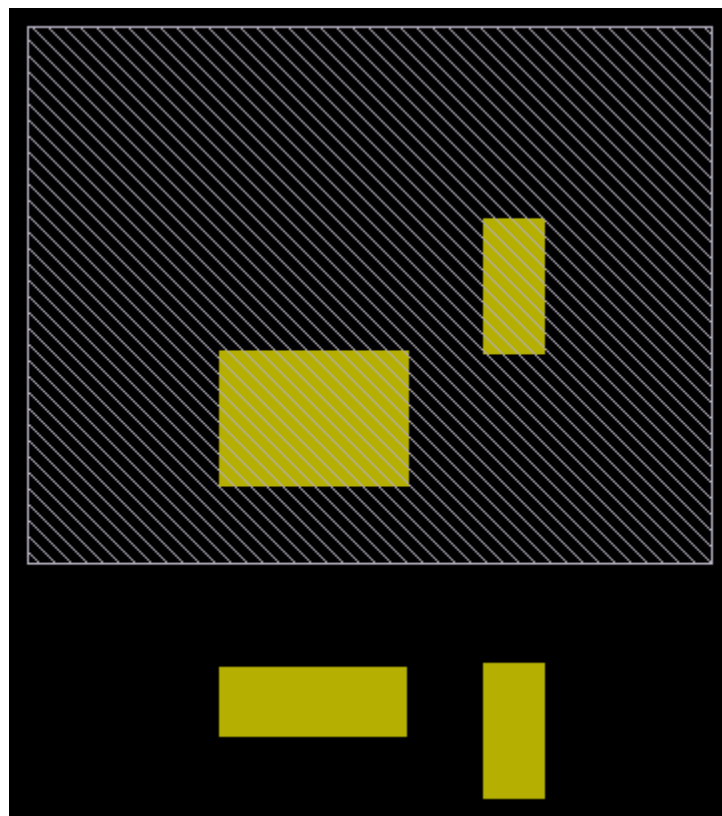
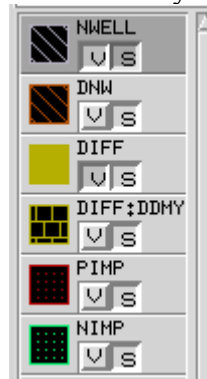


Fig. 4.4: Diffusion areas and body connections



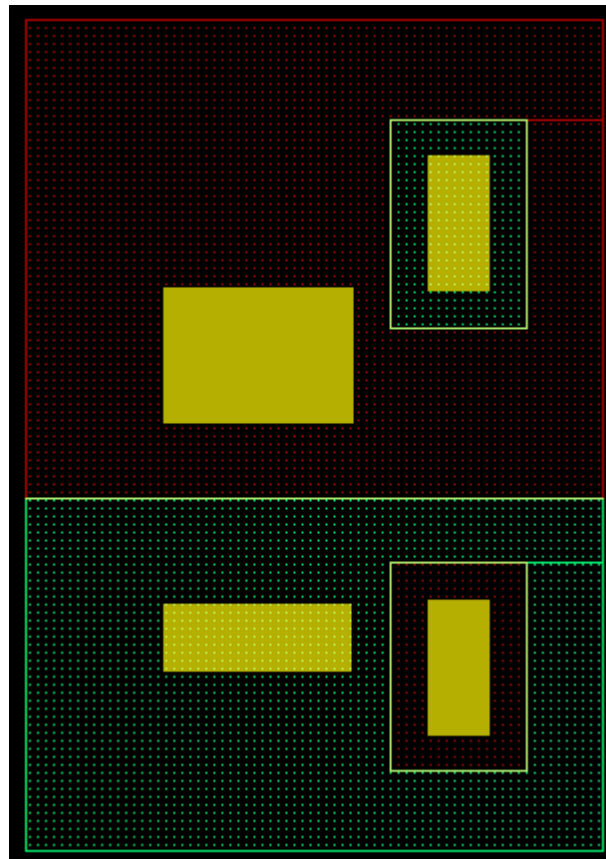
Now We will add the P-implant and N-implant areas. When manipulating layers on top of each other sometimes it is useful to “hide” a layer, like you would do in a program like Photoshop. You can do hide or reveal layers in Cosmos by clicking the 'v' and 'lock' layers by clicking the 's' (Fig. 4.5).

Fig. 4.5: Visualizng and selecting layers



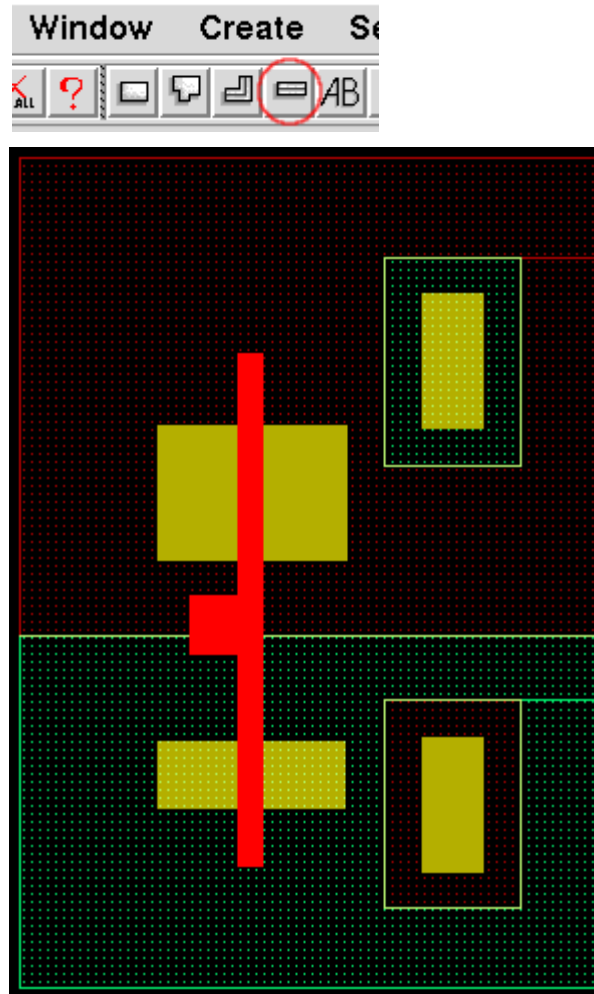
Use the P-implant and N-implant layers with the “Create Rectangle” to cover and surround the diffusion areas. In Fig. 4.5 we have hidden the NWELL layer, but it is important to note that the P-IMP is drawn to the edge of the NWELL where the NWELL meets the NIMP. This can be seen in Fig. 4.6. The PMOS area should be covered with P-IMP and the NMOS with N-IMP, except for the body connections which have the opposite implantation.

Fig. 4.6: Drawing P-implant and N-implant areas



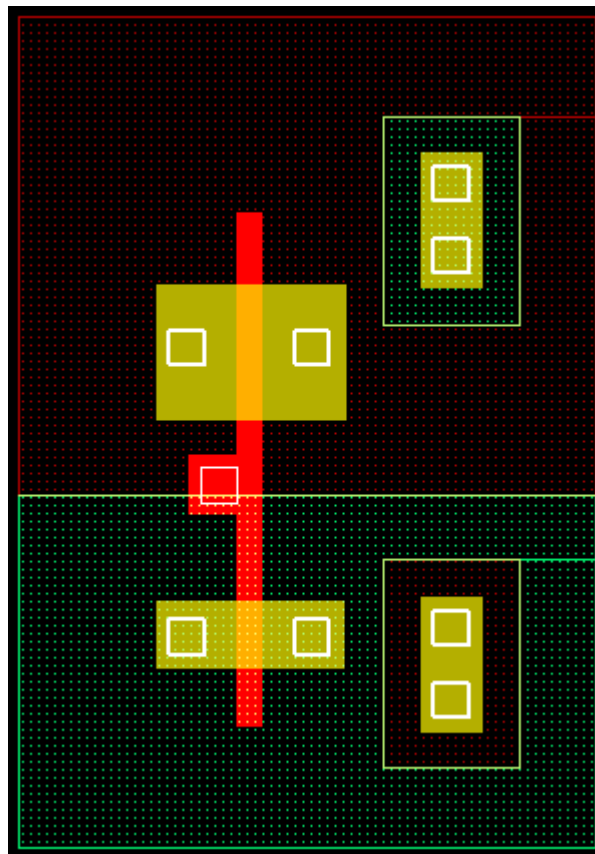
Now select the POLY layer and use the “Create Wire” tool to draw the a strip of poly through both PMOS and NMOS diffusion areas. Make sure the poly is sticking out past the diffusion areas by at least the amount specified in the design rule manual. Create a rectangle of poly in the center of the strip that would be used for the input signal.

Fig. 4.7: Drawing polysilicon



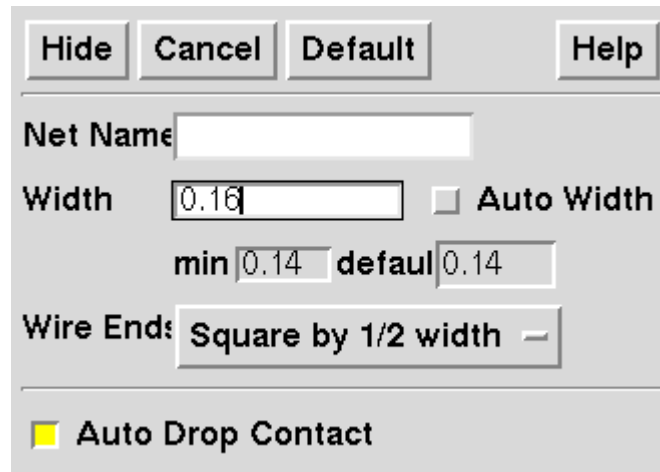
Select the “CO” (contact) layer and use the Create Rectangle or Create Polygon tool in conjunction with rulers to make a contact 0.13 by 0.13. After you have created one contact right click on the contact and make a copy to place the other contacts. Contact placements are shown in Fig. 4.8. Check to see that your contact placements meet the design rules.

Fig. 4.8: Placing contacts



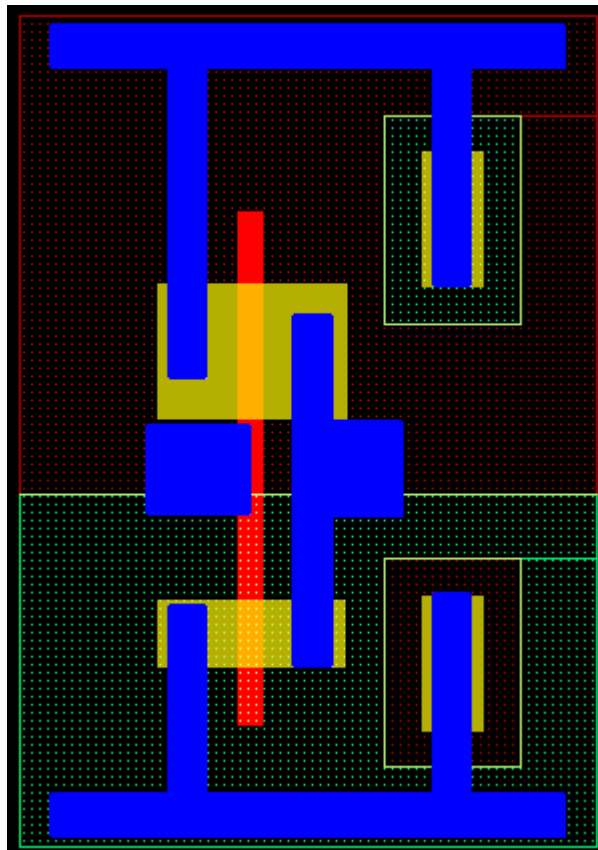
Select the M1 layer and again select the “Create Wire” tool. This time in the “Create Wire” window that pops up, click on the yellow box to unselect “Auto Width”. Then enter 0.16 in the Width field as shown in figure 4.9.

Fig. 4.9: Changing width of wire



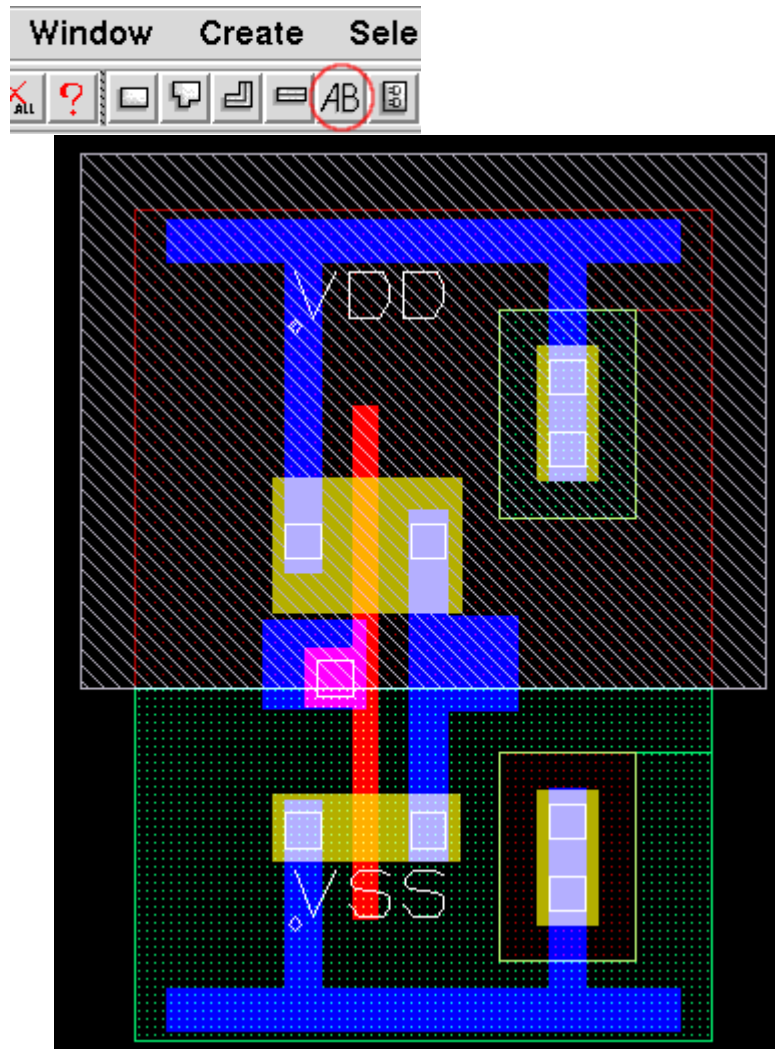
Draw metal one the way it is shown in Fig. 4.10. If you are comfortable with the Create Wire tool, you may also want to try the “Create Path” tool on the left of the Create Wire icon. Make sure the metal is covering the contacts by the amount specified in the design rule manual.

Fig. 4.10: Drawing metal 1 layer



Use the arrows at the bottom of the layer panel to browse through the layers and select the “M1PIN” layer. Select the “Create Text” tool and place text labeling VDD and VSS (Fig. 4.11). You have now completed the initial layout and can move onto DRC.

Fig. 4.11: Creating pin and text



Part 5. Running DRC

After the inverter layout has been drawn to accurately represent the schematic, to verify that the layout meets all the basic design rules, we need to run a DRC(Design Rule Check) . Save the Layout cell by clicking on **Cell > Save**. In CosmosLE, go to **Verification>Hercules>User DRC Runset**.

Fig. 5.1: Execute Hercules window

OK Cancel Default Apply Help

Runset File /packages/process_kit/generic/generic_90n

Input Library Name mylibrary

Input Library Path /courses/engr848/engr848-01

Cell Name 90nminv

View Name CEL

Run Options

Executable hercules

Run Directory /courses/engr848/engr848-01/90nminvDRC

Group Directories

Select Window

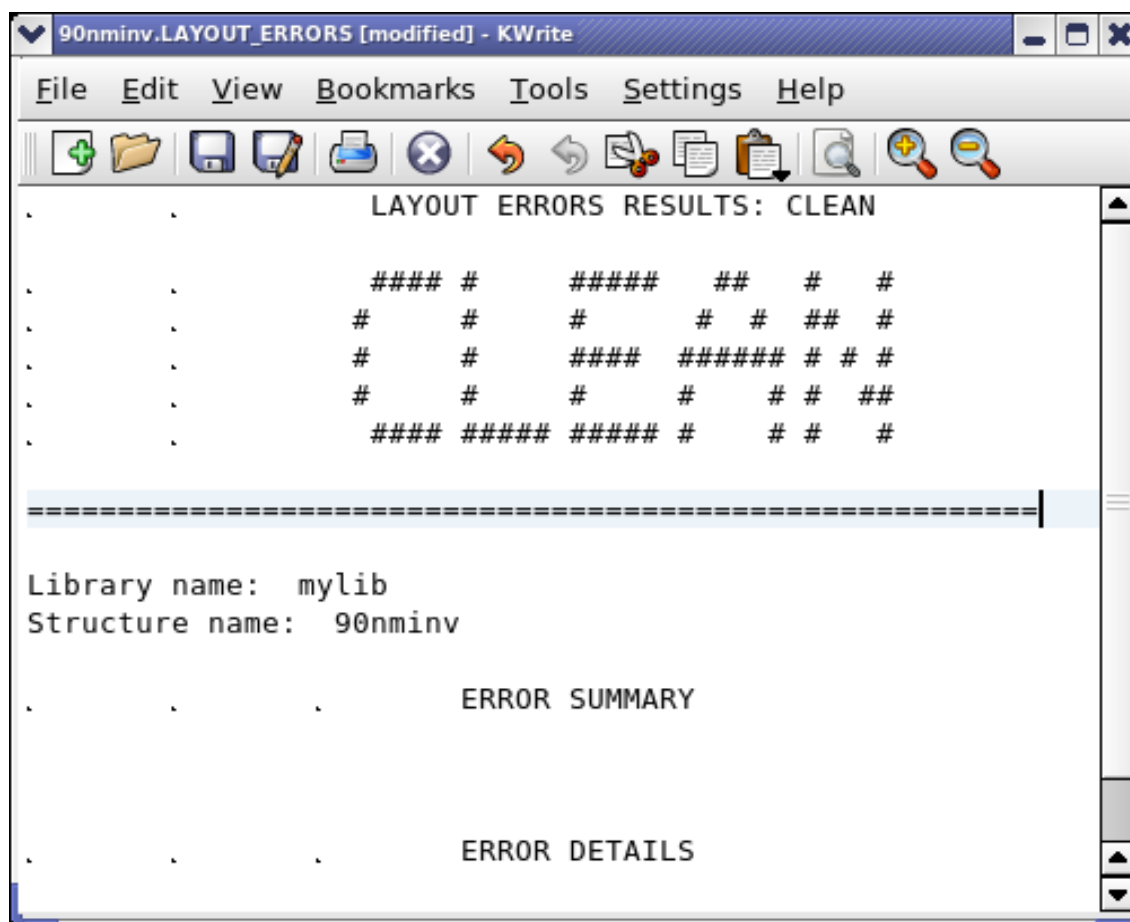
Ref Lib Mode ☒ DEFAULT ☐ HIERARCHICAL ☐ FILE

Locate the runset file from the following directory and click Open.

/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/rules/hercules/drc/rules.drc.ev

When the layout is free from all the errors and meets all the design rules, the output file 90nminv.LAYOUT_ERRORS will say CLEAN as shown below. If there are some errors in the layout, it will say ERROR and the error details are specified in this file. If you have errors in your DRC, check the location and type of errors and correct them. This may take multiple iterations. In the beginning it is advisable to try to correct only a few errors and run the DRC again to check if you corrected them properly. It is important to pass the DRC check before you proceed to LVS and parasitic extraction.

Fig. 5.2: DRC results



Part 6. Running LVS

Before you do the LVS verification it is recommended you create a folder inside your student folder to hold the resulting files that Hercules creates when it runs LVS. In this tutorial the folder created was 90nminvLVS.

In either the schematic or layout window go to **Verification>User LVS Runset**.

Select the file “rules.lvs.9m_saed90.ev” as the Runset File in the following directory:

/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/rules/hercules/lvs/

Under Run Options enter the directory you want Hercules to output to. In this case it is /courses/engr848/engr848-01/90nminvLVS

Under LVS Options select Spice and select the spice netlist we created from the schematic earlier. The default directory is your student folder.

Make sure the fields in your Execute Hercules window mirror the ones in figure 6.1 and click OK.

Fig. 6.1: Execute Hercules window

The screenshot shows a dialog box titled "Execute Hercules" with several sections for configuring a simulation. At the top are buttons for "OK", "Cancel", "Default", "Apply", and "Help".

Runset File: /packages/process_kit/generic/generic_90nm/

Input Library Name: mylibrary

Input Library Path: /courses/engr848/engr848-01

Cell Name: 90nminv

View Name: CEL

Run Options

Executable: hercules

Run Directory: /courses/engr848/engr848-01/90nminvLVS

Group Directories:

Select Window:

Ref Lib Mode: ☒ DEFAULT ☐ HIERARCHICAL ☐ FILE

LVS Options

Schematic Format: ☐ Hercules ☒ Spice ☐ EDIF ☐ Verilog ☐ CDL

☐ Auto Netlist **Spice Netlist Options...**

Schematic Netlist: /courses/engr848/engr848-01/90nminv.spi

Nettran Options: -sp-topCell 90nminv

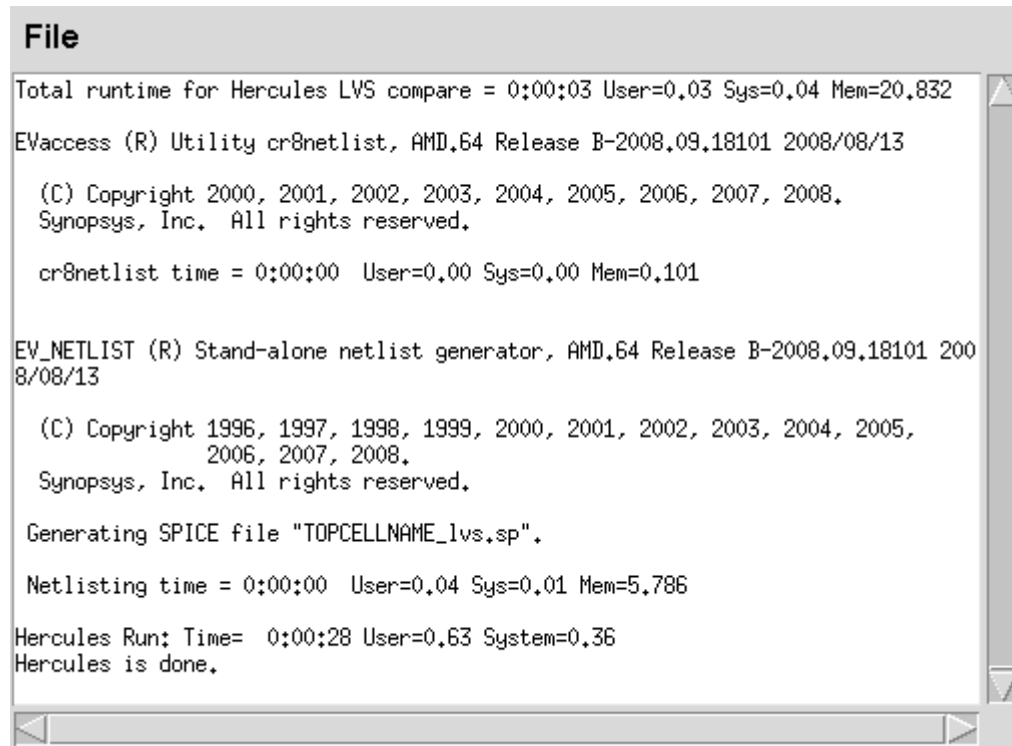
Schematic Top Cel: 90nminv

Equivalence File:

Compare Directory:

A new window called Hercules Output should open and show what Hercules is doing. It should scroll through many processes and will say “Hercules is done.” when it completes.

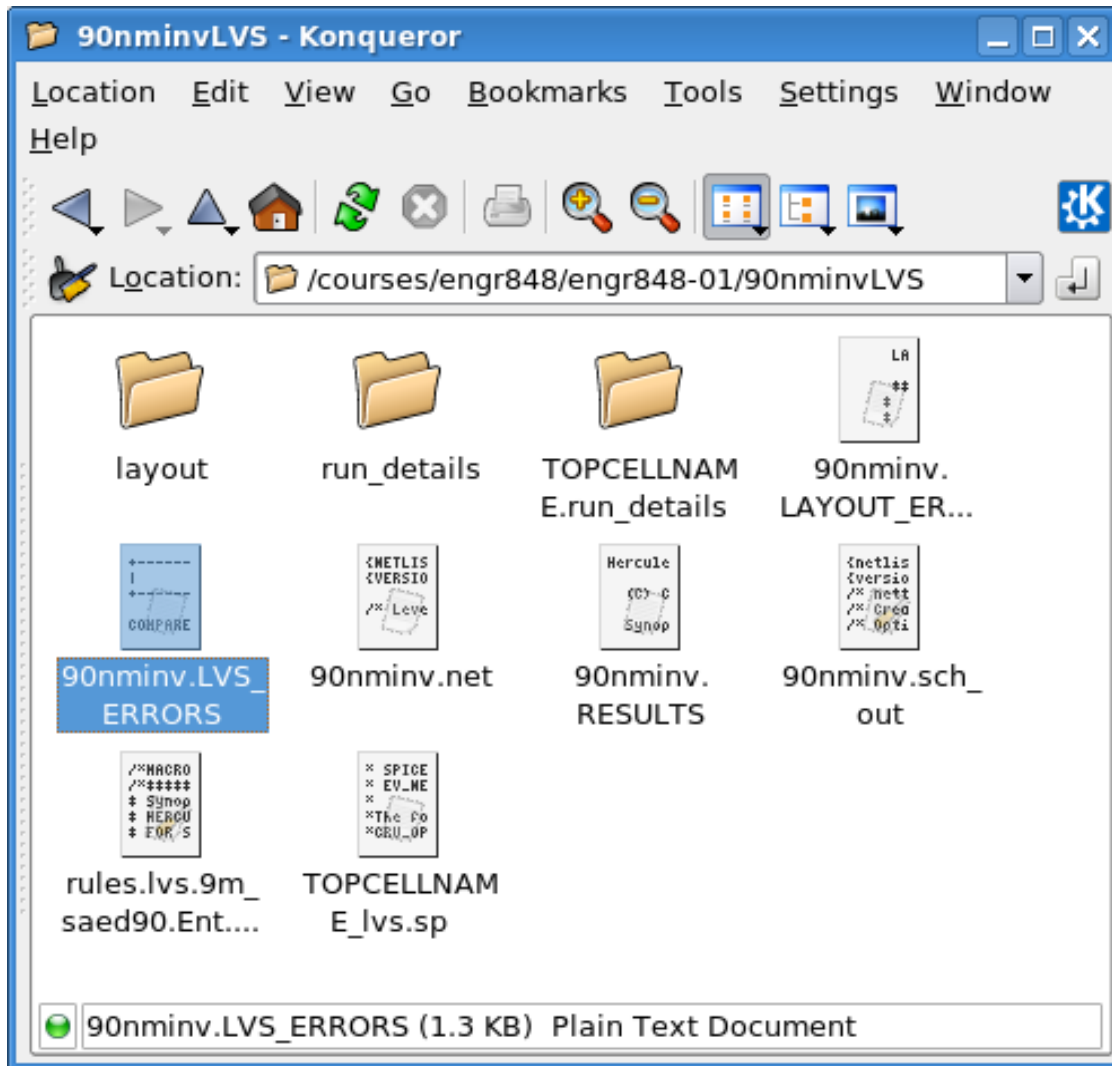
Fig. 6.2: Hercules Output



```
File
Total runtime for Hercules LVS compare = 0:00:03 User=0.03 Sys=0.04 Mem=20.832
EVaccess (R) Utility cr8netlist, AMD.64 Release B-2008.09.18101 2008/08/13
(C) Copyright 2000, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008.
Synopsys, Inc. All rights reserved.
cr8netlist time = 0:00:00 User=0.00 Sys=0.00 Mem=0.101
EV_NETLIST (R) Stand-alone netlist generator, AMD.64 Release B-2008.09.18101 200
8/08/13
(C) Copyright 1996, 1997, 1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005,
2006, 2007, 2008.
Synopsys, Inc. All rights reserved.
Generating SPICE file "TOPCELLNAME_lvs.sp".
Netlisting time = 0:00:00 User=0.04 Sys=0.01 Mem=5.786
Hercules Run: Time= 0:00:28 User=0.63 System=0.36
Hercules is done.
```

Now open the directory that you specified as the Hercules Run directory, in this case /courses/engr848/engr848-01/90nminvLVS. There should be many new files created by Hercules there now. Open 90nminv.LVS_ERRORS

Fig. 6.3: File browser window for LVS



If you have done everything correctly You should see a “PASS” in the 90nminv.LVS_ERRORS file. If it says “FAIL” read the errors it reports and try to fix them on the schematic or layout. If the error is in the schematic make sure to rebuild the spice netlist. Run Hercules again and see if 90nminv.LVS_ERRORS now says “PASS”.

Fig. 6.4: Contents of 90nminv.LVS_ERRORS

```
+-----+
| Hercules LVS Comparison Report |
+-----+
```

COMPARE (R) Hierarchical Layout Vs. Schematic
AMD.64 Release B-2008.09.18104 2008/08/21
Copyright (C) Synopsys, Inc. All rights reserved.

```
-----
LVS error file   = 90nminv.LVS_ERRORS
Layout error file = 90nminv.LAYOUT_ERRORS
Schematic netlist = 90nminv.sch_out
Layout netlist   = 90nminv.net
Equivalence file  = [automatic]
Runset file       = rules.lvs.9m_saed90.Ent.ev
Working directory = /courses/engr848/engr848-01
Compare directory = ./TOPCELLNAME.run_details/compare
Compare start time = 2008-11-11 15:50:56
```

```
-----
Top block compare result: PASS
```

```
#####  ##  #####  #####
#  #  #  #  #  #
#####  #####  #####  #####
#      #      #      #
#      #      #  #####  #####
```

[90NMINV == 90NMINV]

```
-----
Comparison summary
```

1 successful equivalencies
0 failed equivalencies

Schematic and layout agree at all equivalent points.

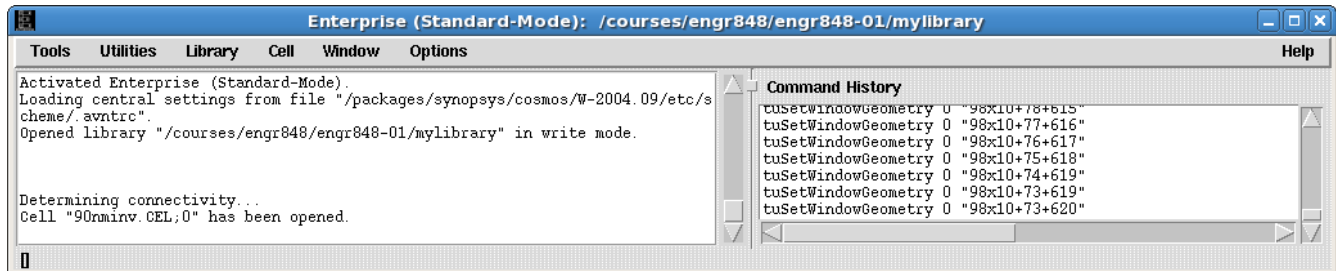
End of LVS comparison report

Part 7. Extracting parasitics

Create a new folder in your account folder called “90nminvSTAR”. This is where we will save the output files created by Star-RCXT.

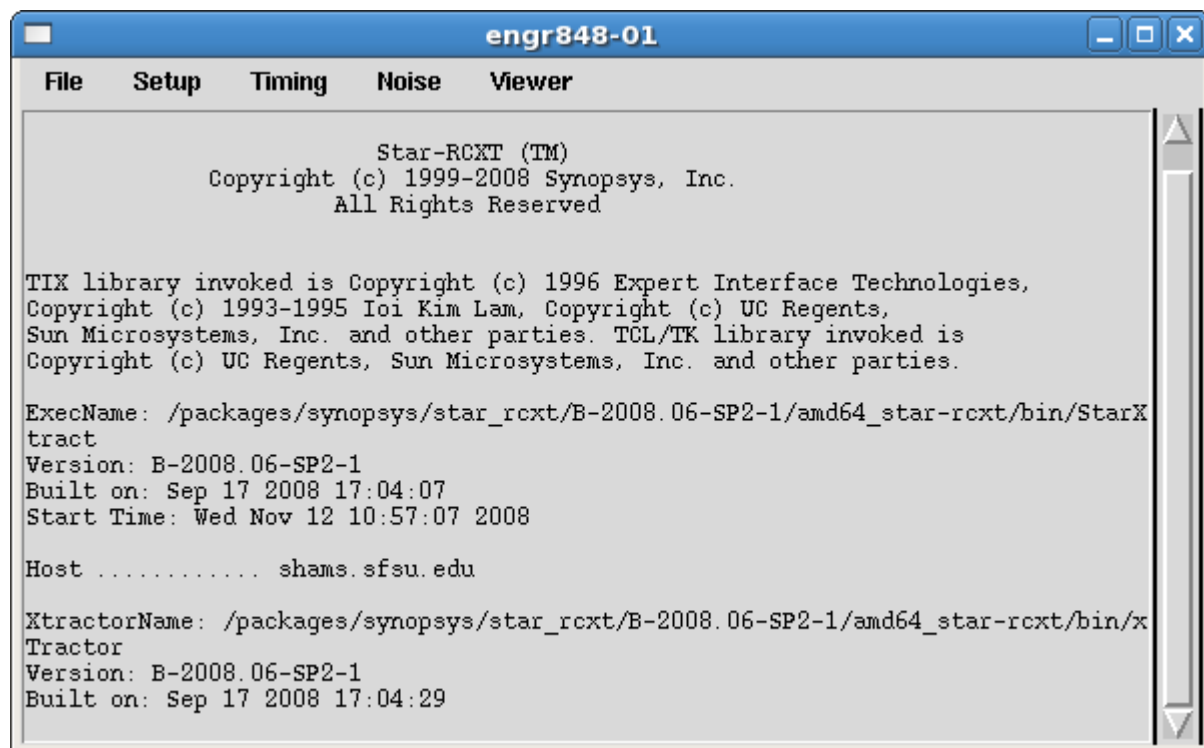
Locate the Cosmos Enterprise Command window which should be located at the bottom of the screen.

Fig. 7.1: Enterprise command window



Now go to **Utilities>StarRC Xtract** (Fig. 7.2).

Fig. 7.2: Star-RCXT window



Go to **Setup>SingleShot**

Fill out the BLOCK field with the name of the layout cell, in our case “90nm1nv”. In the field for MILKYWAY DATABASE, browse for and select the library our cell is in “mylibrary”.

Fig. 7.3: Database tab of Star singleshoot tech form

The screenshot shows the 'Tech Form' dialog box with the 'Database' tab selected. The 'Milkyway' dropdown is set to 'Milkyway'. The 'TIMING' checkbox is unchecked. The 'Database' tab is active, showing fields for 'BLOCK' (90nm1nv), 'MACRO' (empty), 'MILKYWAY DATABASE' (/courses/engr848/engr848-01/mylibrary), 'MILKYWAY CELL VIEW' (empty), 'MILKYWAY ADDITIONAL VIEWS' (empty), 'MILKYWAY REF LIB MODE' (NONE), 'MILKYWAY EXPAND HIERARCHICAL CELL' (NO), 'MILKYWAY TOP LEVEL VIEW' (empty), 'METAL FILL POLYGON HANDLING' (IGNORE), and 'METAL FILL GDS FILE' (empty). There are 'Browse...', 'Add', and 'Remove' buttons for the database, cell view, and metal fill GDS file fields.

When you are done filling out the Database tab, click on the Extraction tab. For the TCAD GRD FILE, select “saed90nm_91m.nxtgrd” in the directory:

/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/rules/starrext

For the MAPPING FILE, select “saed90nm.map” in the directory:

/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/rules/star.txt

Fig. 7.4: Extraction tab of Star singleshot tech form

The screenshot shows the 'Tech Form' window with the 'Extraction' tab selected. The window has a title bar with 'Tech Form' and standard window controls. Below the title bar are buttons for 'OK', 'Cancel', 'Apply', and 'Help'. A dropdown menu shows 'Milkyway' and a checkbox for 'TIMING' is present. The 'Extraction' tab is active, showing a list of configuration items on the left and their corresponding values or controls on the right. The items are: 'TCAD GRD FILE' with a text field containing a path and 'Add', 'Browse...', and 'Remove' buttons; 'MAPPING FILE' with a text field containing a path and a 'Browse...' button; 'EXTRACTION' with a dropdown set to 'RC'; 'TARGET ANALYSIS' with a dropdown set to 'NONE'; 'MODE' with a dropdown set to '100'; 'REDUCTION' with a dropdown set to 'YES'; 'POWER REDUCTION' with a dropdown set to 'YES'; 'INSTANCE PORT' with a text field and 'Add' and 'Remove' buttons; and 'INSTANCE PORT OPEN CONDUCTANCE' with a text field containing '10'.

Parameter	Value/Control
TCAD GRD FILE	/packages/process_kit/generic/generic_90nm/ [Add, Browse..., Remove]
MAPPING FILE	/packages/process_kit/generic/generic_90nm/upd: [Browse...]
EXTRACTION	RC
TARGET ANALYSIS	NONE
MODE	100
REDUCTION	YES
POWER REDUCTION	YES
INSTANCE PORT	[Empty Field] [Add, Remove]
INSTANCE PORT OPEN CONDUCTANCE	10

Open the Processing tab and select the folder “90nmInvSTAR” we created earlier for our STAR DIRECTORY.

Fig. 7.5: Processing tab of Star singleshoot tech form

The image shows a software window titled "Tech Form" with a blue title bar and standard window controls. At the top, there are buttons for "OK", "Cancel", "Apply", and a "Help" link. Below these is a dropdown menu currently set to "Milkyway" and a checkbox labeled "TIMING". The main area contains a series of tabs: "Database", "Extraction", "Processing" (which is selected), "Netlist", "Noise", "Field Solver", "Simulation", and "Xref". Under the "Processing" tab, there are several sections: "STAR DIRECTORY" with a text field containing "/courses/engr848/engr848-01/90nmInvSTAR" and a "Browse..." button; "NETS" with a list box and "Add" and "Remove" buttons; "NETS FILE" with a text field and "Browse..." and "Remove" buttons; and four options with "NO" buttons: "TRANSLATE FLOATING AS FILL", "REMOVE FLOATING NETS", "REMOVE DANGLING NETS", and "REMOVE FLOATING PORTS". At the bottom, there are two empty text fields for "REMOVE NET PROPERTY".

Once you have clicked OK on the SingleShot Tech Form, go to File>Run and select Xtractor (Netlist will also be highlighted). Click OK and the the Star-RCXT window should start showing the processes for the extraction. Star may pause between processes, so wait until it is completely done like shown in figure 7.6.

Fig. 7.6: Star-RCXT processing output window

```

engr848-01
File  Setup  Timing  Noise  Viewer

xTract Post Process DB:  Wed Nov 12 11:07:07 2008
Completed 50% Time=00:00:00 RemainingTime=00:00:00 Mem=29.1367
Completed 100% Time=00:00:00 RemainingTime=00:00:00 Mem=29.6094
  Warnings: 0    Errors: 0
  xTractPP      Elp=00:00:00 Cpu=00:00:00 Utr=0.0    Sys=0.0    Mem=29.6
Done

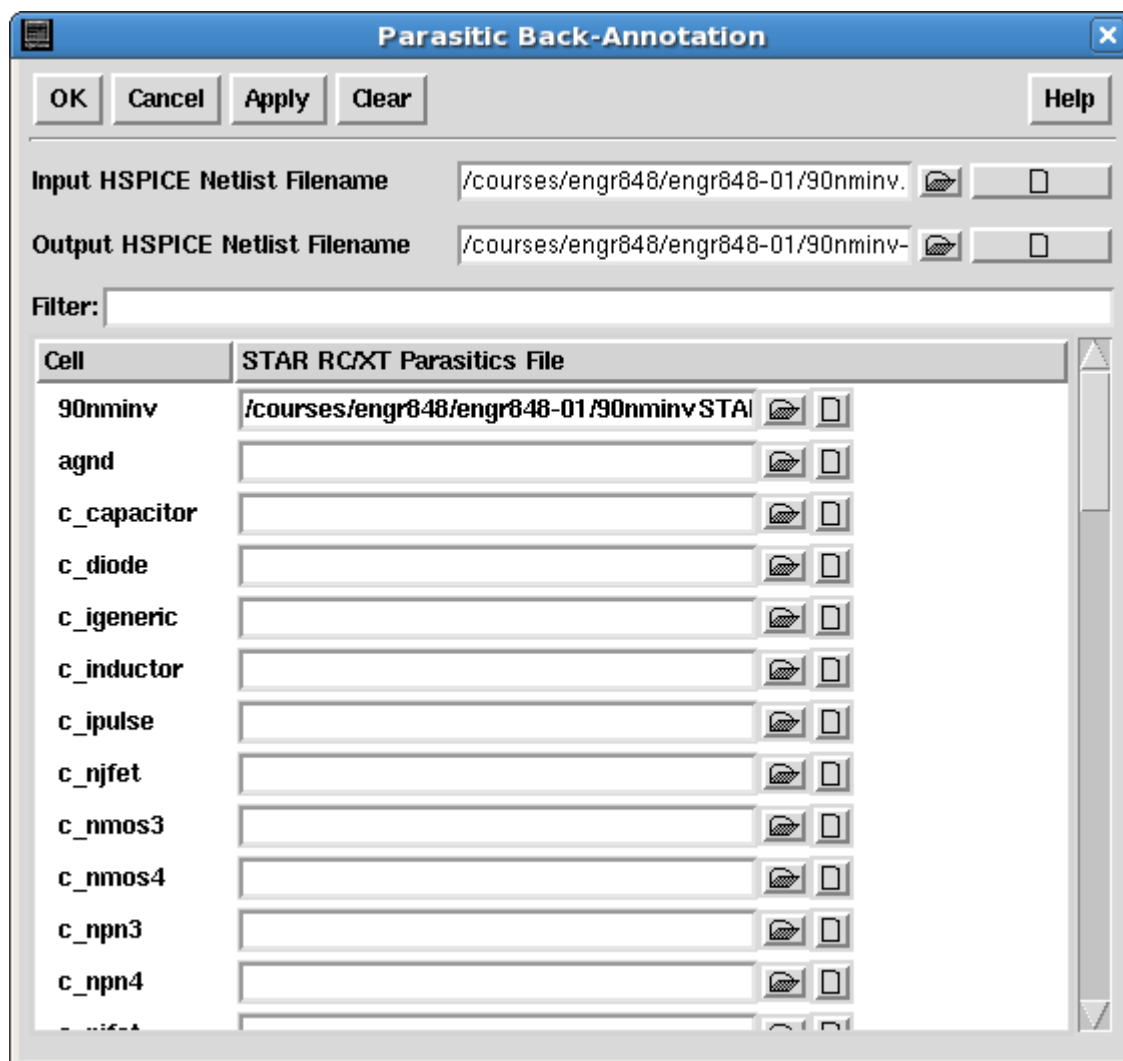
Netlist DB:  Wed Nov 12 11:07:07 2008
Completed 50% Time=00:00:00 RemainingTime=00:00:00 Mem=32.4414
Completed 100% Time=00:00:00 RemainingTime=00:00:00 Mem=32.4414
  Warnings: 0    Errors: 0
  Netlist      Elp=00:00:00 Cpu=00:00:00 Utr=0.0    Sys=0.0    Mem=32.4
Done

Layers      Elp=00:00:00 Cpu=00:00:00 Utr=0.2    Sys=0.1    Mem=134.6
Translate   Elp=00:00:03 Cpu=00:00:00 Utr=0.3    Sys=0.1    Mem=176.4
NetlistSetup Elp=00:00:00 Cpu=00:00:00 Utr=0.0    Sys=0.0    Mem=0.0
xTract      Elp=00:00:22 Cpu=00:00:00 Utr=0.3    Sys=0.1    Mem=98.5
xTractPP    Elp=00:00:00 Cpu=00:00:00 Utr=0.0    Sys=0.0    Mem=29.6
Netlist     Elp=00:00:00 Cpu=00:00:00 Utr=0.0    Sys=0.0    Mem=32.4

Done      Elp=00:00:25 Cpu=00:00:01 Utr=0.8    Sys=0.3    Mem=176.4
  
```

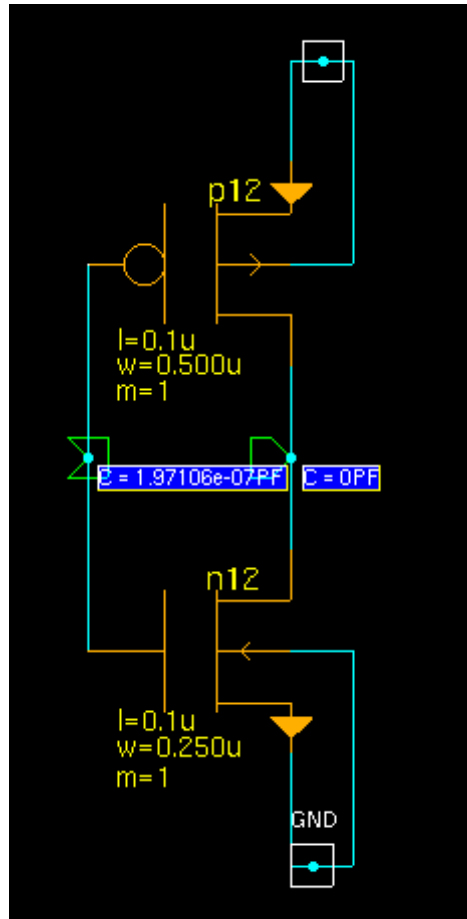
Go to **Simulation>Parasitics** and in the 90nminv field select the file “90nminv.spf” in the 90nminvSTAR folder you created in your account folder.

Fig. 7.7: Parasitic Back-Annotation window



Now you should see that a capacitance has been added to your inverter schematic.

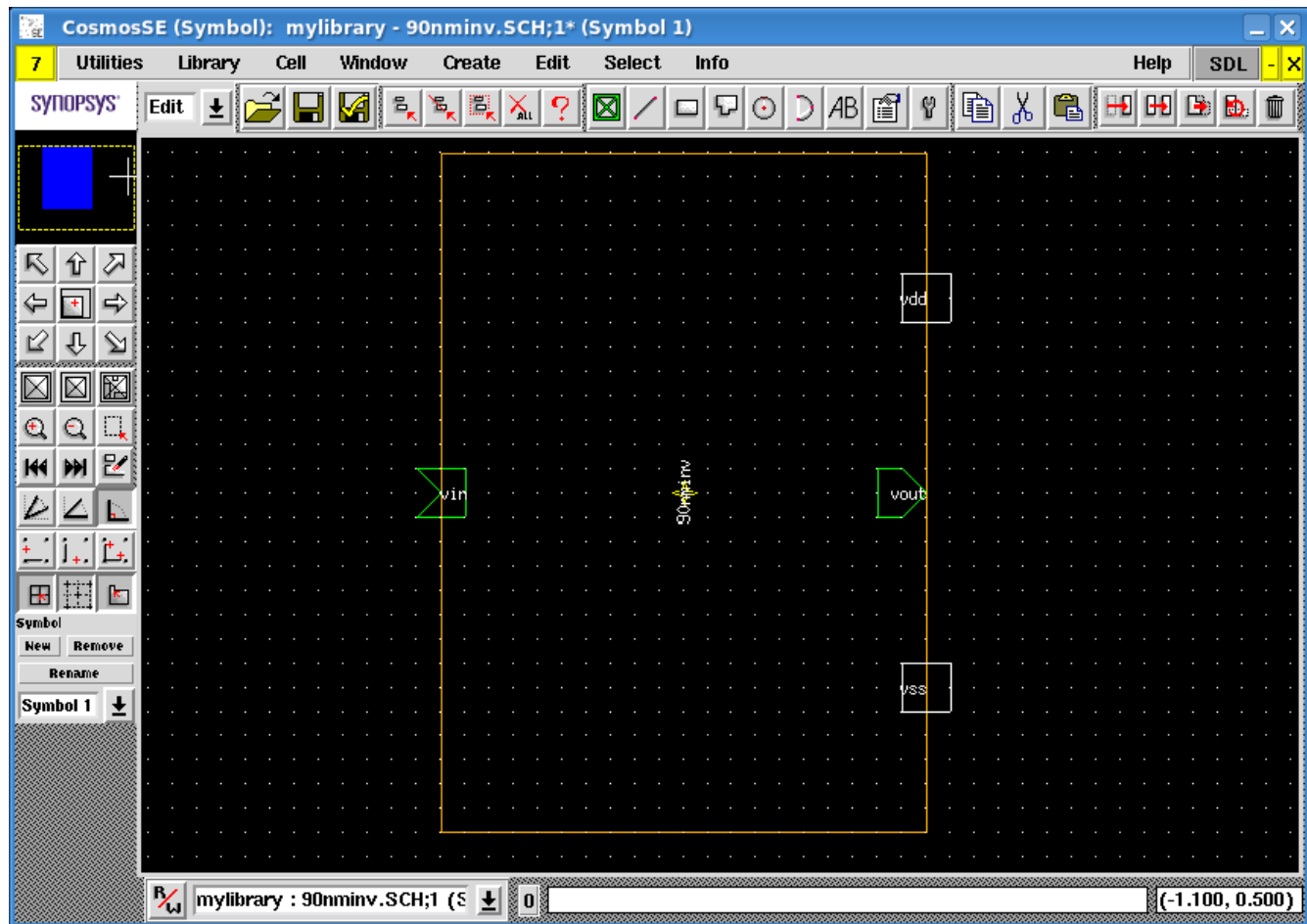
Fig. 7.8: Schematic with parasitics applied



Part 8. Gate level design and simulation

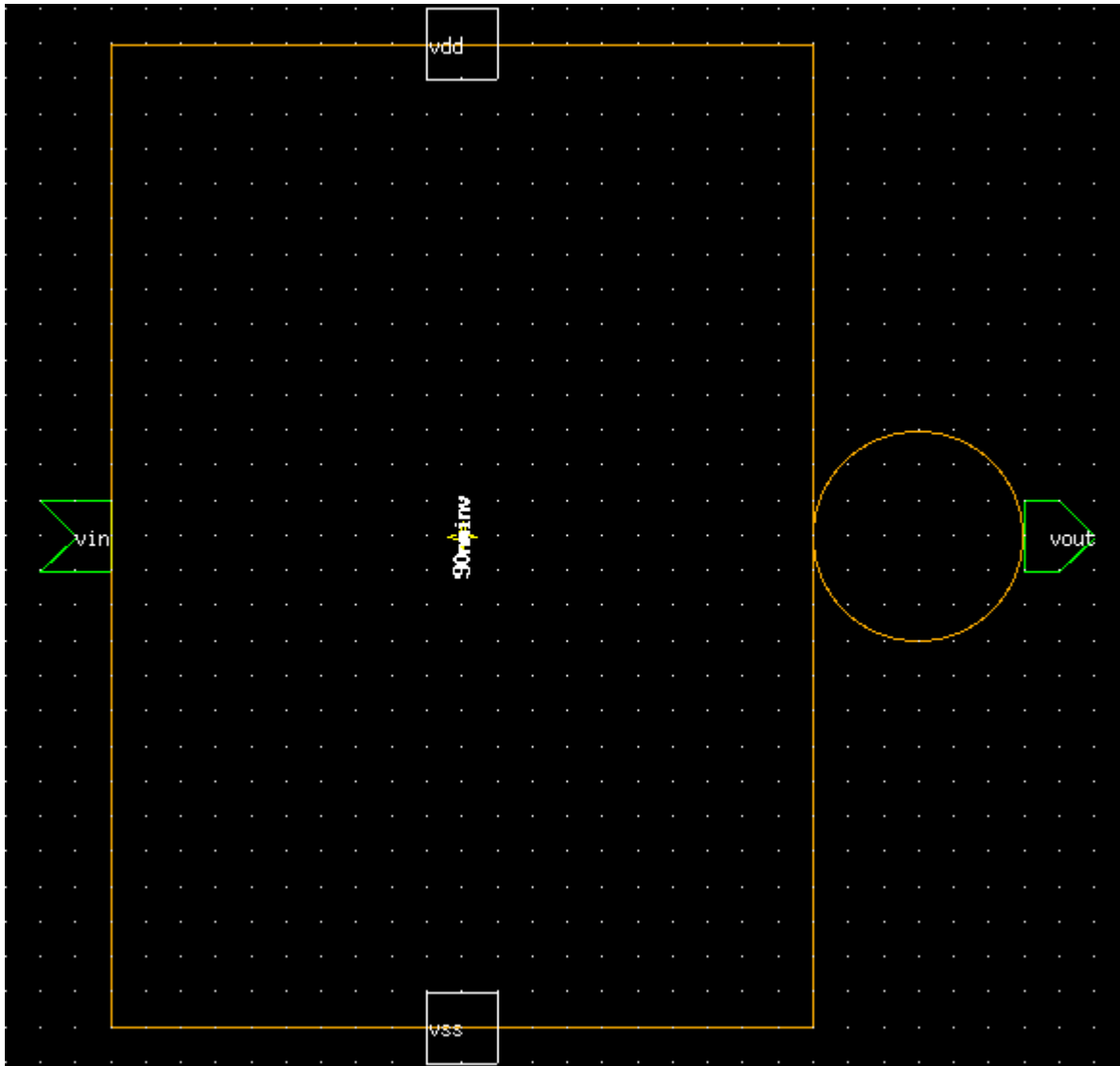
Now that we have a transistor level model of an inverter we can continue on and use that cell in a gate level design of a ring oscillator. First we need to make a symbol for our inverter. In the menu bar go to **Cell>Generate Symbol**. Cosmos will now generate a symbol of the inverter that can be used higher layers of circuit design.

Fig. 8.1a: Generated symbol for inverter



You can edit the symbol to look more like the standard inverter symbol we are used to seeing by moving the ports and drawing a circle with the new tools you see in the tool bar.

Fig. 8.1b: Modified inverter symbol

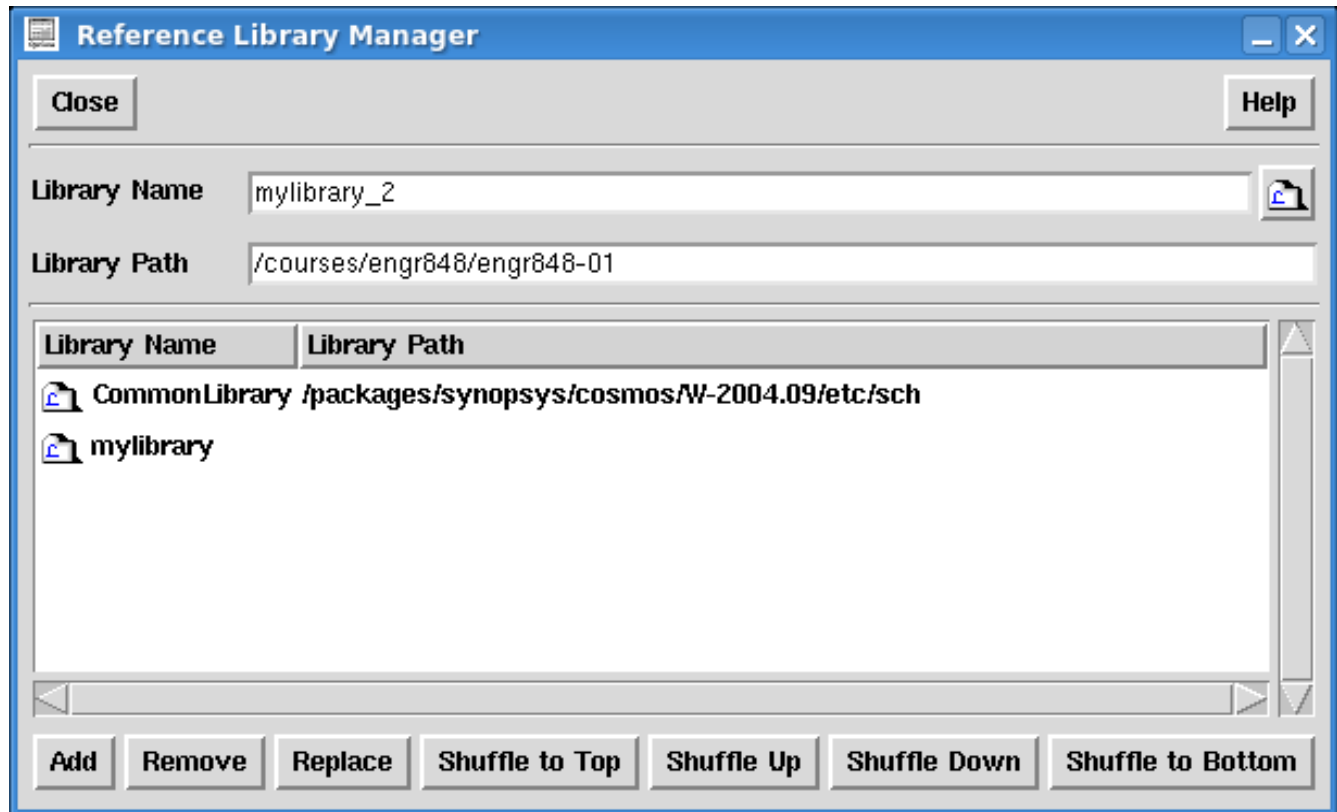


In the menu bar go to **Library>Create**. In the “Library Name” field enter “mylibrary_2” and in the “Tech File Name” field copy and paste this file directory in the field:

/packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/techfile/saed90nm_1p9m.tf

In the menu bar go to **Library>Manager**. Click “Add” and select the Common library, then add the first library we made called “mylibrary”. Click “Close”.

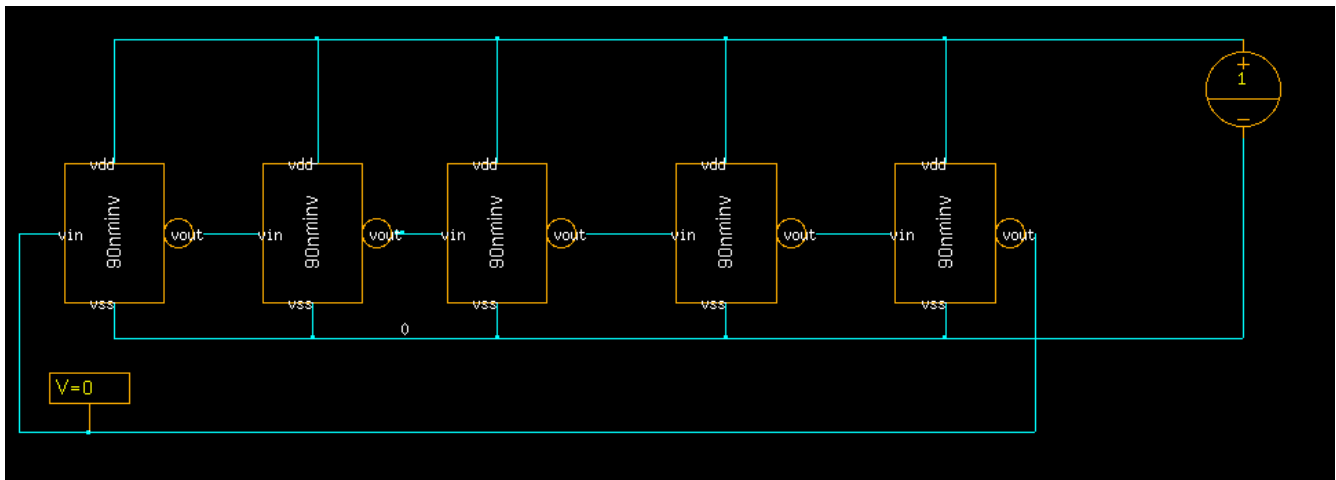
Fig. 8.2: Library manager window



Create a new cell called “ring_oscillator”. Now go to **Create>Instance** to place parts like you did in the first schematic. Now you should see your inverter in the list of cells. Place five of them in series with the output of the last inverter connected to the input of the first like in the schematic below. Connect them to a 1V DC power supply and again make sure the ground net is '0'. Again go to **Create>Instance** and select the cell named “nodeset”. Place it on the net near the first inverter like in the schematic. Nodeset allows us to specify initial conditions for that node, which we need to do to make the oscillator oscillate.

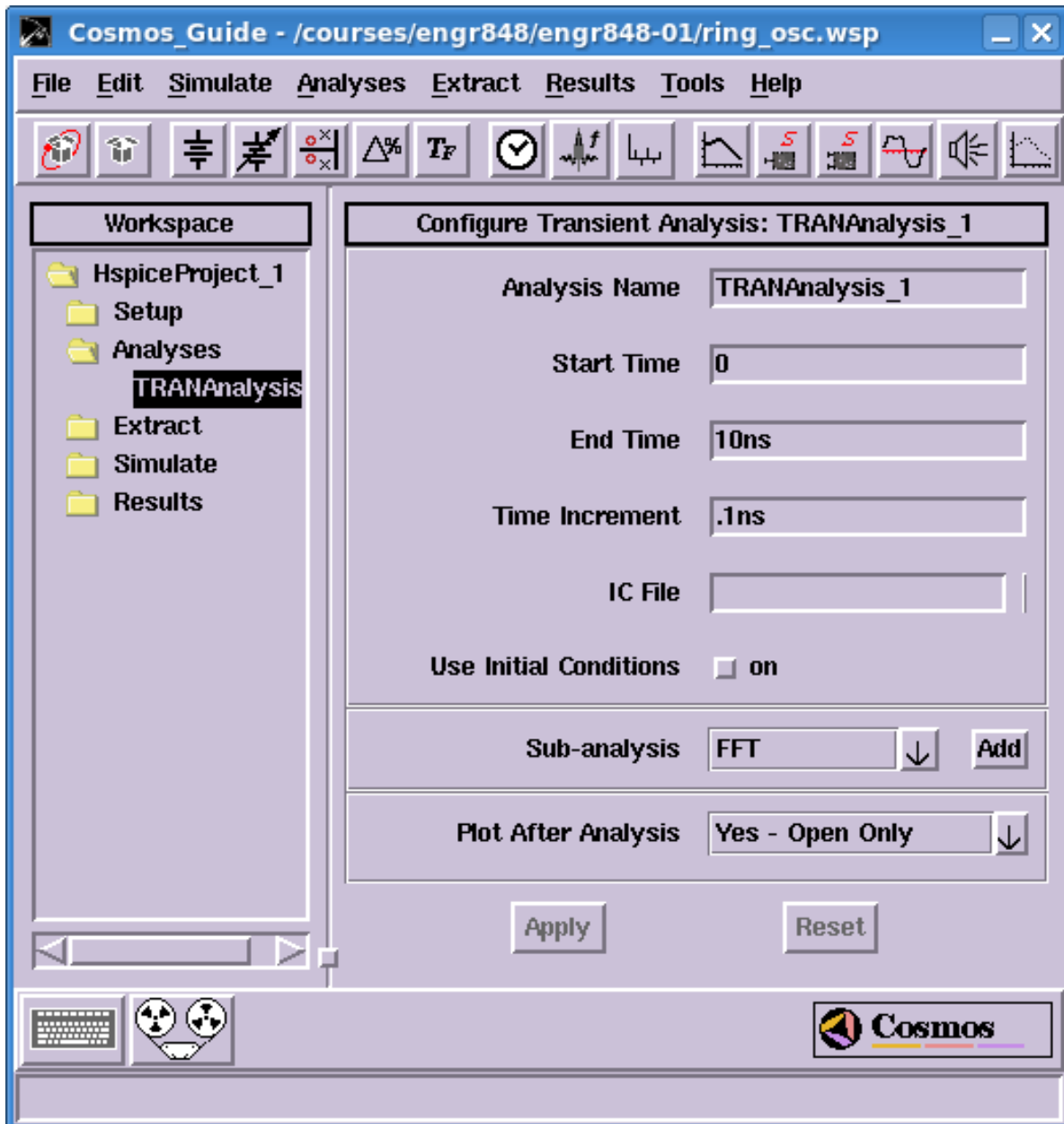
If we didn't specify the initial conditions, the oscillator would stay around 0.5V and not oscillate at all. Change the properties of the nodeset so the initial voltage is zero. You may also want to change the name of the nets. Make sure everything is connected correctly and you have a ground before you proceed to the next step.

Fig. 8.3: Ring oscillator schematic



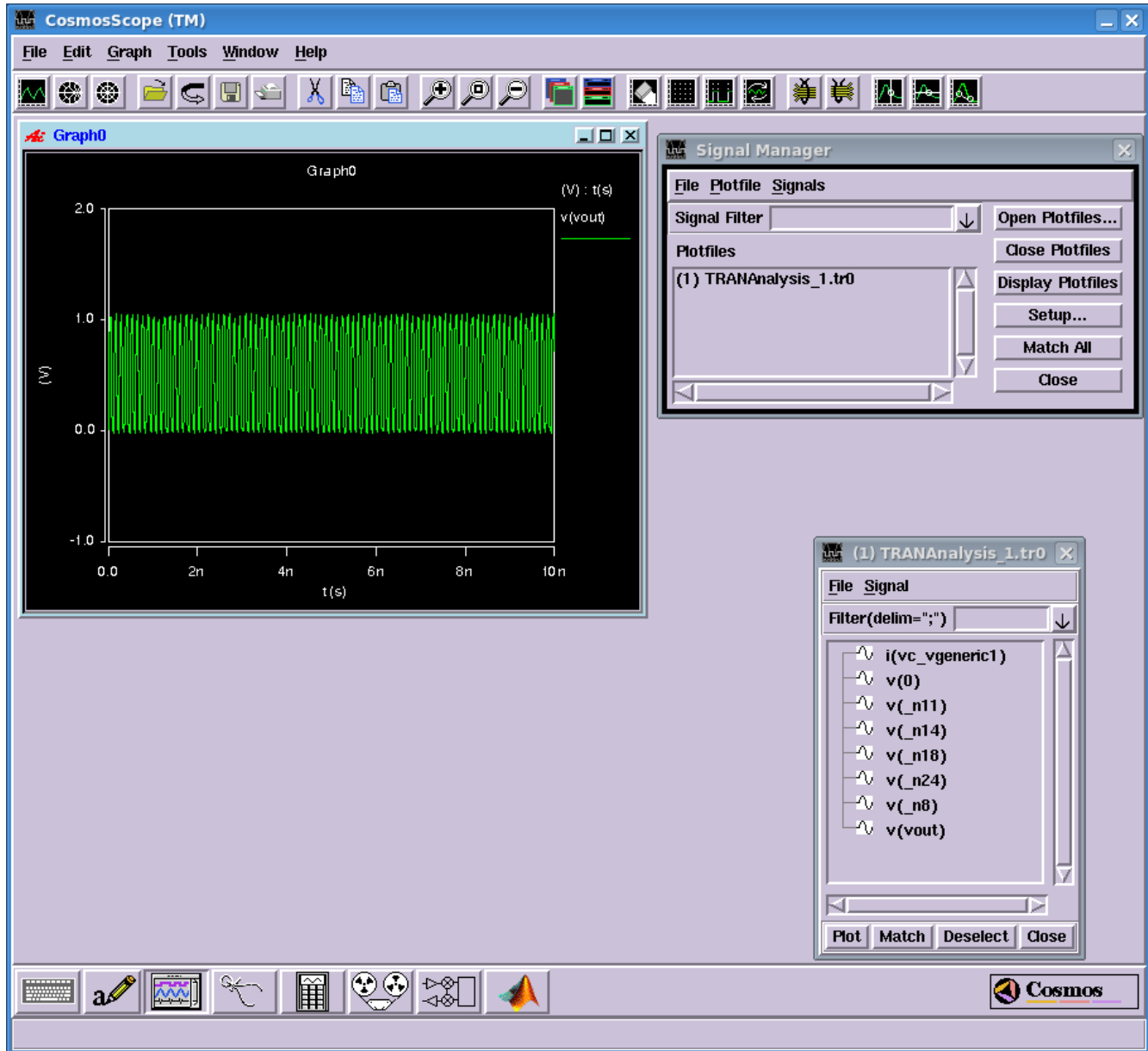
When you are done with the schematic create the netlist by selecting **Simulation>Spice** in the menu bar. Next select **Simulation>Transient Analysis**. Fill out the fields like in the figure 8.4 and click “Apply”.

Fig. 8.4: Transient analysis for ring oscillator in Cosmos Guide



Now go to setup and add the model library like we did in part one on page 13, again selecting TT_12 as our model. When you are done, run the simulation. If you have no errors Cosmos Scope should open and the wave for voltage out of the oscillator should look the same as the one in figure 8.5a

Fig. 8.5a: Cosmos scope of ring oscillator



This waveform has a very high frequency, so we'd like to adjust the time axis of the graph so we can see the waveform better. If you move the mouse over the time axis it will turn red like in figure 8.5b. Right click and select "Attributes". Change the 10n in the range field to 2n and click Apply. Your graph should now look like the one in figure 8.5d.

Fig. 8.5b: Graph of oscillation

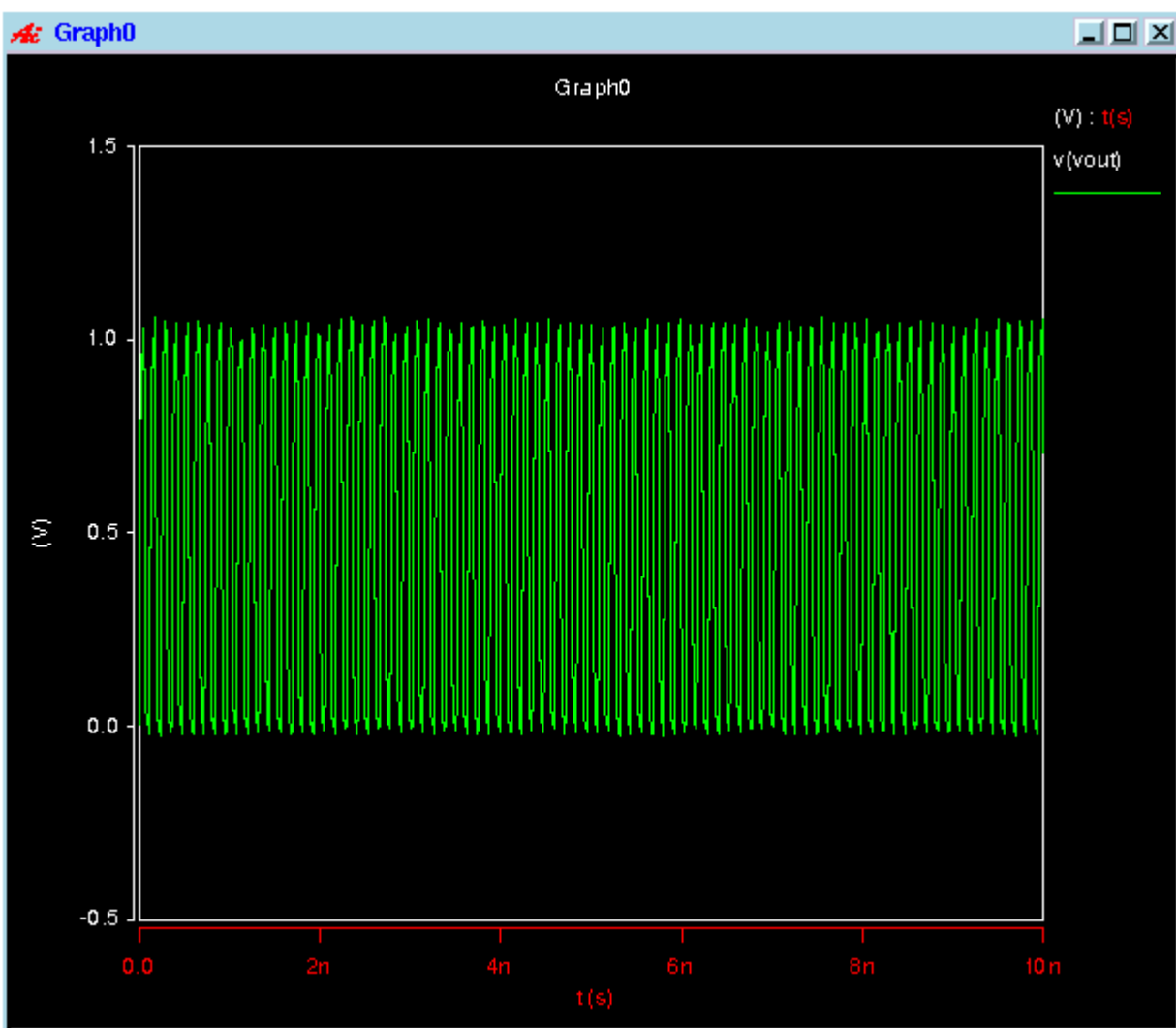


Fig. 8.5c: Edit axis attributes window

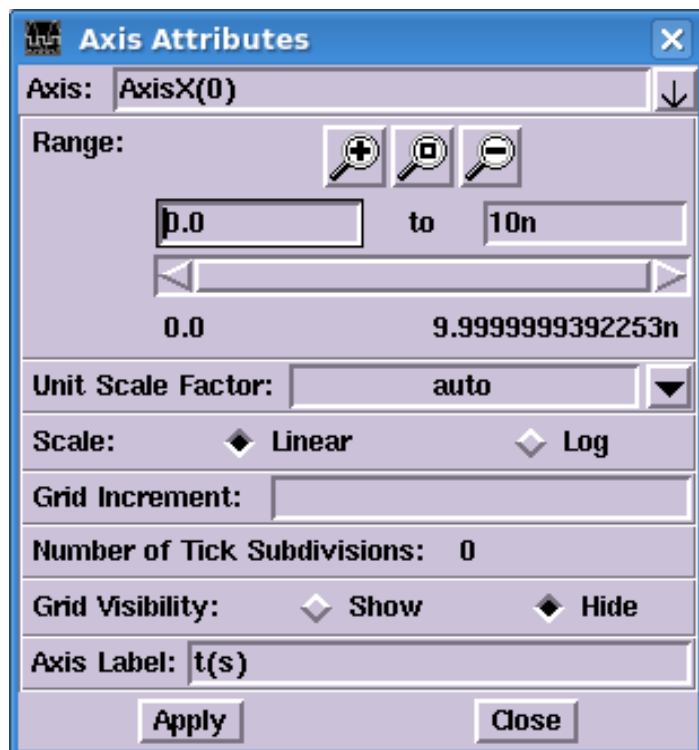
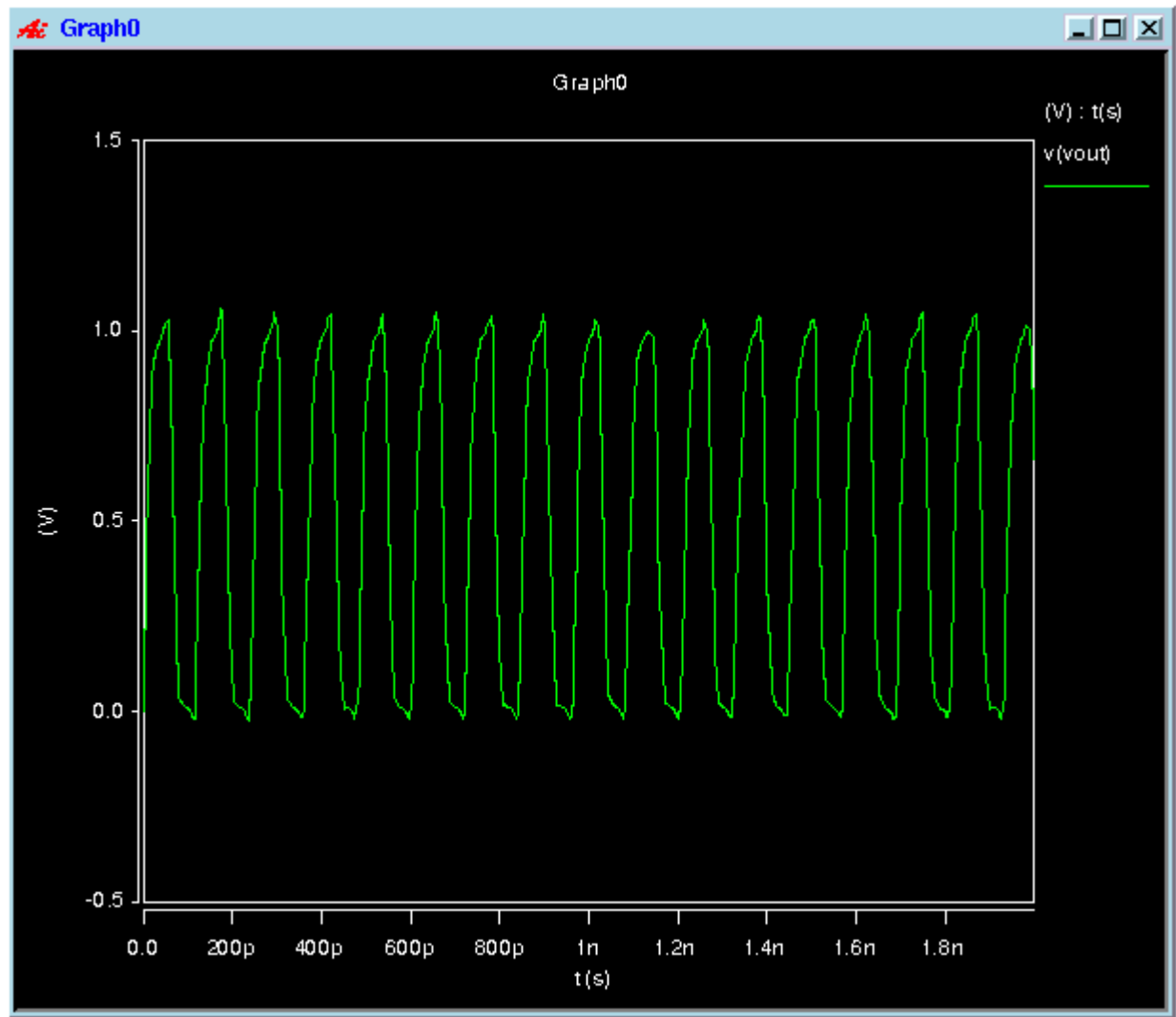


Fig. 8.5d: Adjusted graph of oscillation



Now that we have simulated the ring oscillator we can find the frequency of oscillation. How could we decrease the frequency? How about increasing it? Try altering the schematic or part properties and simulate the new design. What differences do you see?

Also, you can use the other signals to compare V_{in} vs. V_{out} across one inverter. What causes the difference with the transient analysis you did across one inverter in part 3?

Part 9. Trouble Shooting

CosmosLE will not open in the CAD lab:

Try restarting both your SSH session and exit Xming and reopen. Make sure the setup commands have been run successfully.

Reference library, tech file, or runset will not load:

Check to see the the library path is correct after you select a library in the file browser. Sometimes there is a glitch in the fields. If there is a glitch try typing in the file path manually.

Schematic or layout has glitches:

Inside the schematic or layout window scroll away from the object and then return to the object. It should be refreshed. When you select the option to visualize or hide a layer in CosmosLE it is common for the change the change may not be readily apparent. Scroll away and back to refresh.

Window does not close when close window icon is clicked:

*This is an issue with the x-server. Inside the window you want to close go to **File>Quit**.*

Library and cell will open but you are unable to edit cell:

Your cell has a lock on it. Open the library and check the “SCH” and “CEL” folders in the terminal or file transfer window. Delete all files with a “.lock” file extension.