RELIABILITY ANALYSIS OF DYNAMIC LOGIC CIRCUITS UNDER TRANSISTOR AGING EFFECTS IN NANOTECHNOLOGY

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by

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CERTIFICATION OF APPROVAL

I certify that I have read *Reliability Analysis of Dynamic Logic Circuits under Transistor Aging Effects in Nanotechnology* by Milana Ram, and that in my opinion this work meets the criteria for approving a thesis submitted in partial fulfillment of the requirement for the degree: Master of Sciences in Engineering at San Francisco State University.

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Reliability Analysis of Dynamic Logic Circuits under Transistor Aging Effects in Nanotechnology

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As the CMOS technology scales down towards nanoscale dimensions, there are increasing transistor reliability challenges which impact the lifetime of integrated circuits. These issues are known as aging effects, which result in degradation of the performance of circuits. NBTI (Negative biased temperature instability) is a well known aging phenomenon which is also one of the limiting factors for future scaling of devices. In this project we will analyze the impact of NBTI on performance of dynamic logic circuits. Dynamic logic is a popular design methodology in high speed digital electronics. We will first analyze the impact of NBTI on performance metrics of a dynamic logic circuit, namely, delay, power, and Unity Noise Gain (UNG). It is observed that the aging of the PMOS keeper transistor and the PMOS in the output inverter of a dynamic logic circuit have opposing effects of the dynamic logic circuit performance under NBTI. This provides the opportunity to nullify the effect of NBTI on aging of a dynamic logic circuit by carefully optimizing the sizing of the keeper and the inverter PMOS transistors. We propose PMOS sizing optimization to reduce the impact of the reliability issues in dynamic logic circuits. Our results show that optimal sizing of the PMOS transistors in a dynamic logic circuit, the circuit becomes immune to the NBTI aging effect. After the optimization, the degradations in delay, power, and UNG over a 2-year lifetime are measured to be 1.71%, 0%, and 0% in a 32nm CMOS technology. In a non-optimized circuit, this degradation is too high to be ignored.

I certify that the Abstract is a correct representation of the content of this thesis.

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Chair, Thesis Committee Date

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1. INTRODUCTION

Over the recent years there has been aggressive scaling in CMOS. After the silicon technology has entered the nanometer regime the performance of transistors degrades over time. Aggressive scaling has resulted in augmented short channel effects, exponential rise in leakage currents, process variations, depressed gate control for transistors and hysterical power densities. Electrical and physical properties if transistors are deterministic and unpredictable over the device lifetime.

The most important factors that cause degradation in transistor performance are due to Negative Bias Temperature Instability (NBTI) and Positive Bias Temperature Instability (PBTI). NBTI results from interface trapped charges from the broken Si-H bonds at the interface [4]. PBTI results from oxide trapped charges [10]. NBTI and PBTI resultant degradation not only depends on supply voltage and temperature but also threshold voltage and other technology parameters of the MOS transistor. Further scaling results in more threshold voltage degradation. MOS becomes a slower switch with threshold voltage degradation which leads to undesirable operation of circuits consisting MOS transistors. Apart from aging process temperature variations play a vital role in circuit operations.

Low power design has always been of utmost importance to increase the robustness of a circuit. This thesis addresses the issues of NBTI (aging) on a dynamic logic circuit and provides design optimization to critical metrics such as power consumption, delay and noise immunity. Many techniques have been developed so far to reduce the leakage power and noise, however not

much research has been done with consideration of the 3 major parameters such as delay, power and noise. The minimization of propagation delay, power consumption and leakage noise is achieved by optimal sizing of the devices. The two main PMOS transistors which are affected by NBTI are sized till the best combination which results in minimum change due to aging is achieved. The experiments are done with 32nm CMOS dynamic logic circuit. It is observed that:

- In a non-optimized circuit the NBTI degradation can be as high as 10%
- Aging of the PMOS keeper transistor and the PMOS in the output inverter of a dynamic logic circuit have opposing effects on the dynamic logic circuit performance under NBTI. This provides the opportunity to nullify the effect of NBTI on aging of a dynamic logic circuit by carefully optimizing the sizing of the keeper and the inverter PMOS transistors
- NBTI resultant V_t degradation are more significant at higher temperature.

We also analyzed that,

- By adding an inverter load at the output not only the delay but the degradation due to aging also increases
- The width of the PMOS transistor has to be sized at least 2 times that of Keeper transistor. Decreased sizing of the PMOS results in high degradation overage
- As the sizing of the Keeper transistor increases the change in the power consumption overage increases
- The change in the noise immunity of the circuit is of the order 1 mV overage.

The remainder of this thesis is organized as follows. Section 2 includes the introduction to Dynamic Logic and its operations. Section 3 describes performance metrics namely delay, power consumption and Unity Noise Gain. Section 4 discusses the NBTI model. Section 5 describes the effect of NBTI on the 3 performance metrics. In Section 6, we explain the transistor sizing optimization to reduce the effect of aging. Finally section 7 concludes the thesis.

2. Dynamic Logic Circuit and its Operation

Dynamic logic is a popular design methodology in high speed digital electronics which has a reduced implementation area. The proposed dynamic logic circuit is show in Fig 1.

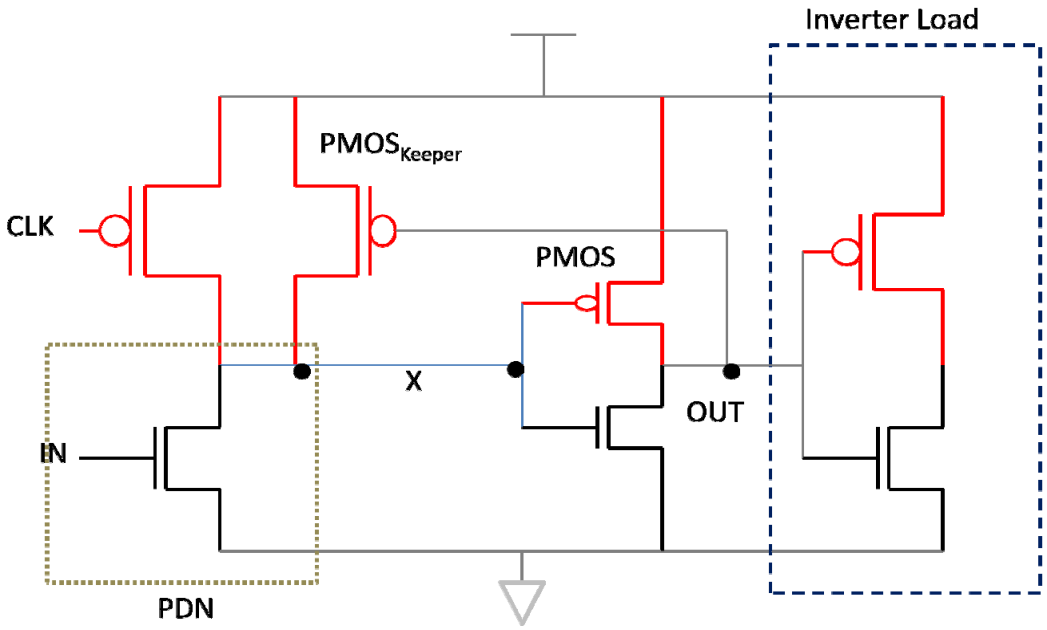

Fig 1. Dynamic Logic Circuit

Fig 1 shows the schematic of a dynamic logic circuit, the pull down network (PDN) is replaced by a single NMOS in our circuit. The operation of this circuit is divided into two major phases: precharge and evaluation, with the mode of operation determined by the clock signal CLK [11]. The PMOS keeper transistor holds the value of the output till the input is changed hence it is referred to as a keeper. The total delay of the circuit is from CLK to node X and node X to Out.

$$T_p = T_{p1} + T_{p2} \quad (1)$$

Where,

T_p: Total delay

T_{p1}: Delay CLK to X

T_{p2}: Delay X to Out

During the precharge the phase the output is high and keeper stores the value of the input. At the evaluation phase the discharge takes place through two phases

Phase 1: T_{p1}: IN to X (Fig 2)

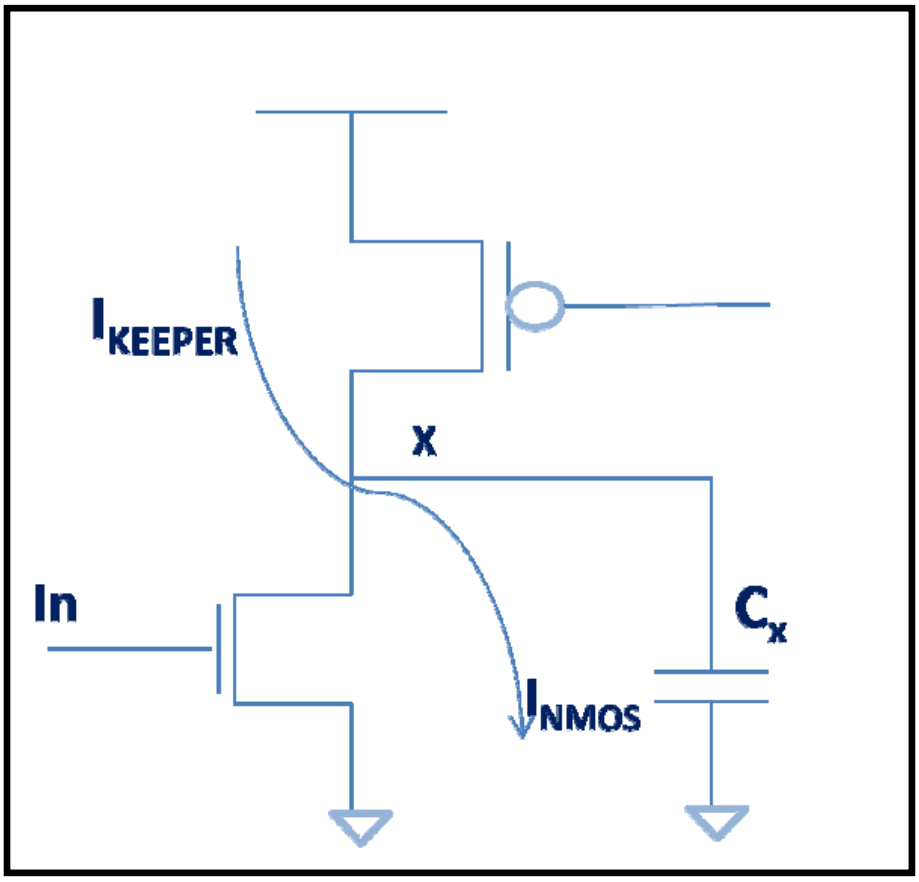

Fig. 2: IN to X delay path

$$T_{p1} = \frac{C_x(V_{dd}/2)}{I_{NMOS} - I_{KEEPER}} \quad (2)$$

Phase 2: T_{p2}: X to OUT (Fig 3)

$$T_{p2} = \frac{C_{out}(V_{dd}/2)}{I_{PMOS}} \quad (3)$$

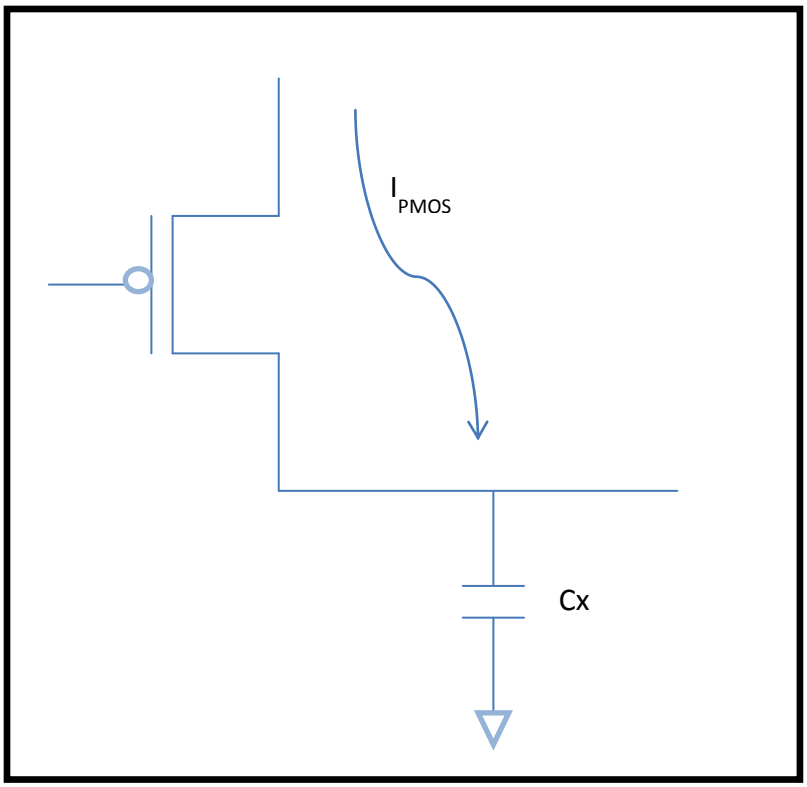

Fig 3. X to OUT delay path

Therefore, $T_{p1}+ T_{p2}$ =

$$\frac{0.5C_X.V_{dd}}{K_n'\left(\frac{W_n}{L_n}\right)(V_{dd}-V_{tn})^2-K_p'\left(\frac{W_{keeper}}{L_{keeper}}\right)(V_{dd}-V_{tkeeper})^2}+\frac{0.5C_{out}.V_{dd}}{K_p'\left(\frac{W_{pmos}}{L_{pmos}}\right)(V_{dd}-V_{tpmos})^2} \quad (4)$$

From the above equation it is observed that threshold voltage of the keeper ($V_{tkeeper}$) and that of the inverter PMOS (V_{tpmos}) have opposing effects on the overall delay. Increase in $V_{tkeeper}$ will result in delay reduction (due to reduction in T_{p1}) whereas increase of V_{tPMOS} will result in increase in overall delay (due to increase in T_{p2}). In other words the delay has negative sensitivity to V_{tPMOS}. The magnitude of the delay sensitivity depends on the sizing of the keeper and the inverter PMOS transistors. Hence, we expect that by accurate sizing of both the keeper and the PMOS (W_{KEEPER} and W_{PMOS}), we can minimize the delay change as a result of V_t increase caused by NBTI and hence improve the performance of dynamic logic circuit. We propose PMOS sizing optimization to reduce the impact of the reliability issues in dynamic logic circuits. We will consider the optimal sizing of the keeper and the inverter PMOS transistors for minimizing the impact of the aging effects.

3. PERFORMANCE METRICS OF DYNAMIC LOGIC CIRCUIT.

Constant field scaling of transistors results in degradation of circuit parameters. If 'S' is the scaling factor 0.7 of each generation (according to Moore's Law). Then Delay is scaled by a factor S, Power by a factor S^2 and switching energy by a factor S^3. Increase in leakage power due to scaling has become a major concern of reliability. There is an urgent need for low power design, leakage reduction and leakage tolerant design. Hence we consider the 3 main parameters of Delay, Power and Noise leakage in order to increase the robustness of a circuit.

3.1 Delay (Loaded and Unloaded)

Total Delay of a circuit is defined as

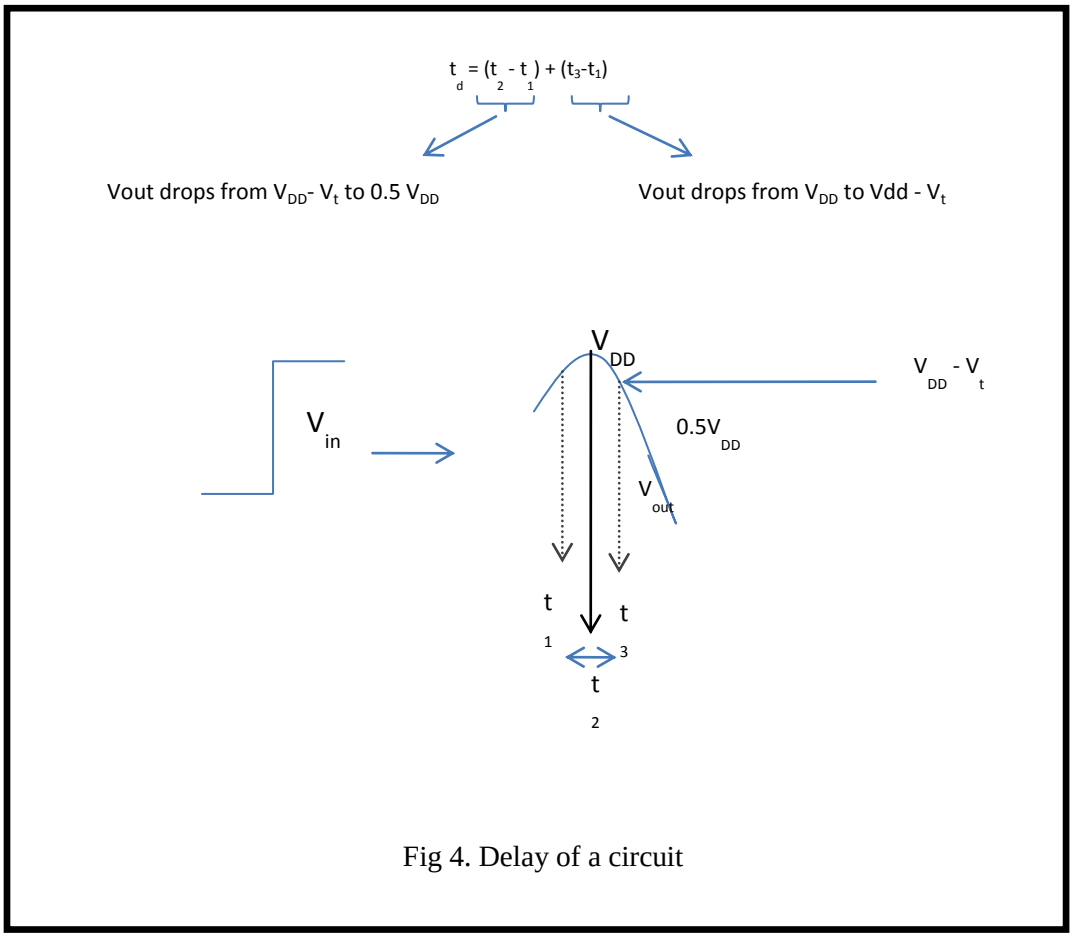

Fig 4. Delay of a circuit

Saturation region from t = t_1 (corresponding to $V_{out} = V_{DD}$) to t = t_2 (corresponding to $V_{out} = (V_{DD} - V_{tn})$). Linear region from t = t_2 (corresponding to $V_{out} = (V_{DD} - V_{tn})$) to t = t_3 [12]

Delay Time is defined as,

$$t_{Dn} = t_3 - t_1 = A_n * \frac{C_l}{\beta_n V_{dd}} \quad (5)$$

Delay α C_L (optimize C_L to increase delay)

$1/\beta_n$ (if W is increased or L is decreased delay decreases)

$1/V_{dd}$ (decrease supply voltage increases delay)

These are the 3 major parameters for optimizing the speed of CMOS [12]. We consider two circuits. The first one is the Dynamic logic Circuit without any load next we add an inverter load at the output and optimize the delay of the circuit. We observe that the delay of the loaded circuit is increased by 25%. We provide design optimizations to both the cases.

3.2 Power Consumption

As the technology is scaled down the threshold voltage decreases, as V_T decreases a few parameters increase which are: I_{OFF} and $I_{D(SAT).}$ As V_T decreases subthreshold leakage increases. Leakage is a hindrance for voltage scaling. Leakage results in power dissipation and robustness of dynamic logic circuits. The two types of power consumption are:

- Dynamic Power consumption: which includes switching power and short circuit power
- Static Power consumption: which includes Leakage

We consider Dynamic Power consumption due to switching as the static power consumption is very minimal and can be ignored. In addition to it dynamic circuits have faster switching speeds also the clock power of dynamic logic can be significant, particularly since the clock node has a guaranteed transition on every single clock cycle. Hence we consider the power consumption due to switching in our circuit.

3.3 Unity Noise Gain:

By scaling down the threshold voltage, V_T needs to be scaled properly to offset the undesired speed loss [5]. Leakage power increases exponentially and there is also deterioration in the noise immunity of the dynamic circuit [9]. In order to design a noise tolerant dynamic circuit, we need to calculate the unity noise gain (UNG) which is defined as the amplitude of the output noise referred to as Von in our circuit

$$UNG = \{V_{NOISE} : V_{in} = V_{NOISE} = V_{ON}\} \quad (5)$$

The input noise stimulus (see Fig. 5) consists of a DC offset V_{DC} (to account for the possible IR drops) and a scalable pulse V_{pulse}, i.e.

$$V_{noise} = V_{DC} + V_{pulse} \quad (6)$$

We calculated the UNG using an input noise pulse that generates an equal output noise pulse. In our experiments, we increased the amplitude of the input noise pulse from 0.1 V to 0.9 V in order to calculate the UNG as shown in Fig 5. We calculated the UNG for standard sizing of PMOS and Keeper Fig 5 gives that the region of UNG lies between 0.5 and 0.6.

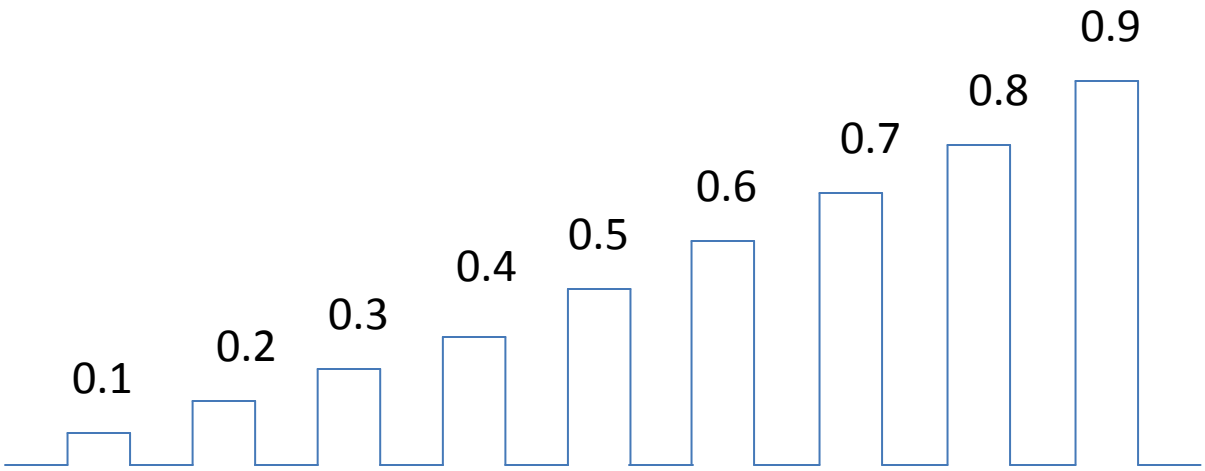

Fig 5. Noise pulse applied to the circuit

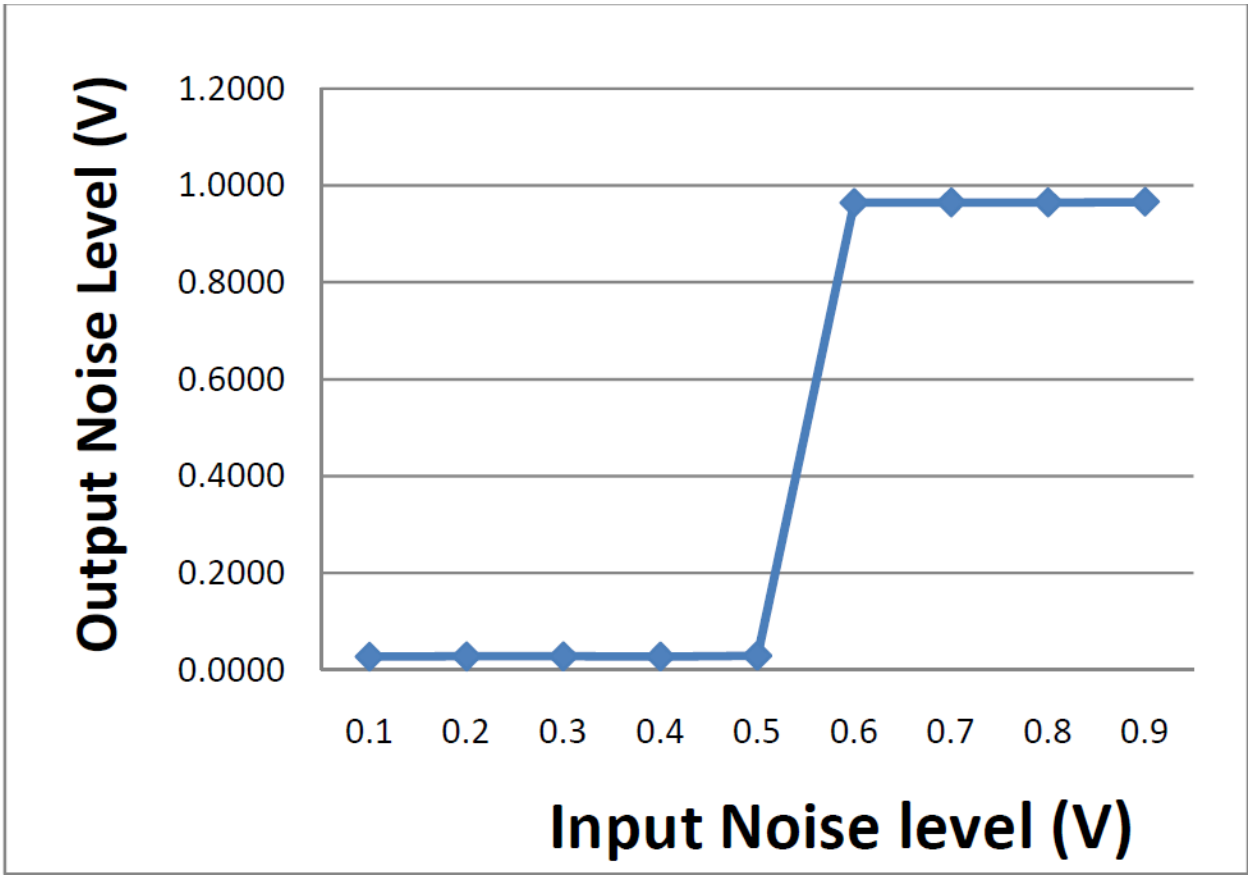

Fig 6. Graph of unity noise gain (UNG)

To calculate the UNG manually it is very cumbersome as it is of the order of mV so it might take around 1000 readings which are not feasible. So we calculate the UNG using linear iterations with a perl code. Then we find the degradation overage and optimize the circuit for the minimum noise leakage overage.

4. MODEL OF NBTI UNDER TEMPERATURE AND PROCESS VARIATIONS

A comprehensive model for NBTI V_t shift is given in [10, 13, 14]. In our research, we simplified models and came up with the following model

$$\Delta V_t = (1+m)K_v t^{0.25} + \delta_v$$
$$K_v = A \cdot t_{ox} \cdot \sqrt{C_{ox}(V_{gs} - V_t)} \cdot \exp\left(E_{ox}/E_o\right) \cdot \exp\left(-E_a/KT\right) \quad (7)$$

Where t_{ox} is the effective oxide thickness, E_{ox} is the electric field across the oxide ($(V_{gs}-V_t)/t_{ox}$). A, E_a, E_0, δ_v , m and K are constants [3, 10], and t is stress time in second.

This model shows the dependence of V_t shift on temperature (T) and process (threshold voltage) variation (V_t).

Fig. 7 shows the percentage of V_t shift in three process corners: low V_t transistors, nominal V_t transistors and high V_t transistors at two temperatures: room temperature (25°C) and worst case (100°C) for SiO_2 dielectrics. These results show that V_t shift is greater at high temperature and the low technology corner. This is due to the dependence of K_v factor in Eq. 1 on the temperature and threshold voltage.

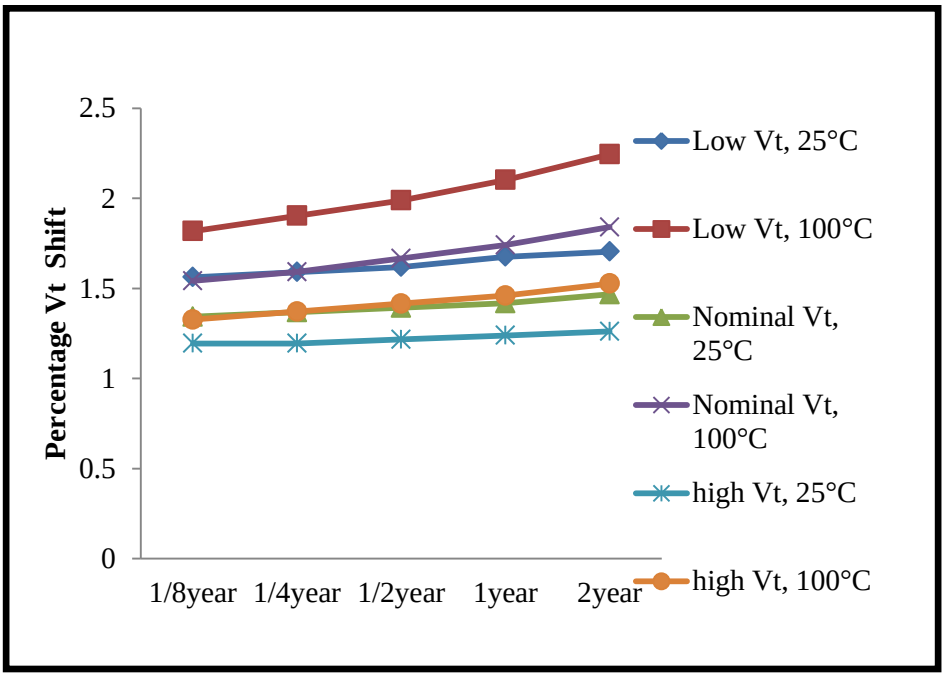

Fig. 7: V_t shift for the three technology corners: low V_t transistors, nominal V_t transistors, high V_t transistors at room temperature (25°C) and worst case temperature (100°C) for SiO_2 dielectrics.

5. IMPACT OF NBTI ON DYNAMIC LOGIC CIRCUITS IMPACT OF NBTI ON DYNAMIC LOGIC CIRCUITS & TRANSISTOR SIZING OPTIMIZATION TO MITIGATE IMPACT NBTI

5.1 Delay:

For robustness measurement, we apply identical pulses to both clock and the input to the PDN in the evaluation phase and then measure the low to high delay of the circuit in 32 nm. Initially the PMOS Keeper and PMOS maintain the standard sizing, W_{PMOS} is 100 nm and $W_{Pkeeper}$ is 40 nm. Random sizing iterations are done to capture the best delay. NBTI is applied to all the PMOS transistors, the worst case is considered after 100,000 clock cycles at a temperature of 100^{o}C. The calculations were done for 2 circuits, one for an unloaded circuit and one for a loaded circuit with an inverter load added. However, for practical purposes it is more feasible to consider a loaded circuit. The best sizing which resulted in the minimum change in delay percentage before applying NBTI and after applying NBTI is as shown.

PMOS Keeper Width in nm	PMOS Width in nm	Delay without NBTI (ps)	Delay with NBTI (ps)	Percentage Delay change
45	80	9.2090	9.3771	1.83%
50	120	9.4425	9.5699	1.35%
50	110	9.4638	9.5848	1.28%

TABLE I. Unloaded Delay Circuit Optimization

PMOS Keeper Width in nm	PMOS Width in nm	Delay without NBTI	Delay with NBTI	Percentage Delay change
50	160	10.68	10.90	2.07%
70	120	12.98	13.21	1.72%
60	140	11.51	11.70	1.71%

TABLE II. Loaded Delay Circuit Optimization:

5.2 Power Consumption:

Power consumption is one of the major reliability metric which needs to be taken into consideration while optimizing a circuit. Given the trend that leakage power increases by a factor of 5X with each technology generation and will become a significant portion of the total power in

future ICs [5]. To analyze the power consumption of a circuit we apply a constant DC voltage of 0.9V to the input and check the power consumption overage. The results were as follows:

PMOS Keeper Width in nm	PMOS Width in nm	Power Consumption with NBTI in pWatt	Power Consumtption without NBTI in pWatt	Percentage change in Power Consumption overage
70	120	374.03	364.80	3%
60	140	378.55	370.63	2%
50	160	361.43	361.68	0%

TABLE III. Power Consumption Optimization

We notice that for the sizing of Keeper 50 nm and PMOS 160 nm results in no change in power consumption even after applying aging. This is the best design optimization if leakage power is the main criteria.

5.3 UNG (Unity Noise Gain)

Noise in applied at the input V_{in} and swept from 0.1V to 0.9V the noise at the output is measured. The typical readings are as such: noise of the output (V_{ON}) is usually of the order of a few mV until 0.5 V then it shoots up to 0.9V and does not change much even if the input noise in increased. The straight line, y=x line, the point where the curve meets the straight line is called as Unity Noise Gain. At that point the input noise and output noise are equal.

PMOS Keeper Width in nm	PMOS Width in nm	UNG without NBTI	UNG with NBTI	Percentage UNG change over age
50	160	0.535	0.534	0%
60	140	0.576	0.577	0%
70	120	0.619	0.619	0%

TABLE IV. UNG Optimization

6. FUTURE WORK

We have performed our experiments in the evaluation phase of the transistors when the input is low and there is dissipation through NMOS transistors. In the evaluation phase the PMOS and Keeper have opposing effects hence we have a method to nullify the effect of NBTI. Similarly in the precharge phase the NMOS and Keeper transistors will have opposing effects on the delay so there is a potential way to optimize the circuit and more scope for research in the precharge phase. There can be an optimized circuit which is not affected by aging in both the evaluation and precharge phases.

7. CONCLUSION

As per our results and data we can come to the conclusion that the effect of NBTI can be nullified by appropriately sizing our transistors. If we consider delay as the main criteria then the best optimized circuit will be $W_{Pkeeper}$ as 60 nm and W_{PMOS} as 140 nm. We can also have the best optimization for UNG and Power consumption according to the criteria.

Also, we notice that the noise immunity of our circuit is not affected by aging there is a difference of 1 mV in the UNG before and after aging. Even this can be avoided with the optimal sizing. This design is the most appropriate for scaled technologies where delay and power are the main trade off for robustness of a circuit.

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