Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

TITLE: ***UPF DESIGN FLOW TUTORIAL***

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ABSTRACT

UPF or the Unified Power Format is an industry wide power format specification to implement low power techniques in a design flow. UPF is designed to reflect the power intent of a design at a relatively high level. UPF scripts help describe which power rails should be routed to individual blocks, when blocks are expected to be a powered up or shut down, how voltage levels should be shifted between two different power domains and type of measures taken for retention registers and memory cells contents if the primary power supply to a domain is removed, hence helping the design to become more efficient. Therefore, with Power becoming an important factor in today's electronic systems it leads to a need to have a more systematic approach to reduce power in complex designs. Keeping this in view, the purpose of this tutorial is to prepare an example driven tutorial on UPF design flow. For better understanding of UPF flow and design for low power circuits, four distinct examples are considered performing different low power techniques on one common design called 'ChipTop'. This tutorial is prepared using Synopsys EDA tools. The synthesis scripts are setup in 'tcl' format that are compatible with the Synopsys synthesis and physical design tools.