Recent Publications

- A. Pushkarna, S. Raghavan, and H. Mahmoodi, "Comparison of Performance Parameters of SRAM Designs in 16nm CMOS and CNTFET Technologies," accepted for IEEE International System-on-Chip Conference, Sep. 2010
- A. Shah and H. Mahmoodi, "Thermal Estimation for Accurate Estimation of Impact of BTI Aging Effects on Nano-Scale SRAM Circuits," accepted for IEEE International System-on-Chip Conference, Sep. 2010
- L. Liu and H. Mahmoodi, "Evaluation of Power Gating under Transistor Aging Effect Issues in 22nm CMOS Technology," International Conference on Mixed Design of Integrated Circuits and Systems, pp. 477-481, June 2010
- H. Singh and H. Mahmoodi, "Analysis of SRAM Reliability under Combined Effect of NBTI, Process and Temperature Variations in Nano-Scale CMOS," International Conference on Future Information Technology (FutureTech), pp. 1-4, May 2010
- A. Pushkarna and H. Mahmoodi, "Reliability Analysis of Power Gated SRAM under Combined Effects of NBTI and PBTI in Nano-Scale CMOS,"; Great Lake Symposium on VLSI, May 2010
- S. K. Krishnappa, H. Singh, and H. Mahmoodi, "Incorporating Effects of Process, Voltage, and Temperature Variation in BTI Model for Circuit Design," IEEE Latin American Symposium on Circuits and Systems, pp. 236-239, Feb. 2010
- F. Moradi, D. Wisland, H. Mahmoodi, Y. Berg, and T. V. Cao, "New SRAM Design Using Body Bias Technique for Ultra Low Power Applications," IEEE International Symposium on Quality Electronic Design, pp. 468-471, Mar. 2010
- M. Cho, J. Schlessman, H. Mahmoodi, M. Wolf, and S. Mukhopadhyay, “Post-Silicon Adaptation for Low-Power SRM under Process Variation,” accepted for IEEE Design and Test of Computers
- S. Paul, H. Mahmoodi, and S. Bhunia, “Low-Overhead Fmax Calibration at Multiple Operating Points Using Delay Sensitive Based Path Selection,” ACM Transactions on Design Automation of Electronic Systems, vol. 15, no. 2, pp. , Feb. 2010

People

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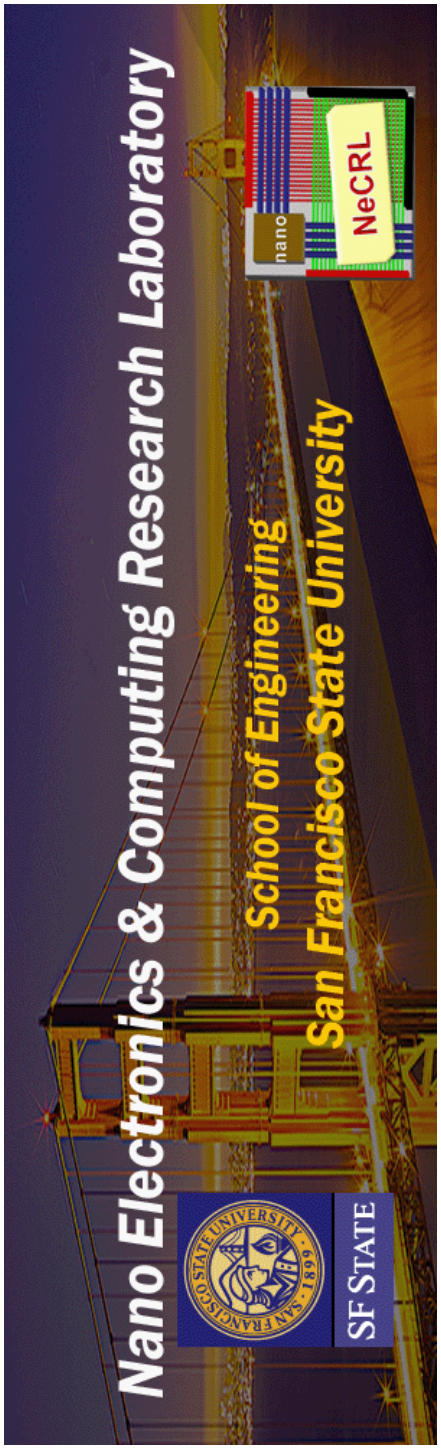
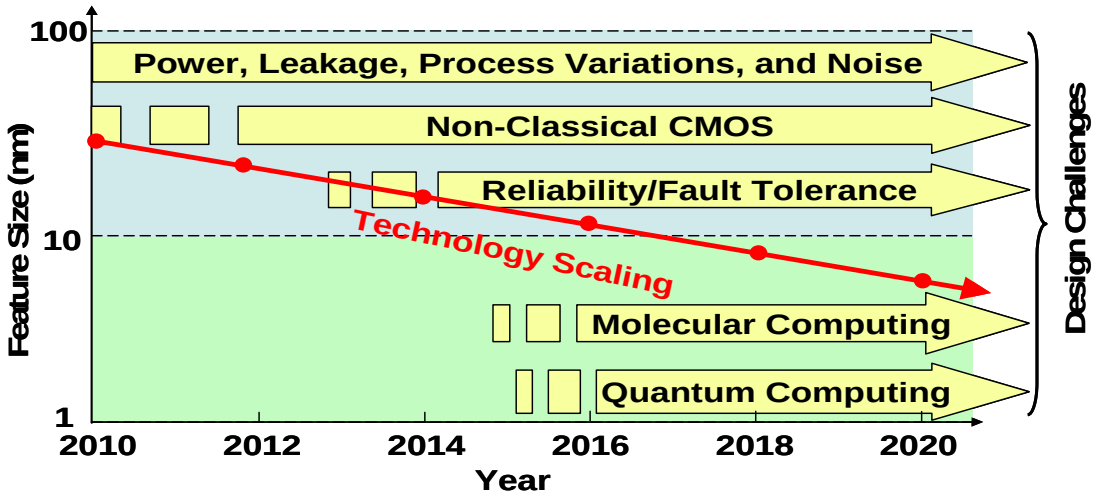


Research Mission

Designing reliable, energy efficient, high performance computing circuits in emerging nanotechnologies is our mission at NeCRL. As the technology continues to scale down towards nanometer regimes, there are grand challenges and barriers. Our research addresses the technology scaling challenges at the circuit and architecture levels of abstraction.



Research Projects

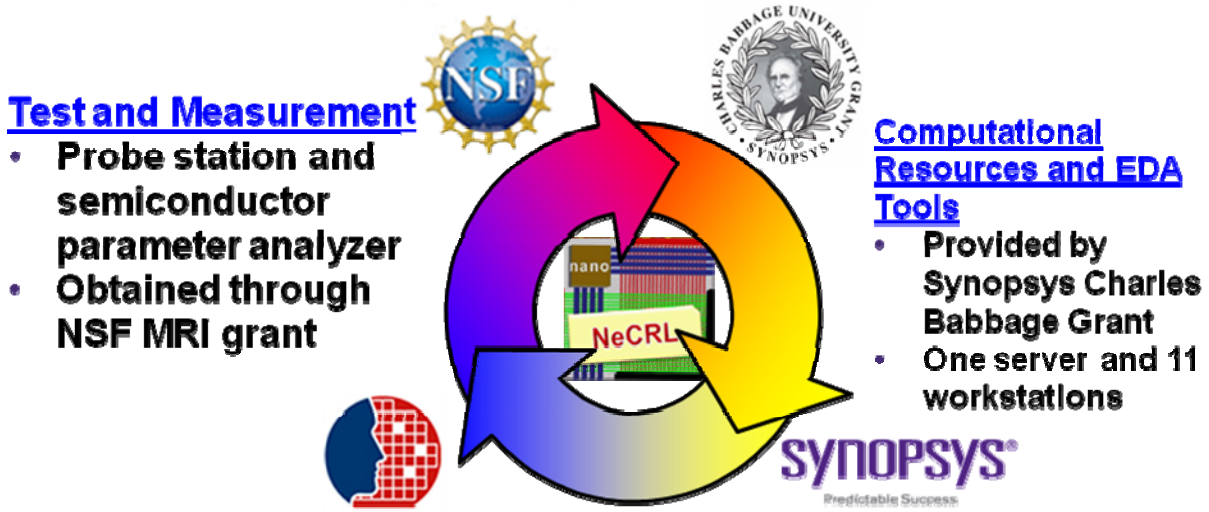
- Reliable computing circuits and architectures for Nano-scale CMOS
- Brain modeling and hardware implementation
- Energy recovery and harvesting

Educational Activities

Courses:
ENGR 856 — Nano-Scale Circuits & Systems
ENGR 852 — Advanced Digital Design
ENGR 848 — Digital VLSI Design
ENGR 453 — Digital IC Design

Tutorials:
ASIC Design Flow Tutorial
Full Custom Design Using Custom Designer
Low Power Flow (under development)

Infrastructure



Test and Measurement
- Probe station and semiconductor parameter analyzer
- Obtained through NSF MRI grant

Computational Resources and EDA Tools
- Provided by Synopsys Charles Babbage Grant
- One server and 11 workstations

Process Design Kit and Access to Fab
- Synopsys generic 90nm for teaching purpose
- Predictive technology models
- IBM 65nm offered via MOSIS Inc. for fab