VLSI Synopsys Tool Manual

CMOS Inverter Layout Using Cosmos LE

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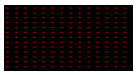
Fall 2008

CMOS Inverter Layout

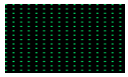
This tutorial is intended to illustrate the steps involved in the creation of an **inverter layout in 90nm technology** using Synopsys Cosmos LE and to do an Net list extraction using Star RXCT.

To Draw a layout, its strongly recommended that you make yourself familiar with the Lambda Rules. This will help in reducing the layout design cycle time and debugging the errors identified by the Design Rules Check (DRC).

Step 1) Drawing the PMOS area

Draw a PIMP  (P Implant) as a big square and Cover it with

N-Well  and Towards the right of the P Implant, Draw a small rectangle

for NIMP (N Implant) 

The combination of all the 3 layers looks like below.

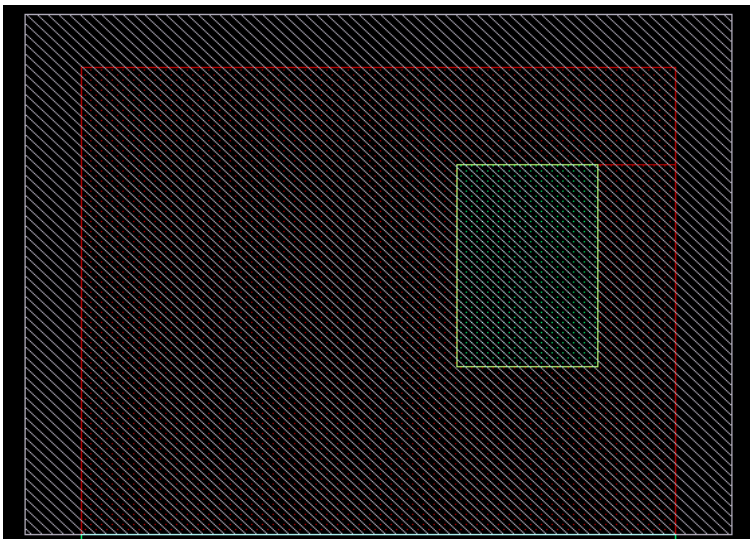


Fig 2.1

Step 2) Drawing NMOS Area

For the NMOS, Drawing the P-IMP and Implanting N-IMP is a little tricky thing to do.

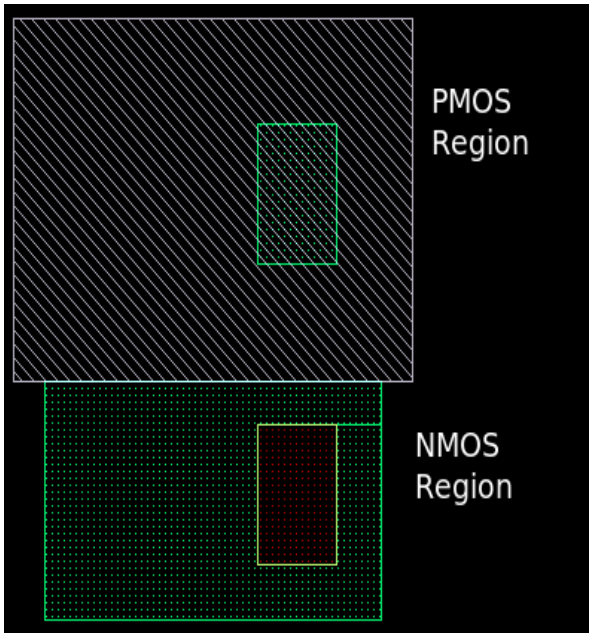


Fig 2.2

First draw a rectangle for P-IMP and draw several rectangles of N-IMP around to cover the P-IMP and right click and merge the N-IMP to form one consistent N-IMP

Step 3) Adding Metal Layers for PMOS

Draw a vertical bar of Metal-1 and extend two branches horizontally one into the P Implant and other into N Implant

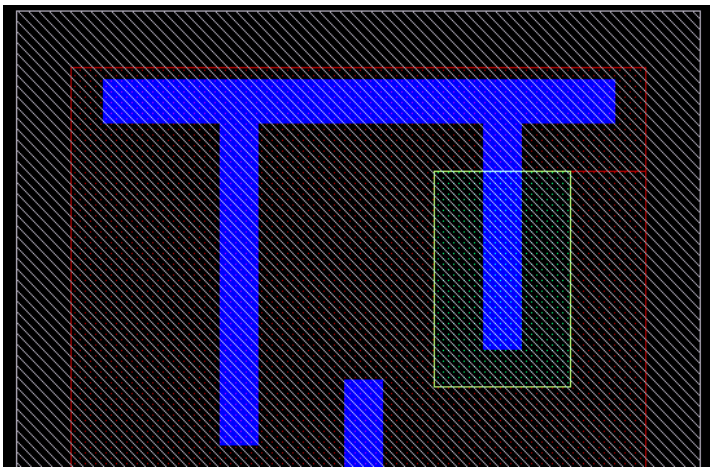


Fig 2.3(a)

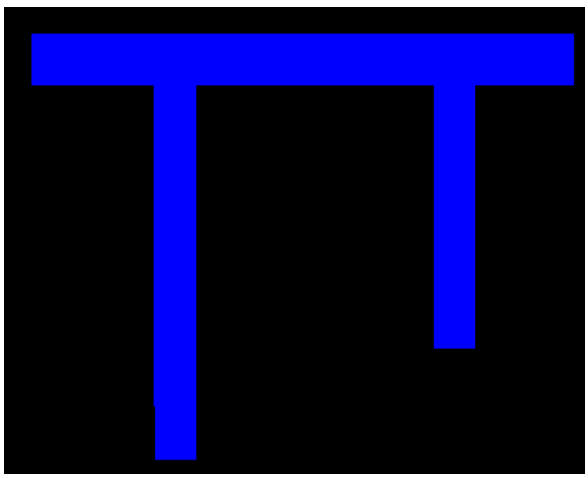


Fig 2.3(b)

Step 4) Adding Metal Layers for NMOS

Draw a vertical bar of Metal-1 and extend two branches horizontally one into the P Implant and other into N Implant

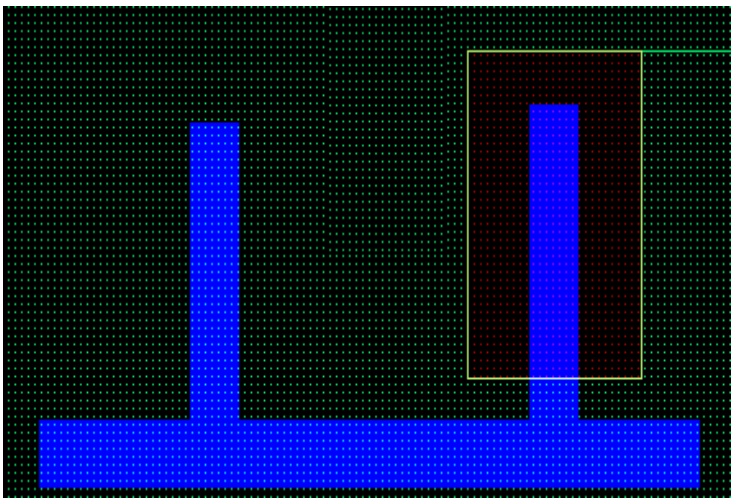


Fig 2.4(a)

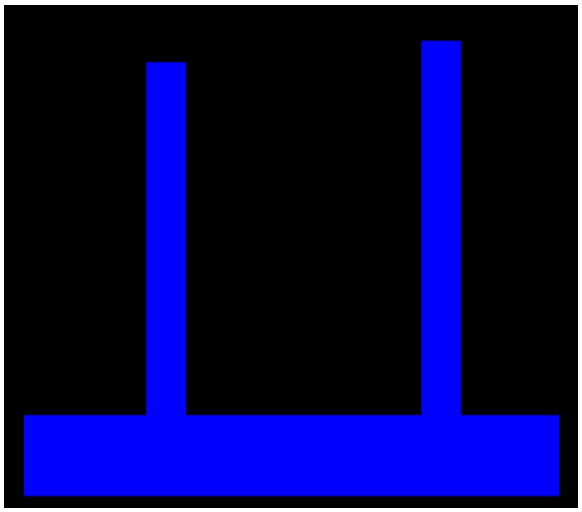
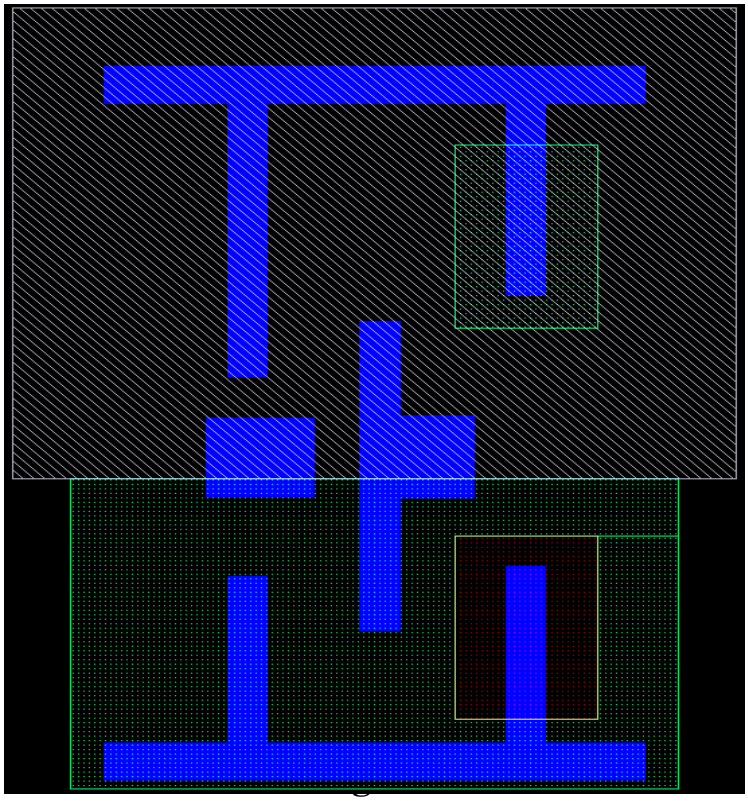


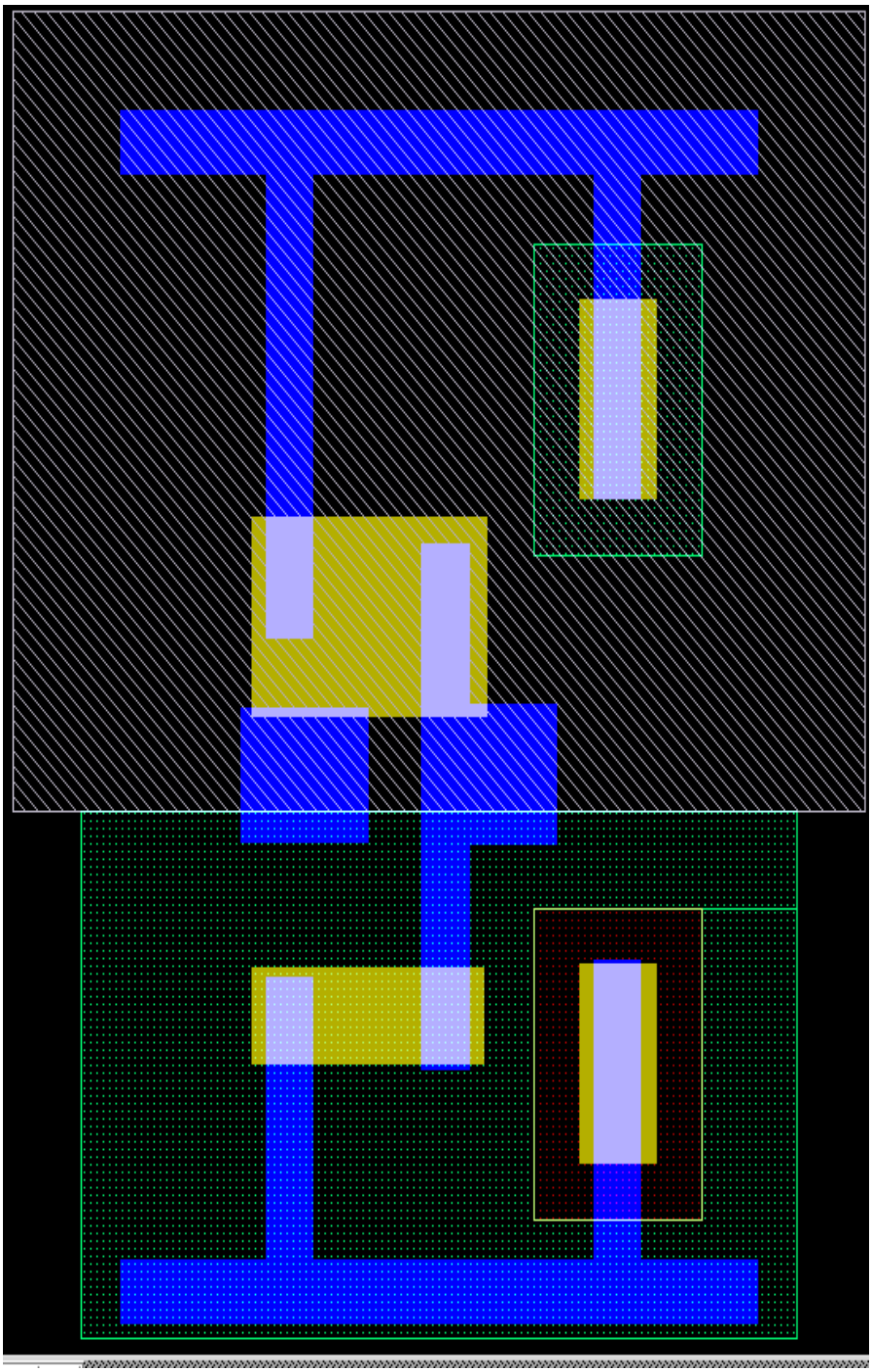
Fig 2.4(b)

After adding Metal -1 to the PMOS and NMOS regions the layout should look like this. The central metal regions should be drawn to add input and output pins.



Step 5) Adding Diffusion layers

Diffusion layers are added to cover metal arms and the input and output contact areas as shown below.



Step 6) Adding Poly Silicon for Channel Formation

A single strip of Poly Silicon  is drawn which extends from N-Well down into the N-IMP. And while its passing through the Diffusion layer, it creates the channels.

Note: Please be sure to check the dimensions of Poly as this will determine the channel width and length. For this tutorial, the Channel widths are as follows.

	Width	Length
PMOS	500 nm	100 nm
NMOS	250 nm	100 nm

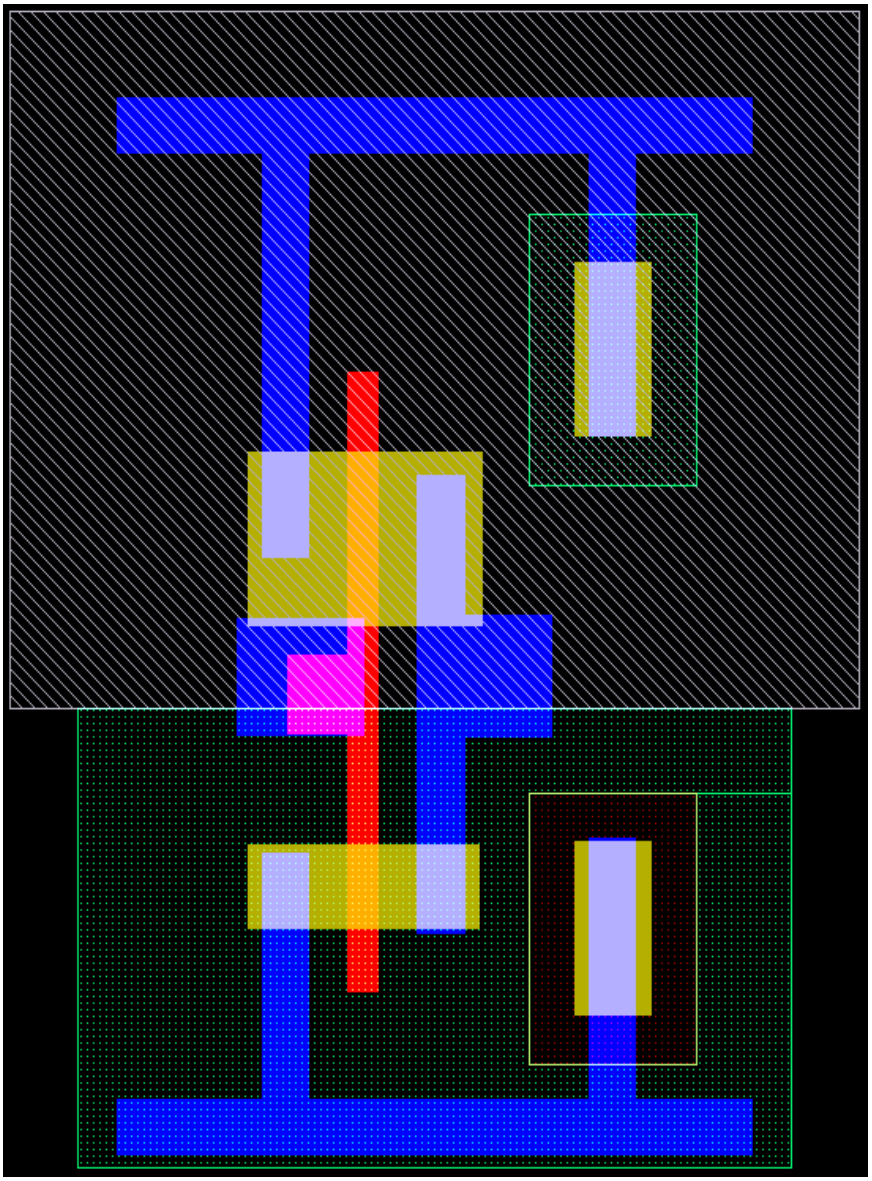


Fig 2.7

Step 7) Adding Contacts 

For a simple CMOS Inverter, 9 contacts are used. The placement of contacts depends on the usage. Following list gives a better understanding.

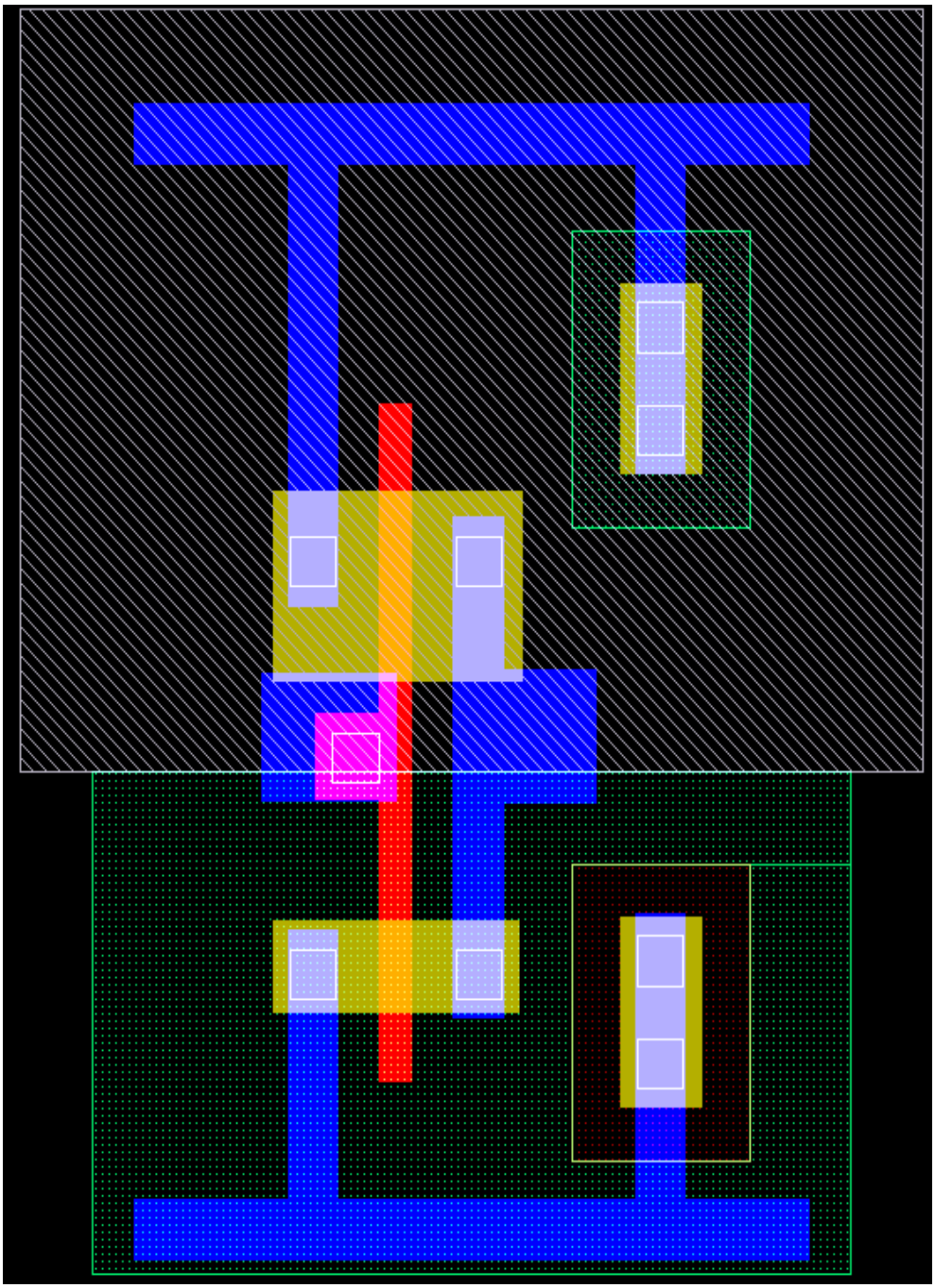


Fig 2.8

Step 8) Adding Pins and Final Layout Review
Add VDD Pin in the Metal-1 in the N-Well.
Add Vin Pin on the metal connecting the Poly.
Add Vout Pin on the metal strip on the
Add VSS Pin on the metal connecting GND to Source of NMOS.

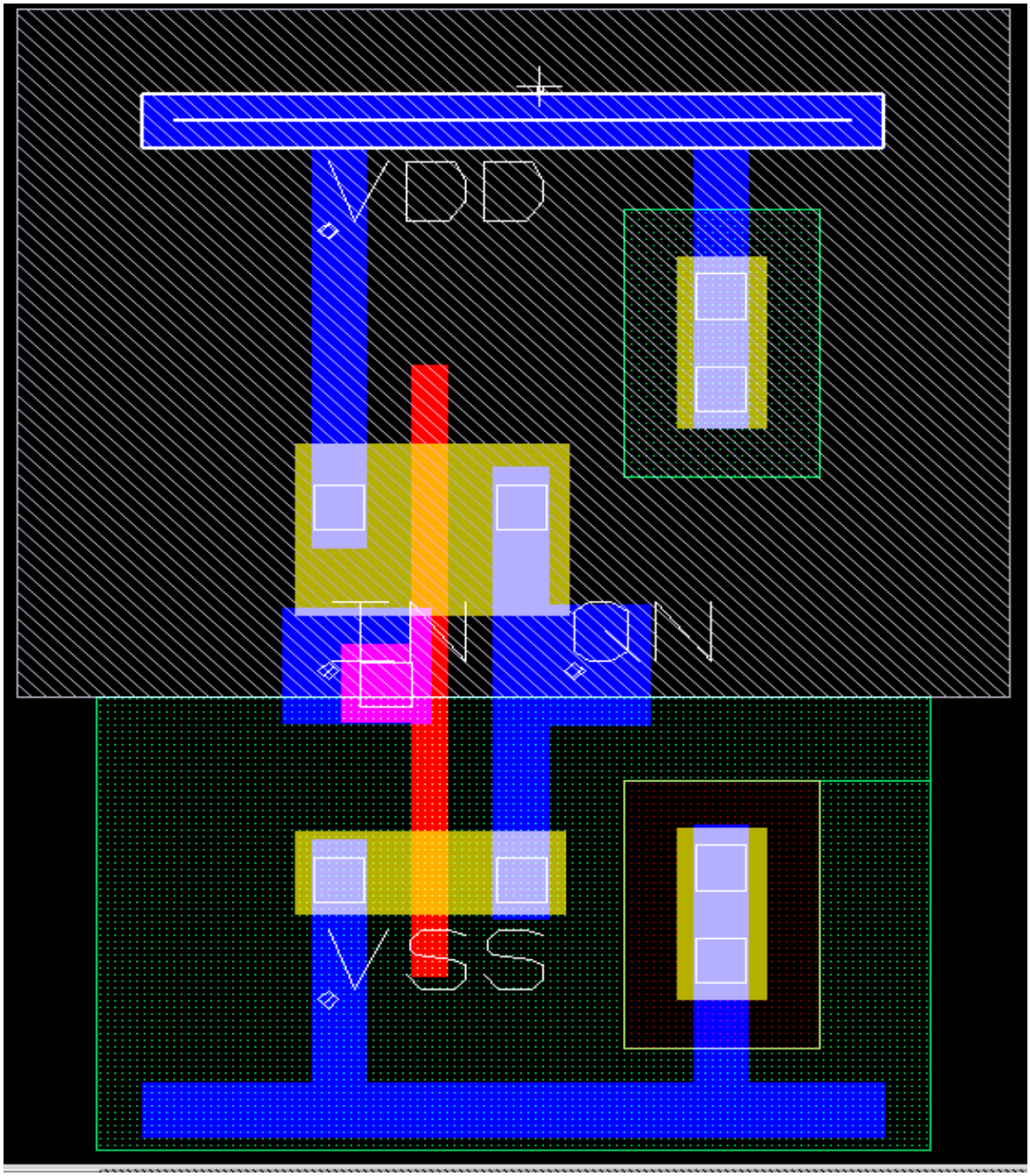


Fig 2.9

The above layout is the final Inverter Layout.

Step 9) Executing Hercules for Design Rule Check (DRC)

After the inverter layout has been drawn to the dimensions same as that in the schematic, to verify that the layout meets all the basic design rules, we need to run a DRC(Design Rule Check) step. Save the Layout cell by clicking on **Cell > Save**. In Synopsys package, **Hercules** is the tool which gives us the option to perform DRC.

Steps to run the DRC

Click on **Verification > User DRC Runset >**

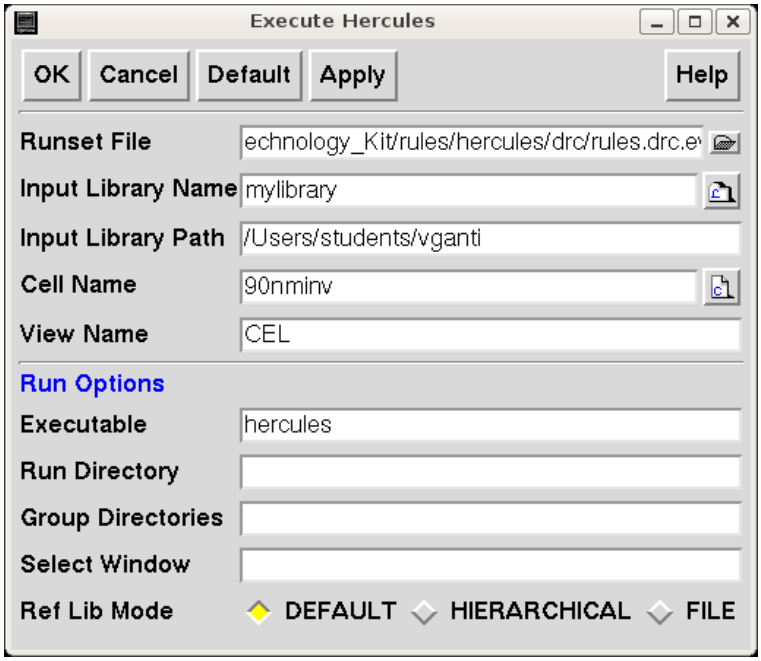


Fig 2.10

Locate the runset file from the following directory and click Open.

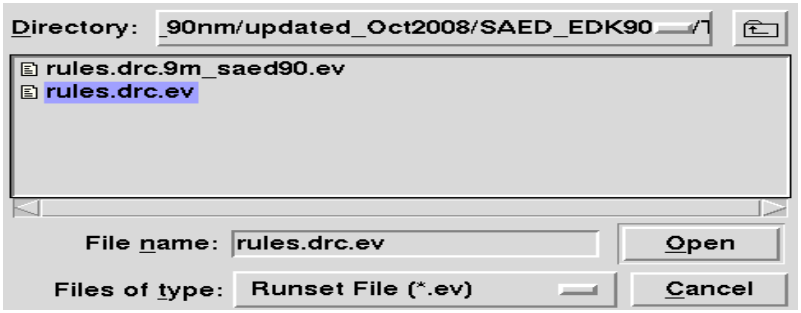


Fig 2.11

packages/process_kit/generic/generic_90nm/updated_Oct2008/SAED_EDK90nm/Technology_Kit/rules/hercules/drc/rules.drc.ev

To run and check all the design rules, Hercules usually takes between 45 seconds to 2 minutes depending on you computer hardware configuration. The output of DRC is created in the Home Directory of your user account. Search for the file having the name as **90nminv.LAYOUT_ERRORS.**

When the layout is free from all the errors and meets all the design rules, the output file 90nminv.LAYOUT_ERRORS would have CLEAN as shown below. If there are some errors in the layout, its displayed as ERROR and the error details are specified in this file. So its a very important step to check the output of DRC. Once the DRC is passed you can proceed to Layout Vs Schematic (LVS) and Net List extraction.

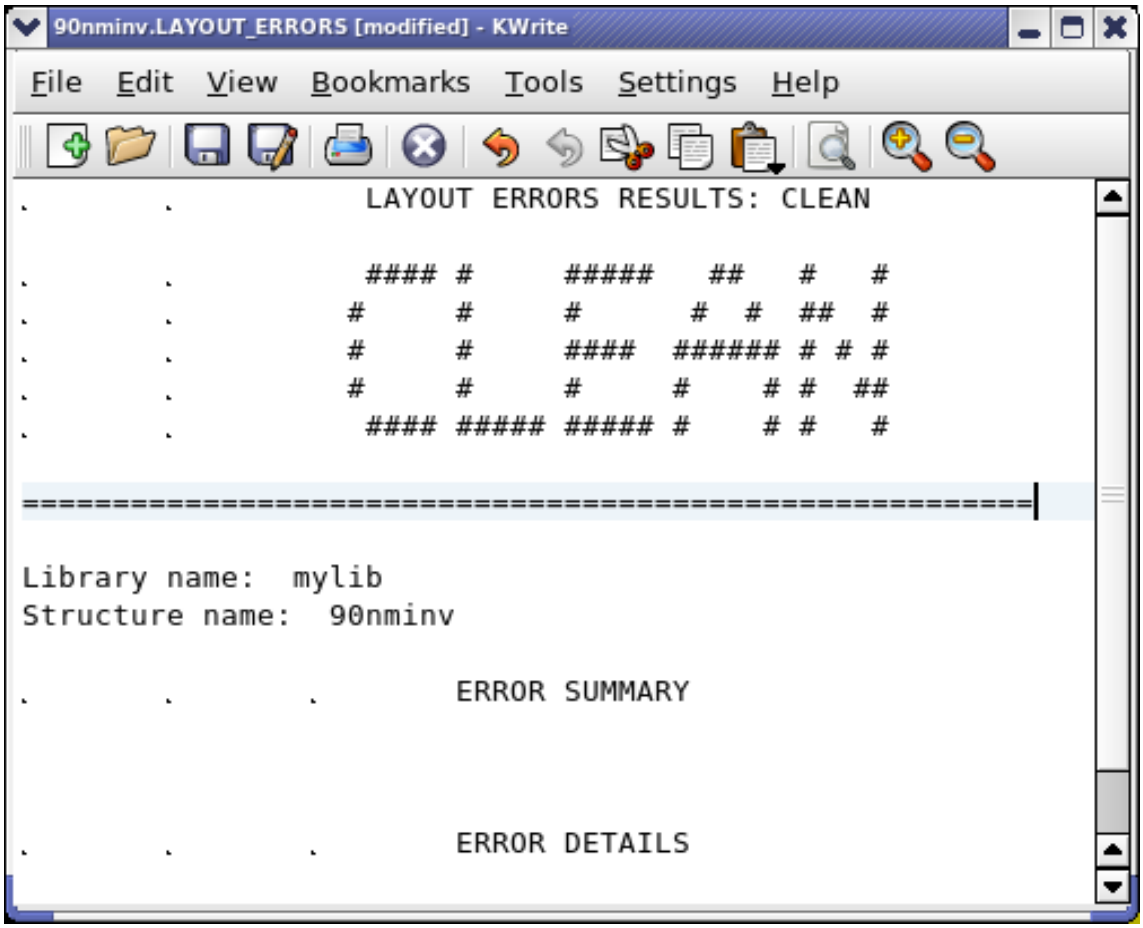


Fig 2.12

Once the DRC is passed, Proceed to LVS and Net List extraction.