Embedded Electrical and Computer Engineering

MASTER ORAL DEFENSE

TITLE: *Datapath Architecture for Reliable Computing in Nanoscale Technology*

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TIME & DATE: **2:00PM, November 4th, 2011** **LOCATION:** **SCI 110**

COMMITTEE CHAIR: **Dr. Hamid Mahmoodi**
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ABSTRACT

Today the process technology is scaling really fast which has given rise to new challenges in Nano electronics. The existing reliability enhancement techniques based on redundancy are very costly in terms of power and area without improving the system performance. There are various architecture models proposed to overcome transient and ungraceful degradation, but they are not efficient enough to provide high performance and low power usage. We propose to overcome this problem by using efficient reliability enhancement framework and using a reliable computing datapath, which is capable of reconfiguring the computing path. Circuit techniques like the transient fault correction, self-test and configuration are also being utilized in proposed architecture. The degradation of the circuit is graceful with minimum errors, better accuracy and with minimum to no latency in transmission of data.