COMPARATIVE ANALYSIS OF SRAM CELL DESIGNS IN NANO-SCALE TECHNOLOGY

A dissertation submitted to the faculty of
San Francisco State University
In partial fulfillment of
The Requirements for
The Degree

Master of Science
In
Engineering: Embedded Electrical and Computer Systems

by

Shreyas Kumar Krishnappa

San Francisco, California

August, 2010

CERTIFICATION OF APPROVAL

I certify that I have read *Comparative Analysis of SRAM Cell Designs in Nano-Scale Technology* by Shreyas Kumar Krishnappa, and that in my opinion this work meets the criteria for approving a thesis submitted in partial fulfillment of the requirements for the degree: Master of Science in Engineering: Embedded Electrical and Computer Systems at San Francisco State University.

_____

Hamid Mahmoodi
Assistant Professor, Electrical and Computer Engineering

_____

Hao Jiang
Assistant Professor, Electrical and Computer Engineering

COMPARATIVE ANALYSIS OF SRAM CELL DESIGNS IN NANO-SCALE TECHNOLOGY

Shreyas Kumar Krishnappa
San Francisco, California
2010

Abstract

Bias Temperature Instability (BTI) is a major reliability issue in Nano-Scale CMOS circuits. BTI effect results in the threshold voltage increase of MOS devices over time. Given the Process, Voltage, and Temperature (PVT) dependence of BTI effect, and the significant amount of PVT variations in Nano-scale CMOS, we propose a method of combining the effects of PVT variations and the BTI effect for circuit analysis. We investigate the PVT dependence of BTI effect on SRAM designs. 6T, 8T and 10T SRAM designs are simulated to observe the impact of aging effects in 32nm CMOS process. By decreasing supply voltage, stand-by Static Noise Margin (SNM) of 8T and 10T cells is scaled down to match that of 6T cell. Simulation results at 100^{o}C of 10T SRAM cell show small SNM degradation of only 2.6% over 10 years of lifetime. 10T cell leakage power reduced by 94% and write margin decreased to 0.1V in 10T, 8T cell compared to 6T cell. Access time increased by 73% in 10T cell and 42% in 8T cell. It is appropriate to choose memory cell based on application with memory parameters and aging effects into consideration. The results show that the SNM of 8T and 10T cells are less affected by aging effects due to their ability to operate at lower supply voltage.

I certify that the Abstract is a correct representation of the content of this dissertation.

_____ _____

Chair, Dissertation Committee Date

ACKNOWLEDGEMENT

First of all, I would like to thank my advisor Prof. Hamid Mahmoodi for providing such a stimulating and enriching environment in which I was able to work for the past two years. I am very grateful to Y. K. Cao for his aging model and his suggestions about my intended analysis of aging effect. I feel privileged to have been able to work with Prof. Hao Jiang, Larry Klingenberg, Lou Ann Bassan. I received guidance from all of them. Hao always had ideas regarding analog radio-frequency projects, Larry introduced me to low power microcontroller designing, and Lou Ann advice at my difficult times. I would also like to acknowledge all of my classmates from the group.

I have been blessed with the opportunity to be a “graduate assistant” at Dept. of Graduate Studies, working with wonderful team. I would like to remember Eddie Ng for supporting me throughout. I thank Dean Dr. Ann Hallum and Mary Menees, the graduate studies senior operations officer, for helping me to finish my thesis work. Mary was my “mother” during my days in graduate studies and will be always remembered for providing support and helping me to fulfill my dream. Finally, I would like to thank my mother (Susheela), my father (Krishnappa), my sister (Swetha), my grandparents (Narayanappa, Lakshmi Narasamma), my uncle (Venkata ramana swamy), my aunt (Vijya, Shobha), and family for their love, support that they have given me throughout the past 27 years of my life. My love and gratitude to all of you.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. INTRODUCTION

With recent introduction of High- *k* material to avoid gate tunneling effect, it has become essential to recognize the required degree of reliability in 32 nm technology and beyond with shrinking technology parameters. Circuit lifetime is varied due to threshold voltage (V_{th}) shift caused by Bias temperature instability (BTI) [1] with interface charge trap generated during device "ON" state. Over time these trapped charges will increase the MOSFET turn-in voltage (threshold voltage). This phenomenon is called aging effect or BTI effect. BTI effect is studied in-depth by [2], [3], [4] and models are provided to predict the life time of MOSFET dependent on process, electric field, time and temperature. In [5], authors provide an overview on aging effect, issues related to each model presented in [2-4]. BTI is classified into positive BTI in n-channel and negative BTI in p-channel devices. NBTI is modeled by considering hydrogen (H^+) as diffusing elements in interfacial layer based on a reaction-diffusion model [2], [3]. Observations made in [2], [3], and [5] provide details of PBTI in high- *k* dielectric. In Nano-Scale technology scaling of channel length have increased reliability concern and other related parameters. For example, fabrication (random dopant fluctuation) issues, CMOS (latch-up, increase in resistance, fan-in/fan-out ratio, BTI effect) issues. It is crucial to analyze the effect of BTI on CMOS circuit performance. For this purpose we choose five stage ring-oscillator (RO) and various SRAM designs to observe V_{th} variation due to BTI effect. In particular, various SRAM designs are analyzed. These designs are conventional six transistors (6T) SRAM cell [6], eight transistor (8T) SRAM cell [7], and ten transistor (10T) SRAM cell [8]. BTI affects the stability of SRAM in terms of Static noise margin (SNM), Write-Margin (WM), Read-Margin (RM), and increased leakage power. Thus, alternative SRAM circuit designs are favored to replace 6T SRAM in 32nm

node [9]. Thus we analyzed 8T [7] and 10T [8] SRAM cells to show that their cell stability is better than the conventional 6T SRAM cell by applying aging effects. The cell stability is better by isolation of Read-word line and Write-word line. For the first time V_{th} shift is applied to 10T SRAM and compared with 8T and 6T SRAM to predict SRAM circuit performance in Nano-scale CMOS technology.

Negative bias temperature instability (NBTI) is deeply studied for Silicon-dioxide (SiO_2) dielectric but for Hafnium (Hf) oxide positive bias temperature instability (PBTI) is reported to be also major bottleneck in deep sub-micron technologies [10]. In this thesis we studied the combined effect of NBTI and PBTI effect in Hafnium-di-oxide (Hfo_2) dielectric devices. Incorporating additional transistors to 6T SRAM comes with a penalty of increased chip area. Recently, [11] reported 6T SRAM can be used until 15nm node by upsizing the transistors for suitable SRAM operation for supply voltage (V_{DD}) of 1.1V to 1.2V. To achieve "More than Moore", scaling of supply voltage with channel length is obvious and necessarily alternative circuit design are predicted in future technologies [1], [12]. Our simulation results are performed in 32nm by using [4], [13] high performance model to observe the stability of SRAM reliability variations for lower supply voltage. Hence 8T, 10T SRAM are optimized to operate at $0.41786V$ ($\approx 0.41V$) and compared with 6T SRAM operating at $0.9V$ because stand-by Static Noise Margin (SNM) is equal in all the three SRAM designs for above mentioned supply voltages (0.9V & 0.41786V) without applying BTI effects. Later, by applying BTI effects on all three SRAM circuit designs, we set up the most reliable of all three designs in 32nm and beyond.

For video processing applications SRAM cell with additional transistors are grounding attention because storing data in SRAM cell is performed once but access to stored data is performed multiple times [14]. In access operation, read SNM is lower than required read SNM then intended operation does not occur and system failures are likely to occur. To report inter-die V_{th} variations, V_{th} = 0.2V die is considered. At 100°C 10T SRAM parameters are decreased by 0.21% write margin (WM), 0.58% in read margin (RM) and 1.38% in leakage power over 10 years of lifetime. Similarly, for 8T SRAM at 100°C percentage decreased by 0.20% in WM, 1.03% in RM and 1.06% in leakage power. The 8T, 10T SRAM cell have minimum aging effect compared to 6T SRAM at similar conditions.

In our previous paper, the effects of process, voltage and temperature on BTI effects for circuit analysis was reported by our group [15]. This thesis paper presents the comprehensive discussion of SRAM circuit designs over lifetime variations. With threshold voltage shift or increase of turn-in voltage of individual transistor impact the circuit reliability is predicted using [4], [13] model with high performance device parameters aimed at combined effect of NBTI and PBTI applied in Chapter II, followed by observation of Ring Oscillator and SRAM circuit designs (6T, 8T, 10T) most suitable in modifying a generalized performance in deep 32nm node by power (supply voltage) scaling technique to impact the effectiveness of comparison made by stand-by SNM results in Chapter III, Chapter IV respectively. The discussion then turns to SRAM designs and rigorous comparison of simulation results after a brief qualitative description of Write, Read margin and Leakage power in Chapter V. Summary of discussions with crucial practical

implementation of 8T or 10T SRAM design issues to be overcome for large scale commercialization in Chapter VI.

2. BTI MODEL INCORPORATING IN-CORPORATING EFFECTS OF TEMPERATURE VOLTAGE AND PROCESS DEPENDENCE

In this section, shift in threshold voltage (V_{th}) with NBTI and PBTI is predicted from PTM [4], [13] in 32nm technology for High- k with metal gate. Conventional threshold voltage shift is controlled effectively by oxide and silicon interface, Eq. (1) presents the mathematical form; Where, Q_{ss} is the oxide charge per unit area at oxide-Silicon interface, C_{ox} is gate oxide capacitance, q is the charge, D_I is the final dose after all diffusion steps is followed in fabrication process of Silicon wafer. It is evident from Eq. (1): Minimizing threshold voltage shift can be obtained by introducing controlled amount of Q_{ss} during fabrication. Fig.1 presents the charges found at semiconductor and insulator (High- k) interfaces. Q_f is fixed oxide charge and Q_{it} is interface trap charge. Combination of high temperature annealing at 900°C to 1000°C to minimize Q_f and low temperature annealing at 400°C to 500°C with 10% H_2 in N_2 to minimize Q_{it}. Every transistor (on wafer) undergoes sintering process step, irrespective of NMOS or PMOS. Thus Hydrogen (H) is the main component that satisfies the Silicon (Si) dangling bonds initially. During stress hydrogen is replaced by majority charge from MOS channel due to weakening of hydrogen-silicon bond at interface and Hydrogen is released from Silicon bond. The replacement with majority charge carries will shift (increase) the device turn-in voltage, coined as BTI effect (aging effect). To predicate the behavior of BTI effect in advanced MOS device, modified model of [15] is used for both NBTI and PBTI.

$$\Delta V_{th} = \frac{Q_{ss}}{C_{ox}} = \frac{q \times D_I}{C_{ox}} \quad (1)$$

$$Where, \quad C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}};$$

From [15] the model is applicable to both stresses; active and dynamic. In [13] Eq. 2(a) is simplified AC model to both stress time, t = (t_1, t_2) and recovery time, t = (t_2, t_3) mode of operation. Fig. 2 illustrates the stress and recovery of a transistor input signal dependent on duty cycle (β). In our research BTI induced V_{th} degradation in continuous DC stress is calculated from modified form of Eq. (3) shown in Eq. (4). Where, K_v is the rate at which H^+ species are generated, β is percentage of time for device is under stress, AC stress β<1, DC stress $\beta = 1$, and t is the total time. T_{ox} is the effective oxide thickness (*EOT*) which is smaller than the physical thickness of the dielectric in the case of high- k [17], K is relative permittivity of the high- k material, t_{hk} is the thickness of high- k. C_{ox} is oxide capacitance per unit area, V_{gs} is gate voltage, V_{th} is threshold voltage (0.2V), E_{ox} electric field in the oxide, V_{ds} is drain to source voltage, E_a is activation energy, k and T are Boltzmann constant and temperature in Kelvin, respectively. Other parameters such as δ_v, A, E_o, η, α are 5mV, 1.8mV/nm/$C^{0.5}$, 2MV/cm, 0.35, 1.3 respectively obtained from [4]. We considered continuous DC stress because discontinuous DC stress will be similar to AC stress as shown in Fig. 2, β = 1 and [18] mentions the same for transistor with stress and recovery mode with-in discontinuous DC stress.

First Phase, Stress time, t = (t_1, t_2)

$$\Delta V_{th} = \sqrt{K_v{}^2 \cdot (t - t_o)^{0.5} + \Delta V_{th1}{}^2 + \delta_v} \qquad (2a)$$

Second Phase, Recovery time, t = (t_2, t_3)

$$\Delta V_{th} = (\Delta V_{th} - \delta_v) \cdot \left[1 - \sqrt{\eta (t - t_o)/t}\right] \qquad (2a)$$

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot t^{0.25} \cdot \left[\frac{1 - \left(1 - \sqrt{\eta (1-\beta)/n}\right)^{2n}}{1 - \left(1 - \sqrt{\eta (1-\beta)/n}\right)^{2}}\right]^{0.5} + \delta_v \qquad (3)$$

$$\Delta V_{th} = K_v \cdot \beta^{0.25} \cdot t^{0.25} + \delta_v \qquad (4)$$

Where,

$$K_v = A \cdot T_{ox} \cdot \sqrt{C_{ox}(V_{gs} - V_{th})} \cdot \exp\left(\frac{E_{ox}}{E_o}\right) \cdot \left[1 - \frac{V_{ds}}{\alpha (V_{gs} - V_{th})}\right] \cdot \exp\left(-\frac{E_a}{kT}\right)$$

$$E_{ox} = \left(V_{gs} - V_{th}\right) / T_{ox}; \quad T_{ox} = EOT = (3.9/K) \cdot t_{hk}$$

V_{th} shift over time is calculated from Eq. 4 implemented in MATLAB with user defined input parameters to estimate the threshold voltage shift. The parameters are: (i) Effective oxide thickness (EOT) for PMOS = 1.2nm, NMOS = 1.15nm. (ii) Gate stress voltage (V_{gs}), (iii) Threshold voltage (V_{th}), (iv) Drain to source biasing voltage (V_{ds}), (v) Percentage stress time (β), (vi) Temperature (T), (vii) Time (t) in seconds. According to the model, the value of ΔV_t should be higher at low V_{th} corner, and with high temperature and high voltage conditions. This is verified by results in Fig. 3 which shows percentage of NBTI induced V_{th} shift over time for a low V_t PMOS at two temperature (25°C and 100°C) and two stress voltages (0.5V and 1V). For example, Fig. 4 is percentage change due to PBTI and NBTI induced V_{th} shift over time for V_{th} = 0.2V NMOS and PMOS respectively with two stress voltages 0.9V and 0.41786V at 100°C. We choose exact 0.41786V because as discussed in Section III, 8T and 10T SRAM cell stand-by SNM at 0.41786V is same as that of 6T SRAM cell at 0.9V. This evidences, Eq. (4) is applicable to different voltage, temperature, time to observe aging effects. At lower supply voltage the impact of NBTI and PBTI is similar, but at higher supply voltage NBTI impact is smaller compared to PBTI effect. Similarly, SRAM cell stability is obtained based on state and biasing voltage which is adjusted to predict the BTI effect on SRAM transistors for same SNM over required life-time.

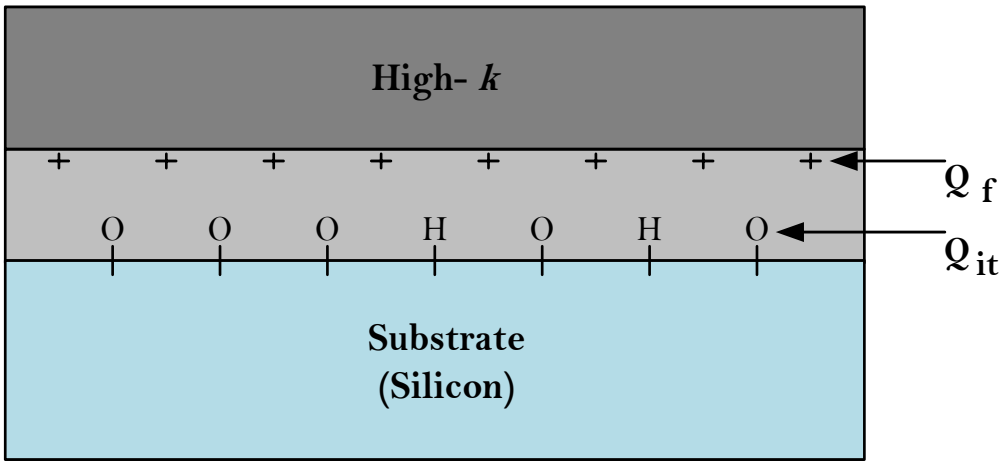

Figure 1: Charges associated with High- *k*/Si interface. Hydrogen (H) ions are created during stress from Silicon dangling bonds.

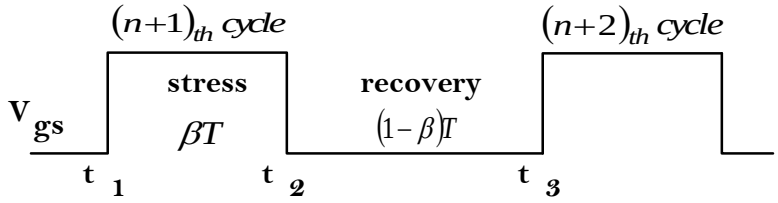

Figure 2: Typical input signal to a transistor.

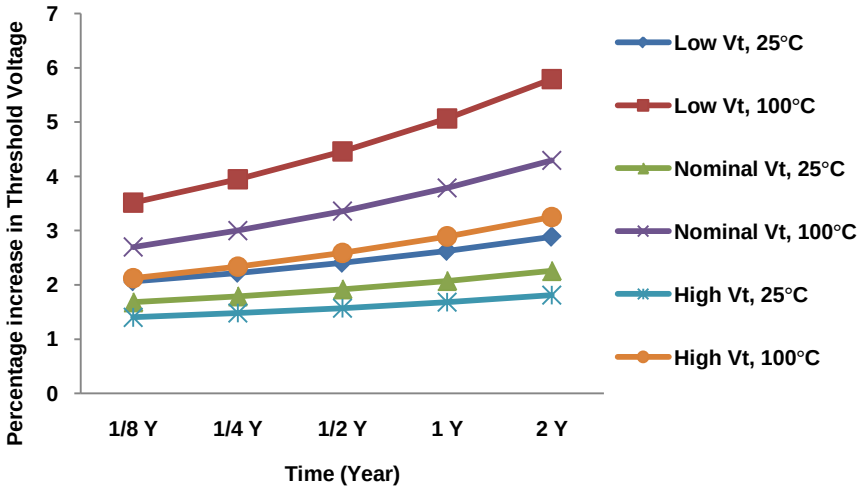

Figure 3: Percentage of NBTI induced Vt shift in high- k dielectric at 32nm PMOS for th three technology corners: Low, Nominal and High Vt at room (25^{o}C) and high (100^{o}C) temperature.

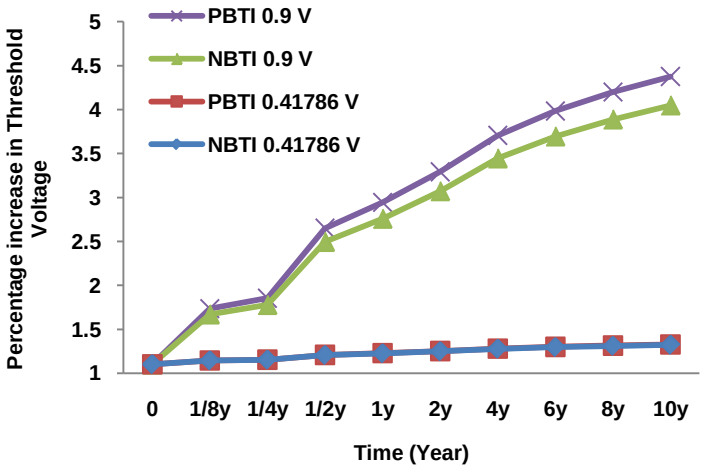

Figure 4: Percentage change in NBTI and PBTI over life-time.

3. COMBINED AGING EFFECT WITH PROCESS, VOLTAGE AND TEMPERATURE DEFERENCE ON RING OSCILLATOR CIRCUIT

To observe the combined effect of BTI with **P**rocess, **V**oltage, and **T**emperature (PVT) variations; while considering PVT dependence of BTI, CAD simulations are performed on five stage ring oscillator (inverter chain) circuit in a predictive 32nm technology (Fig. 5). V_{th} values vs. time are estimated from the model (Eq. 4) by MATLAB and then plugged into the circuit for simulation. We consider two supply voltages: low supply voltage of 0.5V and high supply voltage of 1V. Die-to-die process variations are represented by considering three values of threshold voltage: nominal (0.2V), low (nominal-50mV), and high (nominal+50mV) threshold voltage. Two cases of temperature are considered: low temperature (25°C) and high temperature (100°C). Under each PVT condition, V_{th} values over time are estimated using Eq. 4 and then applied to RO (inverter chain) to observe the impact on circuit parameters (delay and power). The input of the circuit is connected to a 1GHz pulse for delay and power characterization.

To analyze impact of aging effect on circuit delay at different V_{th} corners, a comparison of percentage of delay increase over time is made at 25°C and 1V supply (Fig. 6). The results show the low V_{th} circuit experiences percentage delay increase over time. Fig. 7 shows the percentage delay increase over a 2-year life time for low V_t RO cell at two temperatures (25°C and 100°C) and two supply voltages (0.5V and 1V). The results show that the impact of BTI aging effect on circuit delay is enhanced at higher supply voltage and higher temperature. This is attributed to the increased V_{th} shift at higher voltage and temperature conditions (Eq. 4).

The increased V_{th} due to BTI is expected to reduce the circuit power due to reduction in leakage power as V_{th} increases. This expectation is verified by results in Fig. 8. Fig. 8 (a) shows percentage reduction in active mode power at different conditions of supply voltage and temperature. Fig. 8 (b) shows the percentage of reduction in standby (leakage) power. The results show that the leakage power reduction is more significant at high voltage and high temperature conditions. This is attributed to the exponential dependence of sub-threshold leakage to V_{th} and higher amounts of V_{th} shift at high voltage and temperature conditions. The switching power is not affected by aging effects as it is not V_{th} dependent. Hence, the change in the active power (Fig. 8(a)) is only due to the change in the leakage power portion of the total active power.

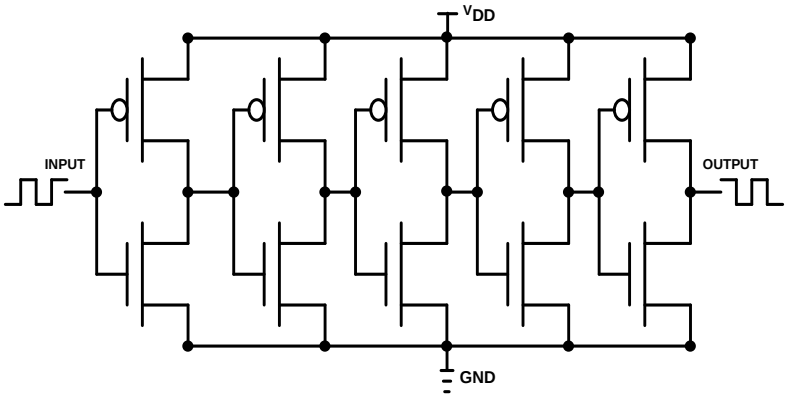

Figure 5: Five Stage Ring Oscillator (inverter chain) test bench.

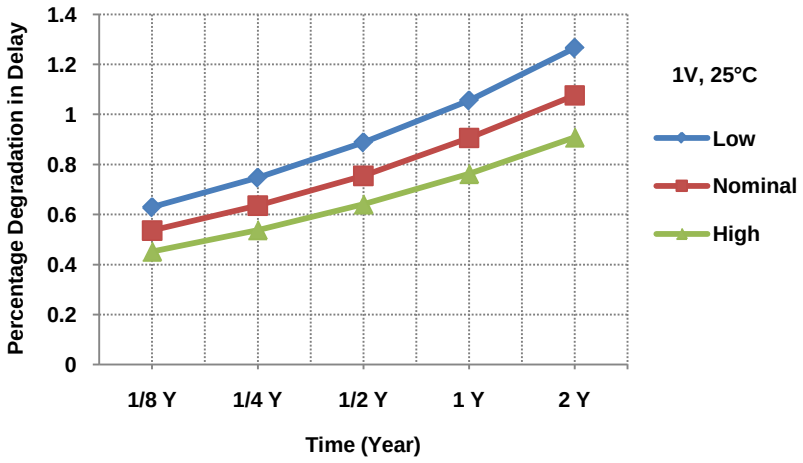

Figure 6: Ring Oscillator circuit degradation over time for three threshold voltage corners: low, nominal, high V_t. Low V_t circuit shows more degradation compared to high Vt circuit.

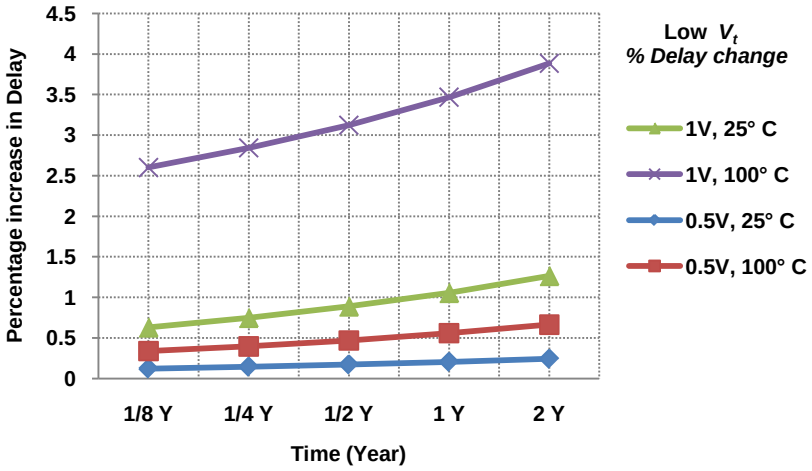

Figure 7: Delay degradation over two years. The circuit experiences more delay increase under high voltage and high temperature conditions.

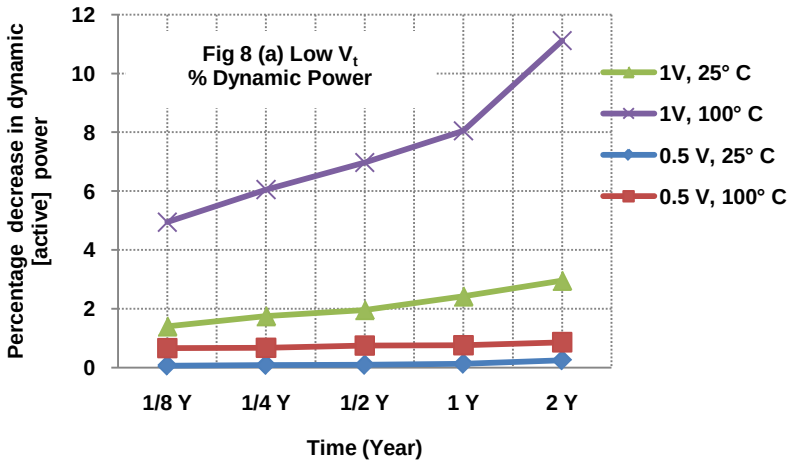

Figure 8(a): Impact of BTI on circuit power: percentage of active mode power reduction over time. Reduction is more at high voltage and high temperature condition.

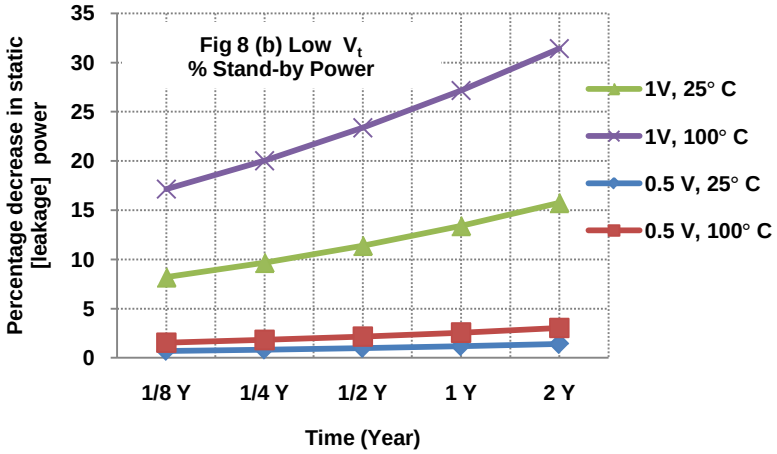

Figure 8(b): Impact of BTI ob circuit power: percentage of stand-by (leakage) power reduction. More change is observed for high voltage and high temperature condition.

4. ANALYSIS OF AGING EFFECTS IN SRAM DESIGNS

In various SRAM designs, reliability and manufacturing cost are utmost importance. For the first time we applied voltage scaling technique to compare the aging effect in 32nm CMOS process. To observe the reliability first, we considered hold SNM of 6T, 8T and 10T SRAM cell. Fig. 9(a) presents a schematic, describing the structure of SRAM cells in 32nm CMOS process. As shown, the basic structure of 6T cell is a pair of cross-coupled inverters under aging effect with a pair of PMOS and NMOS transistors together provides the storage. The storage access transistors M5 and M6 provide read and write operations. The cell supply voltage is 0.9V with threshold voltage V_{th} of 0.2V. Typical width and length used in this work is 71nm and 32nm respectively for SRAM core (NMOS & PMOS). M5 and M6 transistors have 32nm for width and length.

To illustrate the restrictions of 6T SRAM, consider the read operation by pre-charging node Q = “1” and Q’ = “0”. For the case of: (a) PBTI M1 is ON; (b) NBTI M4 is ON; resulting in V_{th} shift over time with increased turn-in voltage and reduce the level of read SNM. Under stress, the trip point of cross coupled inverter comes down with increased V_{th} of M1, M4 and the same for M2, M3. Thus, the cell gets flip during read operation and for write operation too, because the trip point of two inverters is decreased. In fact, BTI effect helps access transistors (M5, M6) to load and discharge easily. Thus the access transistor aging is not considered for simulation purpose. Also, performance limitations affect the stability of 6T cell with increased leakage power for supply voltage less than 1V [1] [8]. In [8] SRAM cell stability can be maximized with larger gains provided by additional transistors used to access the stored data. Conventional 8T

SRAM [7] and 10T SRAM [8] cells are shown in Fig. 9(b) and Fig. 9(c) respectively. Stability of stand-by SNM is increased by separating write and read bit lines. Additional two NMOS transistors M7, M8 with 32nm of width and length form a buffer to perform read operation by isolating the read bit line (RdBL). In 8T SRAM bit-line leakage is not fully limited. Hence two more additional NMOS transistors M9, M10 with 32nm width and length are added to 8T SRAM to perform read operation with minimum leakage power in 10T SRAM cell.

Initially, fresh 6T cell is simulated to obtain stand-by SNM without applying BTI (aging) effect at initial stress time (t=0), high temperature (100°C) and 0.9V. 115mV is the initial stand-by SNM (hold SNM) obtained for these conditions. Since 8T, 10T SRAM have larger SNM, hence to observe similar initial stand-by SNM of 6T cell at time (t = 0), 100°C in 8T, 10T SRAM; supply voltage is scaled to 0.41786V in 8T, 10T cell for simulation and obtained 115mV stand-by SNM. Table I shows the supply voltage adjustment of SRAM cells for same SNM = 115mV, without aging effects. Thus, equally balanced stand-by SNM at different V_{DD} will make reasonable comparison between all three SRAM designs to observe aging effects. From now on, rest of the paper will simulate 8T, 10T cells at 0.41786V. Table II shows the stand-by SNM results at high temperature (100°C) obtained with aging effect applied on pair of cross-coupled inverters (M1) and (M4) or (M2) and (M3) with threshold voltage (0.2V) for 6T, 8T, 10T SRAM. We observed initial SNM at high temperature (100°C) for all three SRAM to be 112.61mV with stress induced V_{th}. Fig. 10 shows the percentage of SNM for V_{th} = 0.2V SRAM cell for high temperature (100°C) with two supply voltage: 0.9V (6T) and 0.41786V ((8T) and (10T)). SNM

degradation is less in case of 8T and 10T SRAM cell compared to 6T SRAM cell. As such, for a stable SRAM based on results, BTI effect can be itemized as follows:

i. Overall SNM degradation for 0.41786V (8T) and (10T) is 4.26% and for 0.9V (6T) is 6.09% in 10 years of continuous DC stress.

ii. Design a SRAM with a minimum stand-by SNM change for the desired supply voltage and achieving a stable read and write SNM.

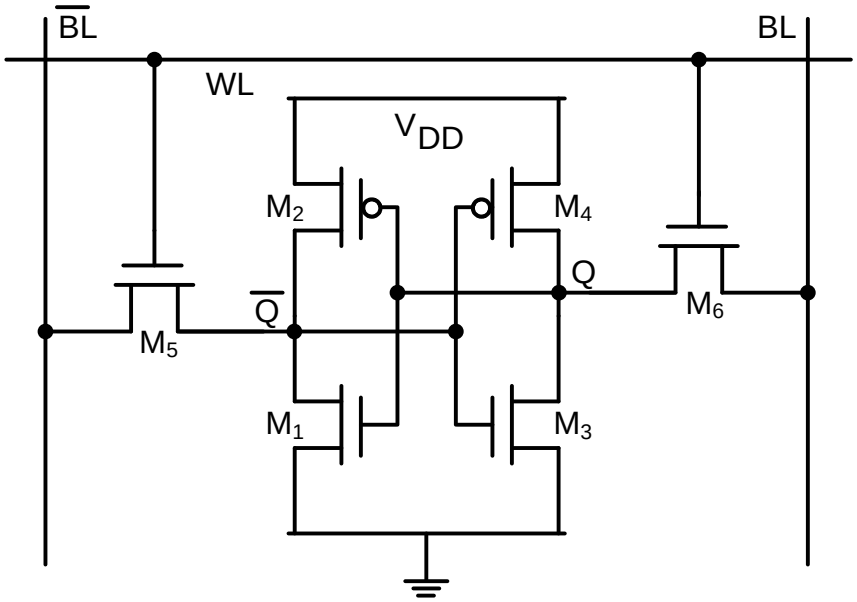

Figure 9(a): Schematic of Six transistor (6T) SRAM cell

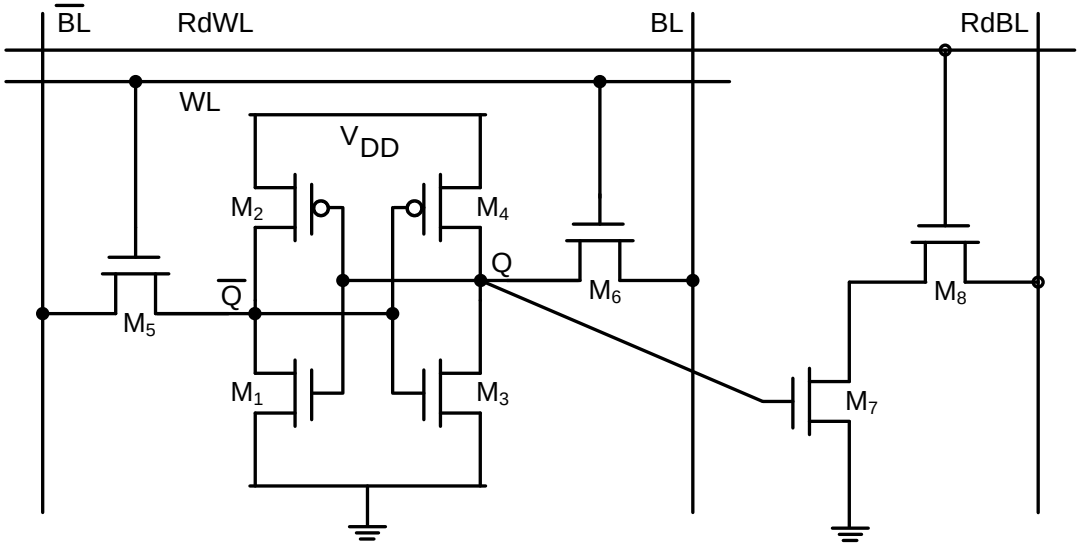

Figure 9(b): Schematic of Eight transistors with separate read-word line and read-bit line with M7 and M8

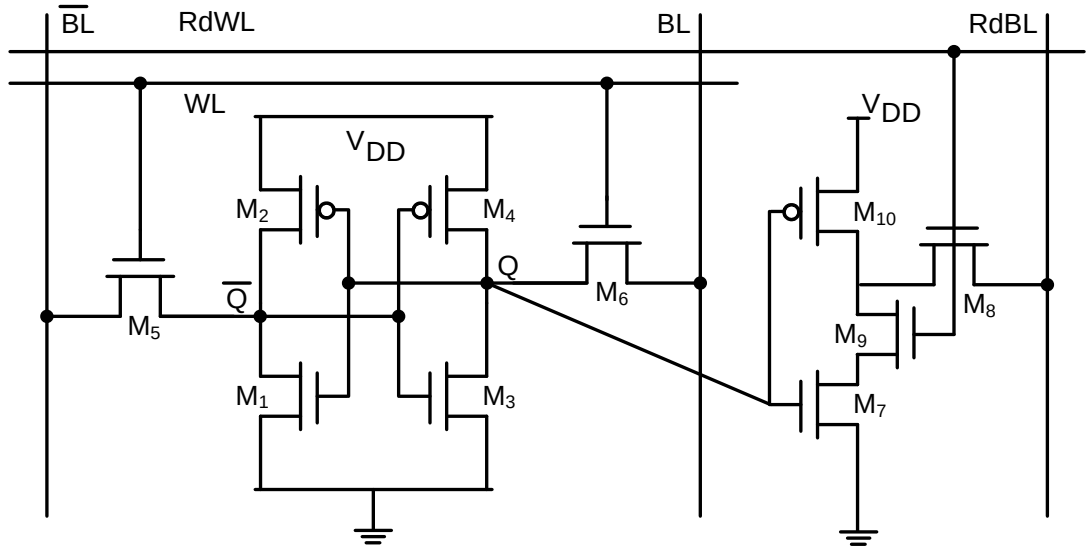

Figure 9 (c): Schematic of Ten transistors with M9 and M10 added to schematic of eight transistor to lower leakage power

TABLE I. SUPPLY VOLTAGE ADJUSTMENT OF SRAM CELLS FOR SAME SNM = $115 \times 10^{-3} V$

Cell	**With-out Aging for V_{th} = 0.2V at 100^{o}C**			
	Supply Voltage (V)	***Leakage Power (n W)***	***Access Time (n sec)***	***Write Margin (V)***
6T	0.9	32.3	0.432	0.296
8T	0.41786	2.09	17.9	0.110
10T	0.41786	1.94	31.3	0.109

TABLE II. SIMULATION REULTS WITH AGING EFFECT AT THRESHOLD VOLTAGE 0.2V FOR STAND-BY NOISE MARGIN (SNM)

Year	***SNM (V)***		
	SRAM Cell		
	6T	8T	10T
0	0.11261	0.11264	0.11264
1/8	0.11126	0.11254	0.11254
1/4	0.111	0.11253	0.11253
1/2	0.10936	0.11241	0.11241
1	0.10876	0.11237	0.11237
2	0.10803	0.11232	0.11232
4	0.10717	0.11226	0.11226
6	0.10658	0.11221	0.11221
8	0.10613	0.11218	0.11218
10	0.10575	0.11216	0.11216

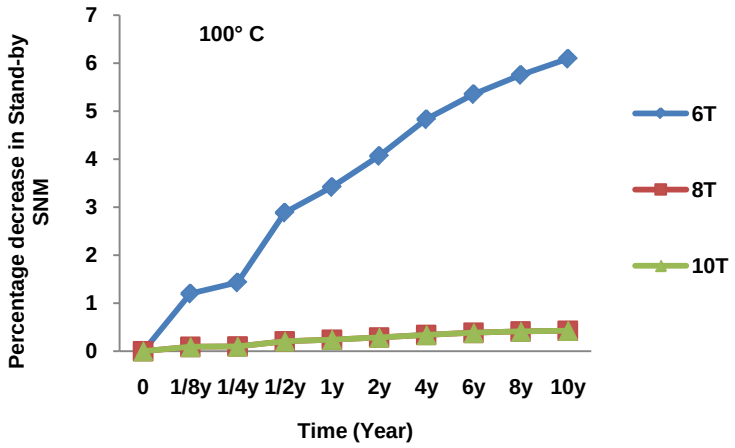

Figure 10: Percentage change in stand-by SNM. 10T, 8T has least change over 6T. 7% change in 6T device over 10 years of lifetime.

5. EFFECT OF AGING ON SRAM PERFORMANCE

To evaluate the impact of NBTI and PBTI effect in high- *k* dielectrics at the same time considering the effects of Process (V_{th}), Voltage, and Temperature variations on the reliability of SRAM cell with respect to SNM of write margin, access time and leakage power in 32nm SRAM cell designs. In general, these parameters are strong dependent of both the dimensions and bias voltage applied to it. In chapter IV we discussed the effect of BTI in stand-by mode and observed the resistivity (noise immunity) of 8T, 10T cell with negligible V_{th} degradation over time with supply voltage of 0.41786V. By using this bias voltage, isolating write (storing), read (accessing) with separate bit lines improves the stability and is necessary to reduce the BTI effect in lower supply voltage. To emphasis the importance of 8T, 10T SRAM design with supply voltage 0.41786V compared by 6T SRAM design simulated at 0.9V for write margin, read margin and leakage power.

5.1 *Write Margin*

To investigate the effect of aging on 6T, 8T and 10T cells for write operation, we evaluate the second write cycle by considering the worst-case condition to store Q = “0” and Q’ = “1” in Fig 9(a). First, B and B’ are connected to GND and V_{DD} respectively. Next, access transistors (M5) and (M6) are turned ON by applying V_{DD} to word line (WL). After first write cycle (storing, Q = “1” and QB’ = “0”), the Pseudo-NMOS inverter (M2) and NMOS (M3) gets aged for consecutive write operations. In our illustration (second write cycle), write margin decrease over time by making pull-down (node Q) and pull-up (node Q’) operation of SRAM cell. As seen from Table (I &III) 8T and 10T cell have nearly similar write margin because isolation of read and write operation from conventional 6T cell. Also, write margin is relatively less compared with 6T cell because 8T, 10T cell are simulated with lower supply voltage. As shown in Fig. 11, the percentage degradation is compared for write margin in V_{th} = 0.2V at 100°C. Characterization of Fig. 11 provides:

1. Write margin degradation for 6T cell is 0.63% for supply voltage of 0.9V over 10 years of lifetime.
2. Similarly, write margin degradation in 8T cell is 0.20% and 10T cell is 0.21% for supply voltage of 0.41786V.
3. Based on the results we can derive that aging effects severely for 6T cell at larger supply voltage.

To improve write margin [8] proposed to increase word line voltage. Alternative technique would be, to increase the size of access transistors in 8T, 10T cell. Appropriate techniques can be used based on circuit application and necessity for larger write margin.

5.2 *Access Time*

As indicated in the ideal 6T SRAM of Fig. 9(a), the function of access and pull down transistors do not provide necessary read margin for successful read operation because of technology scaling and increased aging effect. To improve worst-case read margin (access transistors pulls the stored bit to flip) in 6T core, single ended read operation is employed by adding extra transistors to 6T cell. 8T cell is formed by adding two NMOS to 6T cell and 10T cell is formed by adding one PMOS and three NMOS to 6T cell. Additional transistors provide better read operation and eliminate the worst-case stability condition in 8T, 10T cell compared over increased cell β ratio of 6T SRAM core to improve read operation [7], [8]. Table IV provides evidence for the above statement with aging effects applied and Fig. 12 shows percentage degradation of access time in V_{th} = 0.2V cell at 100°C with 6T SRAM cell simulated at 0.9V; 8T and 10T SRAM cell simulated at 0.41786V. These shows that percentage degradation in access time is more in case of 8T SRAM with 1.03% degradation in read current compared to 10T with 0.58% degradation for 10 years of life time. Although 6T SRAM shows 0.54% degradation of access time over 10 years of life time with supply voltage of 0.9V. [15] shows 6T SRAM at supply voltage of 0.5V has increased access time degradation and more sensitivity to variations (process, voltage, temperature).

5.3 *Leakage Power*

In addition to write margin and access time, leakage power is also extremely important. Initially, SRAM cell is isolated from performing either write or access operation by initializing WL, RdWL to “0”, and B, B’, RdBL are connected to V_{DD} of SRAM cell. 6T SRAM is pre-charged to Q = “0” and 8T, 10T SRAM is pre-charged to Q = V_{DD}. Table V presents simulated results of SRAM designs particularly to address the leakage power. In detail, the 10T SRAM design of column 3 in Leakage power section of Table V at 100°C has minimum leakage power, which actually improves over 8T, 6T SRAM design. Additional transistors are added to break down leakage on RdBL, irrespective of Q value stored in SRAM cell [8] and our simulation proves the observation made with minimum leakage power plus applied aging effect. The combined comparison with 8T, 6T makes 10T SRAM design an excellent consideration for reference memory applications in digital circuits in 32nm technology and beyond. Fig. 13 presents the percentage degradation plot, where the 6T has negligible percentage change, 8T has 1.06% change and 10T has 1.38% change over 10 years of life time, while consuming leakage power less than 1.90nW.

TABLE III. SIMULATION REULTS WITH AGING EFFECT AT THRESHOLD VOLTAGE 0.2V FOR WRITE MARGIN

Year	***Write Margin (V)***		
	SRAM Cell		
	6T	8T	10T
0	0.29511	0.10883	0.10829
1/8	0.29472	0.10878	0.10825
1/4	0.29465	0.10878	0.10824
1/2	0.29419	0.10872	0.10818
1	0.29403	0.10870	0.10816
2	0.29384	0.10868	0.10814
4	0.29361	0.10865	0.10811
6	0.29346	0.10863	0.10809
8	0.29335	0.10862	0.10808
10	0.29326	0.10861	0.10806

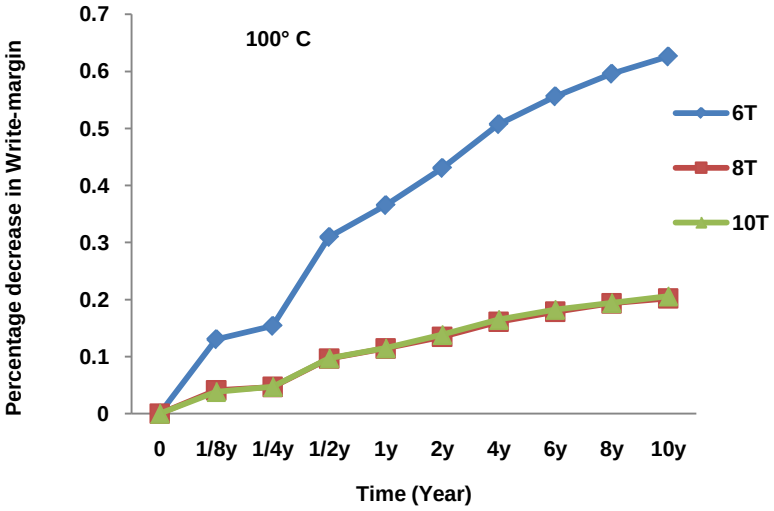

Figure 11: 6T cell is operated in 0.9V, 8T and 10T cell in 0.41786V. Hence, aging effects in 8T and 10T have minimum change in write margin for power scaled to obtain same SNM in Section IV.

TABLE IV. LATION REULTS WITH AGING EFFECT AT THRESHOLD VOLTAGE 0.2V FOR ACCESS TIME

Year	***Access Time (n sec)***		
	SRAM Cell		
	6T	8T	10T
0	0.43280	18.76	32.2186
1/8	0.43323	18.797	32.2539
1/4	0.43333	18.8037	32.2612
1/2	0.43389	18.8509	32.307
1	0.43410	18.8683	32.3238
2	0.43436	18.8888	32.3436
4	0.43466	18.9132	32.3677
6	0.43487	18.9297	32.3834
8	0.43504	18.9423	32.396
10	0.43518	18.953	32.4065

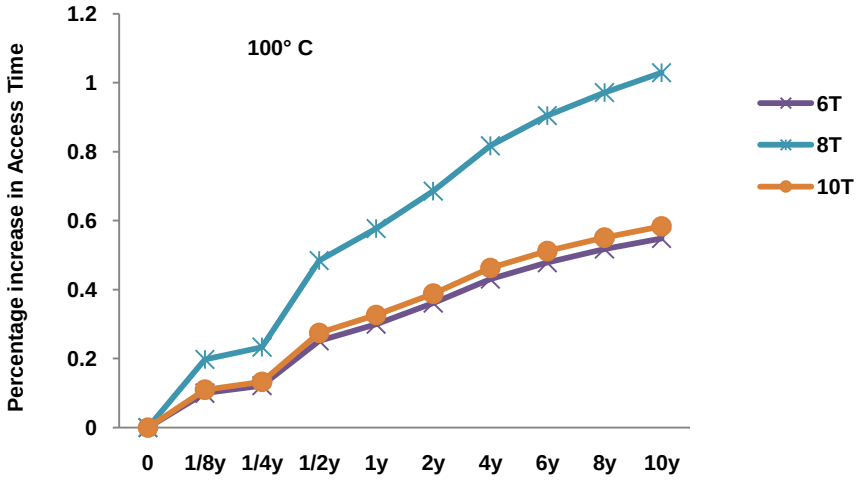

Figure 12: Despite of increased read margin in 8T, 10T cell. Larger percentage degradation is observed for 8T, 10T cell (negligible). 6T cell is more sensitive to variations in 32nm technology. The absolute values in Table V provide information about 6T sensitivity to read time change.

TABLE V. LATION REULTS WITH AGING EFFECT AT THRESHOLD VOLTAGE 0.2V FOR LEAKAGE POWER

Year	***Leakage Power (n W)***		
	SRAM Cell		
	6T	8T	10T
0	32.3	2.13	1.93
1/8	32.3	2.12	1.92
1/4	32.3	2.12	1.92
1/2	32.3	2.12	1.92
1	32.3	2.11	1.91
2	32.3	2.11	1.91
4	32.3	2.11	1.91
6	32.3	2.11	1.91
8	32.3	2.1	1.9
10	32.3	2.11	1.9

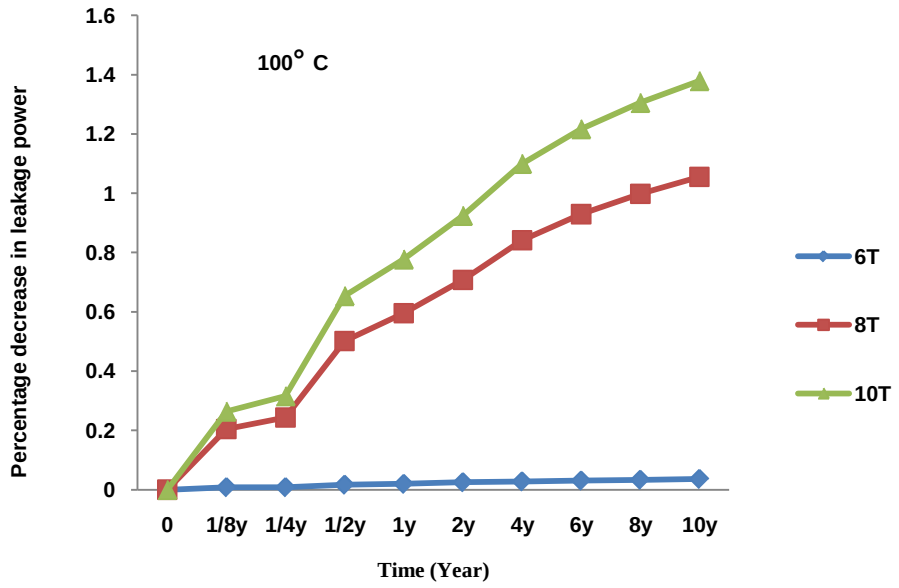

Figure 13: Leakage Power – percentage change is highest for 10T cell at 100°C. The absolute leakage change in 6T is to its maximum and saturates at 0.9V.

6. CONCLUSION

SRAM circuit characteristics using High- k transistors were simulated. We analyzed the reliability of SRAM design under transistor aging in Nano scale CMOS technology. High- k dielectric based simulations of SRAM parameters were performed. The results show 54% of lower supply voltage, agreeable write margin, and increased access time by $32.4 \times 10^{-9} sec$ for 10 years and consuming only 1.9 nW for 10T cell with emphasizing on the benefits yielded by scaling into 32 nm technology. Memory devices have now reached critical performance in various applications and need to commensurate with lower supply voltage, less than 1V. At this lower voltage aging effects is severe and new memory circuits are potential substitution that can eliminate quiescent power loss, allowing devices to operate in lower dynamic mode. Present trend is likely towards lower dynamic power and this work results is beneficial to observe the impact of aging of all three SRAM designs. Since 8T and 10T have negligible SNM degradation and reliability compared with 6T cell, we recommend designing memory arrays by 8T or 10T SRAM cell to reduce the impact of NBTI and PBTI effect.

7. REFERENCE

1. International Technology Roadmap for Semiconductors. [Online]. Available: http://www.itrs.net/

2. S. Zafar, A. Kumar, E. Gusev, E. Cartier, "Threshold voltage instabilities in high-k gate dielectric stacks," *IEEE Trans. Device Mater Rel.*, vol. 5, no. 1, pp. 45-64, Mar. 2005.

3. S. Zafar, et al., "A Comparative Study of NBTI and PBTI (Charge Trapping) in SiO_2/HfO_2 Stacks with FUSI, TiN, Re Gates," *IEEE Symp. on VLSI Tech. Digest of Tech. Papers.* pp. 23-25, 2006.

4. R. Vattikonda, W. Wang, Y. K. Cao, "Modeling and minimization of PMOS NBTI effect for robust nanometer design," *Design Automation Conference, 2006 43rd ACM/IEEE* , vol., no., pp.1047-1052.

5. A. Kerber, E. Cartier, "Reliability Challenges for CMOS Technology Qualifications With Hafnium Oxide/Titanium Nitride Gate Stacks," *IEEE Trans. Device Mater Rel.,* vol. 9, no. 2, pp. 147-162, Jun 2009

6. Seevinck, F. J. List, J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE J. Solid-State Circuits,* vol. SC-22, pp. 748-754, Oct. 1987.

7. L. C Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, W. Haensch, "Stable

SRAM cell design for the 32 nm node and beyond," in *Proc. IEEE Symp. on VLSI Technology Dig. of Tech. Papers.* pp. 128- 129, June 2005.

8. H. Calhoun, A. Chandrakasan, "A 256kb Sub-threshold SRAM in 65nm CMOS," in *Tech. Dig., ISSCC 2006, San Francisco, CA*, Feb. 6-9, 2004, pp. 2592-2601.

9. C.-T. Chuang, S. Mukhopadhyay, J.-J. Kim, K. Kim, R. Rao, "High-performance SRAM in nanoscale CMOS: Design challenges and techniques," in *IEEE Int. Workshop., Memory Technology, Design and Testing,* Taipei, Taiwan, Dec. 3-5, 2007, pp. 4-12.

10. S. Zafar, "Statistical mechanics based model for negative bias temperature instability induced degradation," *J. Appl. Phys.*, vol. 97, pp. 103709-103709-9, May 2005.

11. H. Yamauchi, "A Discussion on SRAM Circuit Design Trend in Deeper Nanometer-Scale Technologies," *IEEE Trans. Very Large Scale Integr. Syst.* vol.18, no.5, pp.763-774, May 2010.

12. Semiconductor Industry Association. [Online]. Available : http://www.sia-online.org/

13. Y. C Cao, (2008, Sep 30) "A new set of predictive technology model for high performance applications, incorporating high-k/metal gate and stress effect," [Online]. Available: http://www.eas.asu.edu/~ptm/.

14. H. Noguchi, Y. Iguchi, H. Fujiwara, Y. Morita, K. Nii, H. Kawaguchi, M. Yoshimoto, "A 10T Non-Precharge Two-Port SRAM for 74% Power Reduction in Video Processing," in

Proc. IEEE Comput. Soc. Annu. Symp. on VLSI, Porto Alegre, Brazil, Mar. 9-11, 2007, pp.107-112.

15. S. K. Krishnappa, H. Singh, H. Mahmoodi, "Incorporating Effects of Process, Voltage, and Temperature Variation in BTI Model for Circuit Design," in *Proc. IEEE Latin American Symp. on Circuits and Syst.*, pp. 236-239, Feb. 2010.

16. J. D. Plummer, M. Deal, P. B. Griffin, "Thermal Oxidation and the Si/SiO_2 Interface," in *Silicon VLSI Technology.* Upper Saddle River, NJ: Prestice-Hall, 2000.

17. J. Robertson, "High dielectric constant gate oxides for metal oxide Si trasistors," Rep. on Prog. Phys., vol 69, no. 2, pp. 327.396, Feb. 2006.

18. A. E. Islam, H. Kufluoglu, D. Varghese, S. Mahapatra, A. M. Alam, " Recent Issues in Negative-Bias Temperatur Insability: Initial Degradation, Field Dependence of Interface Trap Generation, Hole Trapping Effects, and Relaxation," *IEEE Trans. Electron. Devices*, vol. 54, no.9, pp. 2143-2154, Sep. 2007.