School of Engineering

Electrical and Computer Engineering

Master Oral Defense

Title: VERIFICATION OF RECONFIGURABLE PARALLEL ALU VIA SOFTWARE SIMULATION AND HARDWARE EMULATION

Student: VISHAKHA PANDHARIPANDE
Time & Date: 1:00PM, March 22, 2013 **Location: SCI 110**
Committee Chair: Dr. Hamid Mahmoodi
Committee Members: Dr. Hamid Shahnasser

Abstract:

The scaling of transistor dimensions in accordance to Moore's law has exposed semiconductor industry to substantial challenges such as 'Device Unreliability' which results in reducing the device lifetime. The root cause for unreliability is the shift in the threshold voltage which could be introduced either by device degradation or process parameter variation. 'Device Unreliability' is a major bottleneck to further transistor scaling and should be overcome. This research is focused on understanding and thereby validating an architectural level model designed to enhance the device reliability. The proposed model uses an effectual redundancy method in which the redundant modules are dedicated to efficient computation. The validation methodology involves software simulation of the proposed architecture by using Synopsys EDA tools and Hardware Emulation by programming the design into an Altera DE2-115 FPGA board. The research also suggests dynamic Voltage scaling to further improve Power consumption and Reliability.