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SIC(Simplified Instruction Computer)

Memory

1 Word = 24 bits (3 8-bit Bytes) A total Memory of 2^{15} (32,768) bytes i.e., (32 Kilo Bytes) it uses Little Endian format to store the numbers, 3 consecutive bytes form a Word

Registers

There are 5 registers, each 24 bits in length, their mnemonic , numbers are A (Accumulator) - 0, X (Index Register) -1, L (lLinkage Register)-2, PC (Program Counter)- 8, SW (Status Word)- 9

Data Format

Characters stored in 8 bits, in ASCII Format, Integers are stored as 24-bit binary numbers, 2`s Complement representation is used for negitive values. No Floating point Hardware on Standard Version of SIC

Instructions Format

All machine instructions on the Standard Version of SIC have 24 bit format Opcode 8 Bits, 1 Bit X is used to Indicate Indexed Addressing Mode, and 15 bits for Address

Addressing Mode

There are Two Addressing Modes available, indicated by the setting of the X bit in the instruction. The Target Address is Caculated from the Address given in the Instuction. The Type are Direct Mode & Indirect Mode Where Direct mode X= 0, Target Address(TA) = Address, Where in Indexed X= 1, Target Address (TA) - Address + (X), Parentheses are used to Indicate the contents of Regisater.

Instruction Sets

Basic Set of Instruction That are Sufficient for most simple Tasks, These include instructions that load and Store Registers, these instruction set comprises of Arthmetic Operation, CC Condiotional Code (Relational Operations), Conditional Jump Instructions etc., Another Two Instructions are Provided for Subroutine linkage JSUB, RSUB returns by jumping to the Assress Contained REgister.

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Input / Out Put

Input and Output are performed by Transfering 1 Byte at a time. Each Device is assigned a unique 8 bit code, there are 3 I/O Instructions, each of wich specifies the device code as an Operand, TD - Test Device, RD - Read Device, WD - Write Device.Conditional Code is set to indicate the results < ready to send or receive.

SIC X/E (Extra Equipment)

Memory

A total Memory of 2^{20} (1024) bytes i.e., (I Mega Byte) , this increase leads to a change in instruction formats and addressing modes

Registers

B - 3 = Base Register, S - 4 General Rgister, T - 5 General Register, F - 6, Floating Point Accumulator (48 bits)

Data Format

In Addition to Standard Version of SIC there is a 48 bit Floating point data type, 1 bit for sign, 11 bits for exponent and 36 bits for fractions refered as f $* 2^{(e-1024)}$

Instructions Format

Sic X/E supports 4 data Formats ie., 1,2,3,4 which include its Lower version also. F-I has 8 bits, F-II 16 bits, F-III 24 bits , F-IV 32 Bits, Hence instruction format used on SIC is nor longer Suitable

Addressing Mode

Two new Addressing modes are available for the use in Assembly Inst. Base Relative, Program-Counter Relative. In N I X B P E registers BP are used as Diaplacement Fields, X is Index field, I & N are addressing Modes, if I = 0 & N=0 then treated as Immediate. Address / i=0 n=0 then treated as Indirect Address and BPE are part of Address of instruction

Instruction Sets

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SIC/XE Provides all of the Inst. That are available on Sic in addition there are inst. To load and store the New Register (LDB,STB) and to Perform Floating Point Arithametic Operation, RMO Remove Register, SVC, Supervisor Call Register, Register to Register Arithametics

Input / Out Put

SIC/Xe Provides all of the Inst. Of SIC in addition There are I/O Channels hat can be used to perform I/O Operations While CPU is Executing Other Instructions. The Inst. SIO, TIO, HIO ie., Start, Test, Halt the Operation of I/O Channels

CISC (Complex Instruction Set Computers)

VAX (VIRTUAL ACCESS EXTENDED/EXTENSION)

Memory

It Consistes of 8 bit bytes, all addresses used are Byte Addresses , 2 consecutive bytes form a word Byte = 8 bits, word = 16 bits, long word = 32 bits, Quard word =64 bits, Octa Word = 128 bits

Registers

There are 16 General Purpose Registers(GPRs), 32 bits each, named as R0 to R15, Program Counter (R15), Stack Pointer (R14), Frame Pointer (R13), Argument Pointer (AP) (R12), Others Available for general use. There is a Process Staus LongWord(PSL)

Data Format

Integers are Stored as binary numbers in byte, word, Long Word, Quardword, OctaWord. 2`s Complement notation is used for storing negitive numbers. Chracters are stored in 8-bit ASCII codes.

Instructions Format

Uses VAriable-Length instruction formats - OP Code 1 or 2 bytes, Maximum of 6 Operand Specifiers depending on type of instruction. Each operand specifier designates one of the VAX Addressing modes and give any additional informatiom necessary to locate the operand.

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Addressing Mode

Provides a large number of addressing modes, they are Register Mode, Register Deferred Mode, AutoIncrement, AutoDecrement, base relative, Program-Counter Relative, Indexed, Indirect and immediate mode.

Instruction Sets

It has an Instruction Set that is Symmetric with Respect to Data Type. 1. A Prefix that Specifies the Type of Operation, 2) A Suffix That Specifies the Data Type of the Operand 3) A Modifier that gives the number of Operands Involved. Vax Provides all of the usual Types of Instructions for Computation, data Movement and Conversion , Comparasion, Branching etc., In addition there ara a no. of operations that are much more complex than the machine Instruction found on most Computers. These Operations are for the most part HardWare realizations of frequently occurring sequences of Code They are implemented as Single Instructions for Efficiency and Speed

Input / Out Put

Vax are Accomplished by I/O Device Controllers, each Controller has a set of I/O Control/Status and Data Registers. The Portion of the Address space into which the device controllers registers are mapped is called I/O Space. An I/O Device Driver issues commands to the device controllers by Storing the Values into Appropriate registers. These I/O Space and Physical Registers in a device controllers is handled by the Memory Management Routines.

Pentium Pro (Produces Erroneous Numbers Through Incorrect Understanding of Mathematics) 5.5 Million Transistors

Memory

It Consistes of 8 bit bytes, all addresses used are Byte Addresses , 2 consecutive bytes form a word, 4 bytes form a Double Word (Dword). Viewed as collection of segments, address = Segment number + Off set Number 1

Registers

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There are 32 bits, Eight GPRs, Namely EAX, EBX,ECX,EDX,ESI,EDI,EBP,ESP. Used for data manipulation, Other Four are used to hold addresses. EIP - 32 bit contains pointer to next instruction to be Executed. 6 no of 16 bit segment registers

Data Format

This Architecture provides for the Storage of Integers, Floating Point Values , Chracters and Strings, Integers are Stored as 8, 16, 32 bit Binary Numbers, Both Signed and Unsigned. Floating Point Unit can Also Handle 64 Bit Integers. Integers can also be Stored in Binary Coded Decimal (BCD). this Architecture store Three Types of floating point data, Single Precession 32 bit long, Double Precision 64 bit long, Extended Precision format 80 bit long. Chracters are stored one per byte ASCII Format.

Instructions Format

The Instructions yuse variations of the same basic format, this format begings with optional prefixes containing falgs that modify the operations of the instructon. The OPCODE is the only element that is always present in every instruction, Other Elements may or maynot be present and may be different lengths, depending on the operation and the operands invloved.thus there are large no of different potiential instruction formats, varying in length from 1 byte to 10 bytes or more.

Addressing Mode

This architecture provides a Large No.of Addressing Modes. It accepts as Immediate Mode or it may be Register Mode TA= (Base Register)+(Index Register) * Scaling Factor +(Displacement). The address of an operand in memory may also be specified as an absolute location(Direct Mode) or as a location Relative to the relative mode

Instruction Sets

there are Register to Register Instructions, Register to Memory Instructions and few Memory to Memory Instructions, In smome cases operands may also be specified in the Inst. As Immediate Values. INT Data Type uses operands that are 1,2 or 4 Bytes. String data type uses VAriable Length strings of Bytes , Words or Double Words and there are many Inst. that perform Logical and bit Manipulations and support Control of the Processor and Memory Management.

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Input / Out Put

input is performed by Instructions that transfer one byte or Double Word at atime from an I/O port into Register EAX. Vice versa the Out put. Repetition prefixes allow these instructions to transfer an entire string in a single Operation.

RISC (Reduced Instruction Set Computer)

Ultra SPARC (Scalable Processor Architecture (SPARC)) 16 Millions of Transistors

Memory

It Consistes of 8 bit bytes, all addresses used are Byte Addresses , 2 consecutive bytes form a Half Word, 4 bytes form a Word, 8 bytes form Double Word, uses Virtual Address Space of 2^{64} bytes, 8,58,99,34,592 bits divided into pages.

Registers

More than 100 General Purpose Registers with 64 bit length, There are 64 double precision floating registers in a Special Floating Point Unit (FPU), In additon to these, it contain PC, condition Code Registers and Control Registers

Data Format

SPRAC provides the Storage of Integers, Floating Point Values and Chracters, Both Signed and Unsigned integers are supported 2`compelemt is used for Negv. Values. It supports both Big Endian and Little Endian Formats. This Architecture Supports three Floating point data formats, Single Precision, Double Precision and Quad Precision. Chracters are stored one per byte using 8 bit ASCII format.

Instructions Format

There are Three basic instructions formats in the SPRAC architecture . All of these formats are 32 bit long. The First 2 bits of the instruction word identify which format is being used. Format 1 is used to call the Instruction. Format 2 is used for Branch Instruction, Format 3 provides for register Loads and Stores and three Operand Arthimetic Operations. The Fixed instruction Length in the Sparc is Typical fo RISC Systems and is intended to speed the process of instruction fetching and decoding.

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Addressing Mode

Operand vales my be Specified as part of the Instructions itself ie., (Immediate Mode) or it may be Register (Register Direct Mode), it uses the following addressing modes. 1) PC- Relative, 2) Registers indirect with displacement, 3) Register indirect indexed. Pc-Relative Mode is used for only for branch instructions.

Instruction Sets

Instruction execution on a SPRAC system is PIPELINED, while one instruction is being executed, the next one is being fetched from memory and decoded.this technique speeds instruction execution. To make pipeline work more efficiently SPRAC branch instructions are delayed branches. This Means that the instructions immediately following the branch instruction is actually executed before the branch is taken.Communication in MultiProcessor System is facilated with "ATOMIC" Instructions that can ne execuited without allowing other memory accesses to intervence.

Input / Out Put

SPRAC Architecture communication with I/O devices is Accomplished through Memory. A range of memory locations is logically replaced by device registers. Each I/O Device has an Unique address or Set of Addressesassigned to it. When Load or Store instruction refers ot this device register area of memory , the Corresponding device is Activated. Thus Input and Output can be performed with the regular instruction set of the computer and no Special I/O inst. are needed.

CRAY T3E Cray Research Inc(Toxicomanie Europe Echanges Etudes)

Memory

MPP (Massively Parallel Processing System, contains a Large number of Processing Elements (PEs), arranged in a Three Dimensional network. Each PE consists of a DEC Alpha EV5 RISC Processor and Local Memory

Registers

There are 32 General Purpose Registers(GPRs) with 64 bits length each called R0 through R31, contains value zero always, In Addition to these, it has 32 Floating- Point registers , 64 bit Long and 64 bit PC, Status and Control Registers.

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Data Format

The Cray Architecture priovides for the Storage of Integers, Floating Point ccalues and Characters. Intergers are Stores as Long and Quard Wards, 2` Complement is used for Negv. Vlaues. Chracters may be Stored one per Byte using their 8-Bit Ascii Code However only Long Word and Quard Wards can be Transfered b/w Registere and Memory, Usuallu chracters are Stored One PEr LongWord.

Instructions Format

There are 5 basic Instruction formats in Cray T3E Architecture, Some of which have Subforms all of these formats are 32 bit long. The First 6 bits of the Instruction word always specify the OPCODE, Some instructions also have an additional function field.

Addressing Mode

As in Most Architectures an operand value may be specified as part of the Instruction itself(Immediate Mode) or an Register Direct Mode. Cray T3E uses the following two Addresses Modes 1. Pc-relative TA=(PC)+DisPlacement (23 bits Digned) ,
2) Register Indirect with Displacement TA=(Register)+Displacement(16bit, Signed), the 2nd Add Modes is used for Load and Store Opeartions and for SubRoutines jumps. Pc-Relative mode is used for Conditional and unconditional Branches.

Instruction Sets

The Cray T3E Architecture has Approximately 130 Machine Instructions reflecting its RISC Orientation. The Instruction set is designed so that an Implementation of the architecture can be fast as Possible.

Input / Out Put

T3E Systems performs I/O through multiple ports into one or more I/O channels, these channels are Integreated into the networks that interconnected the Processing Nodes. A System may be configured with uo ot one I/O Channel for every 8 Pes. All Channels are Accessible and Controllable from all PEs.