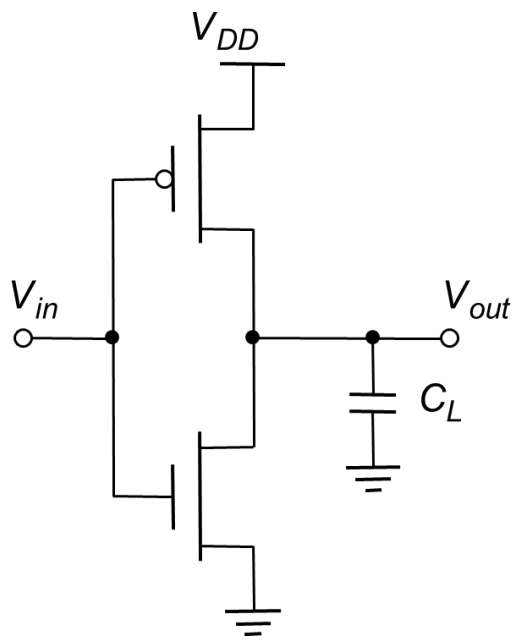
The Inverter

Pravin Zode

Outline

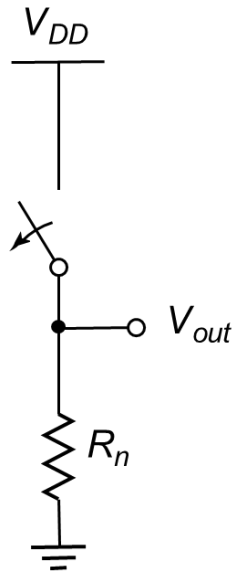
- Inverter Basics
- Transient Response
- DC Characteristics
- Beta Ratio Effect
- Noise Margin

Inverter Basics

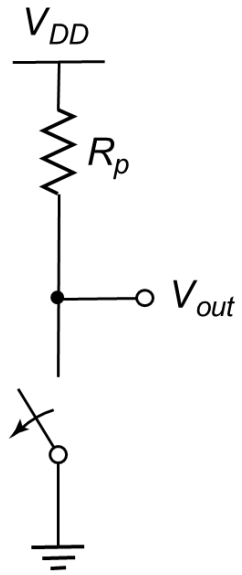


- PMOS on top (connected to VDD)
- NMOS on bottom (connected to GND)
- Both gates connected to input Vin
- Drains connected together to form output Vout

Inverter DC Analysis



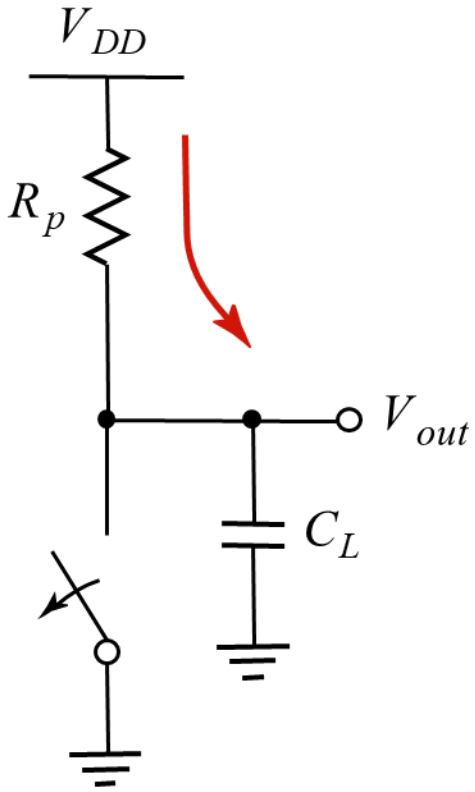
V_{in} 5 V_{DD}



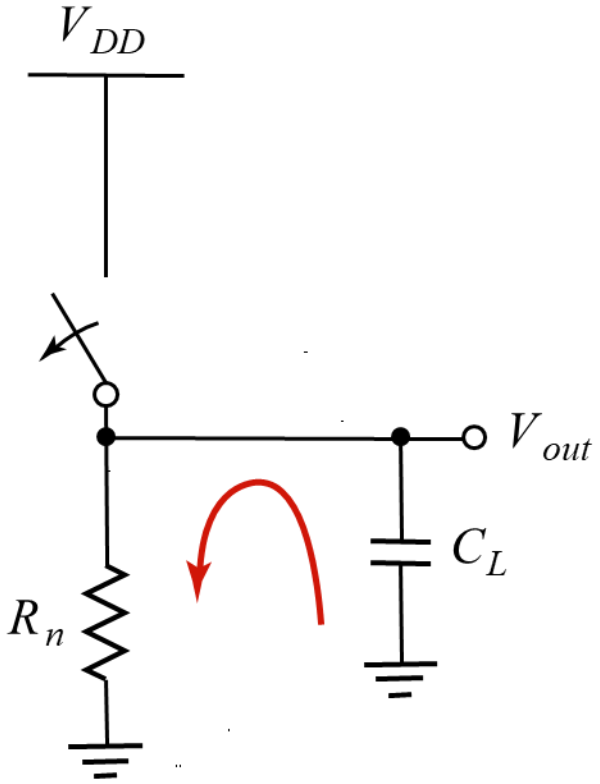
V_{in} 5 0

$$V_{OL} = 0$$
$$V_{OH} = V_{DD}$$
$$V_M = f(R_n, R_p)$$

Inverter Transient Response

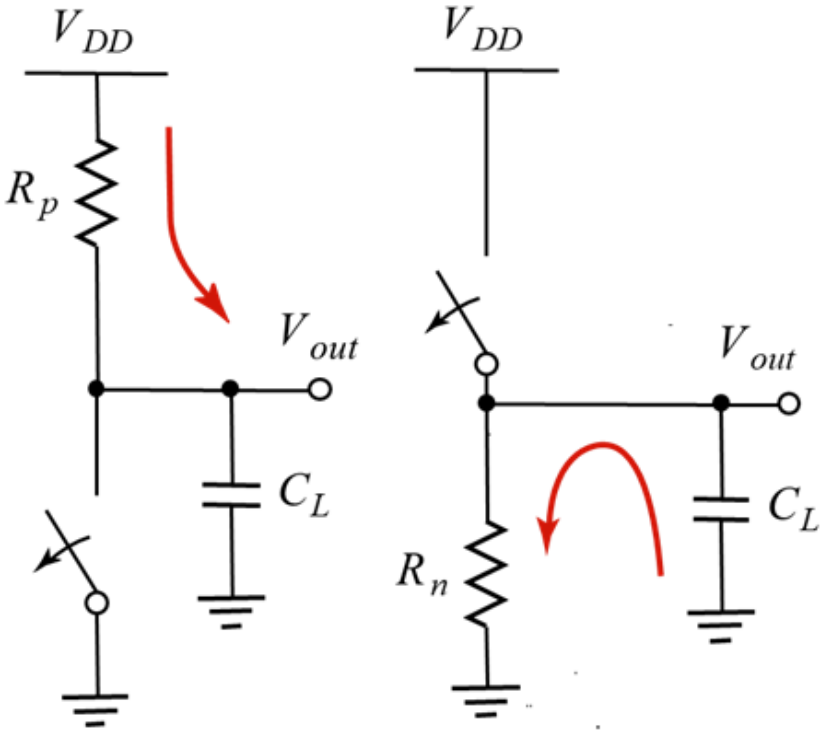


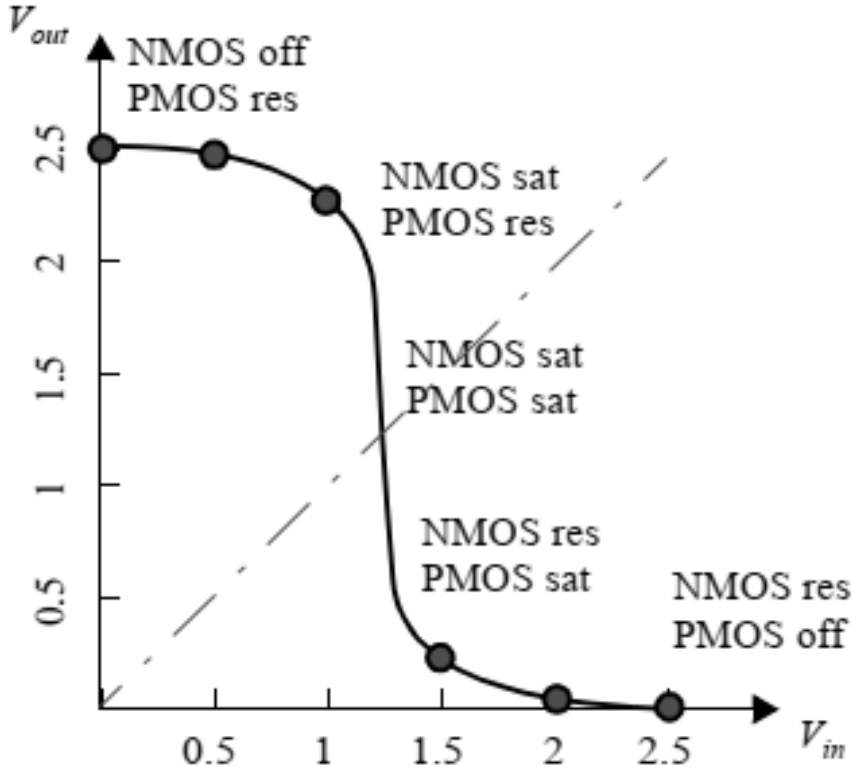
(a) Low-to-high



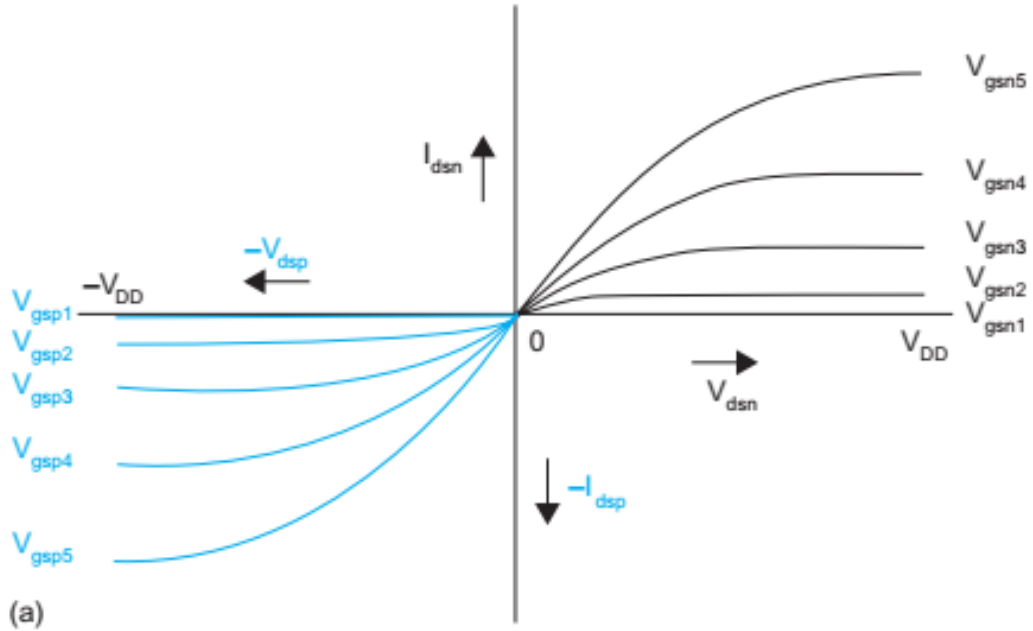
(b) High-to-low

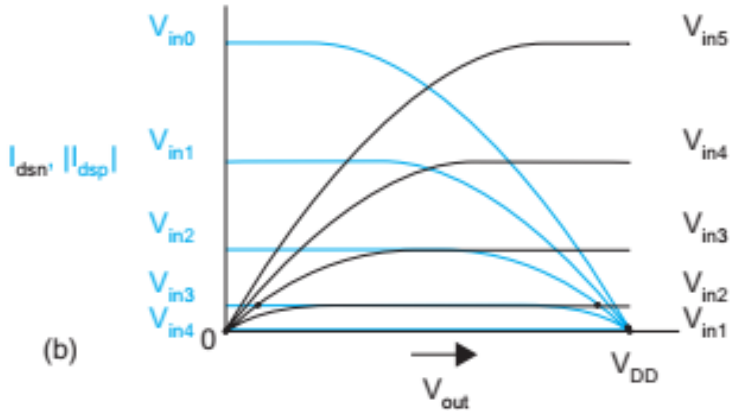
CMOS Inverter Load Characteristics

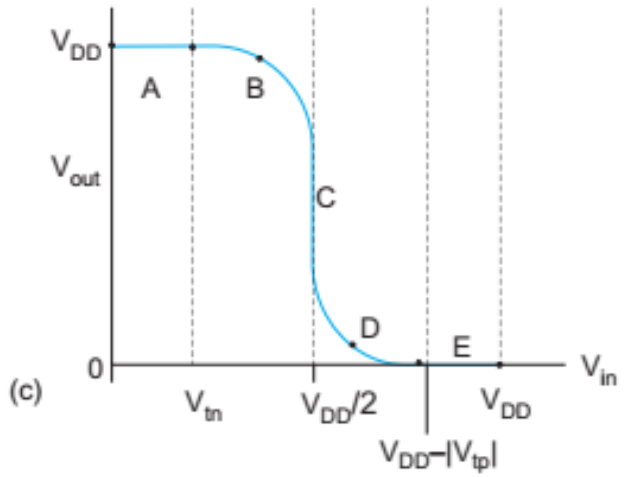


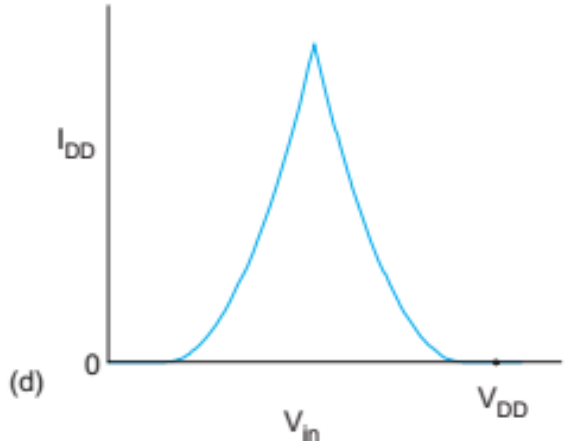


Inverter DC Characteristics

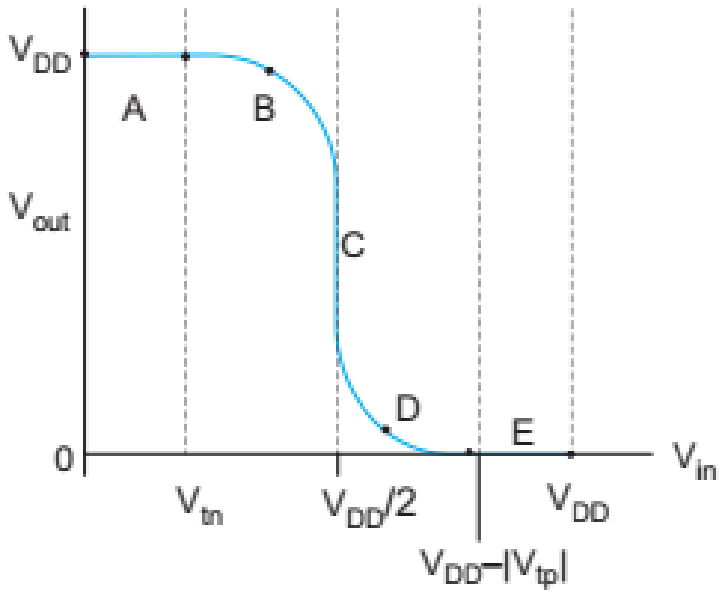








Inverter DC Characteristics

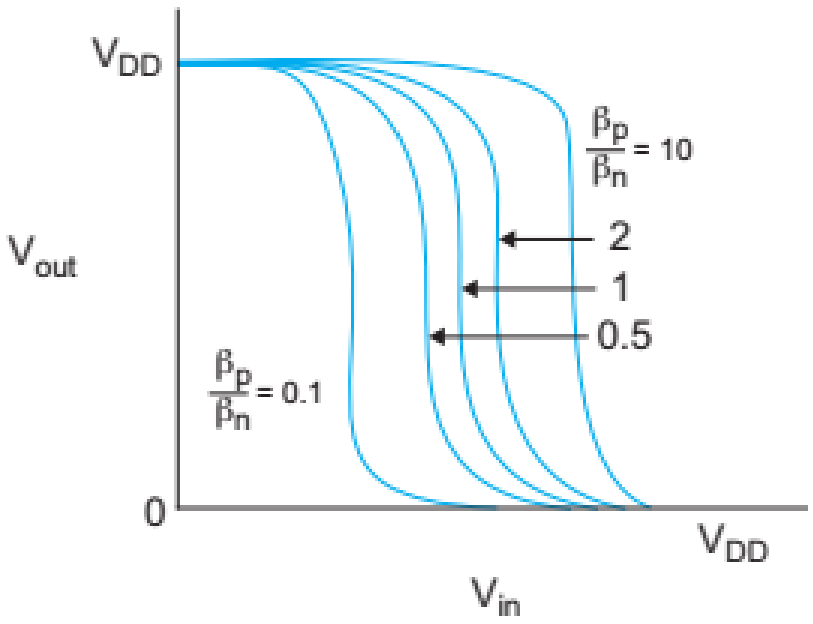


Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \|V_{tp}\|$	cutoff	linear	$V_{out} = 0$

Inverter Threshold

- Inverter threshold is the input voltage at which the output voltage = input voltage for an inverter
- **Ideal condition: Vdd /2**
- Why it is desirable
  - Maximum noise margin
  - Equal rise and fall times for charging/discharging capacitive loads
  - Balanced PMOS (pull-up) and NMOS (pull-down) strengths

Beta Ratio Effect



- Inverters with different beta ratios r = βp /βn are called skewed inverters
  - r > 1: **HI-skewed** – stronger pMOS → higher threshold
  - r< 1 : **LO-skewed** – weaker pMOS → lower threshold
  - r=1 : **Unskewed** inverter – balanced

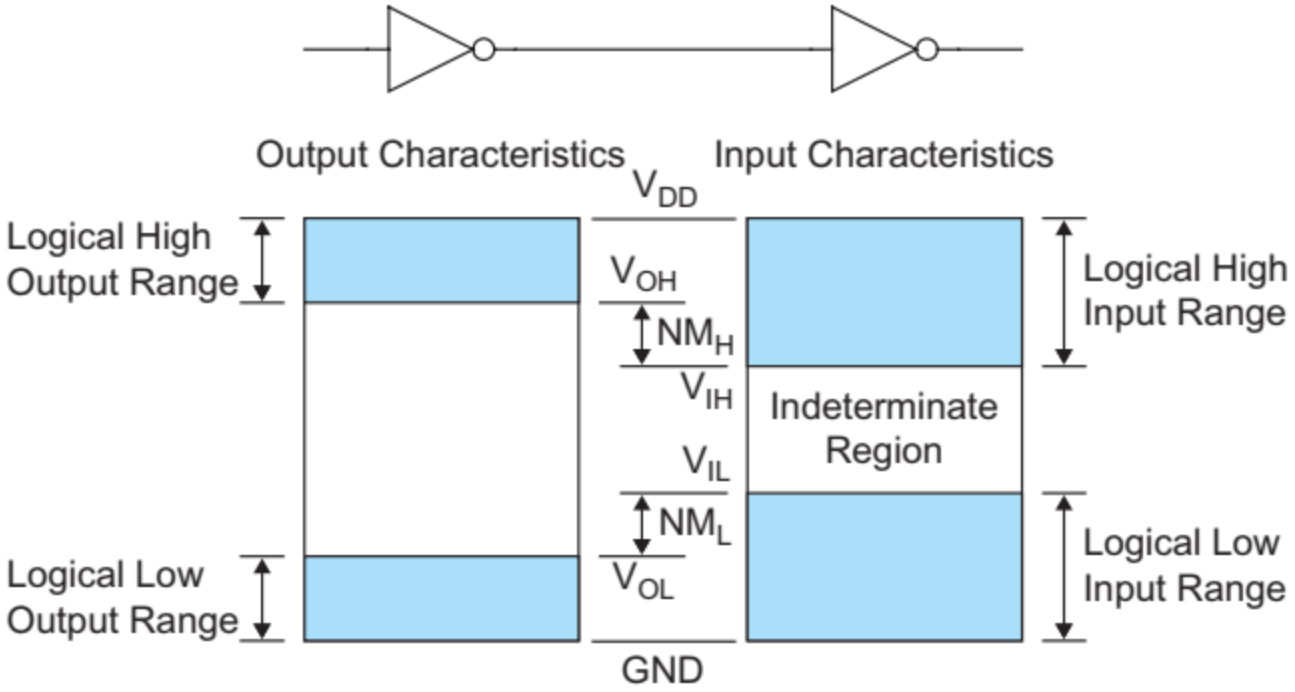
Impact of Skewing:

- Alters switching threshold in DC transfer characteristics
- Sharp transitions maintained despite skewing

Noise Margin

- Noise margin quantifies the tolerance to unwanted voltage fluctuations (noise) on the input without corrupting the output
- Closely related to the DC voltage transfer characteristics
- Characterized by two parameters:
  - LOW Noise Margin (NML)→ Tolerance for noise in logic ‘0’ region
  - HIGH Noise Margin (NMH)→ Tolerance for noise in logic ‘1’ region

Noise Margin



where

V_{IH} = minimum HIGH input voltage
V_{IL} = maximum LOW input voltage
V_{OH} = minimum HIGH output voltage
V_{OL} = maximum LOW output voltage

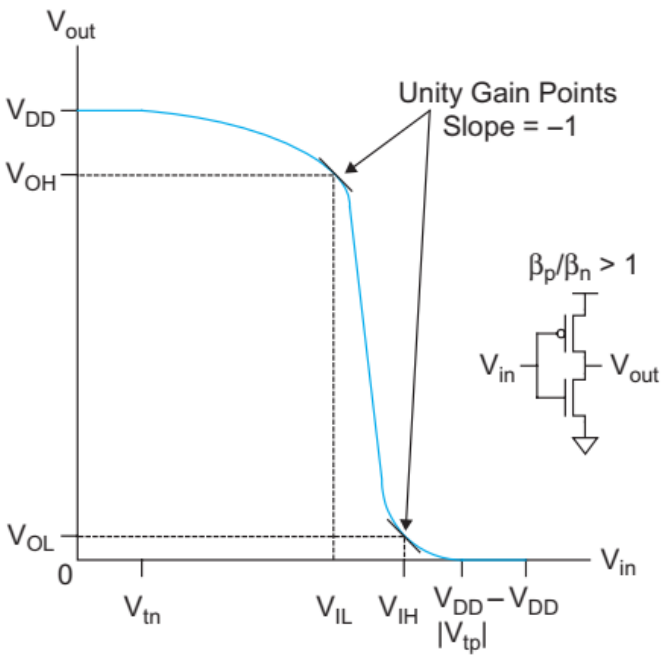
$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Noise Margin

- Let's say a gate outputs a logical HIGH as VOH = 4.8V, and the next gate requires at least VIH = 3.5V to reliably detect a HIGH: NMH = VOH – VIH = 4.8V – 3.5V = 1.3V
- This means: Up to 1.3V of noise can interfere, and the signal will still be understood as HIGH
- Similarly, for LOW:
- Suppose VOL = 0.2V, and the input accepts LOWs up to VIL = 1V: NML = VIL – VOL = 1V – 0.2V = 0.8V
- So, up to 0.8V of noise can be tolerated while still being recognized as LOW.

Inverter Noise Margin

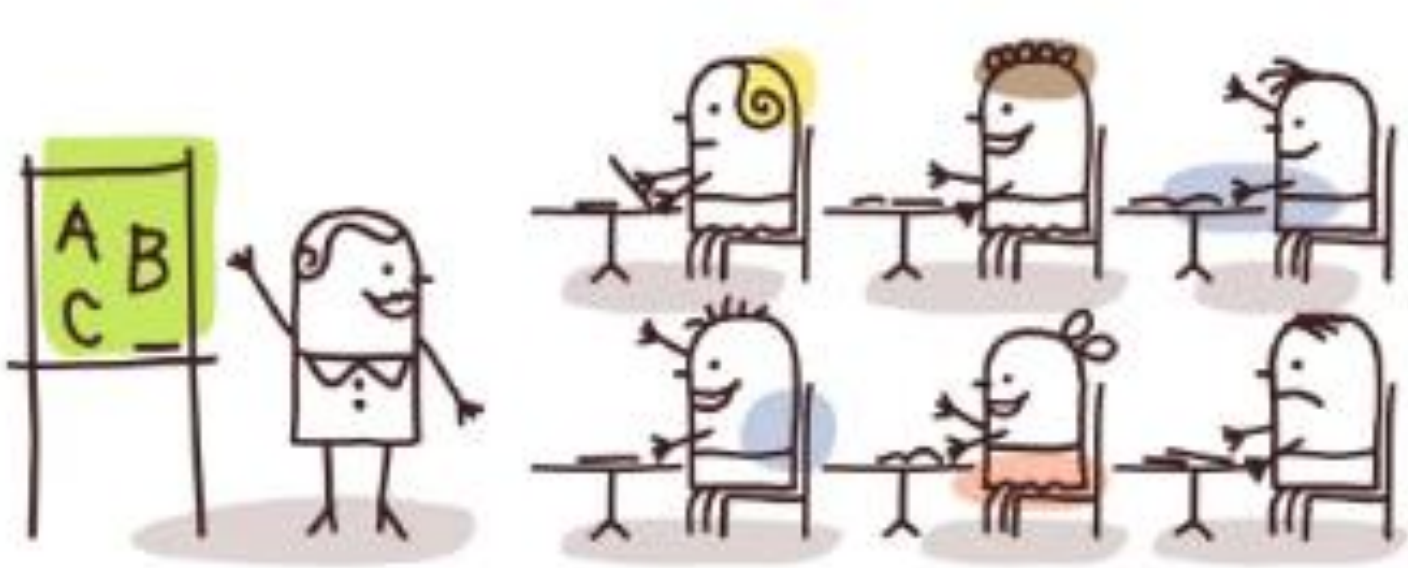


- If NML or NMH is small, gate is more susceptible to input noise
- Unskewed gates have balanced noise margins, improving resistance to random noise
- Skewed gates can favor NMH or NML depending on the dominant input noise condition
- Speed vs. noise margin is a common trade-off; higher speed often reduces noise margins

- Noise margins are relative to VDD , 0.4 V margin is good in 1.8 V process but poor in 5 V.

Summary

- Beta ratio determines the inverter's switching threshold
  - r = 1 → Balanced inverter → Vdd /2
  - r > 1 → HI-skewed (stronger pMOS) → Higher threshold
  - r < 1 → LO-skewed (stronger nMOS) → Lower threshold
- Skewing affects rise/fall times, noise margins, and power
- Adjusted by changing transistor widths
- Noise Margin defines tolerance to unwanted input voltage noise
- Larger noise margins → More reliable operation
- Unity gain point (slope = –1) defines logic levels
- Expressed relative to V_{DD} for process scaling



Thank you !

Happy Learning