Design Issues in VLSI

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Outline

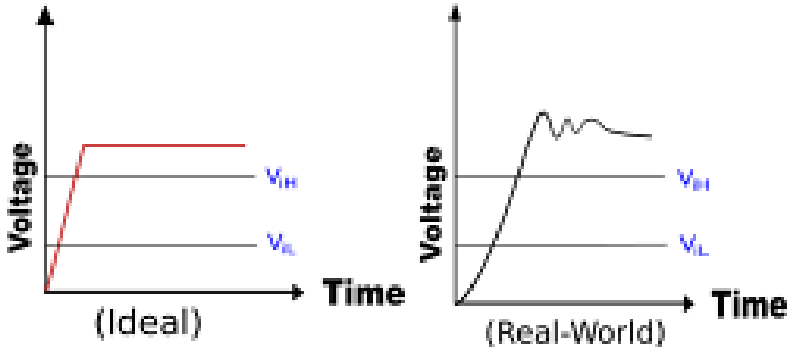
- Signal Integrity in VLSI
- Antenna Effect
- Electromigration Effect
- Body Effect
- Capacitive crosstalk
- Inductive Crosstalk
- Drain Punch-Through

Introduction

- VLSI circuits are prone to several physical design issues due to the high density of components and interconnects
- Understanding these effects is crucial for reliable, efficient, and manufacturable chips
- As technology nodes shrink, parasitic effects become more prominent and need careful handling
- Early detection of these design issues helps avoid costly re-fabrication and improves chip performance

Signal Integrity

- In digital circuits all signal are subject to noise, distortion and loss
- Signal integrity (SI) refers to the quality and reliability of electrical signals as they travel through interconnects
- It ensures correct logic values at the receiver
- Issues arise due to High frequencies, Aggressive scaling, Dense interconnects



Signal Integrity in Physical Design

Digital system SI analysis are done in three levels :

- Logic level
- Circuit level (Interconnect modeling)
- EM field level (Crosstalk, ground bounce etc.)

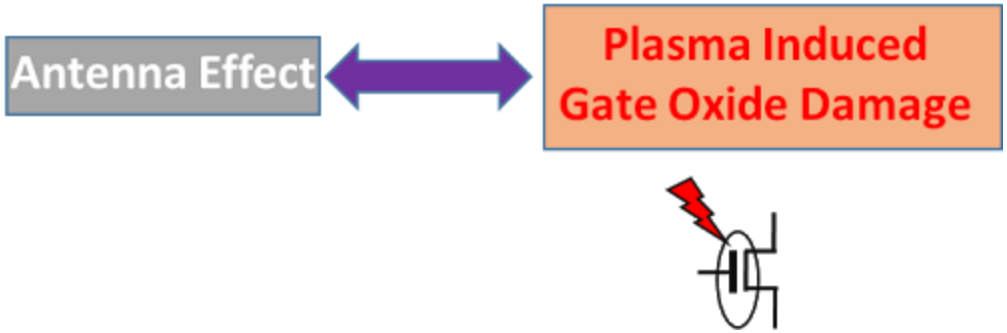
Issues concerning Signal Integrity

Major issues concerning signal integrity are

- Cross-talk Delay
- Cross-talk Noise
- Ringing & Ground bounce
- IR (voltage) drop in power lines
- Electro - migration
- Manufacturing-related issues that if not addressed can lead to chip failure (Antenna Effect)

Antenna Effect

- Antenna Effect is also called as Plasma Induced Gate Oxide Damage.
- Antenna effect arise in the intermediate steps of CMOS manufacturing process i.e. during dry etching(Plasma)
- Charge accumulation on long metal interconnects during fabrication can damage gate oxides



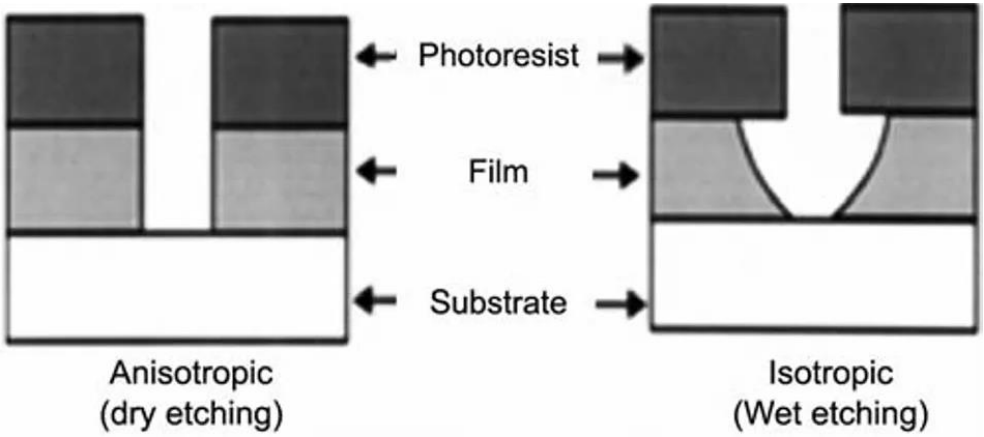
Antenna Effect – Etching

Dry Etching

- Stable gases are used for etching (Plasma, gaseous chemical)
- Anisotropic in nature i.e. it etches only in one direction
- Result : **Clean etching**

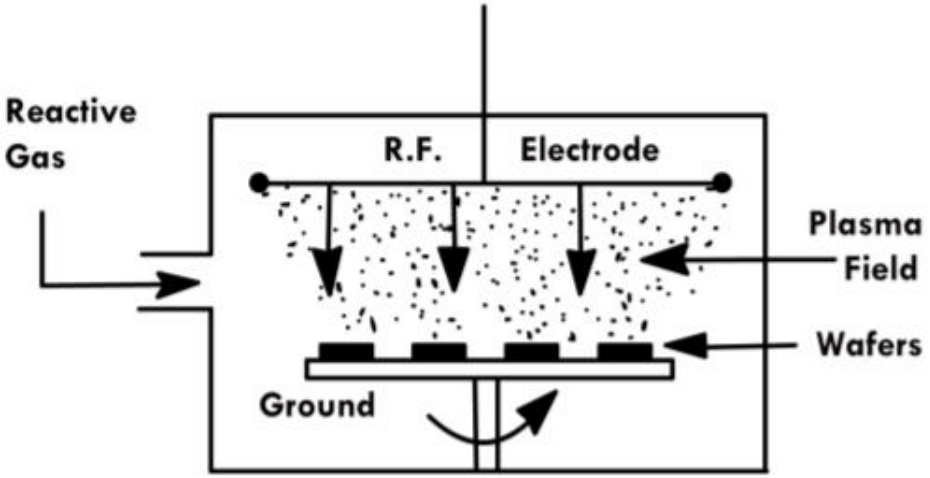
Wet Etching

- Chemicals are used for etching
- Isotropic in nature : Etches equally in both directions , vertically as well as horizontally
- Result: **Undercut**



Plasma Etching

- Utilizes plasma (ionized gas) to selectively remove material from the wafer
- Plasma is created using radio frequency (RF) voltage in a vacuum chamber
- Ions and neutral species are generated from process gases.
- These reactive species bombard the wafer, removing specific material based on mask patterns.



Antenna Effect : How it happens

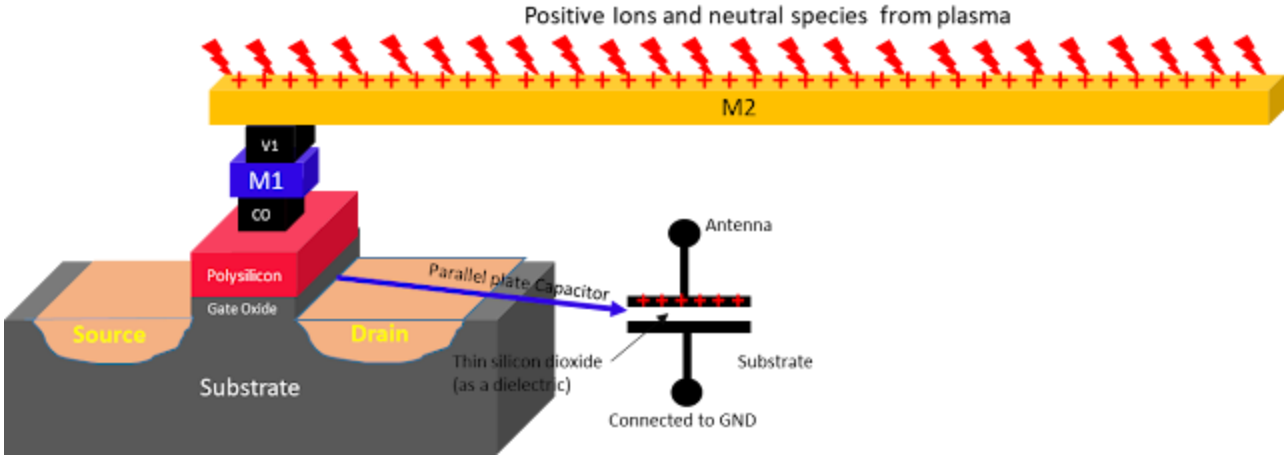
- Plasma used in etching releases charged particles (ions, electrons)
- Metal interconnects exposed to plasma collect charge
- If these interconnects are connected to a transistor gate, charge is transferred to the gate oxide
- The gate oxide is very thin and can't withstand high voltages
- Result
  - Gate oxide breakdown
  - Permanent device damage
  - Degraded performance or yield loss

Interconnects **act like antennas**, collecting charge from plasma (not radio signals)

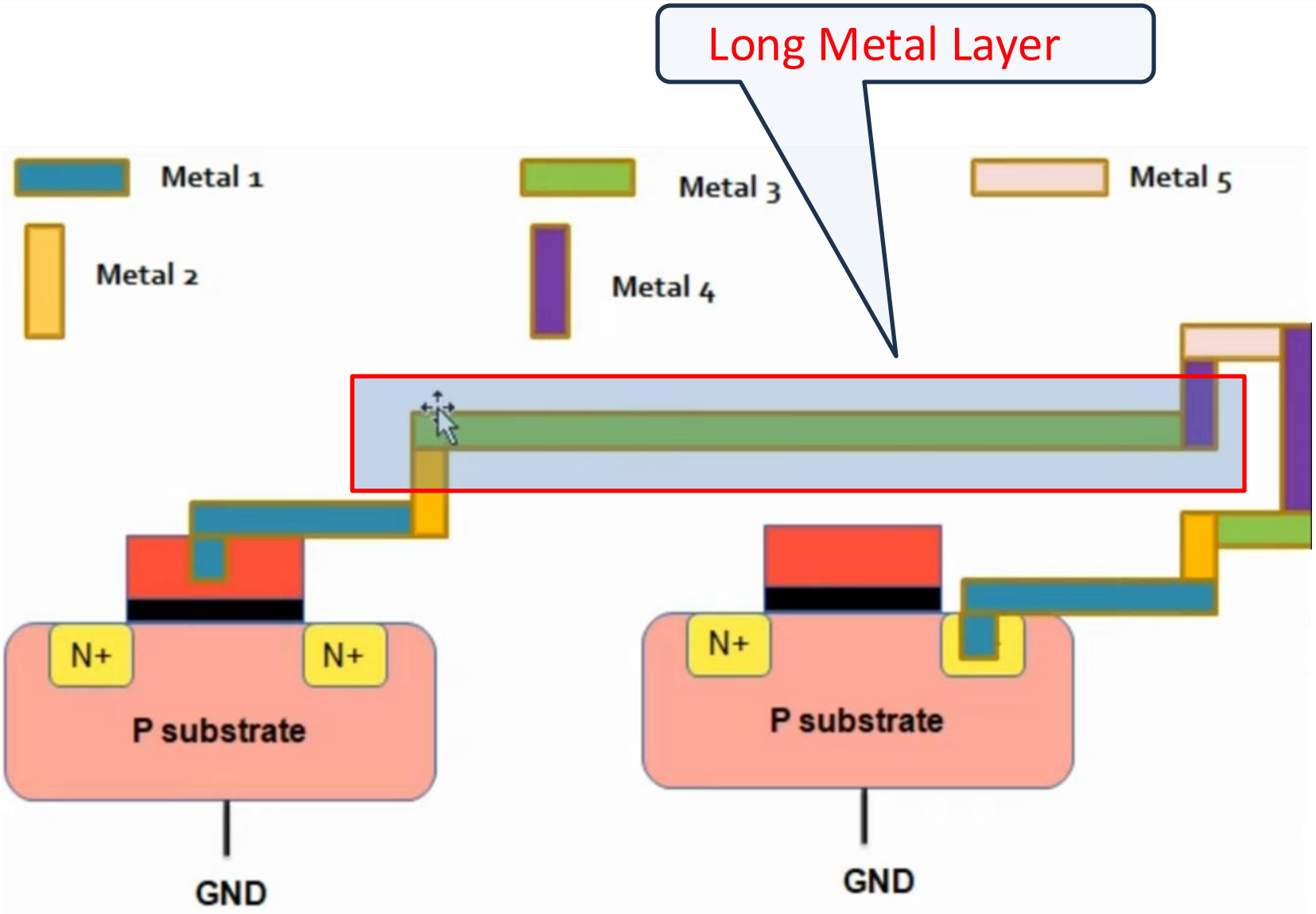
Antenna Effect : Antenna Ratio

$$\text{Antenna Ratio} = \frac{\text{Area of Metal connected to Gate}}{\text{Area of Gate}}$$

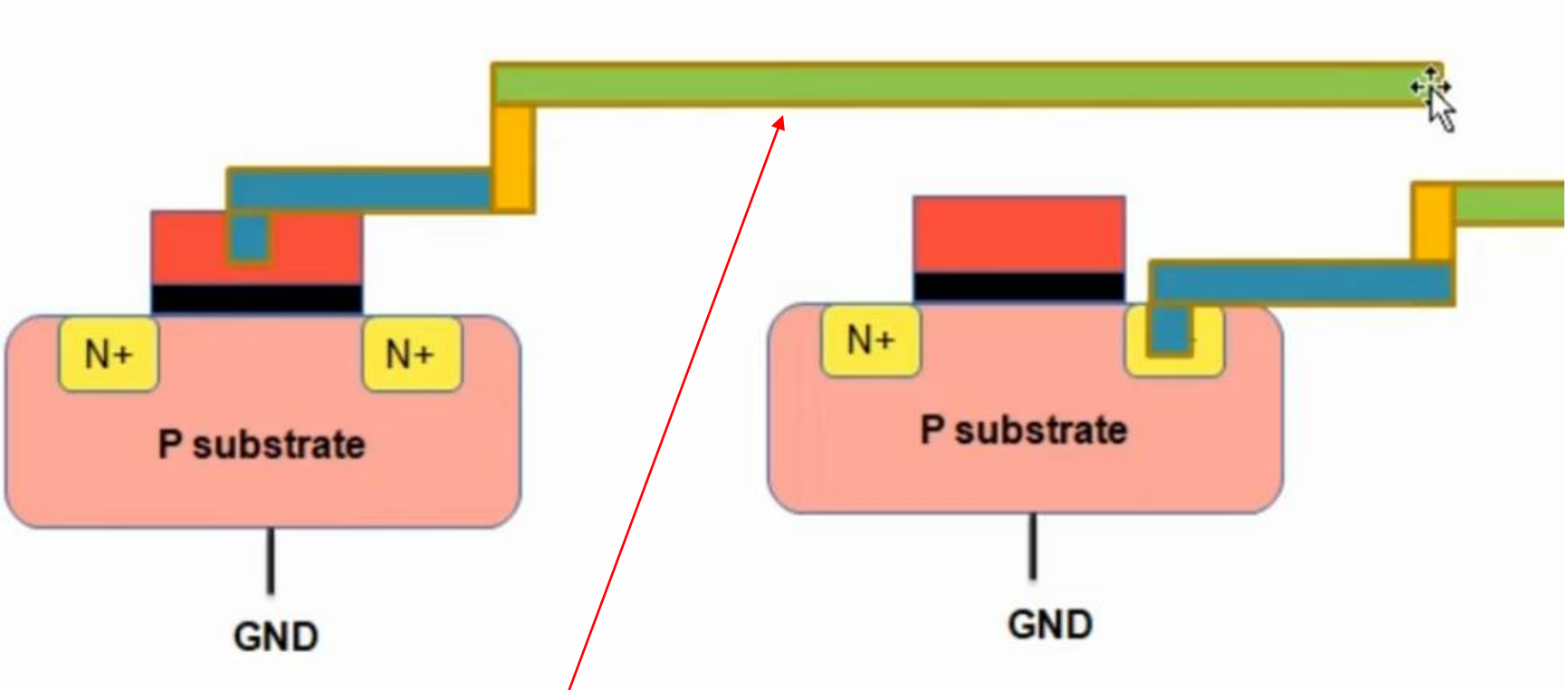
Higher ratio = greater risk of antenna effect.



Antenna Effect : Causes



Antenna Effect : Causes



- Metal layer 3 is long (accumulate the charges , causing antenna violation)
- There is no discharge path , charges will discharge through Gate, and damage the gate

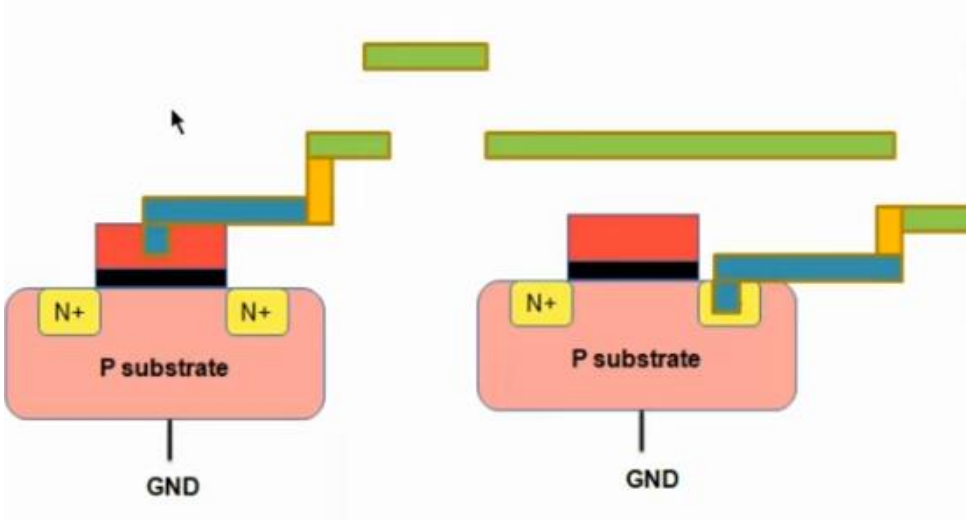
Method to Resolve Antenna Effect (Jumpers)

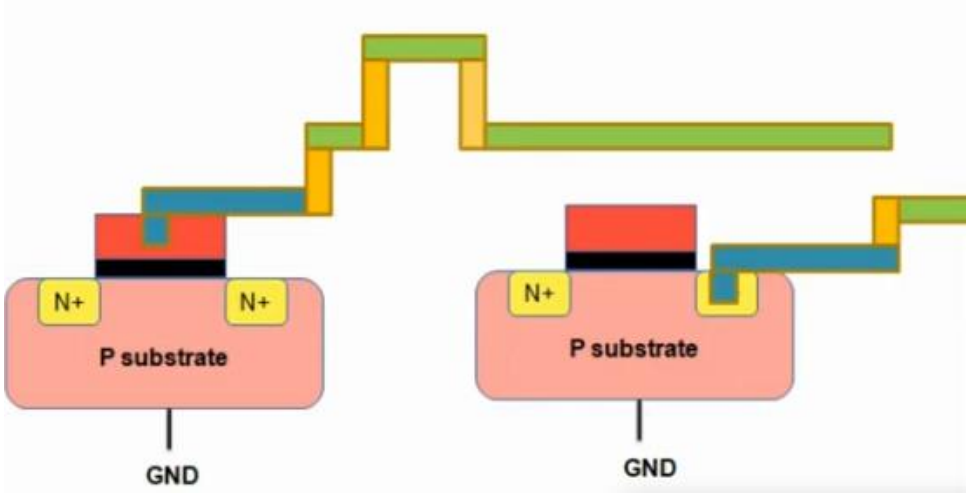
Metal Jumpers

Add Metal Jumper in higher metal layers

Ex: Metal 3 is broken and jumper is adder in layer 4

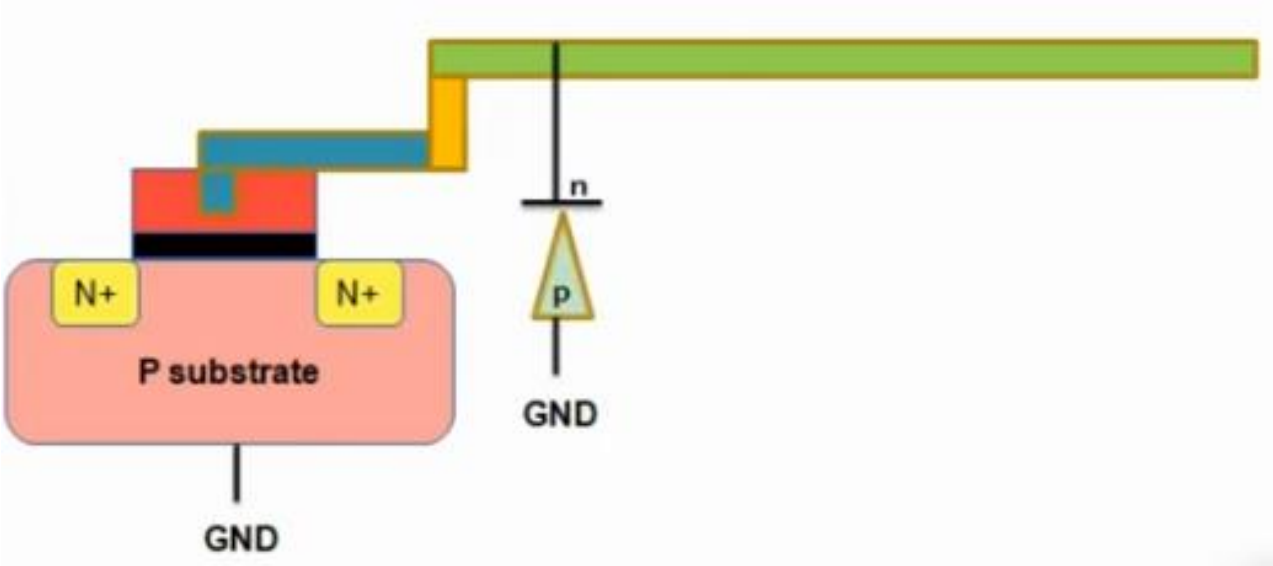
Metal jumper are always added at higher layers





Methods to resolve Antenna Violation (Diode)

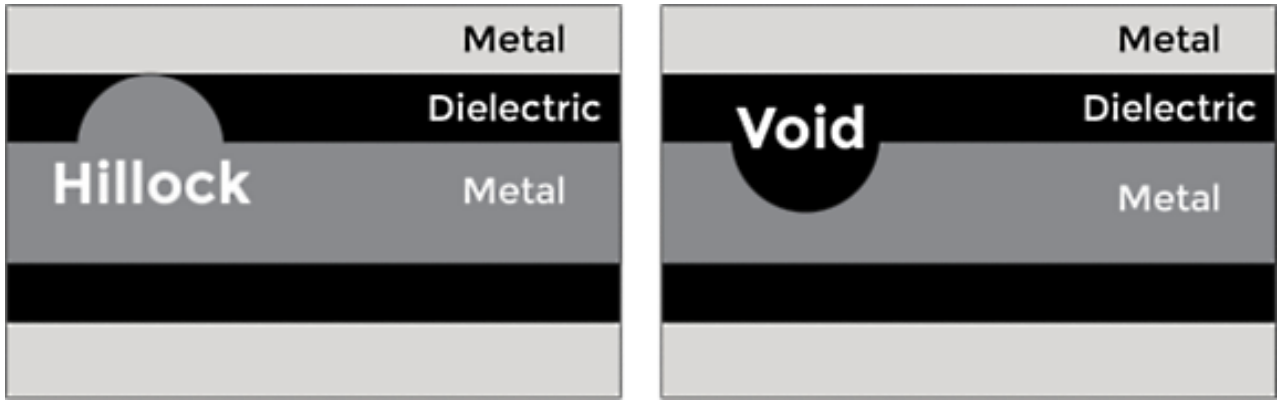
- Add reverse biased diode near the gate



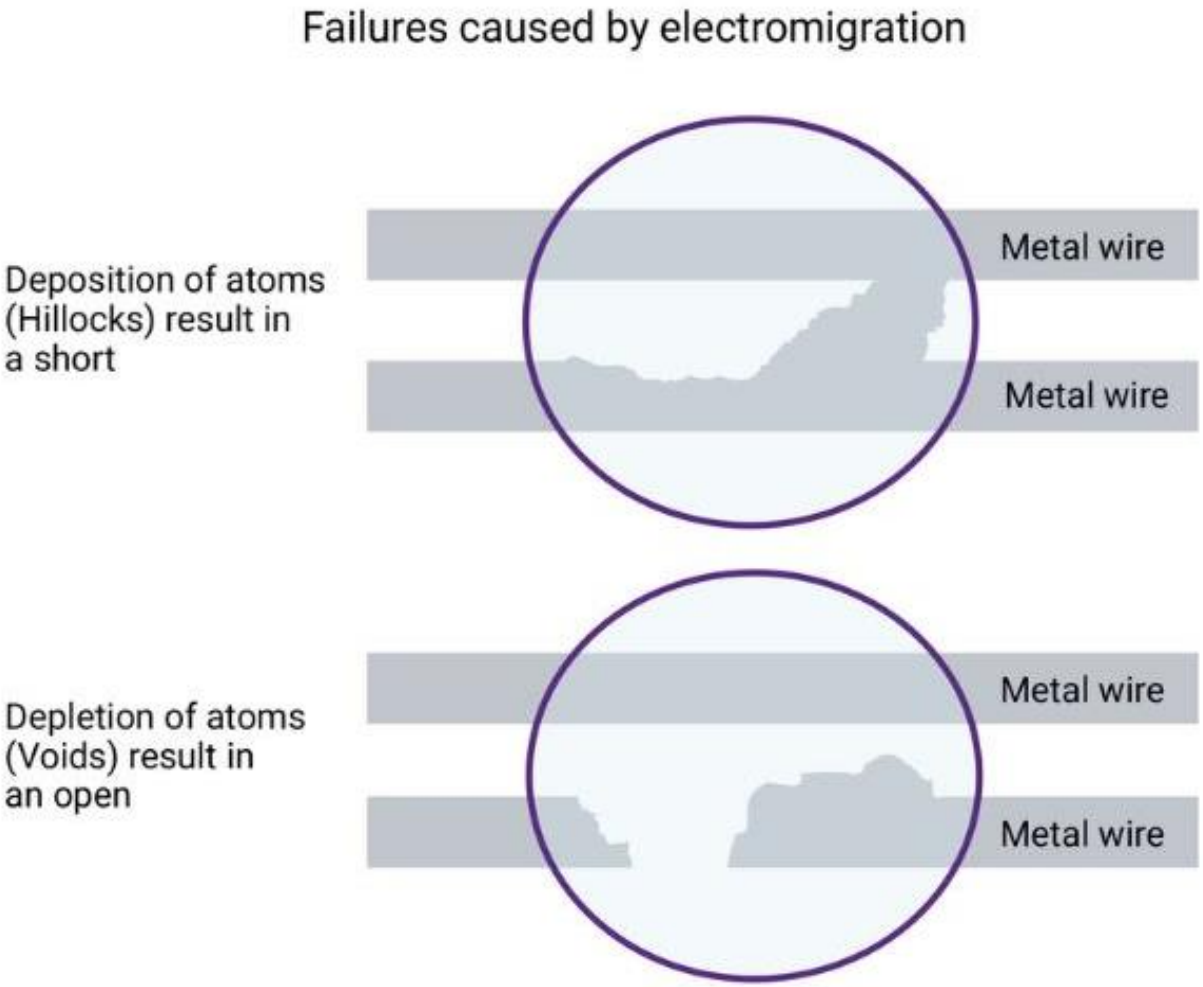
- Forward biased diode is not used as it hampers normal operation (normally design work at low voltages)

Electromigration Effect

- Electromigration is the transport of material caused by the momentum transfer from electrons to metal atoms.
- High current density → momentum transfer → atom displacement
- Occurs mostly in metal interconnects (Al, Cu)
- Causes voids and hillocks in metal lines
- Leads to open circuits (failure) or short circuits
- Reduces lifetime and reliability of ICs.



Electromigration Effect



Mitigate the Effects of Electromigration

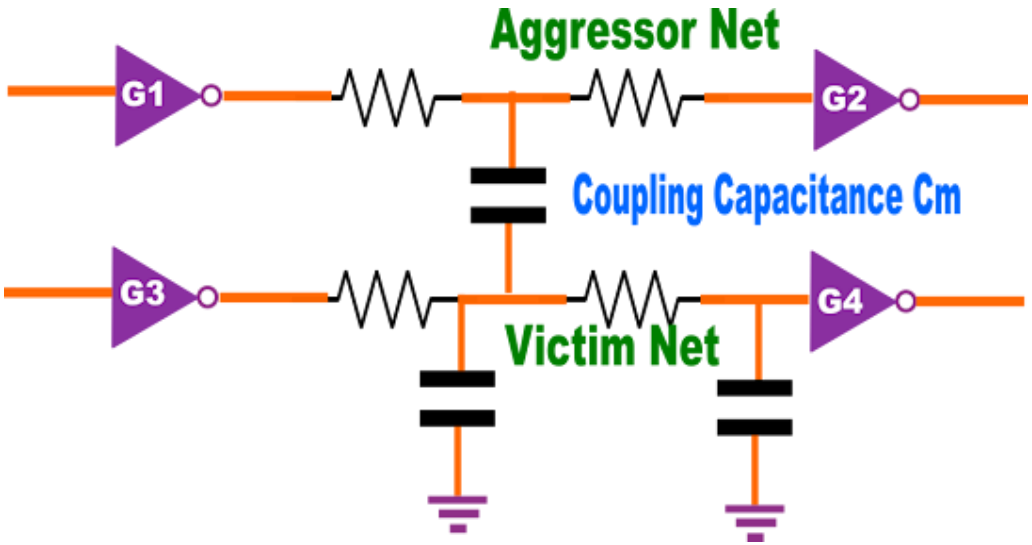
- Increasing interconnect width to reduce current density.
- Using materials with high electromigration resistance, such as gold and copper.
- Diverting current intensity using redundant vias.
- Decreasing spacing between interconnects.
- Designing the circuit for lower voltage levels

Crosstalk

- Unintended coupling between signal lines due to electromagnetic interference
  - Capacitive Crosstalk (electric field)
  - Inductive Crosstalk (magnetic field)

Capacitive Crosstalk

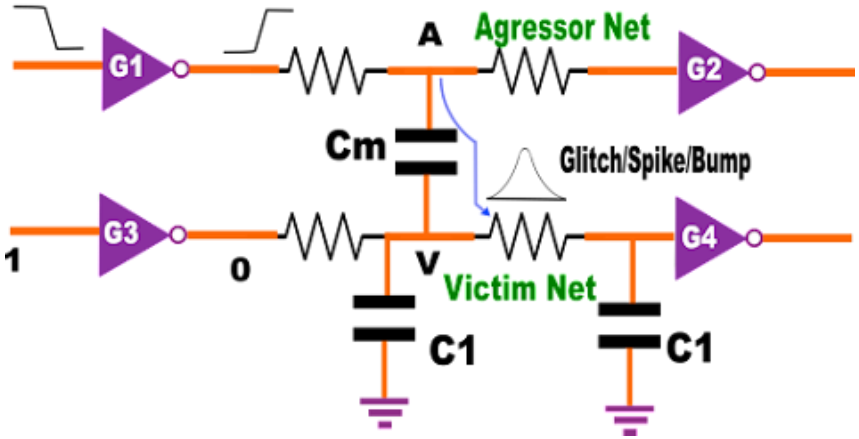
- Capacitive Crosstalk is the undesired coupling of signals between adjacent interconnects due to parasitic capacitance
- It can cause timing errors, logic glitches, or signal integrity issues in high-speed digital circuits



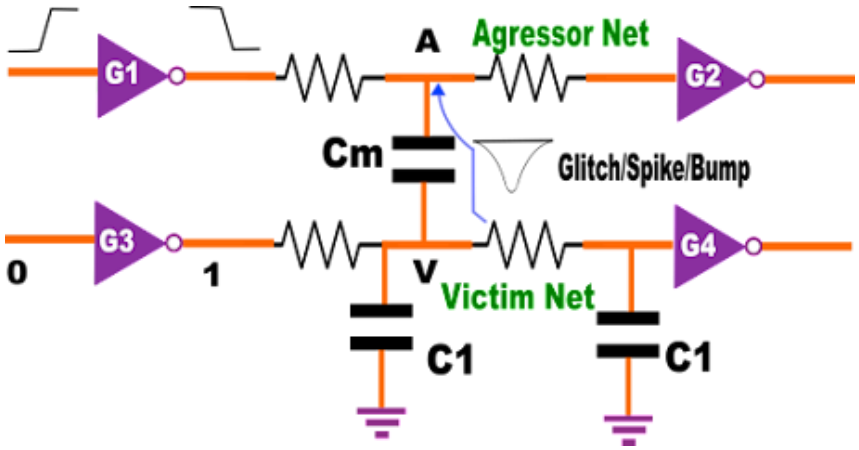
Cross-talk has two effects : Cross-talk Noise & Cross-talk Delay

Cross-talk Noise/Cross-talk Glitch

- Signal transition in aggressor causes a noise bump or glitch on victim net. This in known as cross-talk noise
- Cross-talk noise/glitch/bump occurs when aggressor net switches and the victim nets remain in a steady state



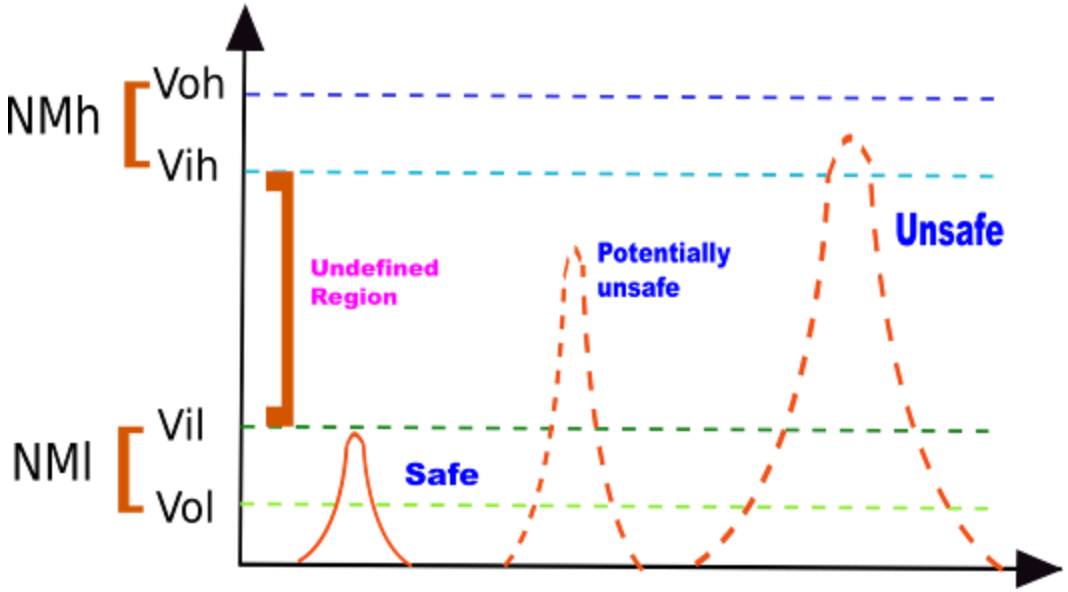
Rise Glitch



Fall Glitch

Range of Safe/Unsafe Glitch

- **Safe Glitch** : Has no effect on logic state of victim net.
- Glitch height < Noise Margin Low (NML), a safe glitch.
- Glitch height > Noise Margin High (NMH), a **unsafe glitch.**
- NML < Glitch Height < NMH , an **unpredictable case**

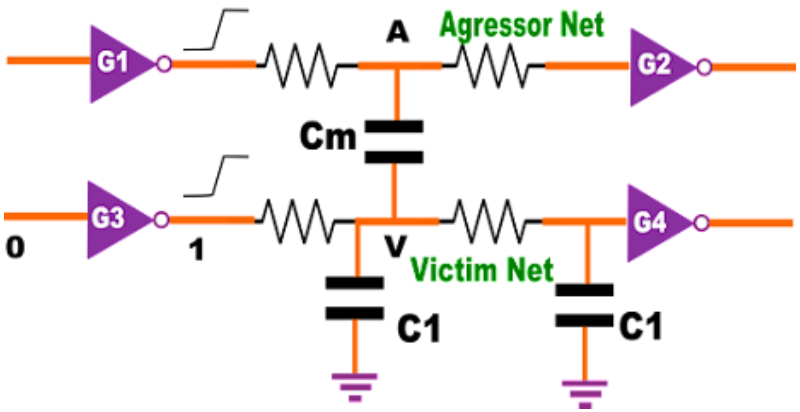


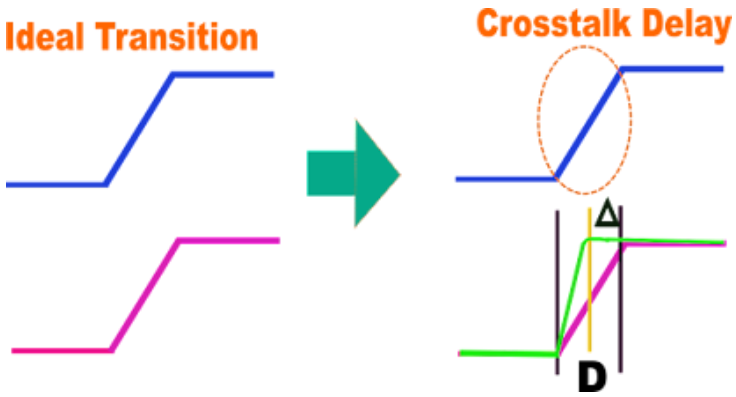
Cross-talk Delay/Cross-talk Delta Delay

- Signal transition in aggressor create delay in the output transition of victim. This is known as cross-talk delay
- Cross-talk delay occurs when both aggressor and victim nets switch together
- There are two types of cross-talk delay:
  - Negative Crosstalk Delay
  - Positive Crosstalk Delay

Negative Cross-talk Delay

- Aggressor and victim nets switch in the same direction

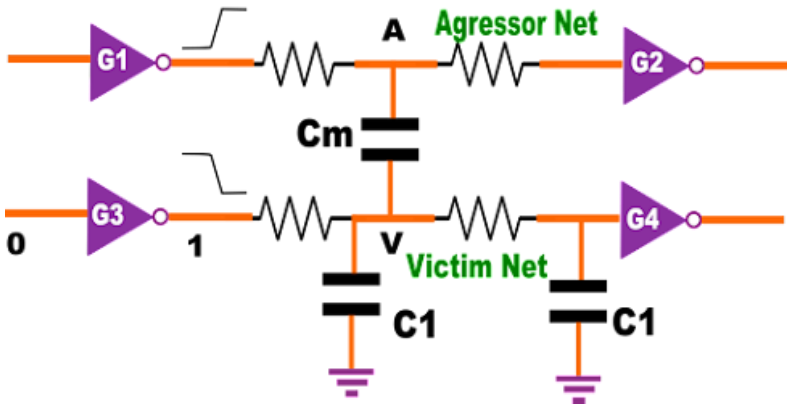


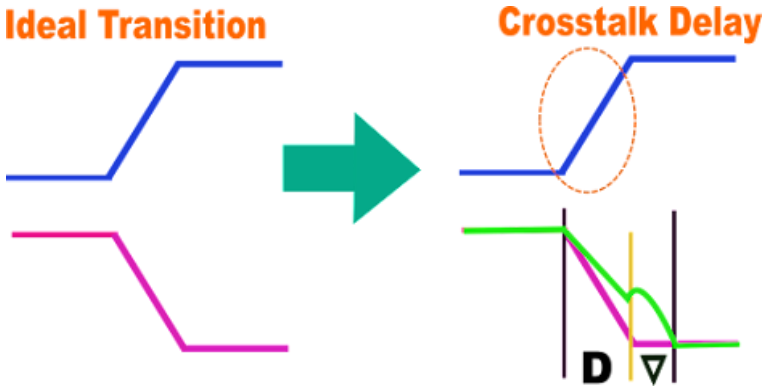


- If aggressor has higher driving strength, transition will happen faster.
- A potential difference from node A to V will be developed.
- Node A will try to pull up the victim node
- Transition of the victim node will have a bump.
- Victim net will reach from 0 to 1 earlier and transition time will decrease.
- Cross-talk will be decrease the delay by Δ and the new delay will be (D – Δ).

Positive Cross-talk Delay

- Aggressor and victim nets switch in the Opposite direction

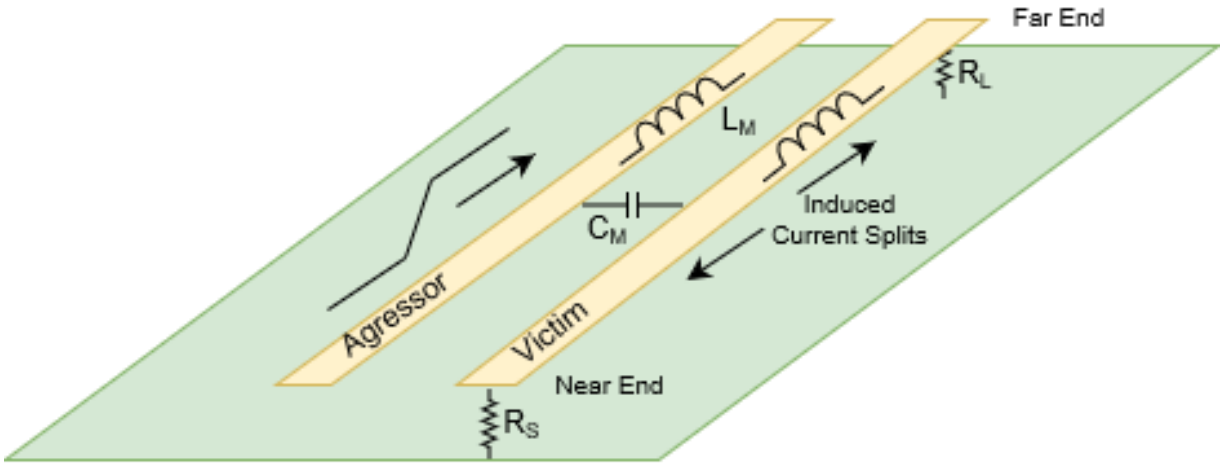




- Aggressor net and node A switches from 0→ 1.
- Victim net or node V switches from 1→ 0.
- There will be a potential difference from node A to V.
- Node A will try to pull up node V.
- There will be a bump in victim net waveform.
- Transition of the victim node will have a bump.
- Victim net will take longer time to reach from 1 to 0.
- Transition time will increase

Inductive Crosstalk

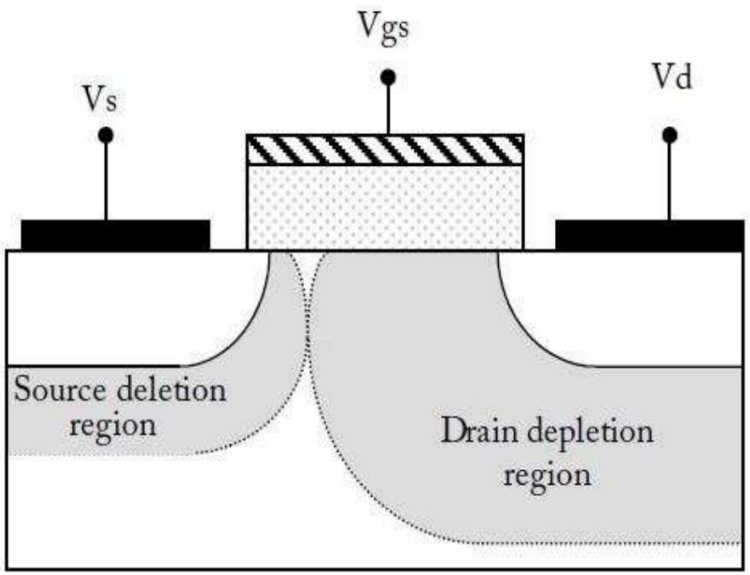
- Inductive crosstalk is the unintended electromagnetic coupling between nearby conductors due to changing magnetic fields
- Occurs when a time-varying current in one wire induces a voltage in a nearby wire through mutual inductance.



Drain Punch-Through

- Occurs in short-channel MOSFETs
- Depletion region of drain extends toward source as channel length decreases
- At very short lengths, drain and source depletion regions merge
- This allows leakage current to flow even when gate voltage is below threshold
- Causes loss of gate control, degrading device performance
- Leads to higher off-state current and power consumption.

Drain Punch-Through



- Schematic diagram for punch through. When we drain is a High enough voltage with respect to the source, the depletion region around the drain may extend to the source, causing current to flow irrespective of gate voltage

Body Effect

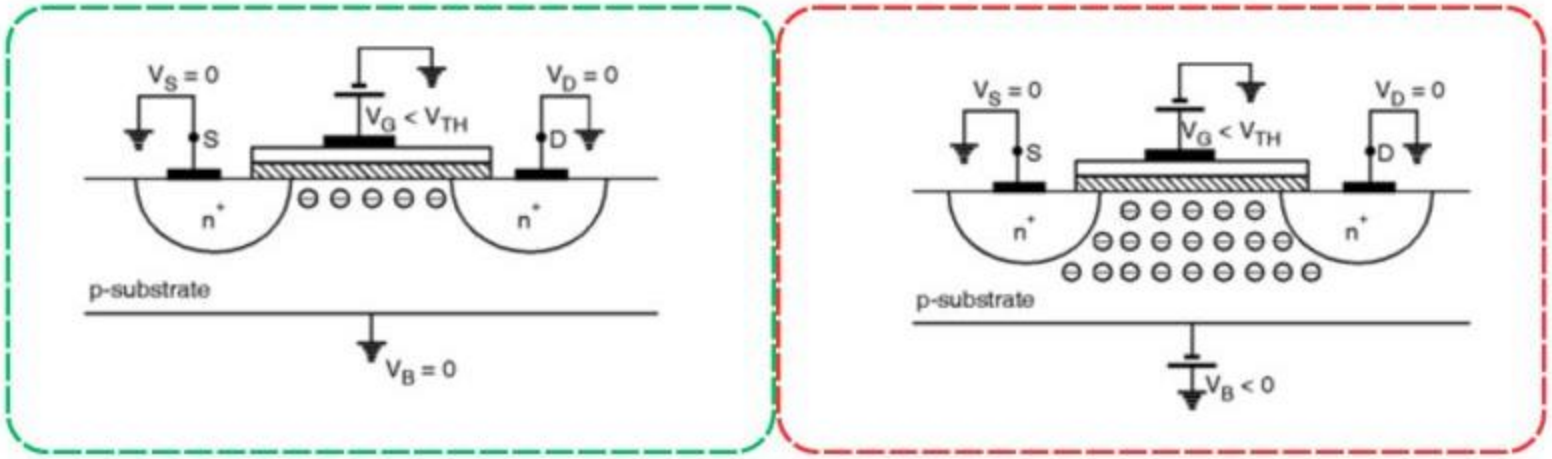
- Threshold Voltage is minimum voltage Vgs required to form a inversion layer (Channel) in source and drain
- Threshold voltage determines the operation of MOSFET
- If Vgs is less than threshold voltage MOSFET stays in cutoff
- Due to voltage at substrate(Body), threshold voltage changes, it is called as Body Effect

Body Effect

$$V_{th} = V_{th0} + \gamma \left(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|} \right)$$

- V_{th0}: Threshold voltage at zero V_{SB}
- γ: Body effect coefficient
- V_{SB}: Source-to-body voltage
- ϕ_F: Fermi potential

- **For NMOS:**
  - $V_{SB} > 0 \Rightarrow V_{th} \uparrow$
- **For PMOS:**
  - $V_{SB} < 0 \Rightarrow |V_{th}| \uparrow$
- Higher threshold → **reduced current drive, slower switching**



No Body Effect **Body Effect**

Thank you !

Happy Learning