Power

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Outline

- Power Definitions
- Inverter power dissipation
- Sources of Power dissipation
- Conclusion

Introduction

- The ***Instantaneous Power P (t)*** consumed or supplied by a circuit element is the product of the current through the element and the voltage across the element

$$P(t) = I(t)V(t)$$

- The ***Energy*** consumed or supplied over some time interval T is the integral of the instantaneous power

$$E = \int_0^T P(t)dt$$

- The ***Average Power*** over this interval

$$P_{\text{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt$$

Introduction

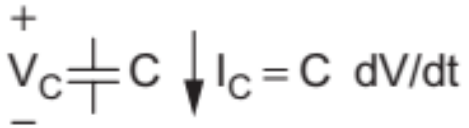
- The ***Instantaneous Power P (t)*** *dissipated in the resistor*

$$P_R(t) = \frac{V_R^2(t)}{R} = I_R^2(t)R$$

- Power proportional to its current

$$P_{VDD}(t) = I_{DD}(t)V_{DD}$$

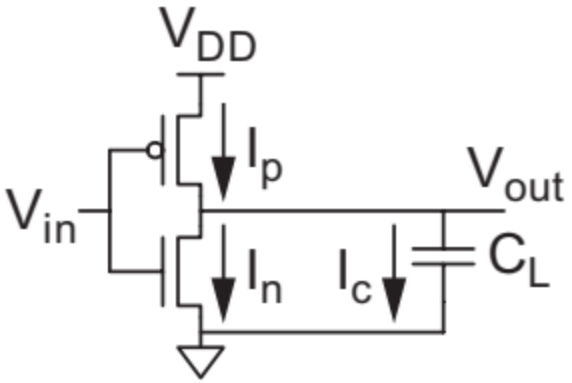
- Capacitor Energy charge and discharge



$$E_C = \int_0^{\infty} I(t)V(t)\,dt = \int_0^{\infty} C\frac{dV}{dt}V(t)\,dt = C\int_0^{V_c} V(t)\,dV = \tfrac{1}{2}CV_C^2$$

Inverter

- Energy Stored in Capacitor

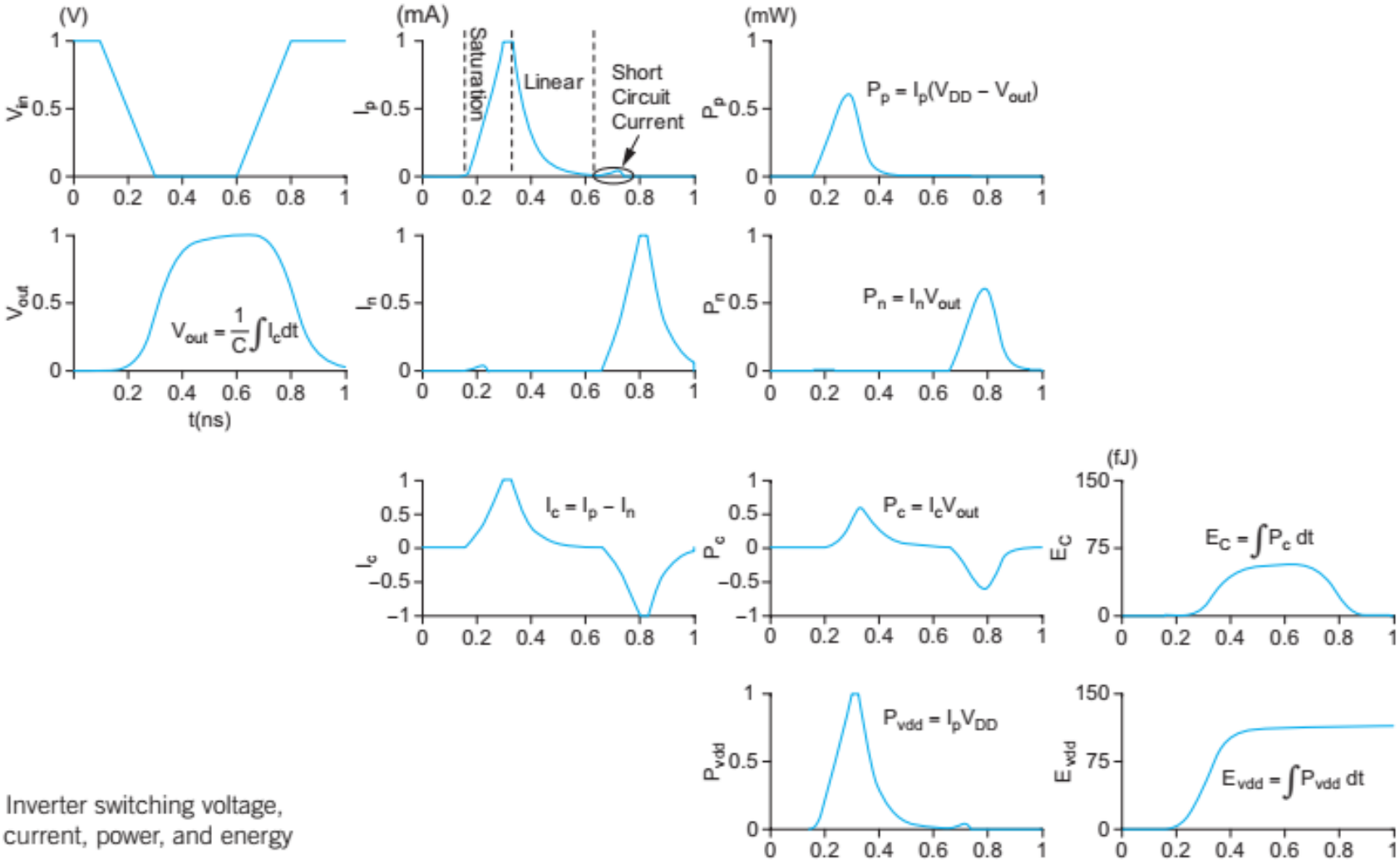


$$E_C = \frac{1}{2} C_L V_{DD}^2$$

- Energy delivered from the power supply

$$E_C = \int_0^{\infty} I(t) V_{DD} dt = \int_0^{\infty} C \frac{dV}{dt} V_{DD} dt = C V_{DD} \int_0^{V_{DD}} dV = C V_{DD}^2$$

Inverter Switching



Inverter switching voltage, current, power, and energy

Switching Frequency

- Gate switches at some average frequency f_{sw}

$$P_{\text{switching}} = \frac{E}{T} = \frac{Tf_{\text{sw}}CV_{DD}^2}{T} = CV_{DD}^2 f_{\text{sw}}$$

- This is called the *dynamic power* because it arises from the switching of the load
- Most gates do not switch every clock cycle, it is often more convenient to express switching frequency f_{sw} as an activity factor α times the clock frequency f

$$P_{\text{switching}} = \alpha CV_{DD}^2 f$$

Sources of Power Dissipation

Power dissipation in CMOS circuits comes from two components:

Dynamic dissipation due to

- *charging and discharging* load capacitances as gates switch
- "*short-circuit*" current while both pMOS and nMOS stacks are partially ON

Static dissipation due to

- subthreshold leakage through OFF transistors
- gate leakage through gate dielectric
- junction leakage from source/drain diffusions
- contention current in ratioed circuits
- Putting this together gives the total power of a circuit

Total Power Dissipation

Total Power dissipation

$$P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{short circuit}}$$

$$P_{\text{static}} = \left(I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}}\right)V_{DD}$$

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}}$$

Power can also be considered in active, standby, and sleep modes

Total Power Dissipation

Active Power

- Power consumed while the chip is doing useful work

Standby power

- Power consumed while the chip is idle
- If clocks are stopped and ratioed circuits are disabled, the standby power is set by leakage

Sleep mode

- the supplies to unneeded circuits are turned off to eliminate leakage

Activity Factor

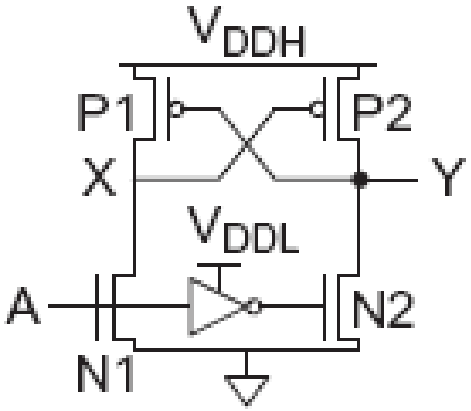
- If a circuit can be turned off entirely, the activity factor and dynamic power go to zero
- Blocks are typically turned off by stopping the clock; this is called *clock gating*
- When a block is on, the activity factor is 1 for clocks and substantially lower for nodes in logic circuits
- The activity factor of a logic gate can be estimated by calculating the switching probability.
- Glitches can increase the activity factor

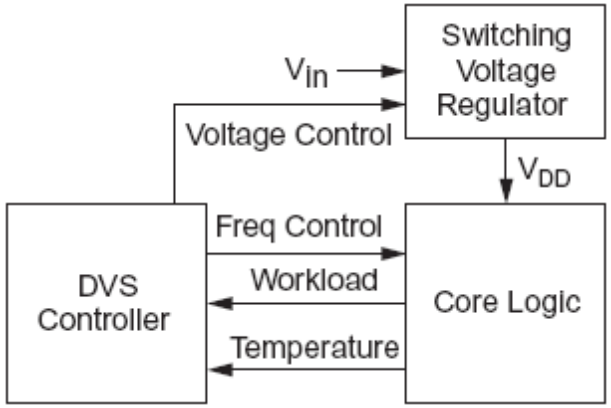
Capacitance

- ***Gate capacitance***
  - Fewer stages of logic
  - Small gate sizes
- ***Wire capacitance***
  - Good floorplanning to keep communicating blocks close to each other
  - Drive long wires with inverters or buffers rather than complex gates

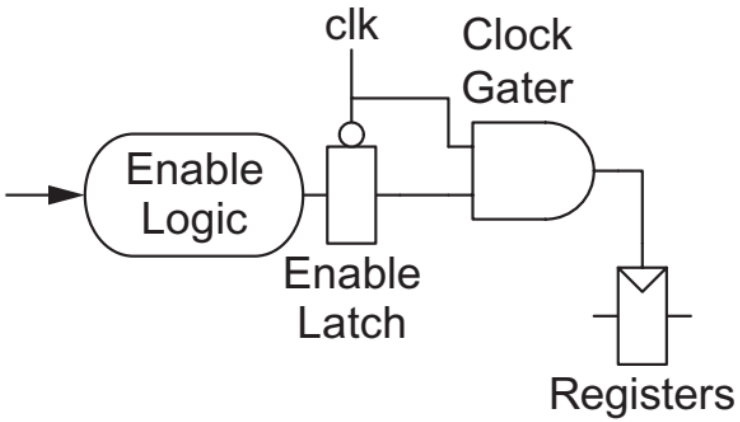
Voltage / Frequency

- *Run each block at the lowest possible voltage and frequency that meets performance requirements*
- *Voltage Domains*
  - *Provide separate supplies to different blocks*
  - *Level converters required when crossing from low to high VDD domains*
- *Dynamic Voltage Scaling*
  - *Adjust VDD and f according to workload*





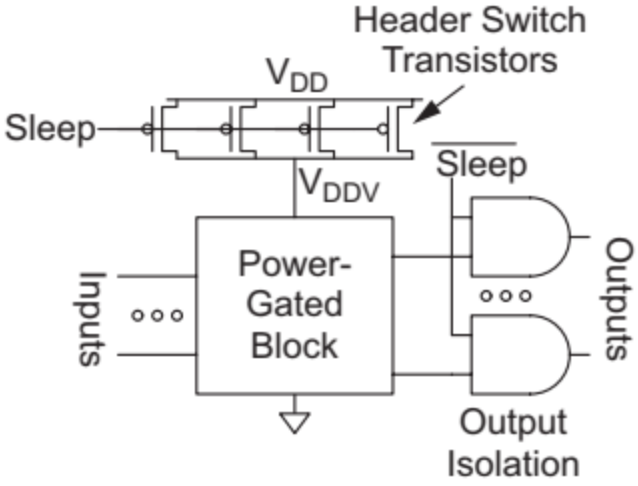
Clock Gating



- Clock gating ANDs a clock signal with an enable to turn off the clock to idle blocks
- It is highly effective because the clock has a high activity factor
- Gating the clock to the input registers of a block prevents the registers from switching and stops all the activity

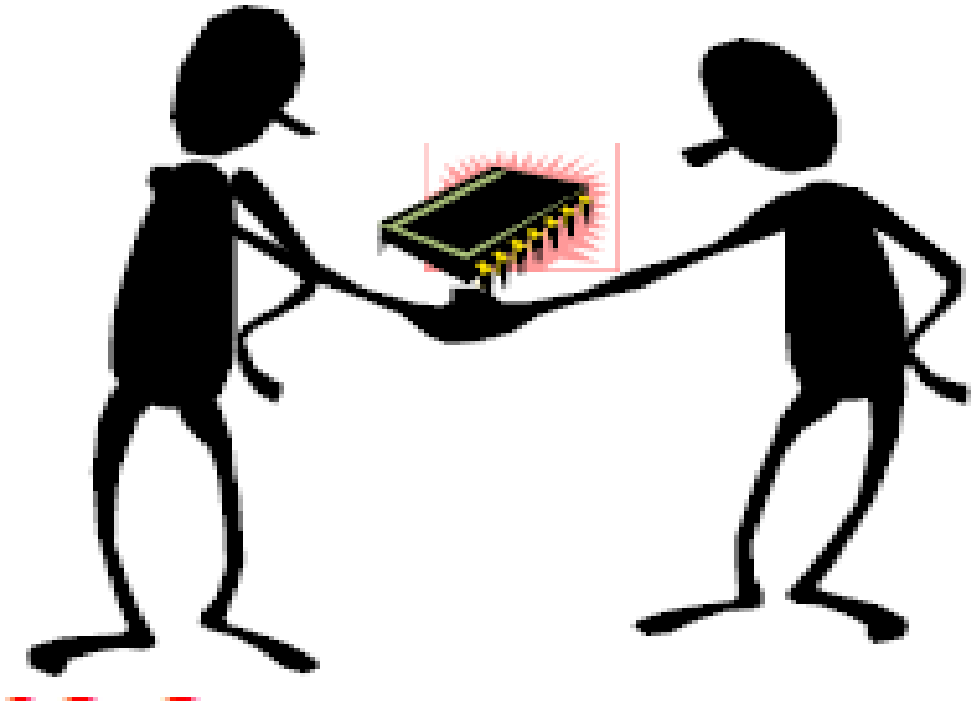
Power Gating

- Turn OFF power to blocks when they are idle to save leakage
  - Use virtual V_{DD} (V_{DDV})
  - Gate outputs to prevent invalid logic levels to next block
- Voltage drop across sleep transistor degra performance during normal operation
  - Size the transistor wide enough to minimize impact
- Switching wide sleep transistor costs dynamic power
  - Only justified when circuit sleeps long enough



Conclusion

- Higher frequency and activity at nodes lead to increased dynamic power.
- Higher load capacitance results in greater energy per transition
- Reducing Vdd is one of the most effective ways to lower power
- Clock Gating and Power Gating: Reduces unnecessary switching and leakage in inactive sections
- Multi-Voltage Domains: Allows selective scaling of voltage for different circuit sections to save power without impacting performance
- Reducing power often comes with trade-offs in speed, area, and design complexity



Thank you !

Happy Learning