# Assignments

Design following CMOS Circuits using Xschem Schematic Circuit Design, Draw Layout with clean DRC errors and perform LVS check

1. Inverter
2. NAND Gate
3. NOR Gate
4. XOR Gate
5. Compound Gate (Any Expression)

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Following documents are expects in the submission

**Simulation :**

- Proper Circuit schematic in Xschem
- SPICE Netlist from Xschem
- Simulation Waveforms

**Layout**

- Stick Diagram
- Layout with clear DRC
- Testbench

LVS

**Xschem SPICE netlist without testbench**

- remove voltage source, pulse sources, code shown
- Attach ipin and opin at appropriate location ( ex. Vdd, Gnd, Input, Output )

**Magic Extracted Netlist**

- Extract the netlist from the magic

Compare netlist using **Netgen** and submit the assignment