CMOS Basics

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Outline

- Introduction
- Benefits of Integration
- Why CMOS ?
- CMOS Gate Design
- Compound Gate Design

Introduction

- VLSI refers to the process of creating integrated circuits (ICs) by combining thousands to millions of transistors on a single chip

Key features

- **High Complexity**: Enables the integration of complex circuits
- **Low Power Consumption:** Optimized for power efficiency in modern devices
- **Miniaturization:** Small, compact ICs with powerful functionality

Benefits of Integration

Benefits

- **Increased Performance:** Greater speed and functionality
- **Cost Efficiency:** Reduces manufacturing costs as circuits are smaller
- **Energy Efficiency:** Reduced power consumption in devices

Challenges

- **Design Complexity:** As transistor counts increase, design and verification become harder
- **Heat Dissipation:** Managing heat in densely packed chips.

Why Study CMOS ?

- Low Power Dissipation
- High Integration Density
- CMOS gates allow rail-to-rail output logic voltage swings
- Rail-to-rail swings provide better noise immunity and aid in designing reliable logic circuits
- Symmetrical Transient Response
- Merger of bipolar with CMOS (Speed)

Why Silicon CMOS ?

- **Abundance:** Silicon is the second most abundant element on Earth **(Gallium Arsenide does not occur naturally**)
- **Semiconductor Properties:** Exhibits both insulator and conductor properties, making it ideal for switching operations in transistors.
- **Technology Know-How:** Silicon is the best studied element on earth

Semiconductor Properties

Carriers (Electrons and Holes)

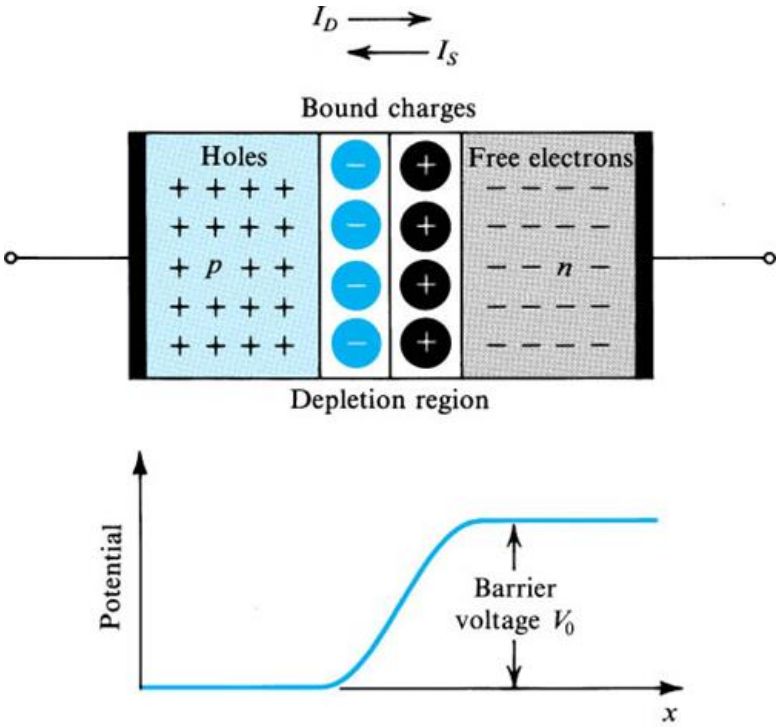
- **Electrons** are negatively charged particles, and **holes** are positively charged vacancies created when electrons move

Intrinsic vs. Extrinsic Silicon

- **Intrinsic Silicon:** Pure silicon with equal numbers of electrons and holes, having limited conductivity.
- **Extrinsic Silicon:** Doped with impurities to enhance conductivity
  - **n-type:** Doped with elements like phosphorus, adding extra electrons (negative charge carriers).
  - **p-type:** Doped with elements like boron, creating more holes (positive charge carriers).

P-N Junction

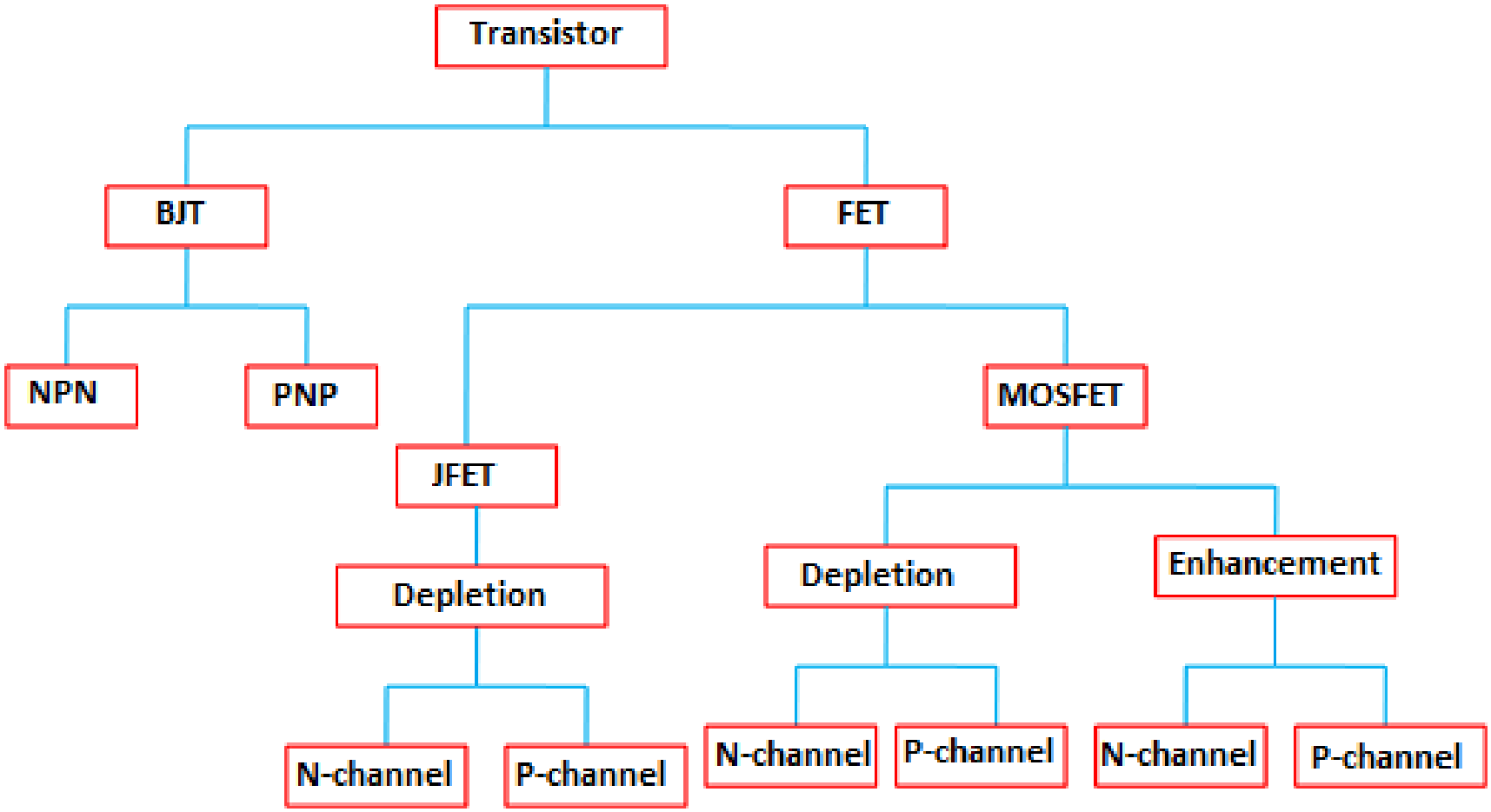
- **PN junction** is formed when a p-type semiconductor **(rich in holes)** and an n-type semiconductor **(rich in electrons)** are joined together



- Depletion region **decreases** in width as more charge carriers move across the junction
- Depletion region increases in width as charge carriers are pulled away from the junction

Modulation of the depletion region to control current flow

Transistor

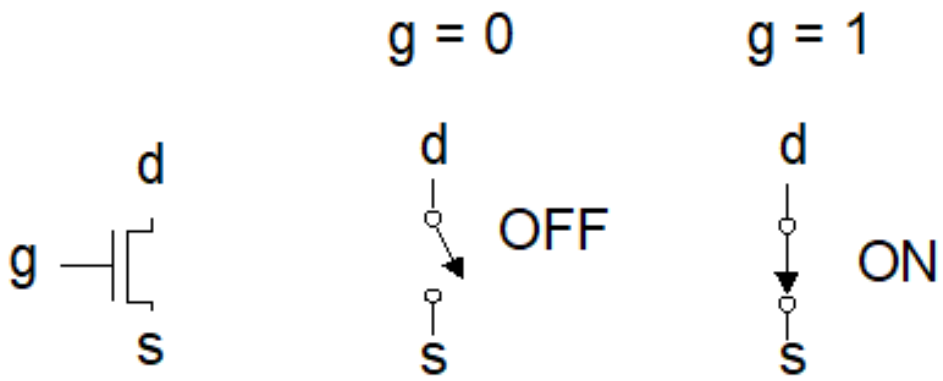

Transistor
BJT
FET
NPN
PNP
JFET
MOSFET
Depletion
Depletion
Enhancement
N-channel
P-channel
N-channel
P-channel
N-channel
P-channel

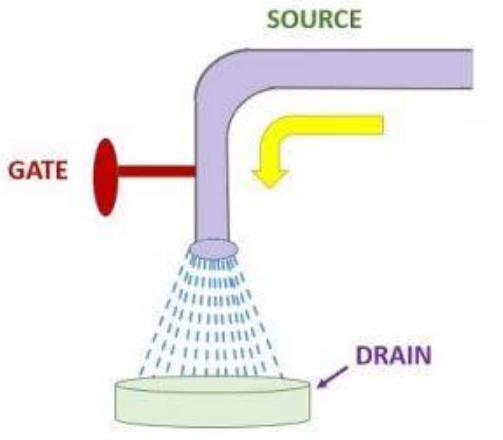
CMOS

- CMOS stands for Complementary Metal-Oxide-Semiconductor
- It is a widely used technology for building integrated circuits (ICs)
- CMOS transistors include n-channel (NMOS) and p-channel (PMOS) MOSFETs, working together
- Offers low power consumption by only drawing power during switching
- Essential for VLSI (Very Large Scale Integration), used in microprocessors, memory chips, and digital logic circuits

NMOS (N-Channel MOSFET)

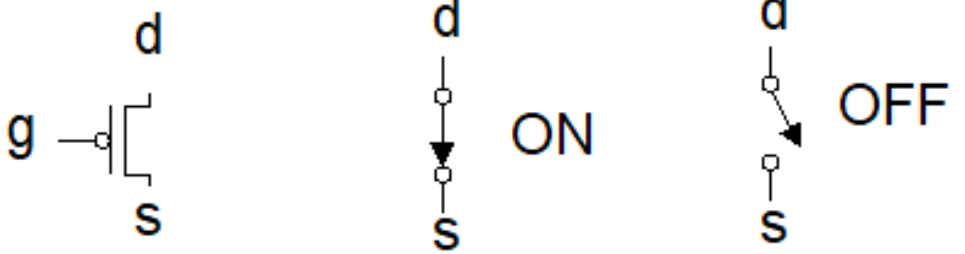
- Carries electrons as the primary charge carriers
- Gate voltage turns the transistor ON by attracting electrons, forming a conductive channel
- Faster than PMOS due to higher electron mobility

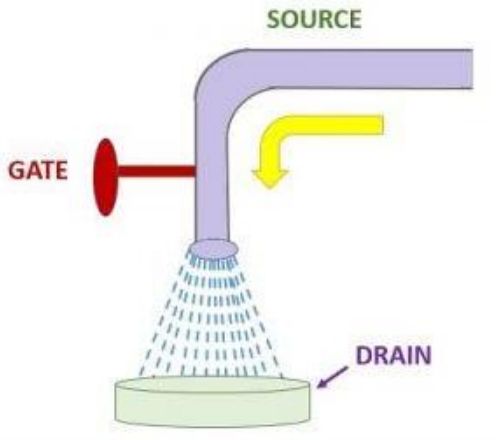




PMOS (P-Channel MOSFET)

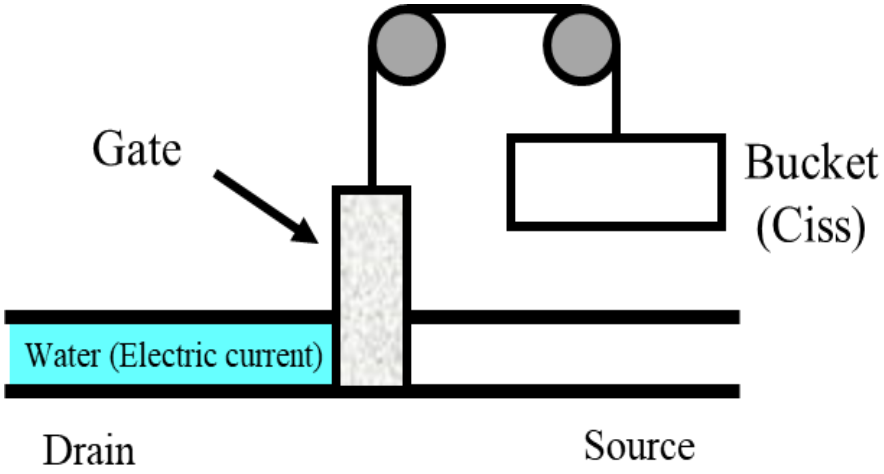
- Carries holes as the primary charge carriers
- Gate voltage turns the transistor ON by attracting holes, forming a conductive channel
- Slower than NMOS due to lower hole mobility.



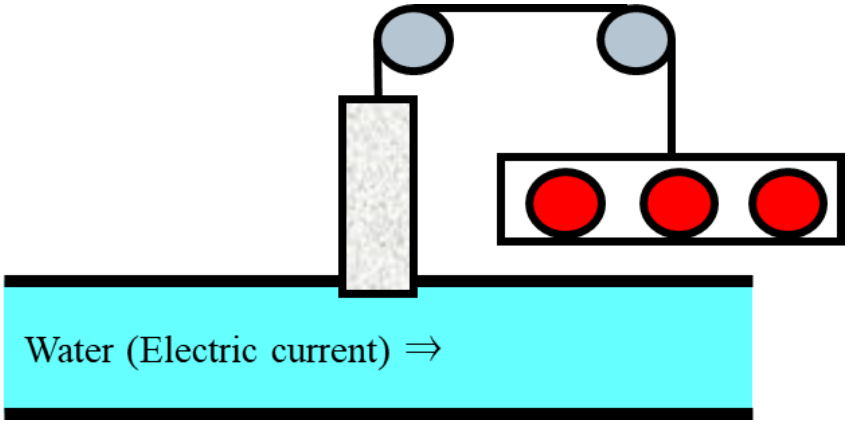


MOSFET as Switch

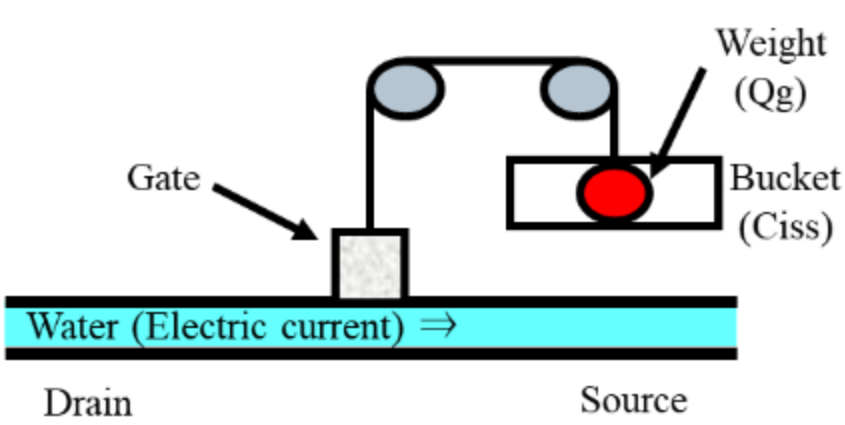
OFF state

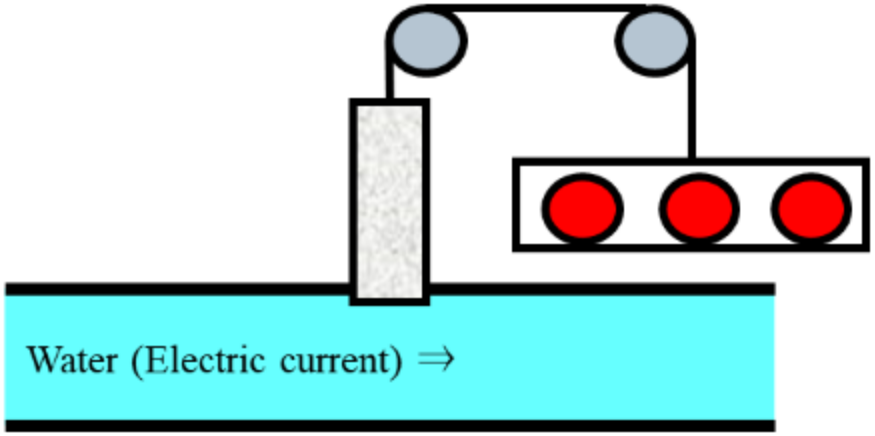


ON state



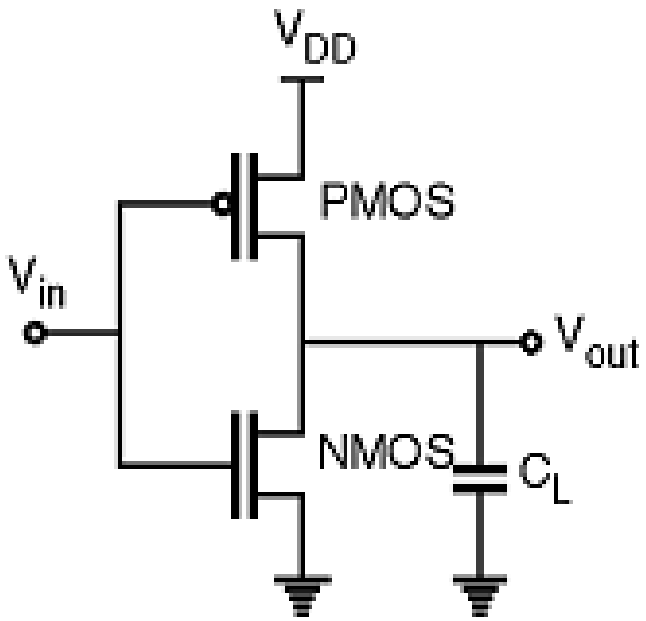
MOSFET controlled conduction

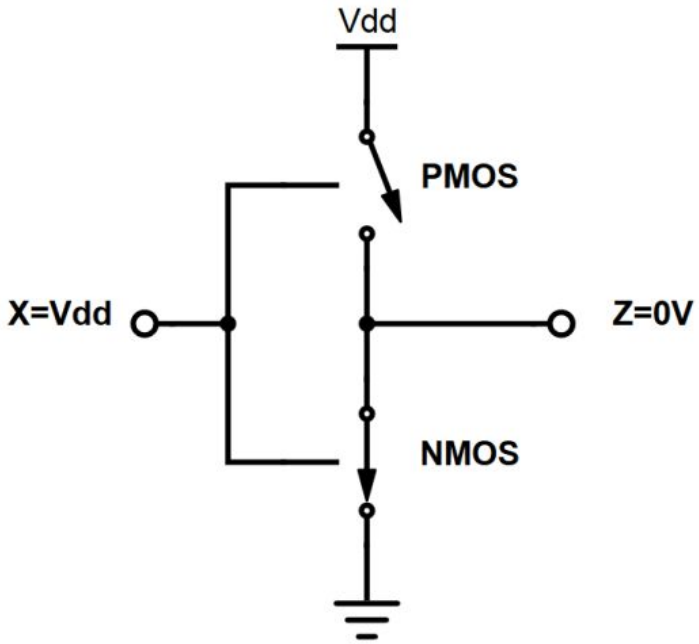




CMOS Inverter

- Basic building block of CMOS logic circuits.
- Consists of an NMOS and PMOS transistor connected in series





CMOS Inverter

- Consumes almost no power in steady state (except during switching).
- Power is only consumed during the transition between states (switching).
- Provides robust performance with high noise margins, making it ideal for digital circuits
- Widely used in logic gates, flip-flops, and digital ICs like microprocessors

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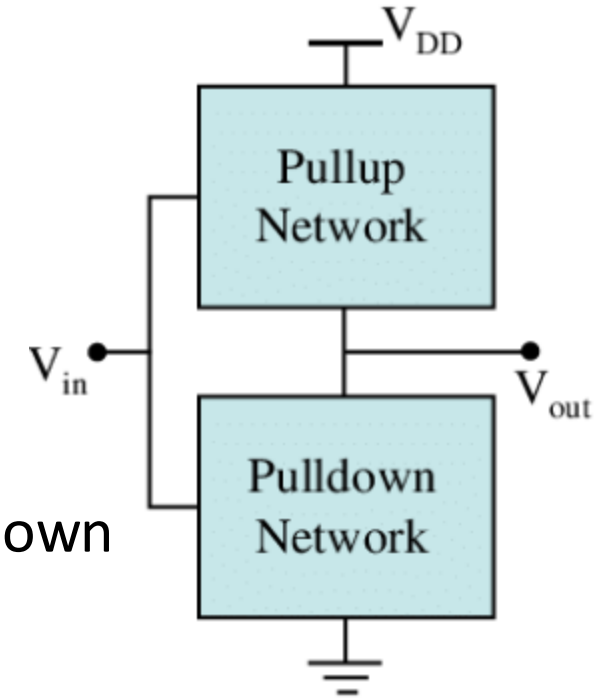
CMOS Gate Design

- Complementary CMOS logic gates
  - nMOS pull-down network
  - pMOS pull-up network
  - a.k.a. static CMOS

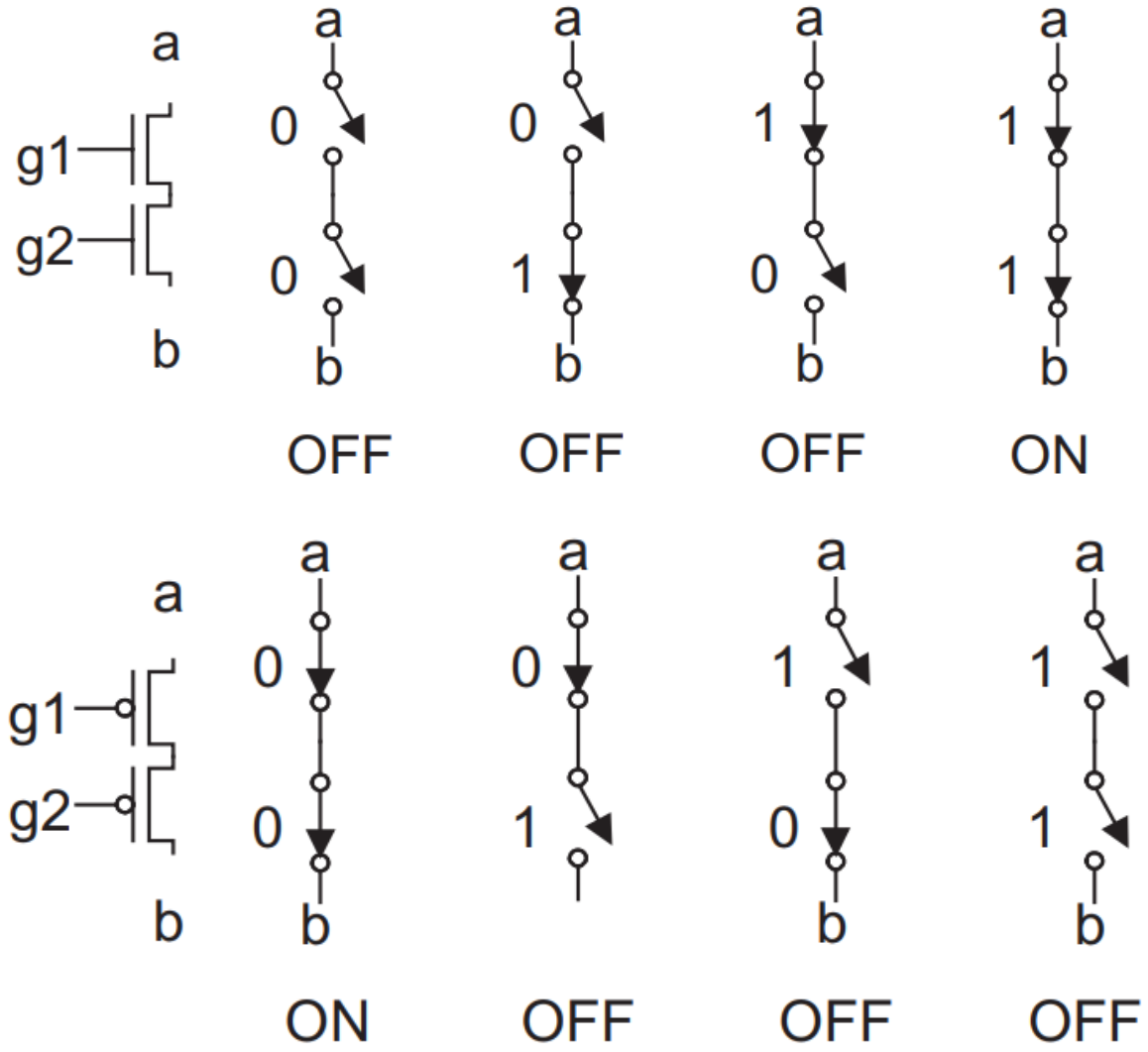


Rule of Conduction Complements

- Pull-up network is complement of pull-down
- Parallel -> series, series -> parallel

	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

MOS Series Connections



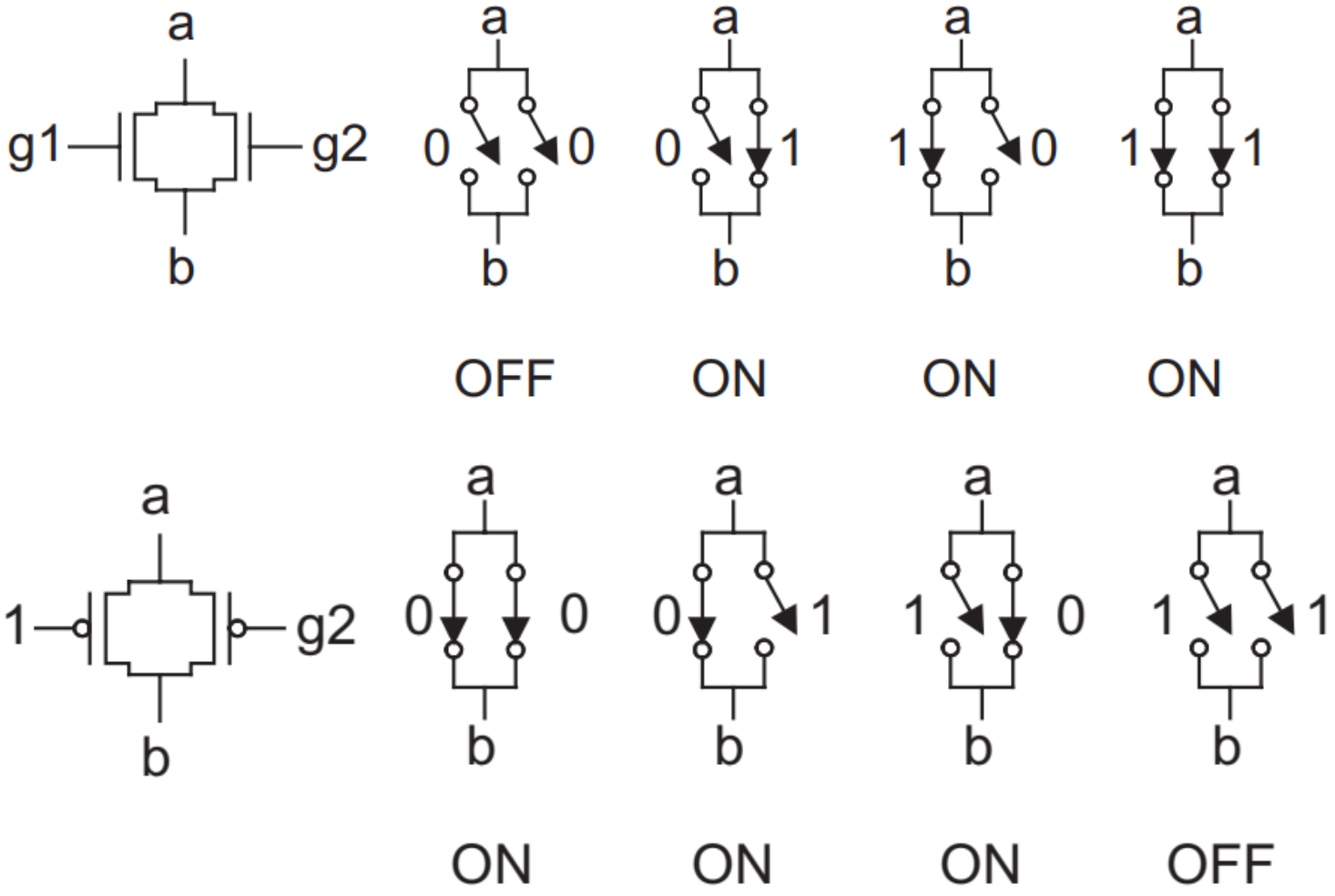
nMOS: 1 = ON

pMOS: 0 = ON

Series: both must be ON

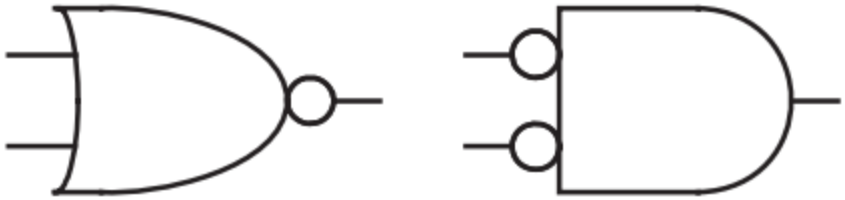
Parallel: either can be ON

MOS Parallel Connections

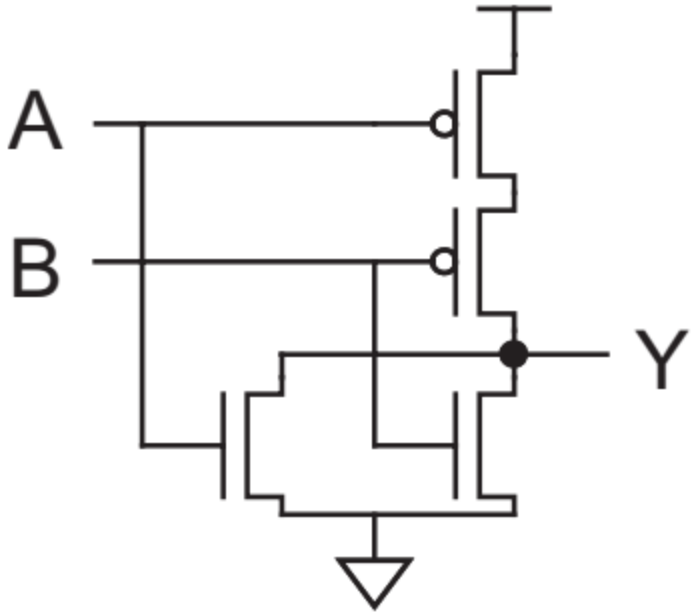


NOR Gate

$$Y = \overline{A + B}$$

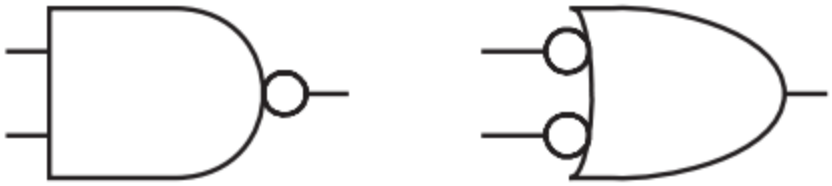


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

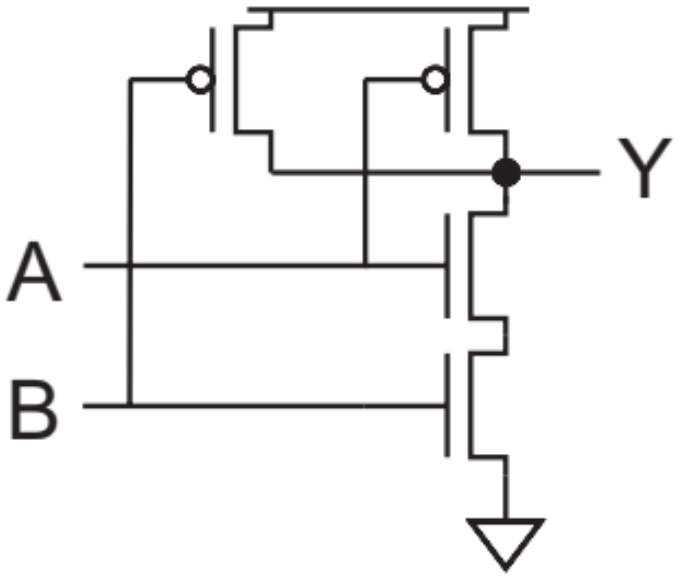


NAND Gate

$$Y = \overline{A \cdot B}$$



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Compound Gates

- A compound gate implements a **complex Boolean function** with **fewer transistors** than combining individual gates

Advantages :

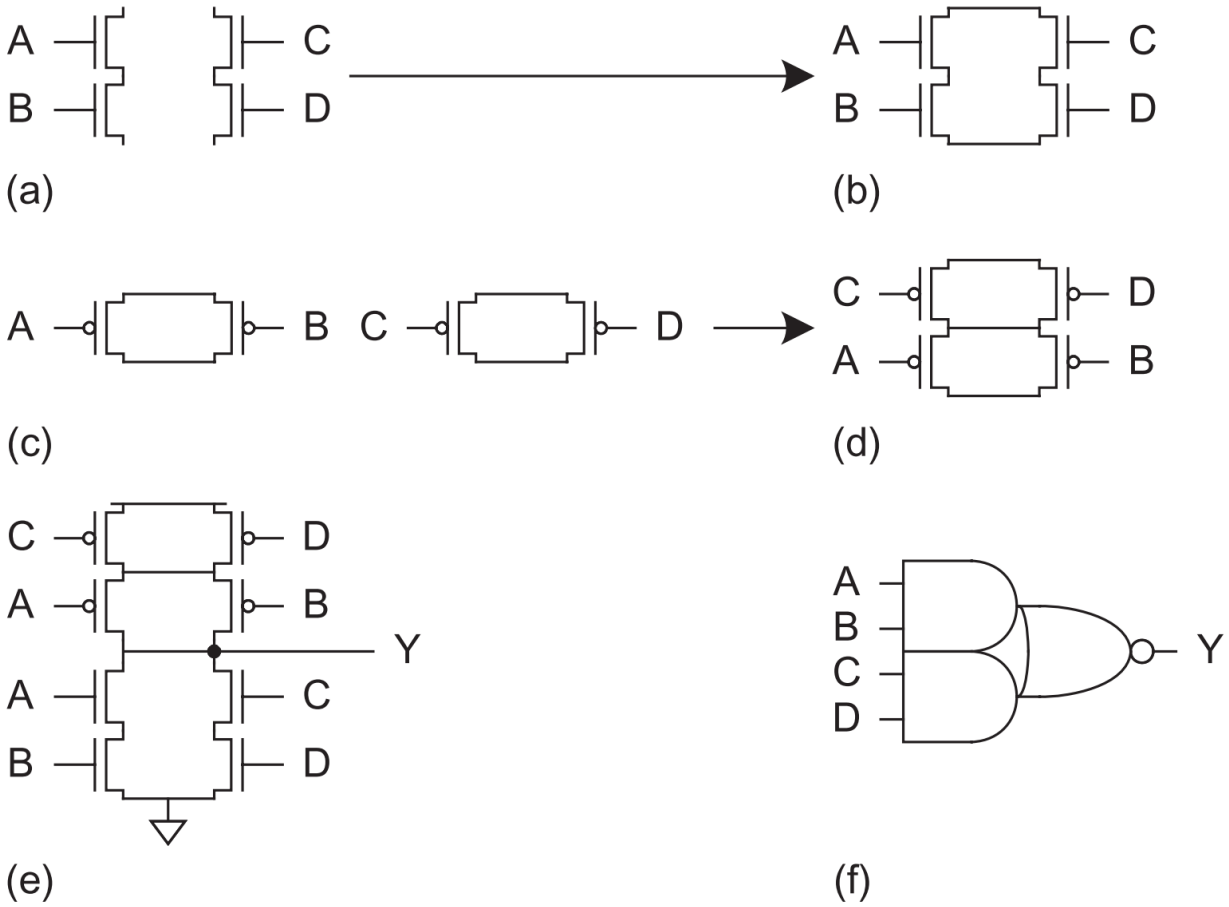
- **Reduced Delay:** Fewer stages of logic
- **Compact Design:** Optimized for area efficiency
- **Power Efficiency:** Fewer switching events

Examples:

- **AND-OR-Invert (AOI):** Combines AND, OR, and NOT
- **OR-AND-Invert (OAI):** Combines OR, AND, and NOT

Compound Gates

$$Y = \overline{(A \cdot B) + (C \cdot D)}$$



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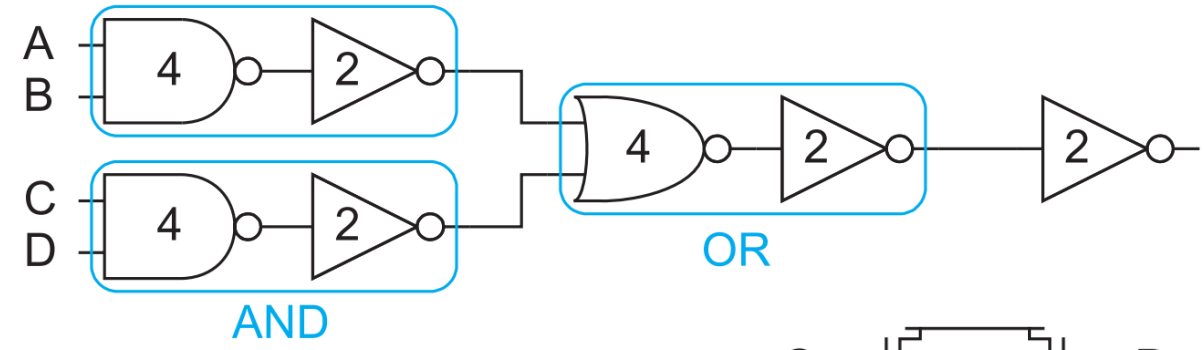
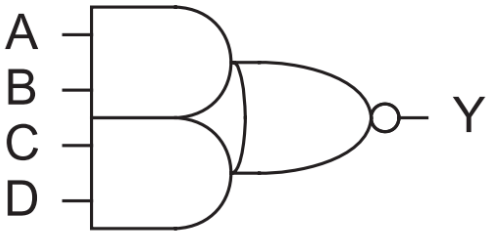
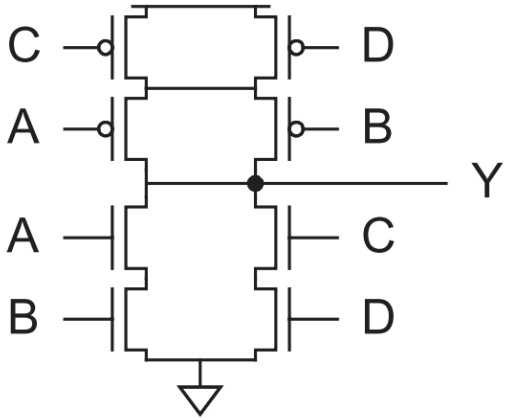


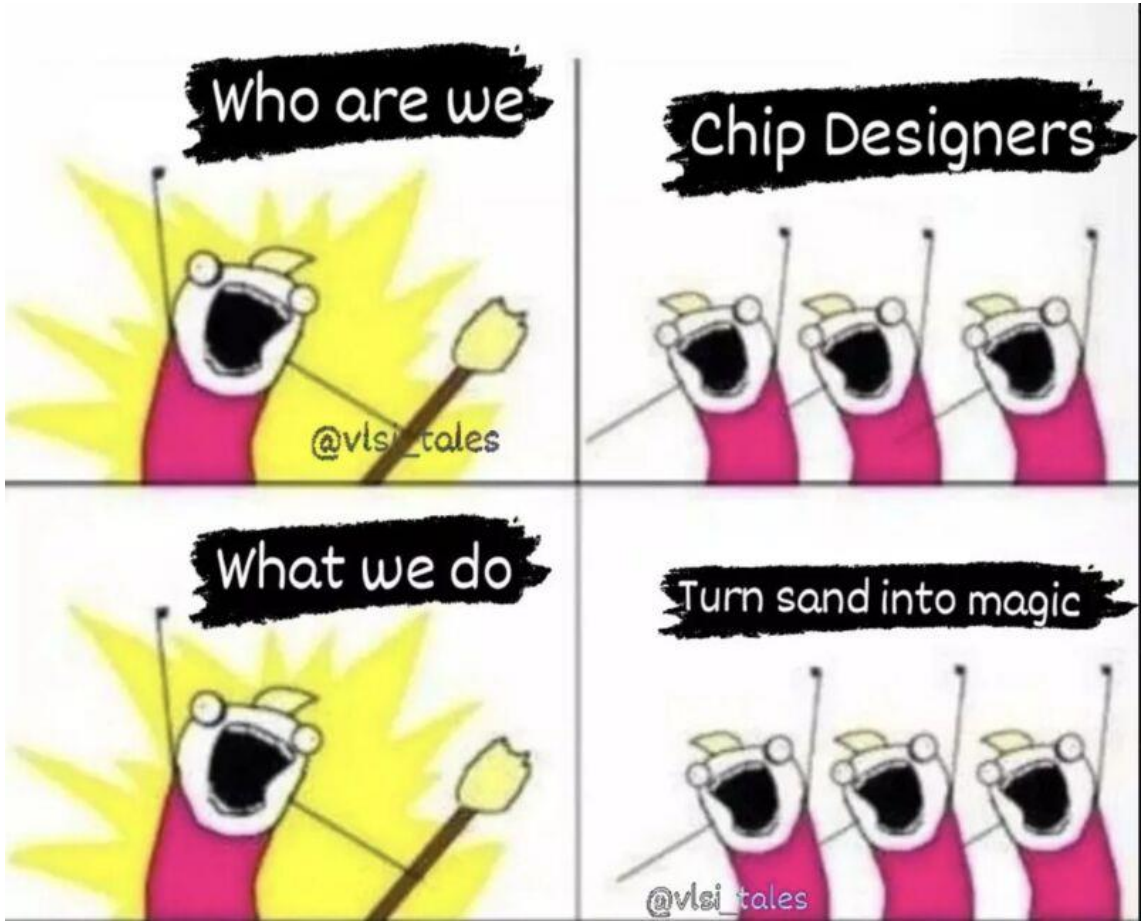




20 Transistors for AND-OR-Invert
8 Transistors for Compound Gate

Summary

- Integration in VLSI reduces cost, size, and power while improving speed and reliability.
- CMOS technology is preferred due to its low static power consumption and high noise immunity.
- CMOS gates use complementary PMOS and NMOS networks to achieve efficient logic implementation.
- CMOS gate design ensures minimal power dissipation in steady state and full voltage swing at output.
- Compound gate design allows realization of complex logic functions with fewer transistors and lower delay.



Thank you !

Happy Learning