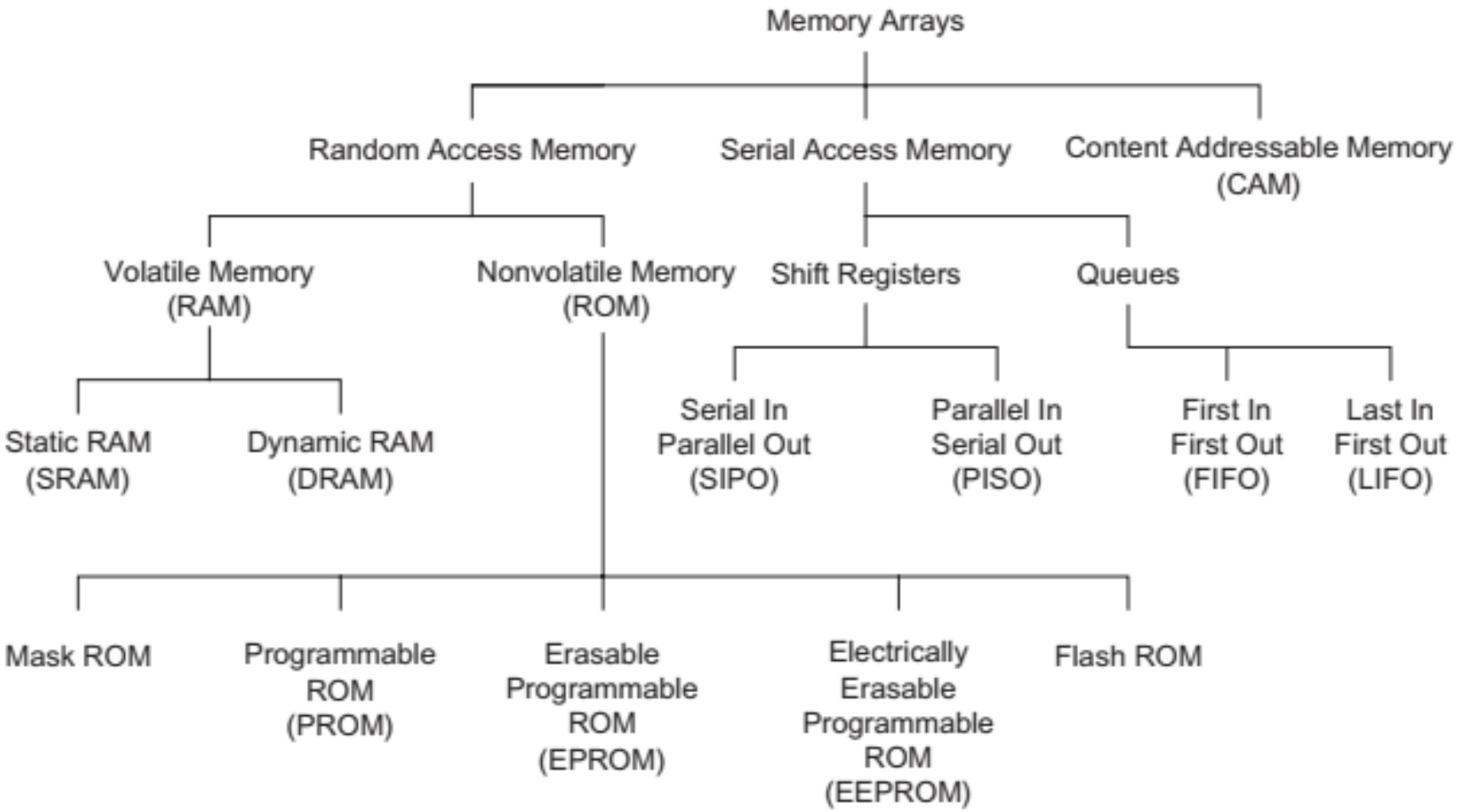
Memory using CMOS

Pravin Zode

Outline

- Memory Classification
- General Memory Design
- SRAM Memory Cell
- DRAM Memory Cell

Memories Classification



Memories Classification

Memory cells used in volatile memories can be divided into static structures and dynamic structures

- Static cells use some form of feedback to maintain their state
- Dynamic cells use charge stored on a floating capacitor through an access transistor
- Charge will leak away through the access transistor even while the transistor is OFF, so dynamic cells must be periodically read and rewritten to refresh their state
- Static RAMs (SRAMs) are faster and less troublesome, but require more area per bit than their dynamic counterparts (DRAMs)

Random Access Memories

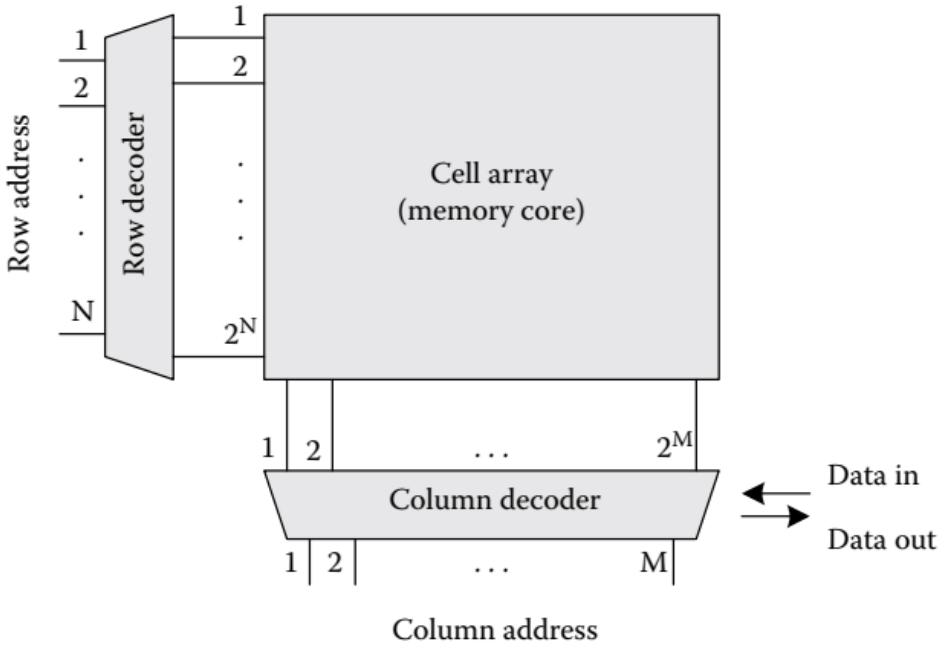
SRAM

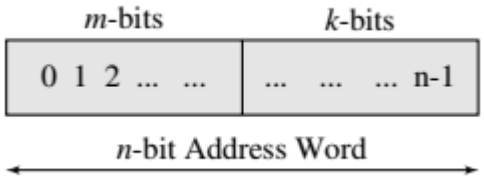
- Data is stored as long as power is supplied
- Relatively large cells, 6-transistors, lower density (vs. DRAM)
- Fast – use closer to computation
- Compatible with CMOS technology

DRAM

- Data must be periodically refreshed
- Small cells, 1 transistor, VERY dense
- Slower, use in larger main memories
- Process not compatible with standard CMOS

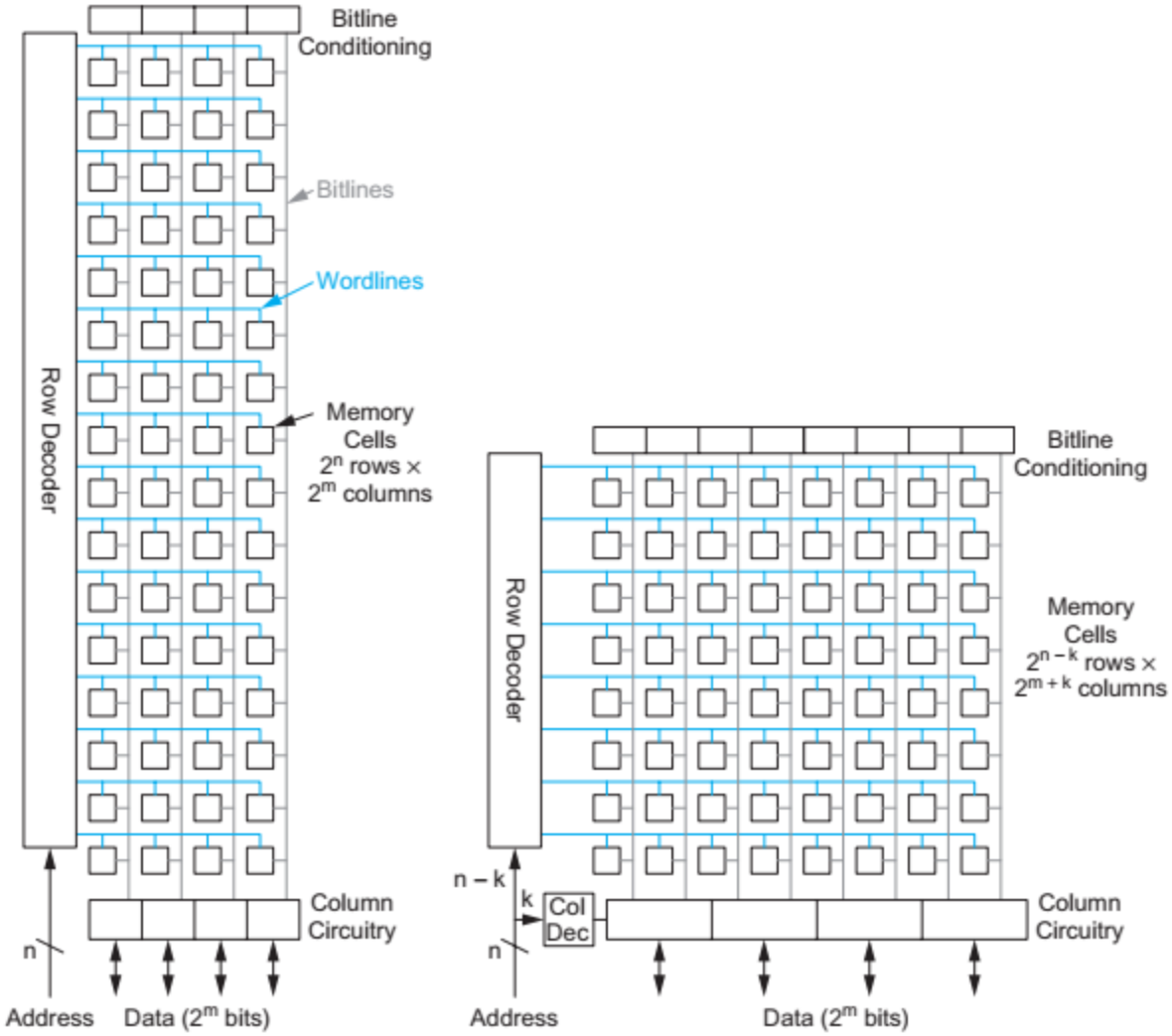
General Memory Design





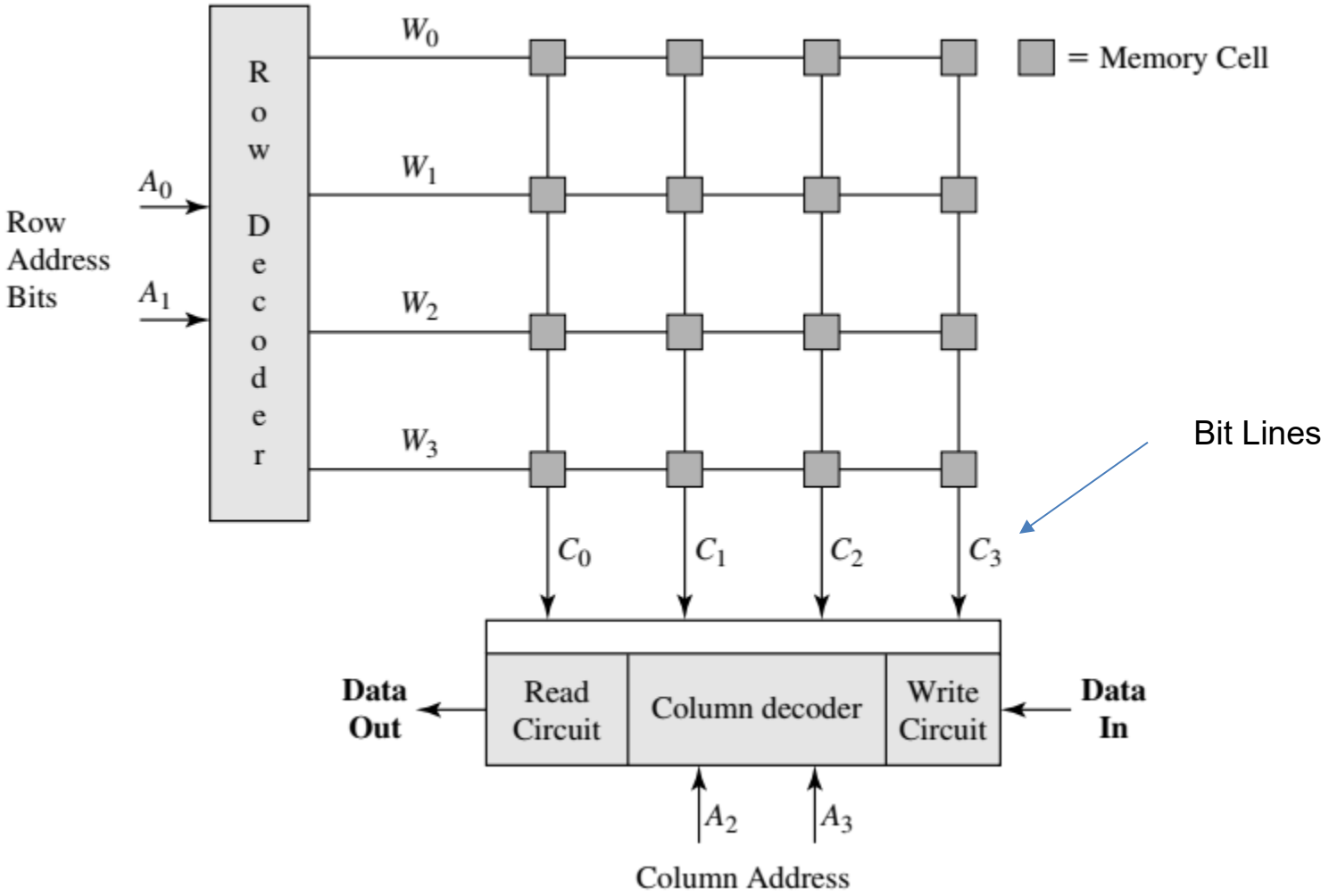
- Memories use an address word to select a specific bit
- n-bit address word is divided into two sections
- one section contains the m-row address line bits and other the k-column bits
- There are 2^m rows and 2^k columns
- The total number of cells in the memory are $2^{m+k} = 2^n$

General Memory Design

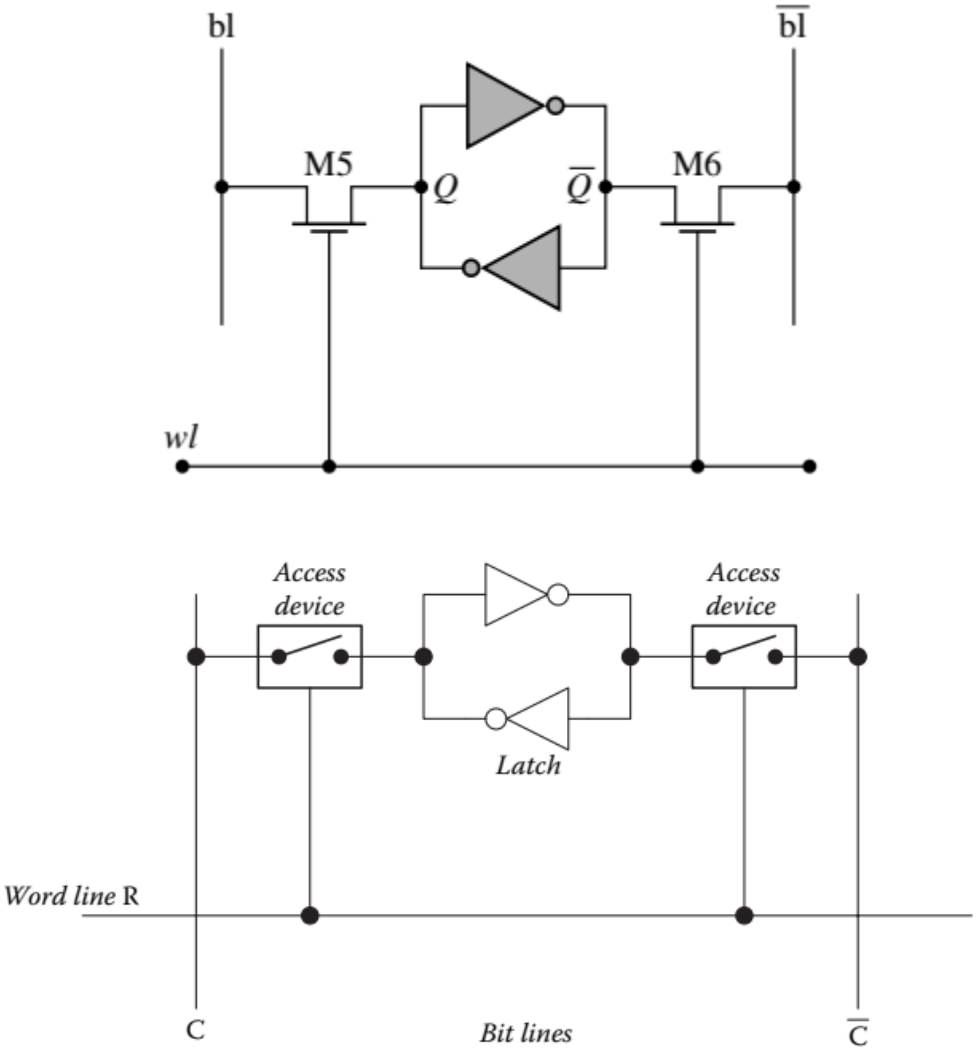


- Good regularity – easy to design
- Very high density if good cells are used

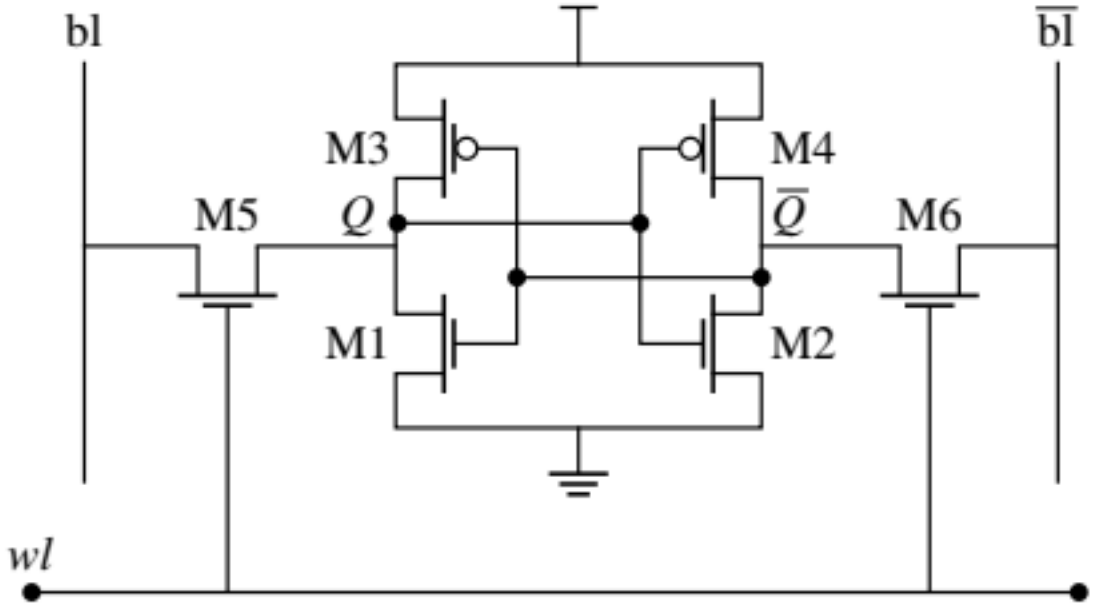
Memory Circuit Organization



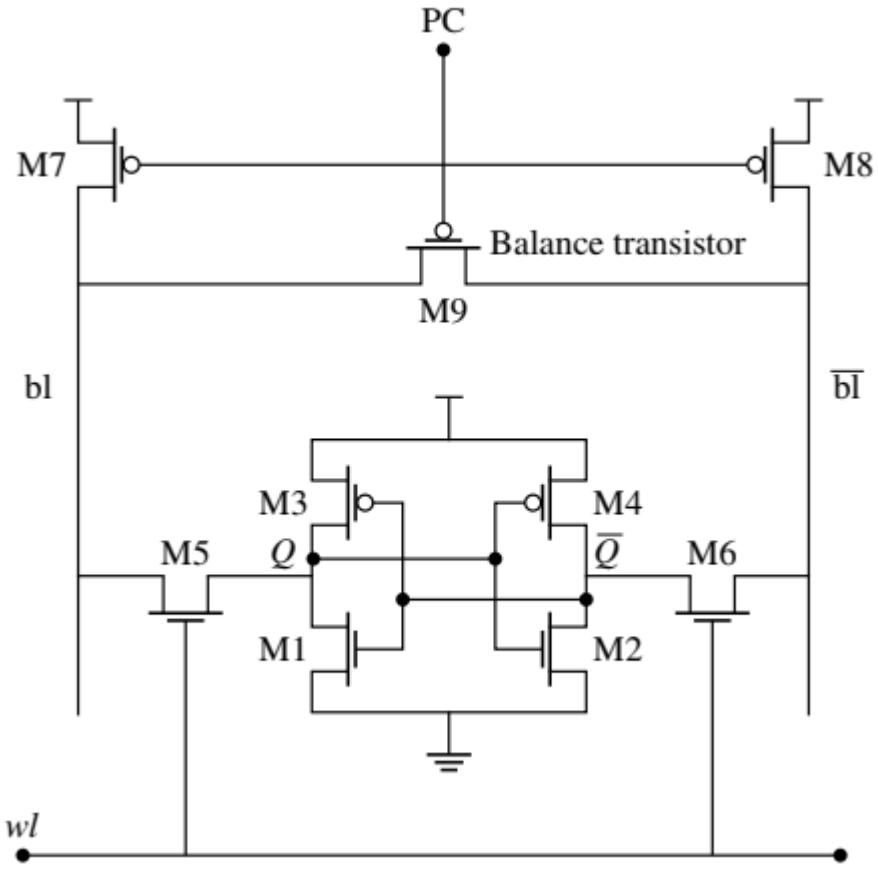
SRAM Memory Cell 4T



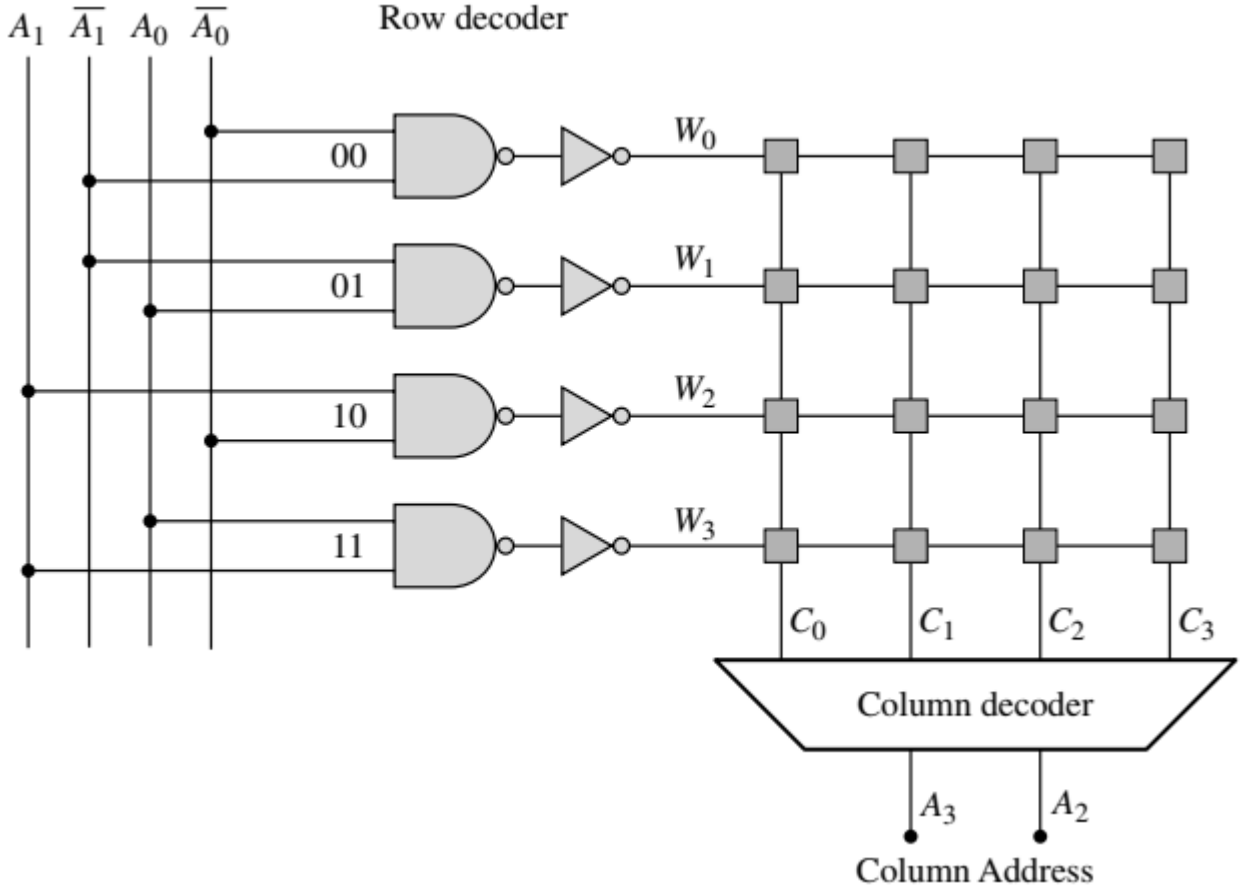
Memory Cell 6T



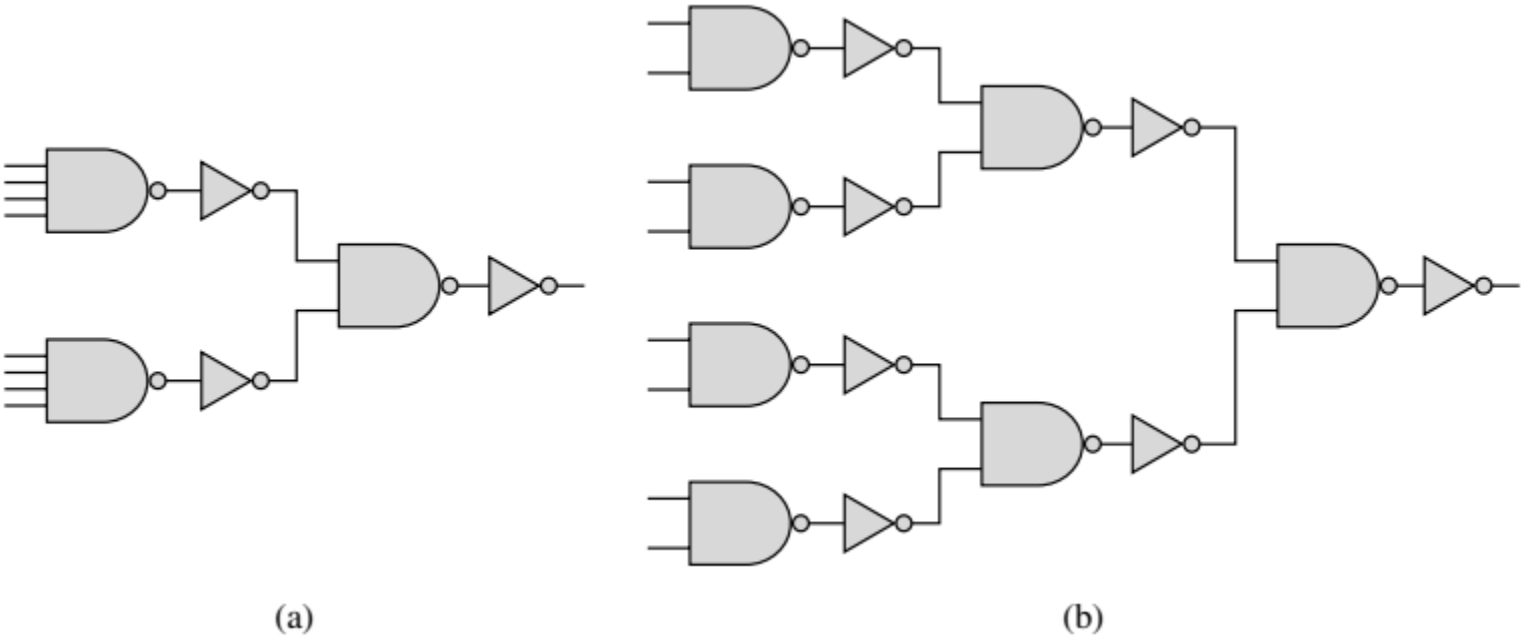
Memory Cell with Pre-Charge Transistor



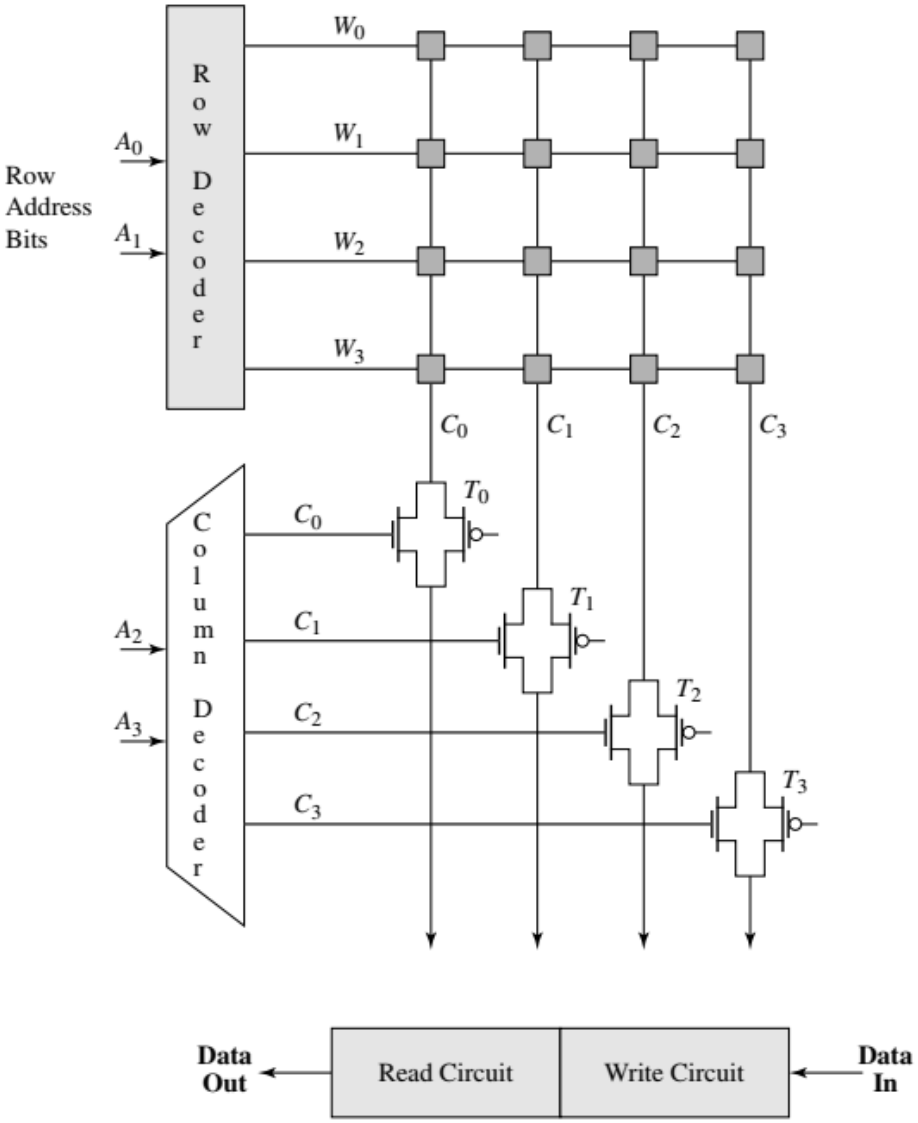
Memory Decoder (Row)



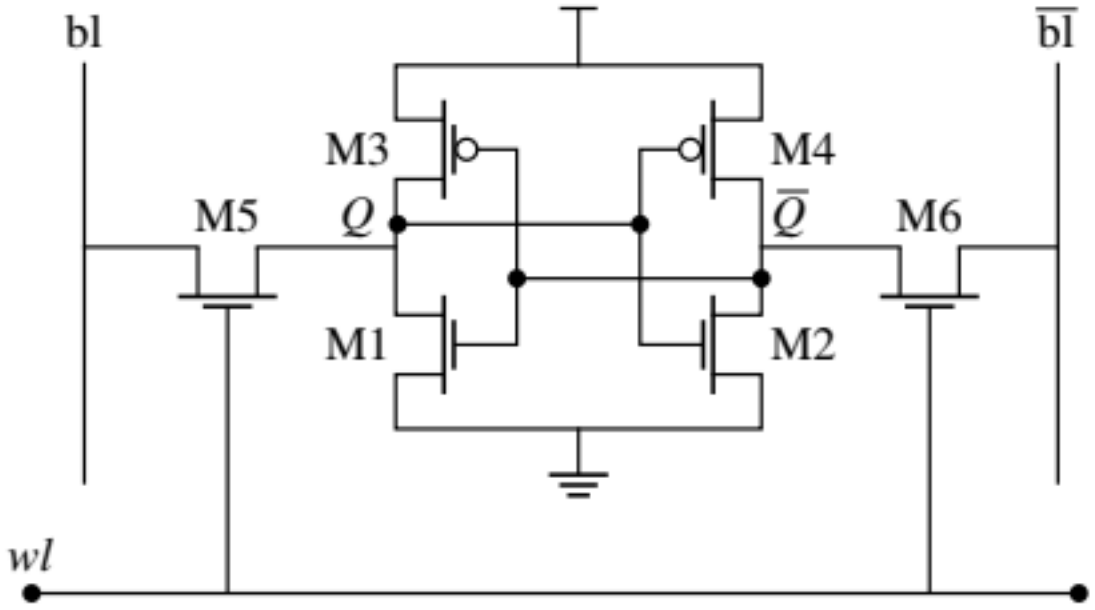
Memory Decoder (Row)

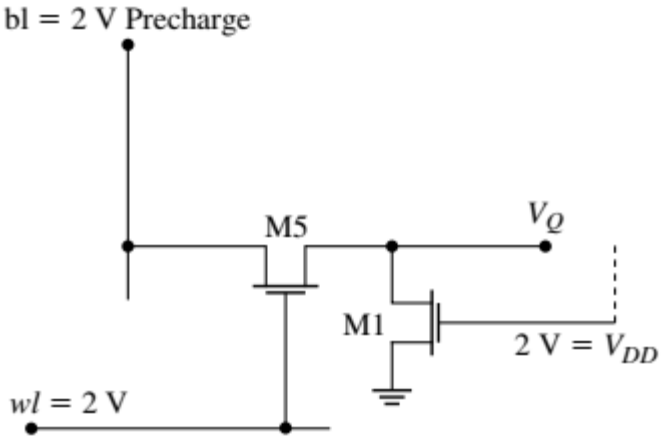


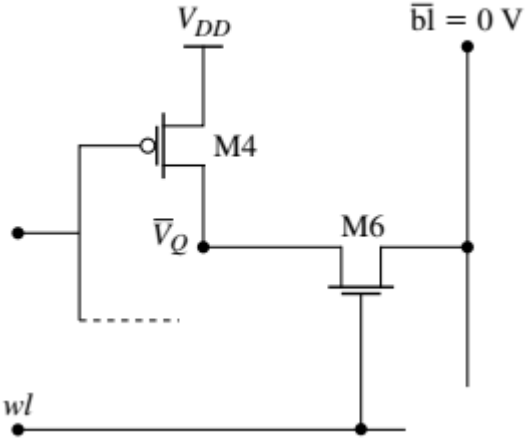
Memory Decoder (Column)



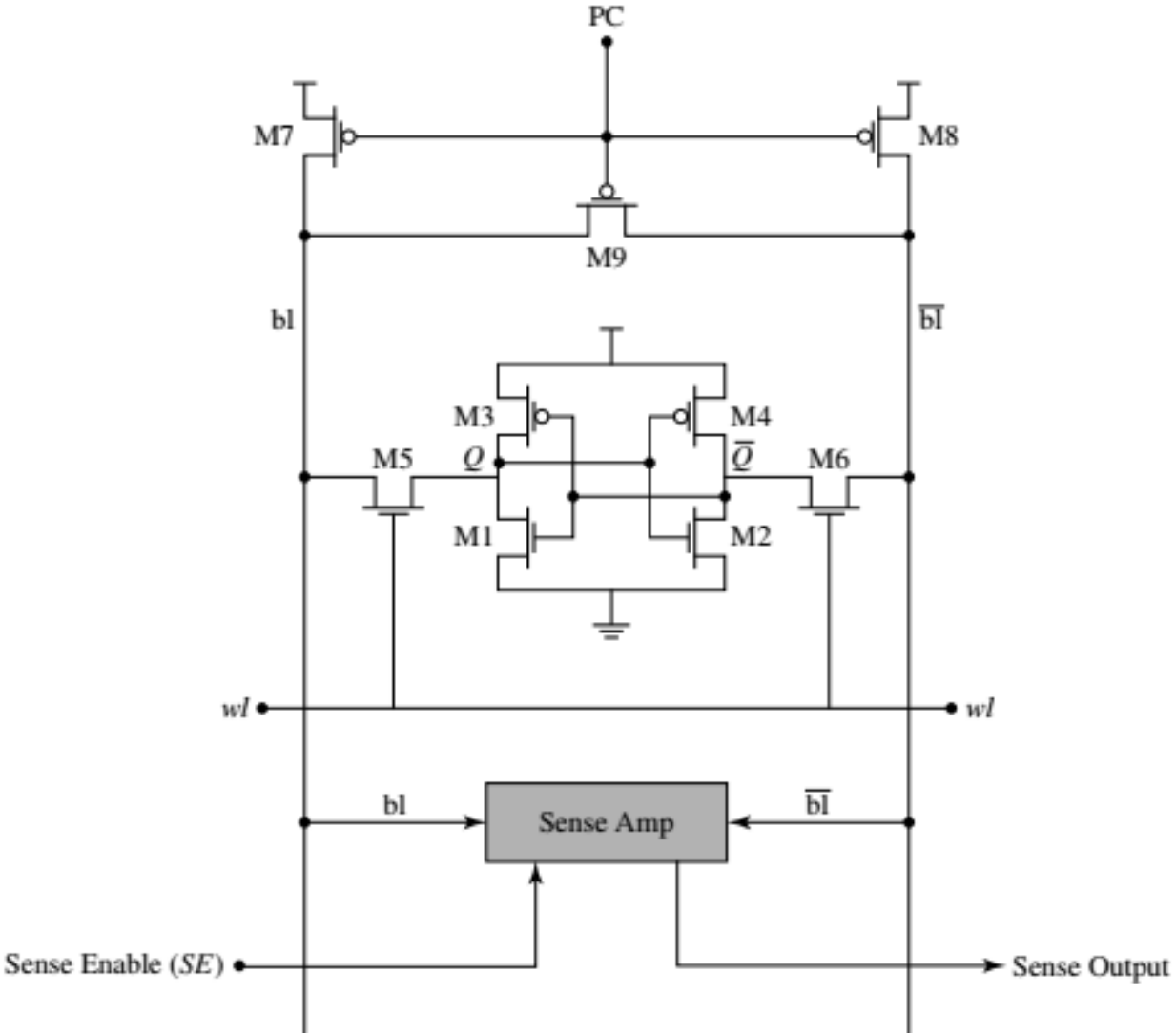
Read and Write Operation



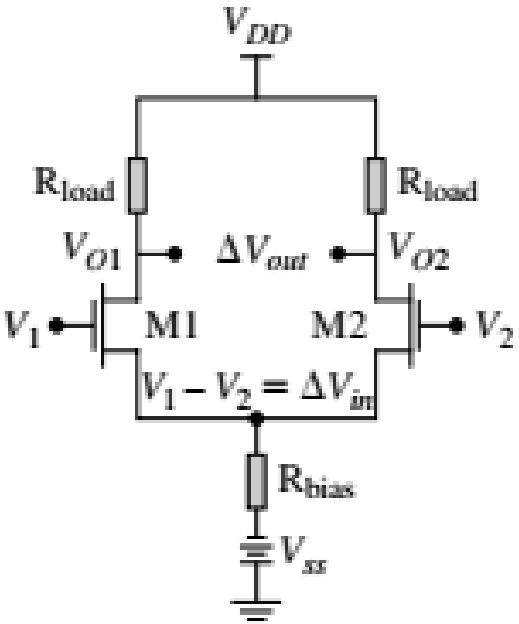




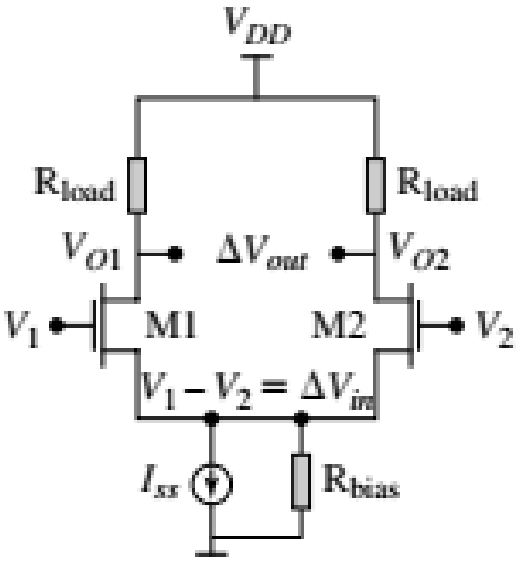
Sense Amplifier



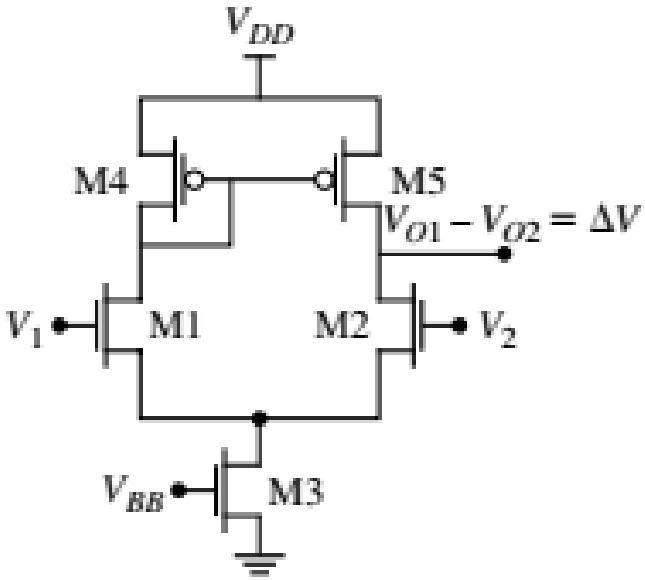
Sense Amplifier (Diff. Amplifier)



Differential amplifiers

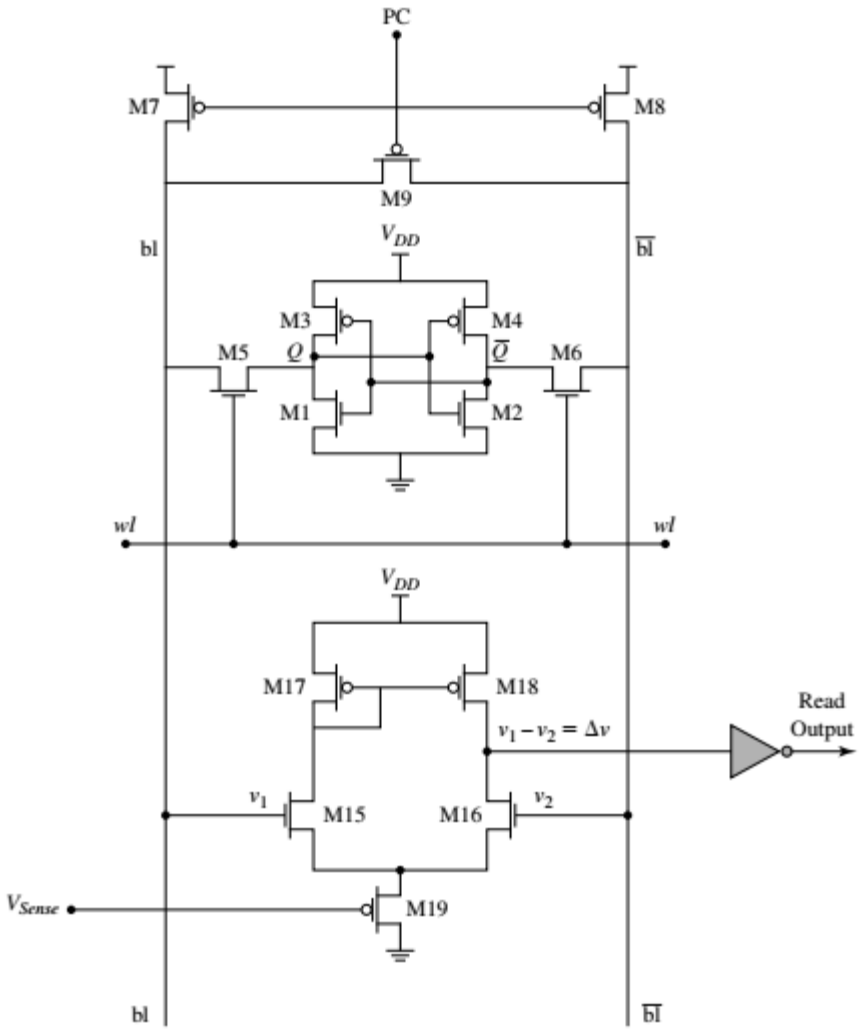


Approximate current source biasing

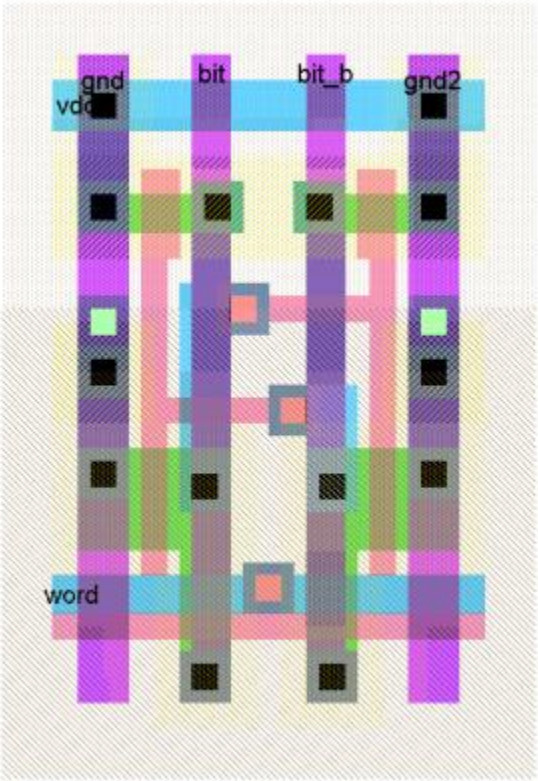


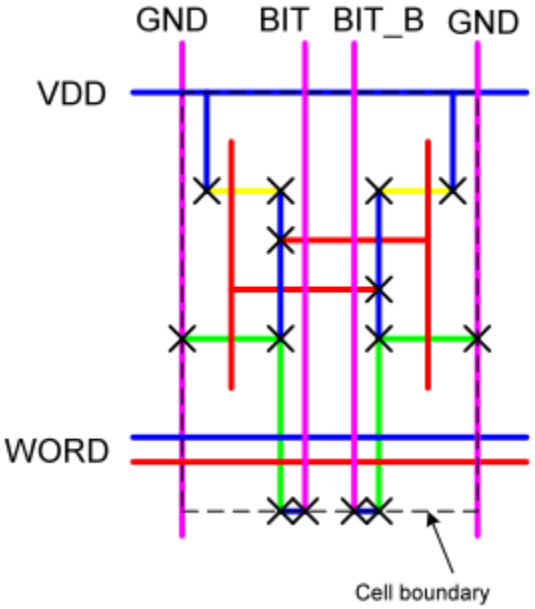
Active load transistors M4 and M5

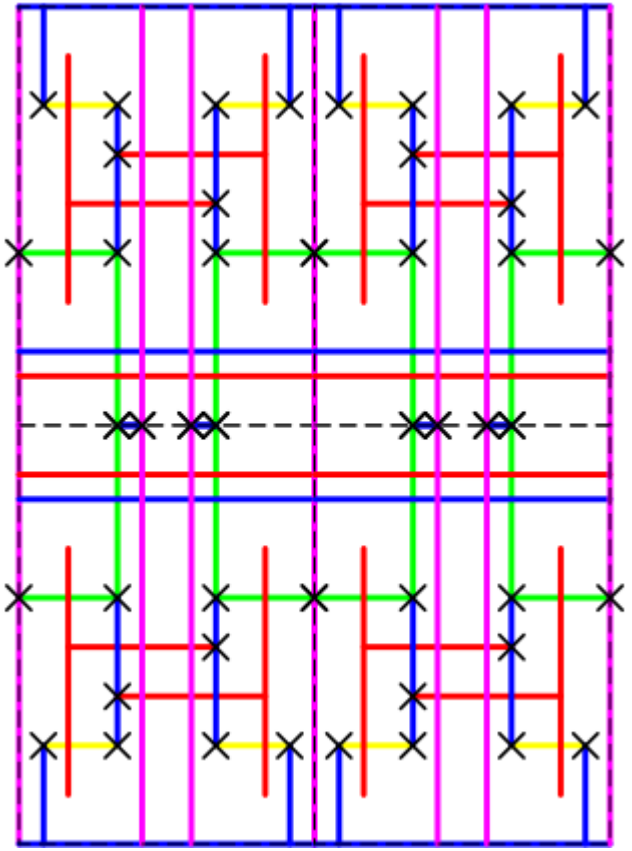
Read Operation Circuitry



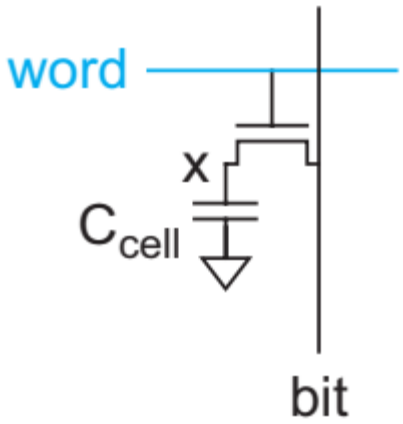
SRAM Layout


gnd
bit
bit_b
gnd2
vdd
word


GND
BIT
BIT_B
GND
VDD
WORD
Cell boundary



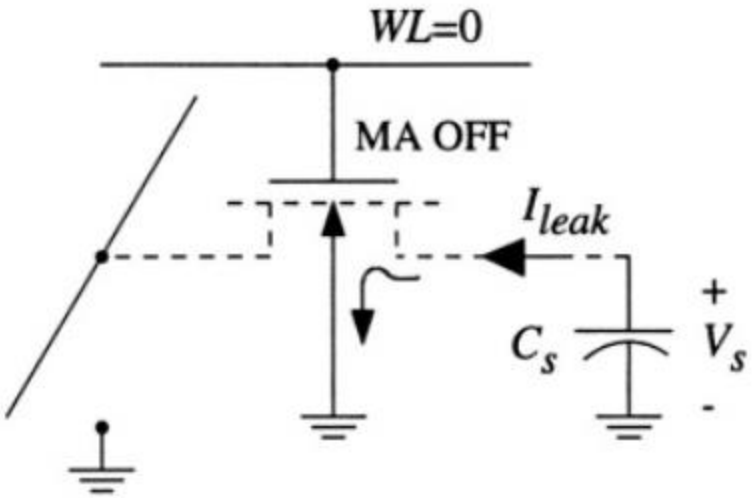
DRAM Basics



1-transistor (1T) dynamic RAM cell

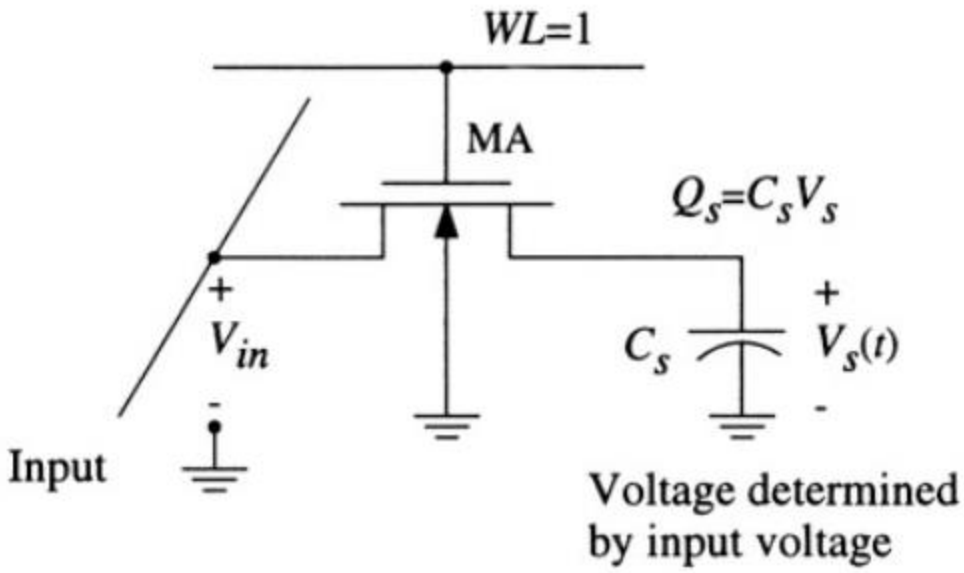
- DRAMs achieve higher density than SRAMs because they are constructed with three or fewer transistors per bit
- Dynamic RAMs (DRAMs) store their contents as charge on a capacitor rather than in a feedback loop
- Basic cell is substantially smaller than SRAM
- Cell must be periodically read and refreshed so that its contents do not leak away

DRAM Hold Operation



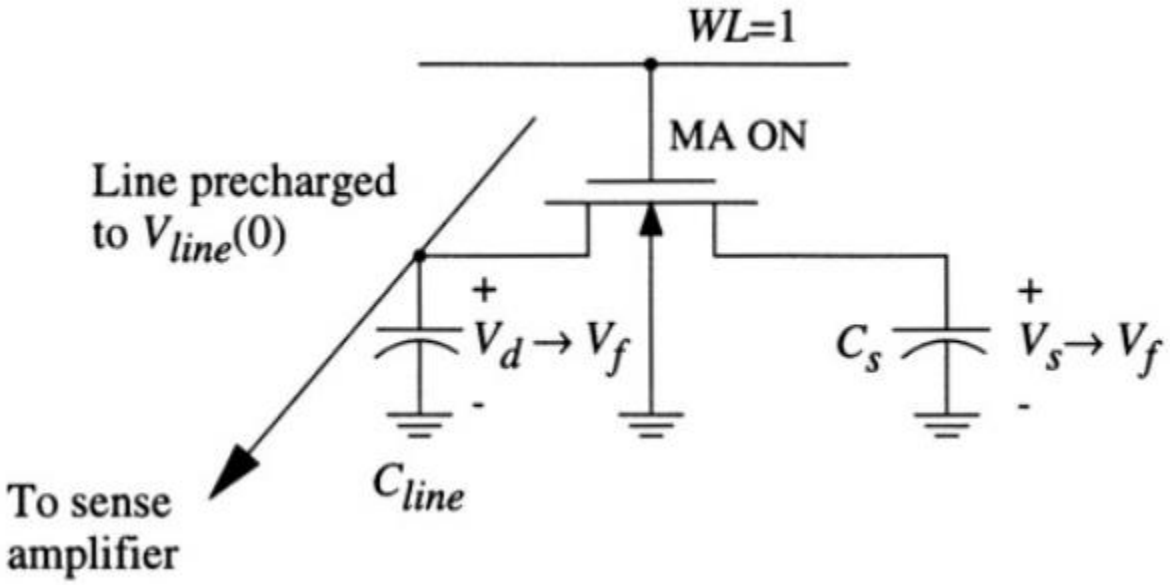
Hold Operation dynamic RAM cell

DRAM Write Operation



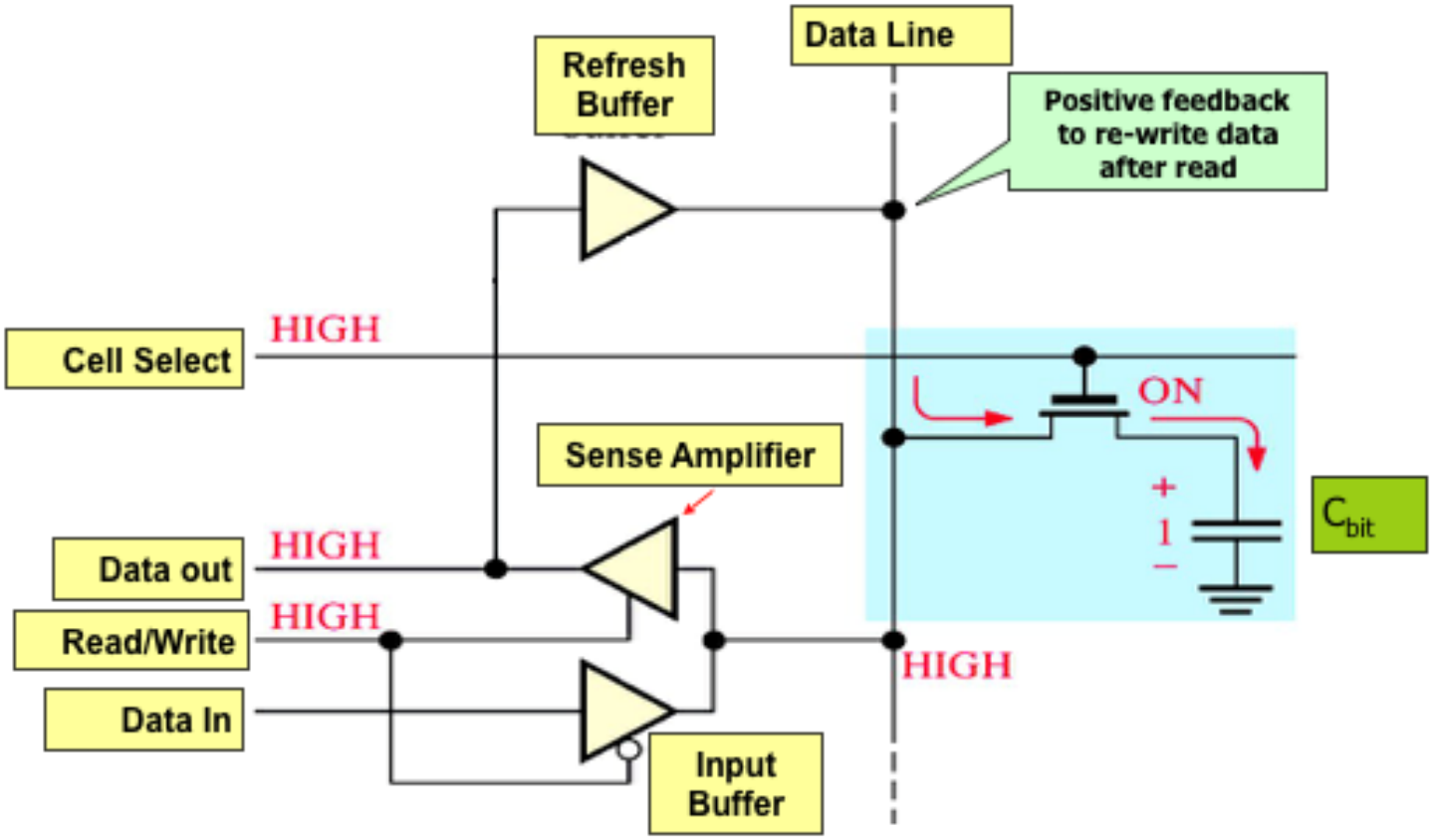
Write Operation dynamic RAM cell

DRAM Read Operation



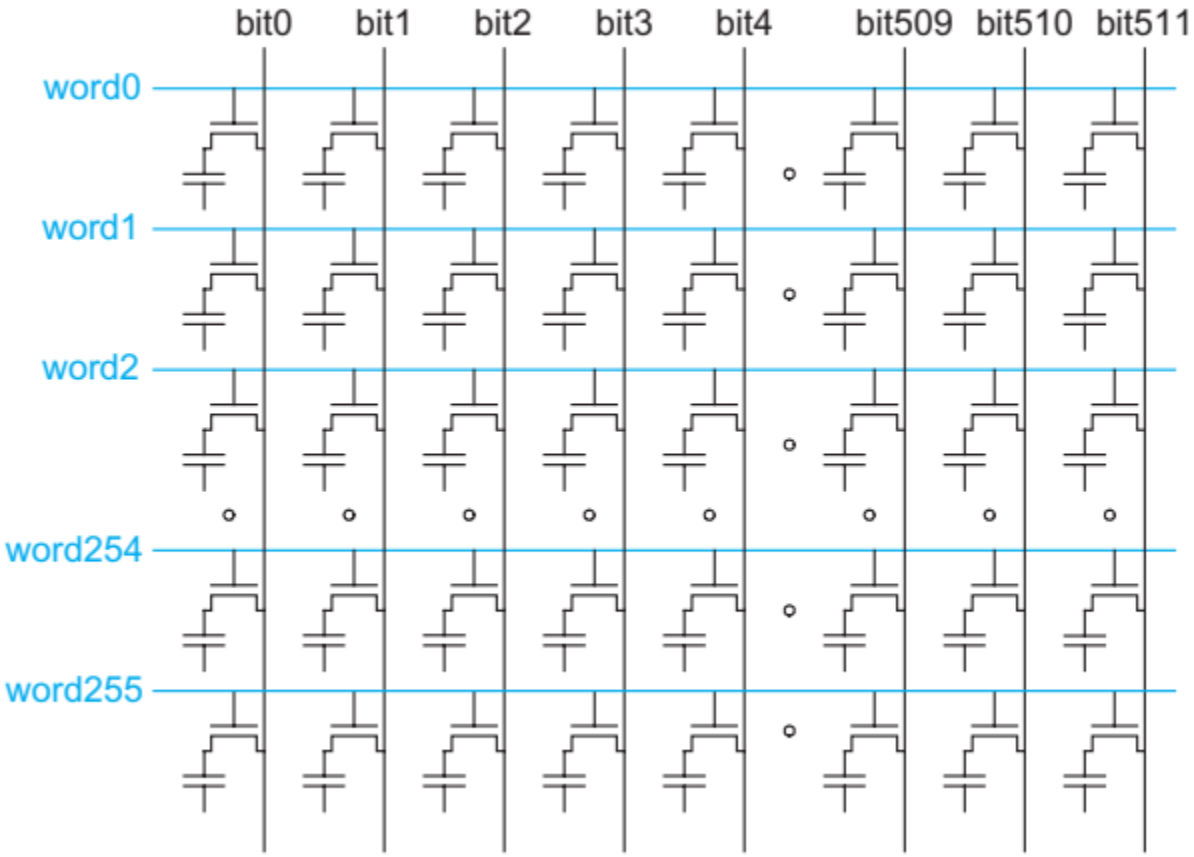
Read Operation in dynamic RAM cell

DRAM Refresh Operation



Refresh Circuitry dynamic RAM cell

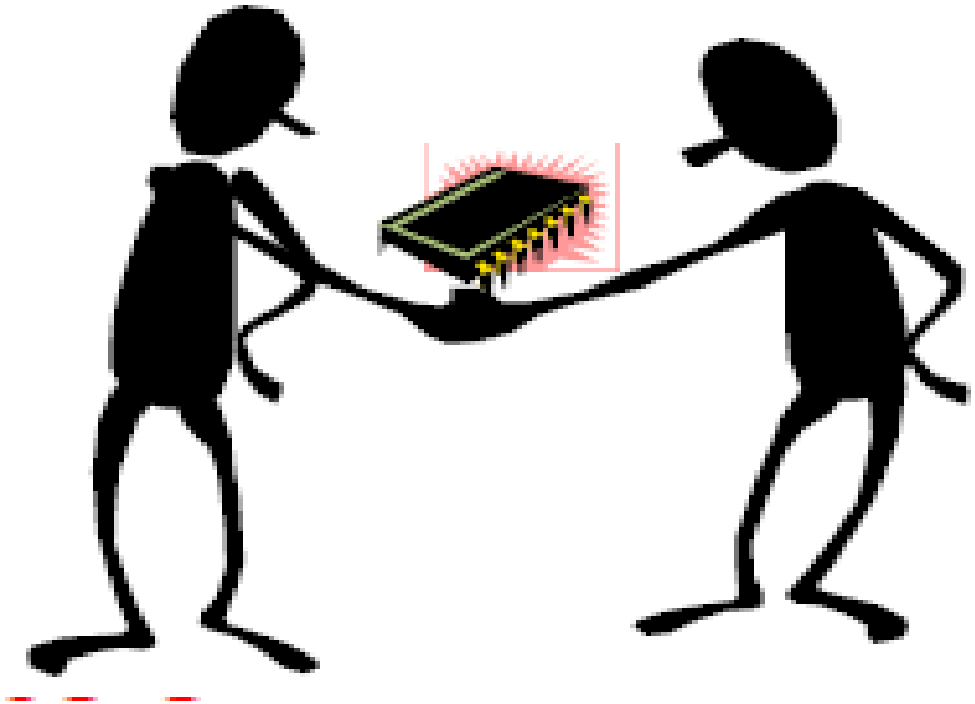
DRAM Subarray



DRAM Subarray

Conclusion

- **SRAM (Static RAM):** Fast, stable, and no refresh needed. Ideal for high-speed, low-latency uses like CPU caches, but lower density and higher cost
- **DRAM (Dynamic RAM):** High-density, cost-effective, but requires refreshing, leading to slower access. Used in main memory for high-capacity storage
- SRAM is chosen for performance; DRAM for capacity. Together, they fulfill diverse memory needs in computing systems.



Thank you !

Happy Learning