Back-Annotation and Post layout Simulation

Pravin Zode

Outline

- Design Flow and File Formats
- Timing Analysis
- Back-Annotation & Post-Layout Simulation

Design Flow and File Formats

- Back-end focuses on physical design after RTL synthesis.
- Key file formats:
  - GDSII, DEF, LEF for layout
  - SPEF, SDF for timing and parasitic info
- Design includes:
  - Netlist-to-layout mapping
  - DRC, LVS checks

GDSII (Graphic Data System II)

- Binary file format used in VLSI design
- Represents the physical layout of integrated circuits
- Originally developed by Calma Company
- Industry-standard format for mask data exchange
- Used to transfer layout data between EDA tools and fabrication facilities

Key Components of a GDSII File

- **Layers:** Each layer represents a different part of the fabrication process (e.g., diffusion, metal, polysilicon). Layers are defined by a number and a name.
- **Geometric Shapes:** polygons, rectangles, and paths that define the physical layout of the circuit elements.
- **Text and Labels:** You can include text annotations or labels that provide additional information about specific parts of the layout.
- **Hierarchy:** Allowing for the inclusion of instances of other layouts (cells) within a main layout.
- **Properties:** Additional properties can be associated with shapes, such as layer-specific attributes or custom properties.
- **Bounding Boxes:** GDSII files include bounding boxes that help define the spatial limits of shapes for processing.

Sample GDSII File

- A GDSII file is binary and not human-readable

```
HEADER: GDSII File Version
BGNLIB: Library Name
BGNSTR: Structure Name
  LAYER: 1 (e.g., diffusion layer)
  DATATYPE: 0
  PATH: (x1, y1) (x2, y2) ... (xn, yn)   // Define a path
  BOX: (x_min, y_min) (x_max, y_max)     // Define a rectangle
  POLYGON: (x1, y1) (x2, y2) ... (xn, yn) // Define a polygon shape
  TEXT: (x, y) "Label"                    // Define text label
ENDSTR: End of Structure
ENDLIB: End of Library
```

Tools for Viewing GDSII File

- Cadence Virtuoso
- Mentor Graphics
- Synopsys Design Compiler
- KLayout (an open-source layout viewer)

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DEF (Design Exchange Format)

- Standard ASCII format used in VLSI physical design
- Represents the physical layout of an IC design instance
- Facilitates data exchange between EDA tools during the back-end flow

DEF (Design Exchange Format)

Key parameters in DEF Files are

- Die area and chip dimensions
- Placement of standard cells, macros, and I/O blocks
- Net connections including wire segments, vias, and layers
- Clock trees, rows, and tracks
- Pin locations and orientation on the die
- Special nets (e.g., power and ground routing)
- Routing guides and constraints for detailed routing tools

LEF (Library Exchange Format)

- ASCII format used to describe the physical layout abstract of standard cells and macros
- Contains technology and cell library information without full transistor-level details.

LEF (Library Exchange Format)

Key parameters in LEF Files are

- Cell dimensions (height, width)
- Pin locations and metal layer usage
- Cell blockage areas (to prevent routing over specific regions)
- Routing grid and layer definitions (e.g., preferred direction, pitch)
- Via definitions and design rules

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Timing & Parasitic File Formats: SPEF and SDF

SPEF (Standard Parasitic Exchange Format)

- ASCII format for representing parasitic resistance and capacitance values
- Describes RC networks of interconnects post-layout.
- Includes:
  - Net parasitics (R, C values)
  - Pin-to-pin delays
  - Capacitive coupling
- Essential for accurate timing analysis and signal integrity checks
- Generated by extraction tools after routing

Timing & Parasitic File Formats: SPEF and SDF

SDF (Standard Delay Format)

- ASCII format used for timing information exchange between tools
- Contains delay values for:
  - Cell internal delays
  - Interconnect delays
  - Setup, hold, rise/fall times
- Used in Static Timing Analysis (STA) and timing simulation
- Can be annotated onto gate-level netlists for post-layout timing simulations

Timing Analysis

- Evaluates if signals meet required timing constraints (setup, hold, clock skew)
- Two main types:
  - **Static Timing Analysis (STA)** – Fast, deterministic analysis using delay models
  - **Dynamic Timing Simulation** – Simulates logic transitions over time
- Uses timing libraries (e.g., .lib) and optionally parasitic extraction data.

Parasitic Extraction

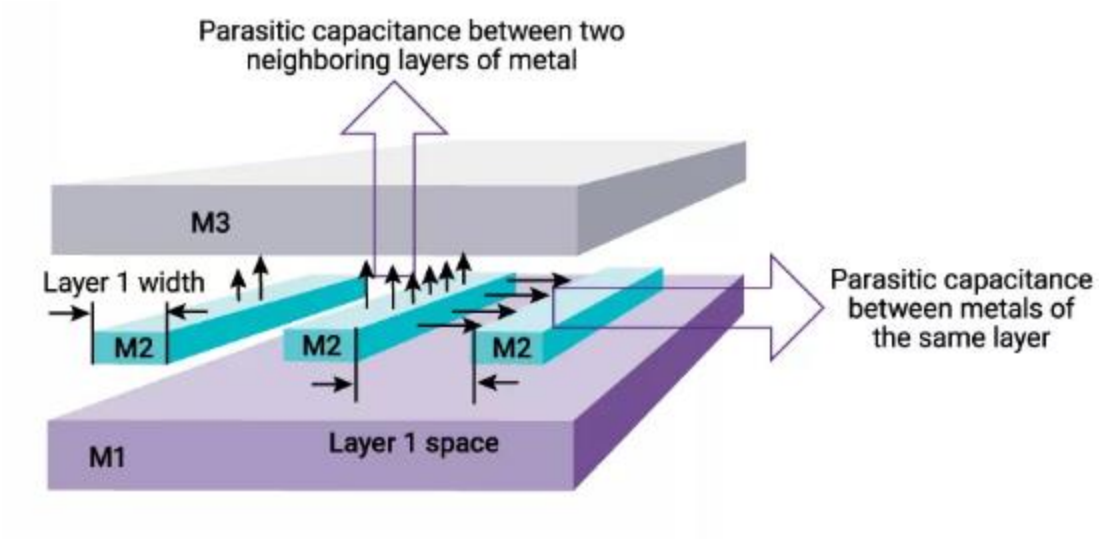
- Parasitic extraction is the process of identifying unintended resistive (R), capacitive (C), and inductive (L) effects in a layout after physical design.
- Parasitic extraction is done in order to create a more accurate and realistic analog model of the final layout.
- This is done so that the STA or simulations can emulate the actual design and analog circuit responses
- Without accurate parasitic extraction,
  - Inaccurate STA analysis
  - Crosstalk
  - Capacitive Loading
  - Inductive Loading

Applications and Critical Impact

- **Timing Analysis** : Helps identify real delays due to interconnect RC.
- **Power Analysis** : Accurate IR drop and dynamic power estimation
- **Signal Integrity Analysis** : Identifies crosstalk, glitches, and ringing
- **Circuit Simulation** : Post-layout SPICE-level simulation with parasitics.

Different Categories of Parasitics

- **Front-end of the Line (FEOL) :** Parasitics associated with the semiconductor devices.
- **Middle-end of the Line (MEOL) :** Parasitics associated with the contacts on semiconductor devices.
- **Back-end of the Line (BEOL) :** Parasitics associated with the interconnect layers.



How to ensure quality of extraction ?

For high quality extraction

- No LVS (Layout vs. Schematic) mismatches
- Avoid name mismatches
- No missing cells or nets
- No opens in the layout
- No shorts between unintended nets

For Accurate Coupling Capacitance (CC):

- Dummy cell fill must be present
- Oxide fill should be included

Back Annotation

- **Captures real-world characteristics** of the design after synthesis or layout(e.g., actual delays, parasitics, interconnect effects)
- **Enables timing-accurate simulations**(uses real delay values instead of ideal estimates)
- Allows **functional validation under realistic timing** conditions(detects glitches, race conditions, timing mismatches)
- Helps **detect setup and hold time violations**(ensures timing closure and functional correctness)
- Improves **accuracy of power analysis**(using real switching activity and parasitic loading)

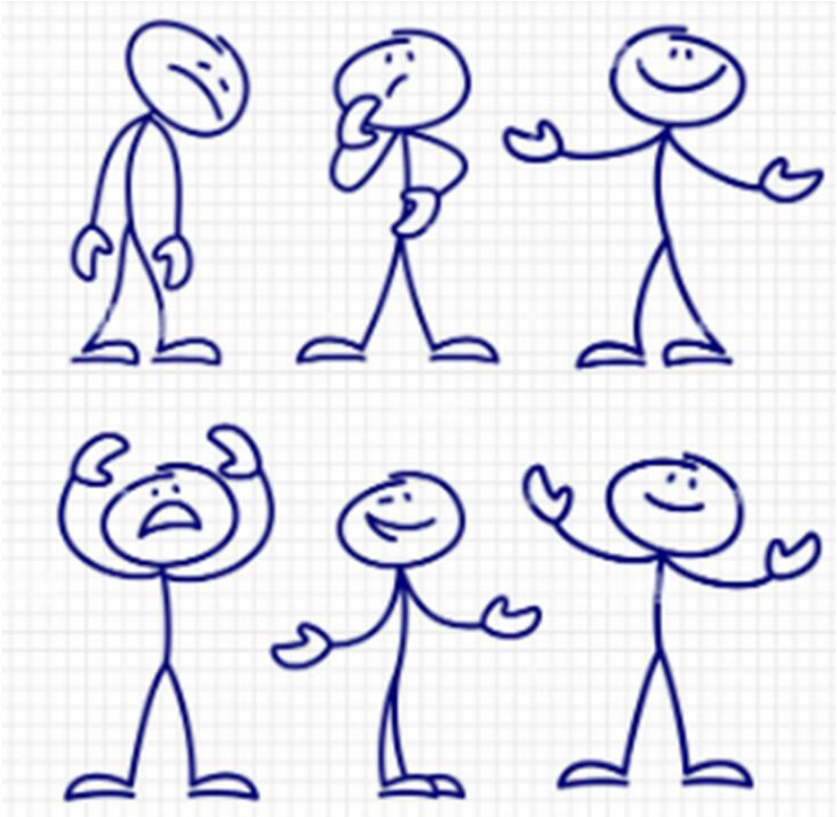
Post Layout Simulation

Post-Layout Simulation Flow:

- Layout ↔ Schematic Check (LVS)
- Parasitic Extraction → SPEF/DSPF file
- Netlist + Parasitics → SPICE / FastSPICE tools
- Run transient, timing, or power simulations

Summary

- Design Flow & File Formats defines the step-by-step physical design process Involves multiple file formats
- Extracts resistive, capacitive, and inductive effects from interconnects
- Essential for accurate timing, power, and signal integrity analysis
- Detects performance bottlenecks and functional/timing failures before tape-out



Thank you !

Happy Learning