CMOS Circuit Design Styles PTL and TG

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Outline

- Merits of Static CMOS Circuits
- Bubble Pushing and CMOS circuits
- Ratioed Circuits
- Cascode Voltage Switch Logic (CVSL)
- Pass Transistor Logic (PTL)
- Transmission Gate Circuits

Introduction

- Static CMOS circuits are used for the vast majority of logic gates in integrated circuits as they have
  - Good noise margins,
  - Fast and low power
  - Insensitive to device variations
  - Easy to design
  - Widely supported by CAD tools
  - Readily available in standard cell libraries

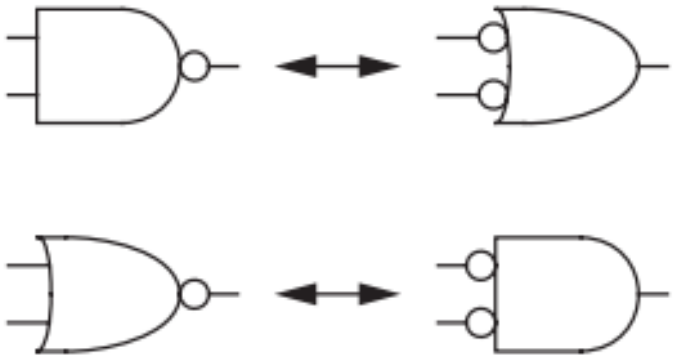
Static CMOS

- Designers accustomed to AND and OR functions must learn to think in terms of NAND and NOR to take advantage of static CMOS
- In manual circuit design, this is often done through bubble pushing
- Compound gates are particularly useful to perform complex functions with relatively low logical efforts
- Using smaller pMOS transistors can reduce power, area, and delay

Bubble Pushing

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$

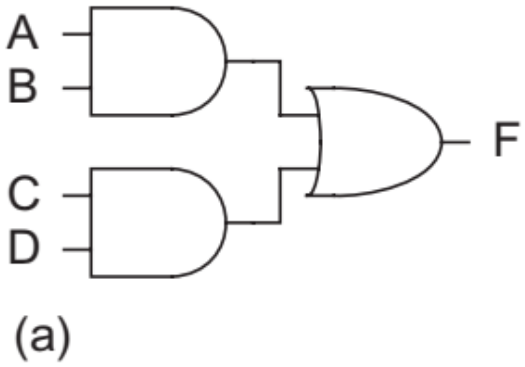
$$\overline{A + B} = \bar{A} \cdot \bar{B}$$



- CMOS stages are inherently inverting, so AND and OR functions must be built from NAND and NOR gates
- NAND gate is equivalent to an OR of inverted inputs
- NOR gate is equivalent to an AND of inverted inputs

Example

Design a circuit to compute F = AB + CD using NANDs and NORs



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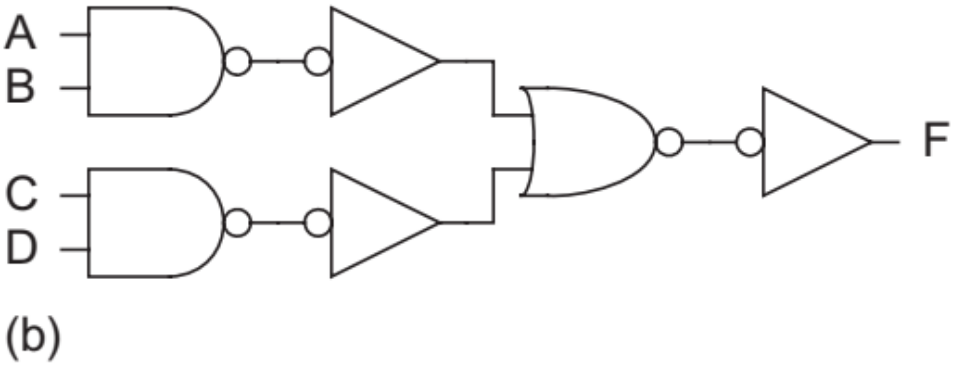

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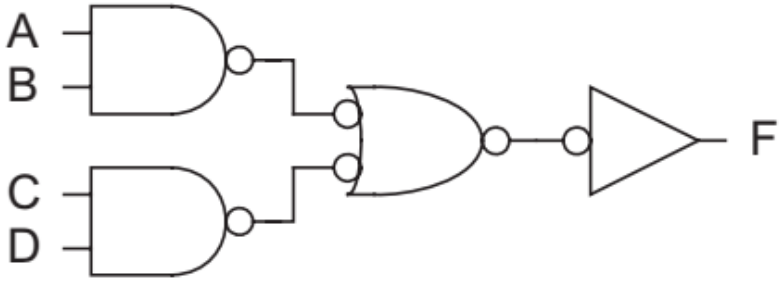

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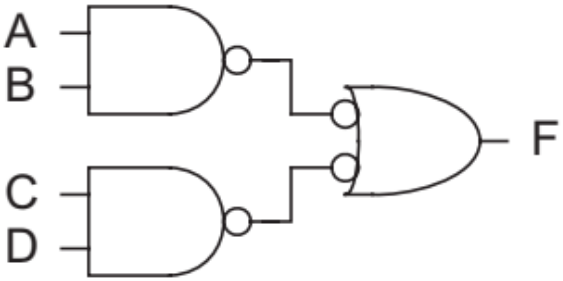
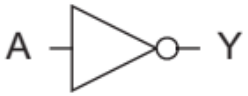


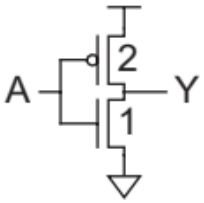
(d)

AOI Gates

Unit Inverter

$Y = \overline{A}$



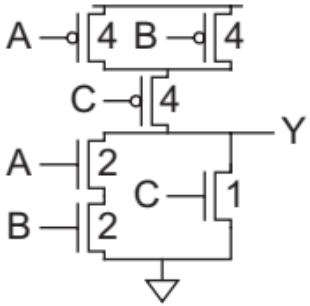


$g_A = 3/3$

$p = 3/3$

AOI21

$Y = \overline{A \cdot B + C}$



$g_A = 6/3$

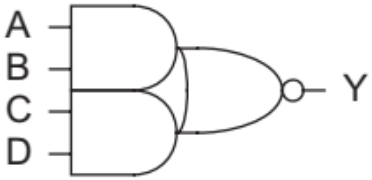
$g_B = 6/3$

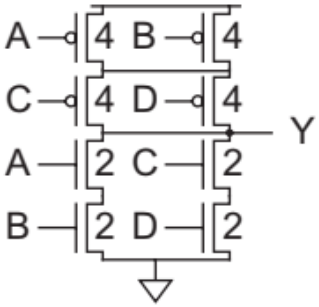
$g_C = 5/3$

$p = 7/3$

AOI22

$Y = \overline{A \cdot B + C \cdot D}$





$g_A = 6/3$

$g_B = 6/3$

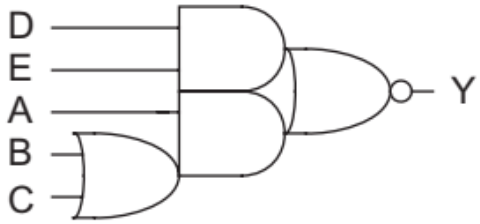
$g_C = 6/3$

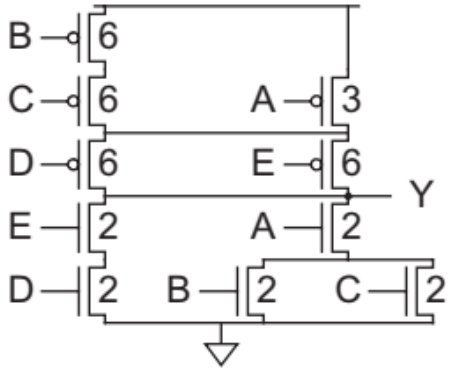
$g_D = 6/3$

$p = 12/3$

Complex AOI

$Y = \overline{A \cdot (B+C) + D \cdot E}$





$g_A = 5/3$

$g_B = 8/3$

$g_C = 8/3$

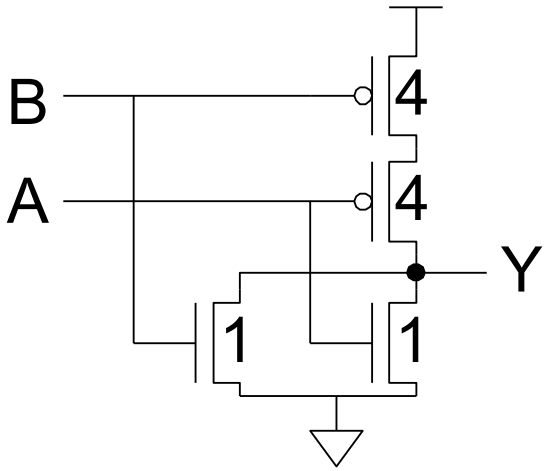
$g_D = 8/3$

$g_E = 8/3$

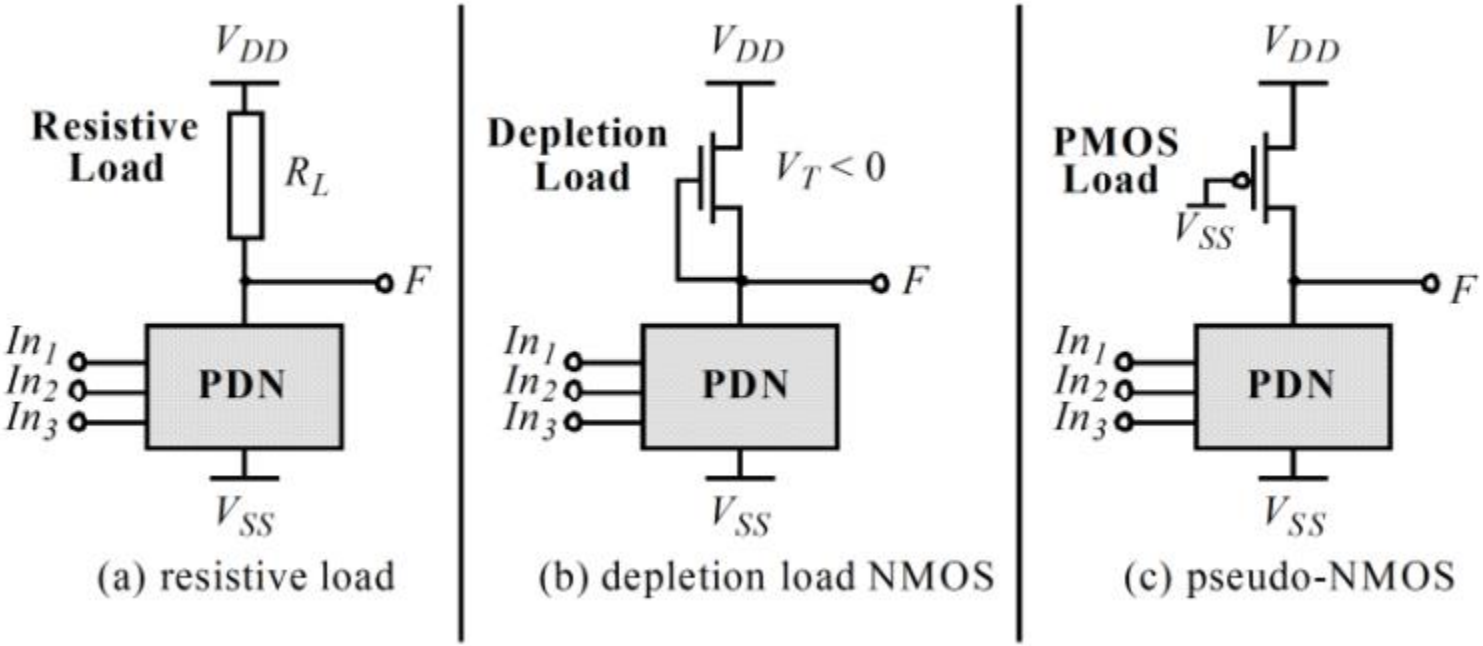
$p = 16/3$

Introduction

- What makes a circuit fast?
  - $I = C\,dV/dt \quad \rightarrow \quad t_{pd} \propto (C/I)\,\Delta V$
  - low capacitance
  - high current
  - small swing
- Logical effort is proportional to C/I
- pMOS are the enemy!
  - High capacitance for a given current
- Can we take the pMOS capacitance off the input?
- Various circuit families try to do this…

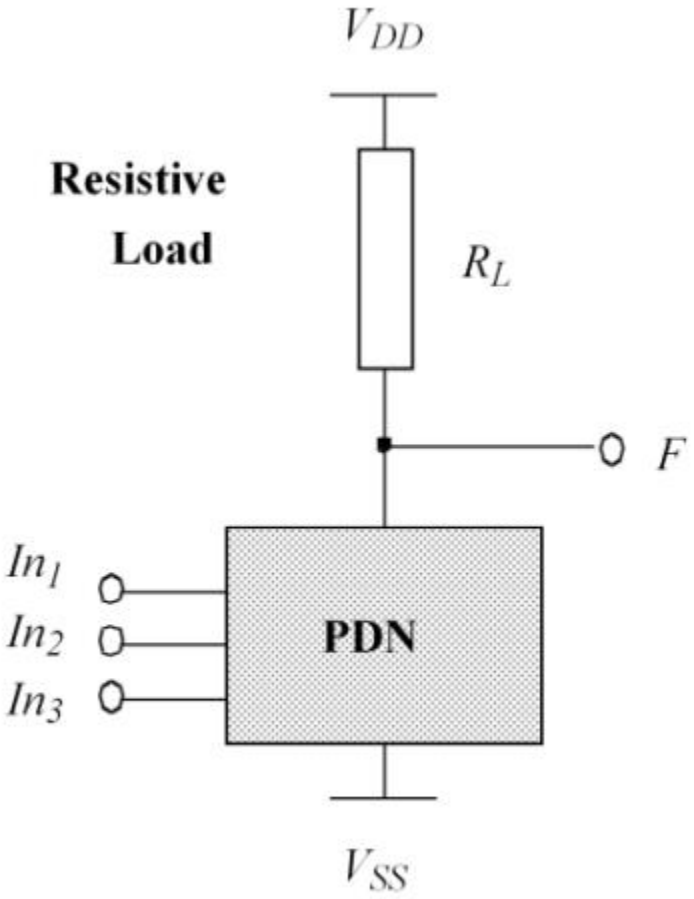


Ratioed Logic



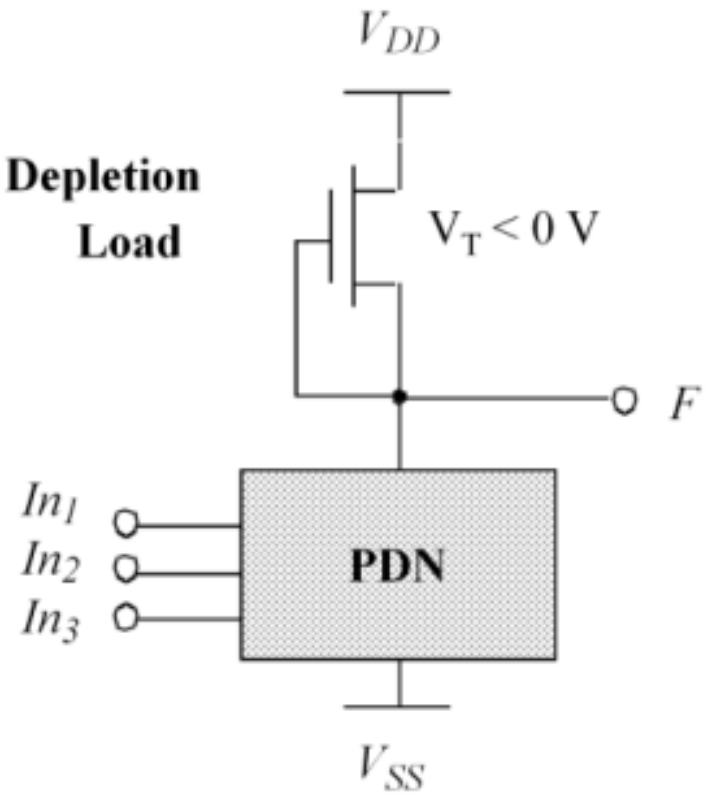
Goal : to reduce the number of devices over complementary CMOS

Ratioed Logic

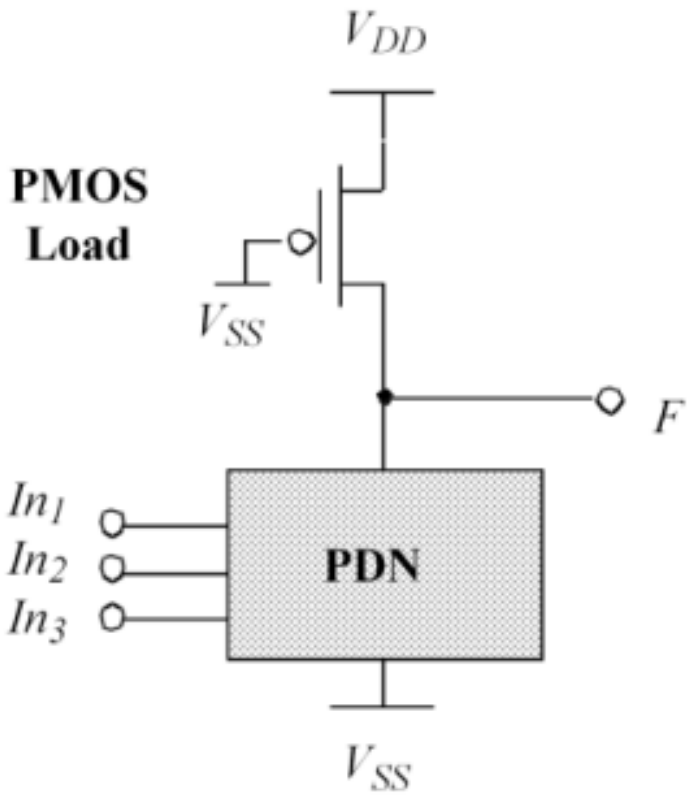


- **N transistors + Load**
- **$V_{OH} = V_{DD}$**
- $V_{OL} = \frac{R_{PDN}}{R_{PDN} + R_L} V_{DD}$
- **Assymmetrical response ($t_r > t_f$)**
- **Static power consumption**
- **$t_{pLH} = 0.69 R_L C_L$**

Active Loads

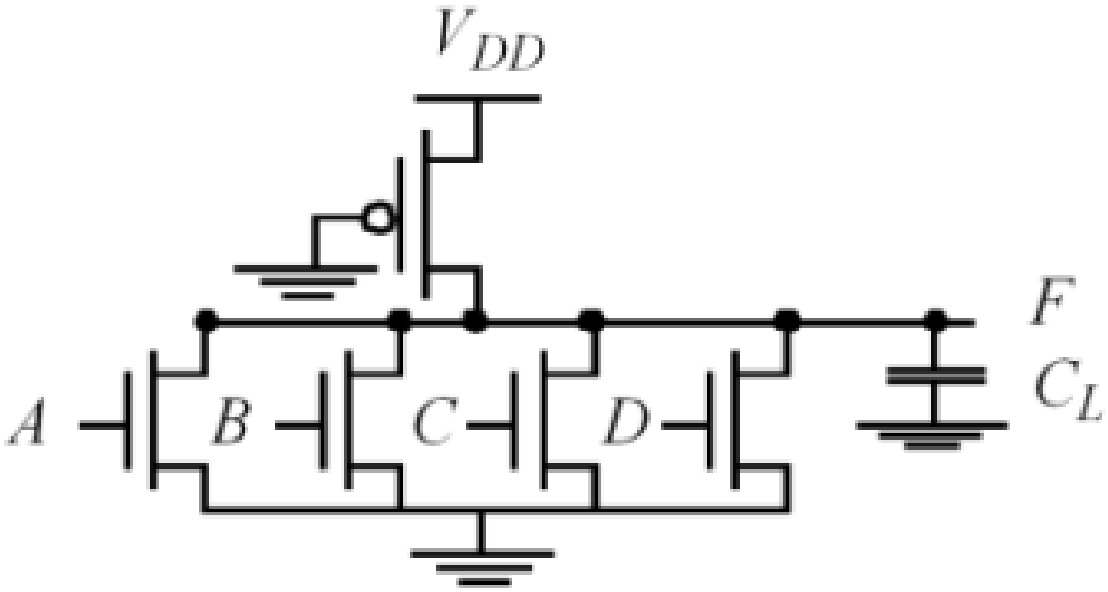


depletion load NMOS



pseudo-NMOS

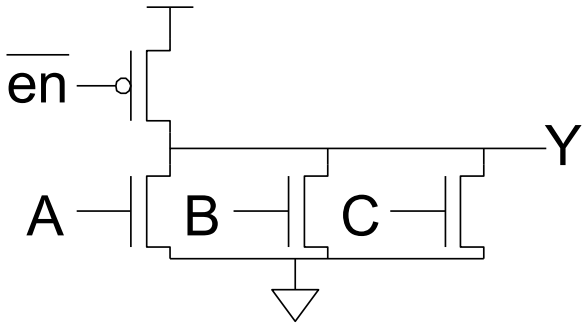
Pseudo NMOS NOR Gate



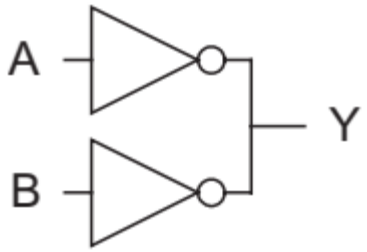
Smaller Area and load but Static Power Dissipation

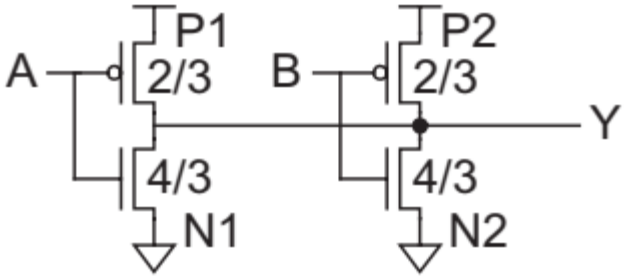
Pseudo-nMOS Power

- Pseudo-nMOS draws power whenever Y = 0
  - Called static power $P = I_{DD}V_{DD}$
  - A few mA / gate * 1M gates would be a problem
- Use pseudo-nMOS sparingly for wide NORs
- Turn off pMOS when not in use



Ganged CMOS

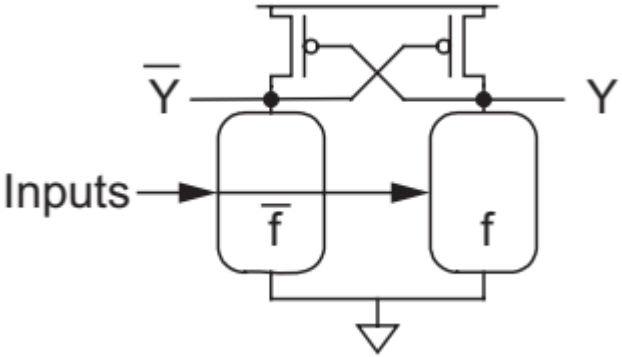


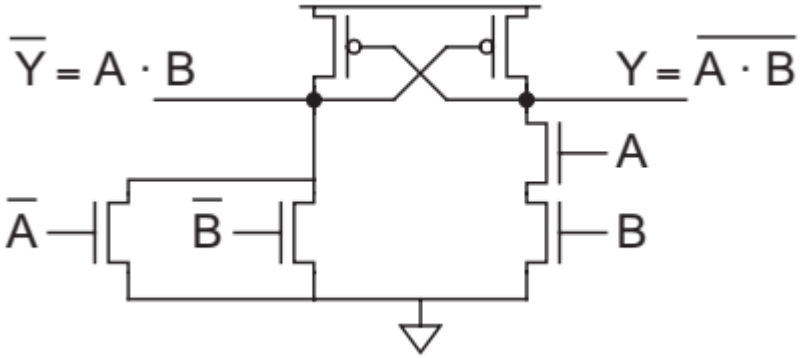


$g_u = 1$
$g_d = 2/3$
$g_{avg} = 5/6$

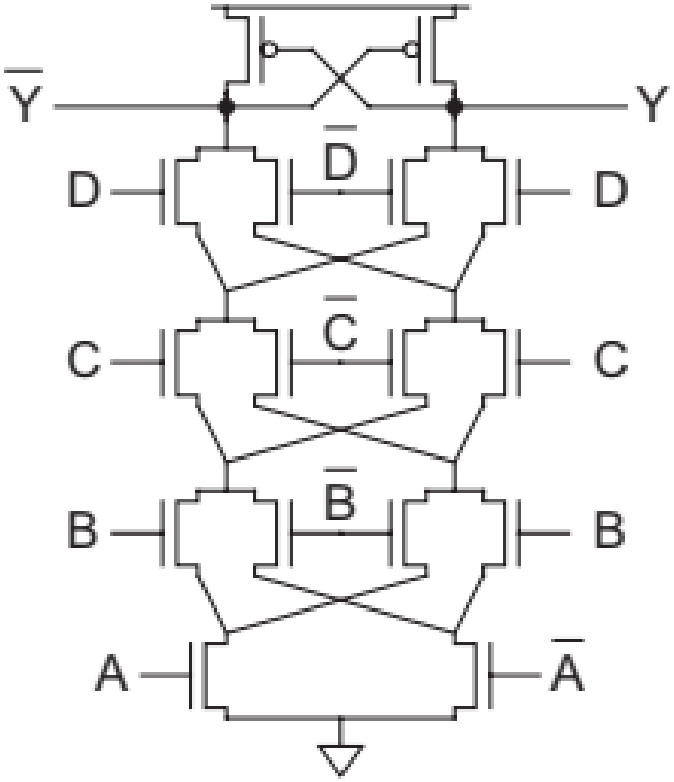
A	B	N1	P1	N2	P2	Y
0	0	OFF	ON	OFF	ON	1
0	1	OFF	ON	ON	OFF	~ 0
1	0	ON	OFF	OFF	ON	~ 0
1	1	ON	OFF	ON	OFF	0

Cascode Voltage Switch Logic





CVSL – XOR Gate 4 Input



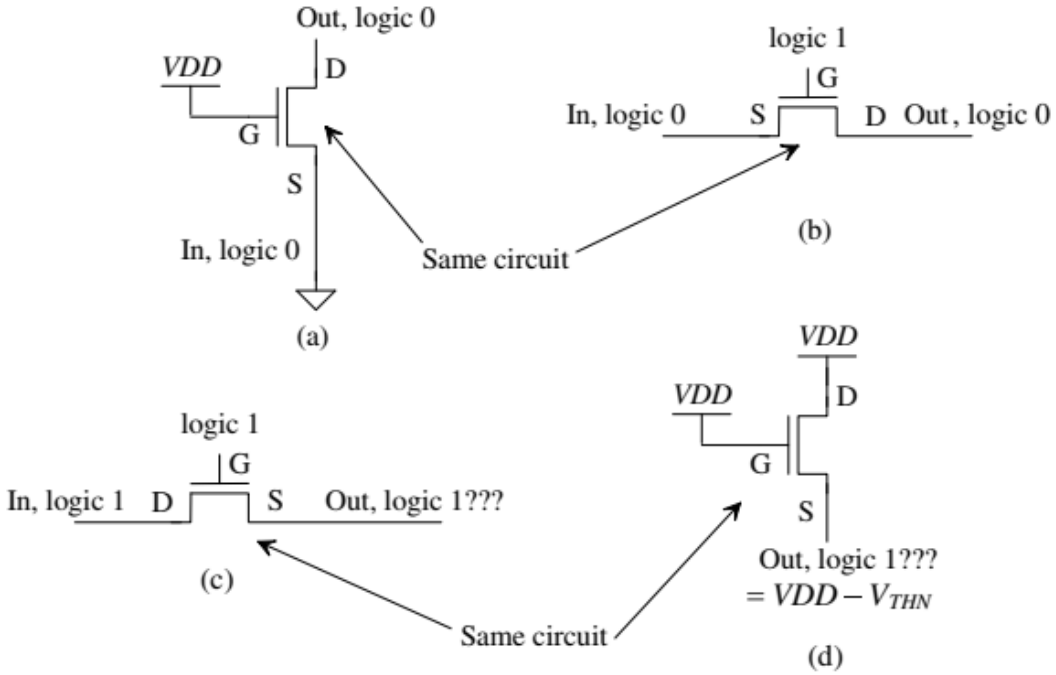
4-Input CVSL XOR Gate

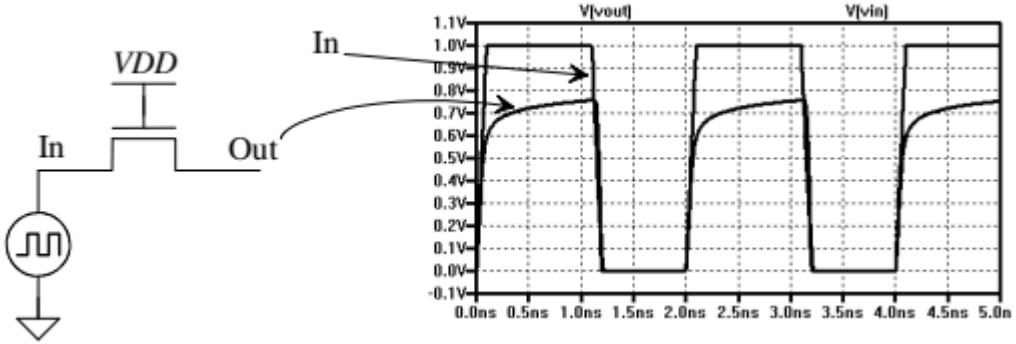
Summary CVSL

- A differential CMOS logic style that uses a dual-rail structure to provide both true and complementary outputs.
- High speed, reduced power dissipation, and good noise immunity due to its differential nature.
- Increased transistor count and design complexity compared to standard CMOS.
- Suitable for high-performance VLSI circuits, especially in noise-sensitive and high-speed applications

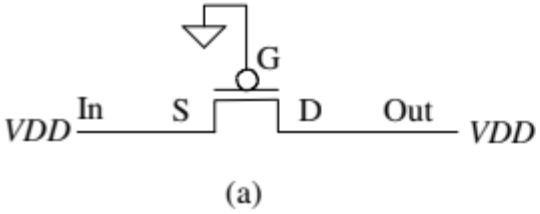
Pass Transistor Logic

NMOS Switch as Pass Gate

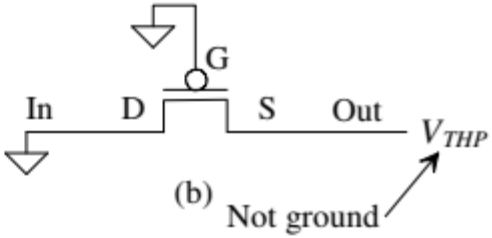




PMOS Switch as Pass Gate



(a)



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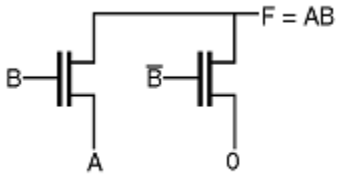
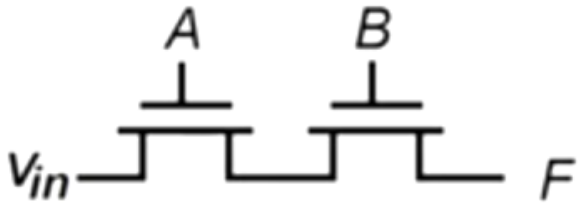
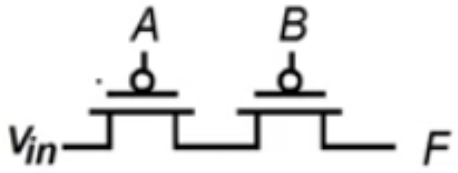


AND gate using pass transistor logic

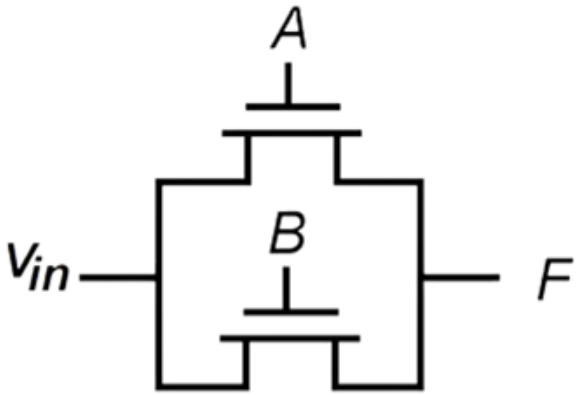
Pass Transistor Gate



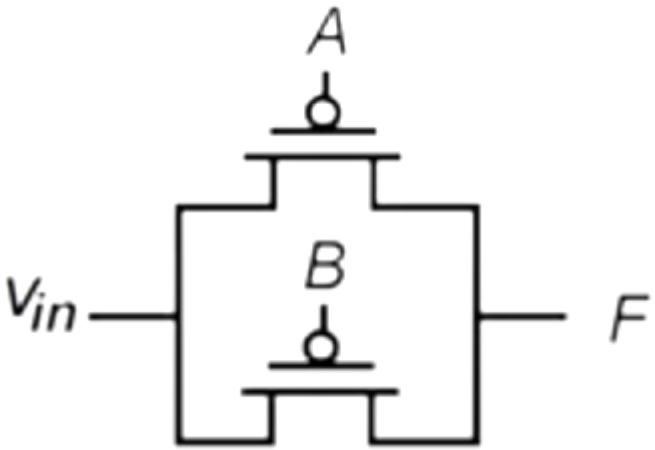
AND Gate



NOR Gate

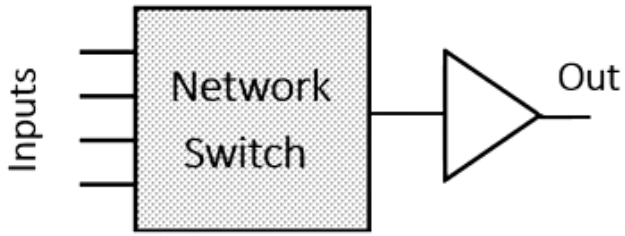


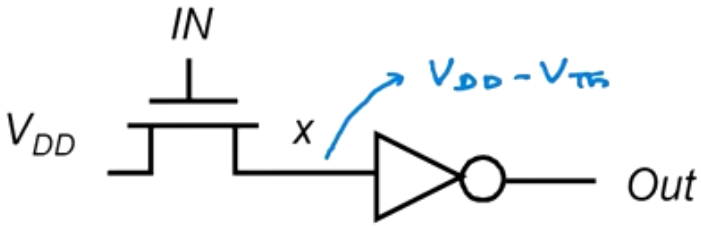
OR Gate



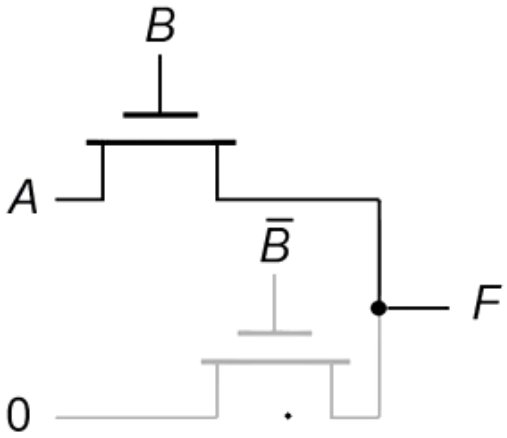
NAND Gate

Pass Transistor Gate



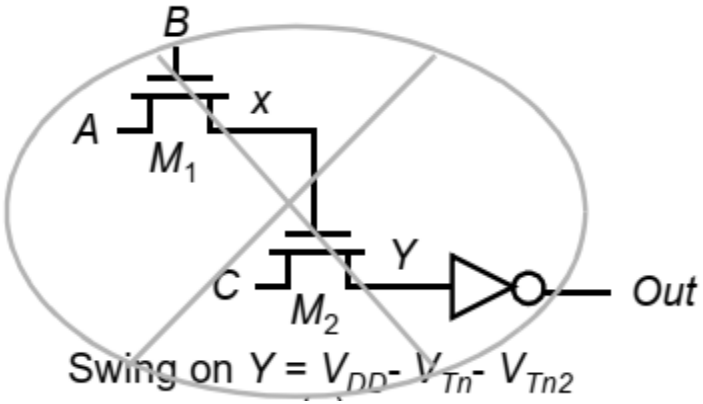


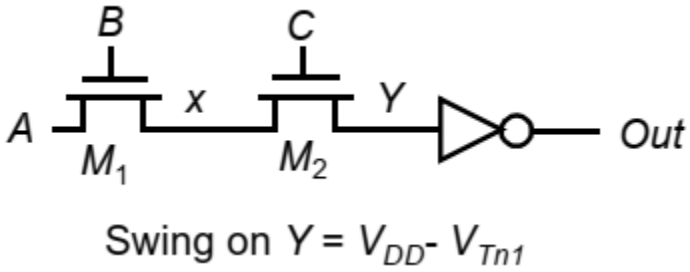
Implement $F = \overline{(A + B).C} \; \overline{(A + B)} + \bar{C} \; \bar{A}.\bar{B} + \bar{C}$



Problem with PTL

Pass Transistor Logic gates cannot be cascaded by connecting the output of a pass gate to the gate input of another pass transistor

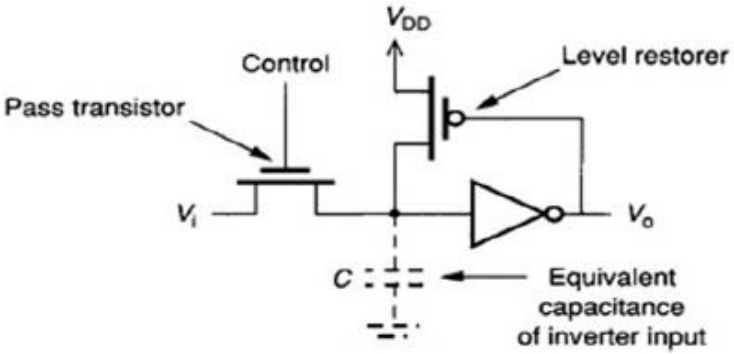


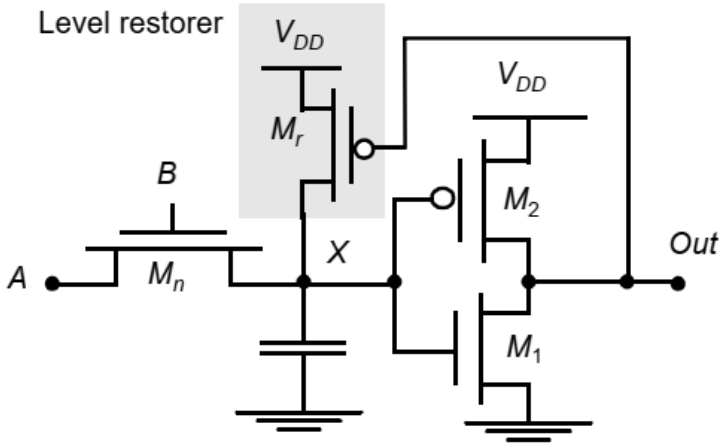


Level Restorer with PTL

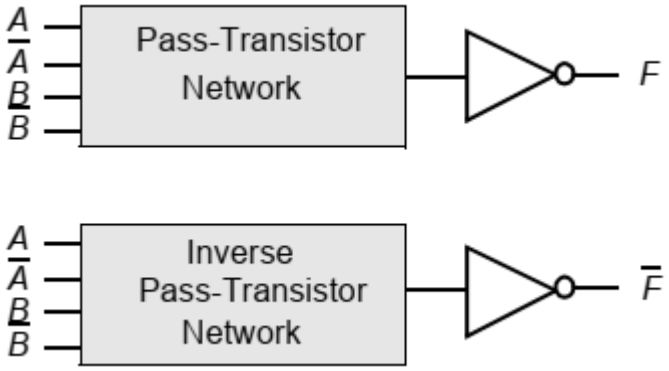
A level restorer is typically implemented using PMOS transistors.

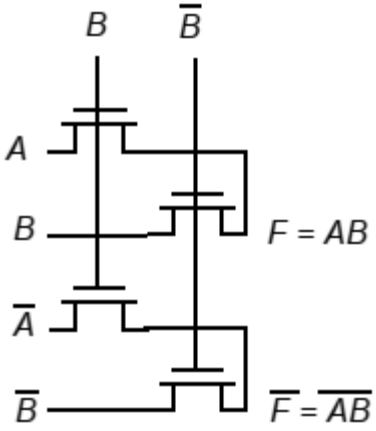
It works by pulling the degraded high signal back to the full Vdd .



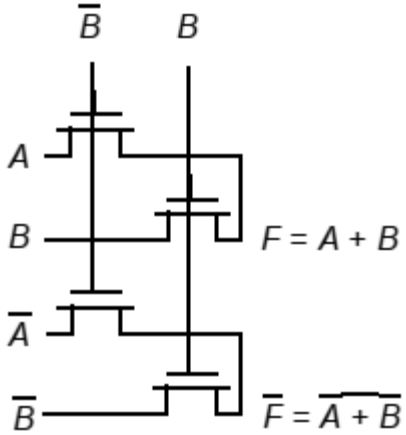


Complimentary/Differential Pass Transistor Logic

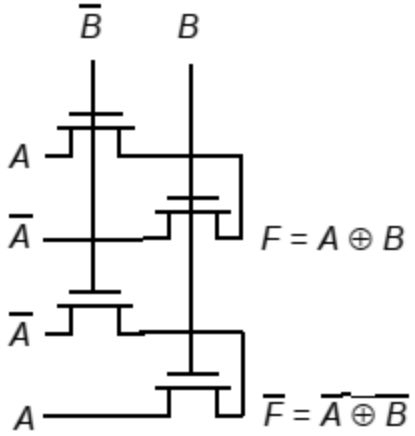




AND/NAND

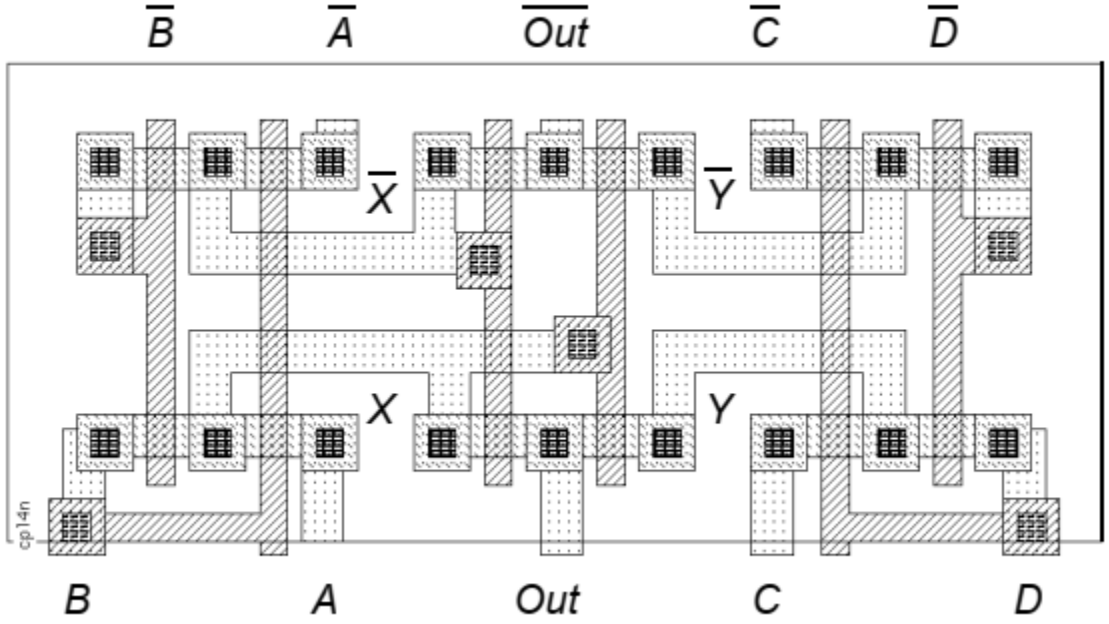


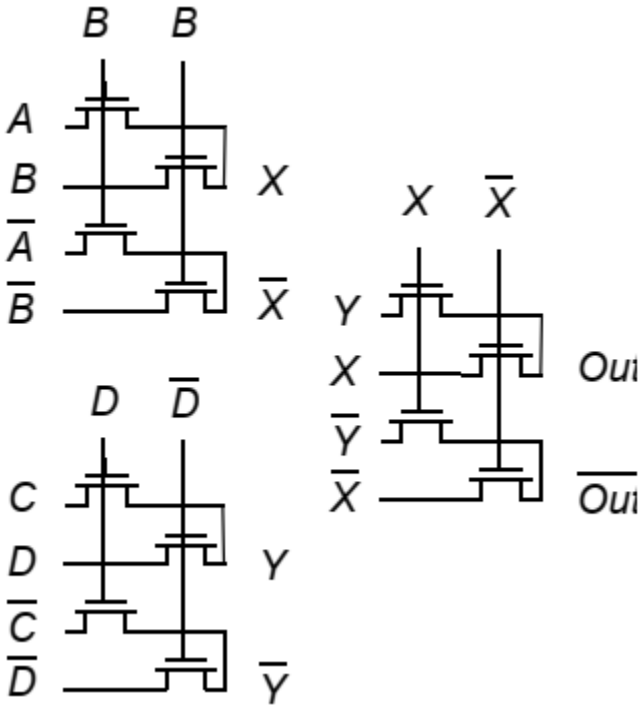
OR/NOR



XOR/NXOR

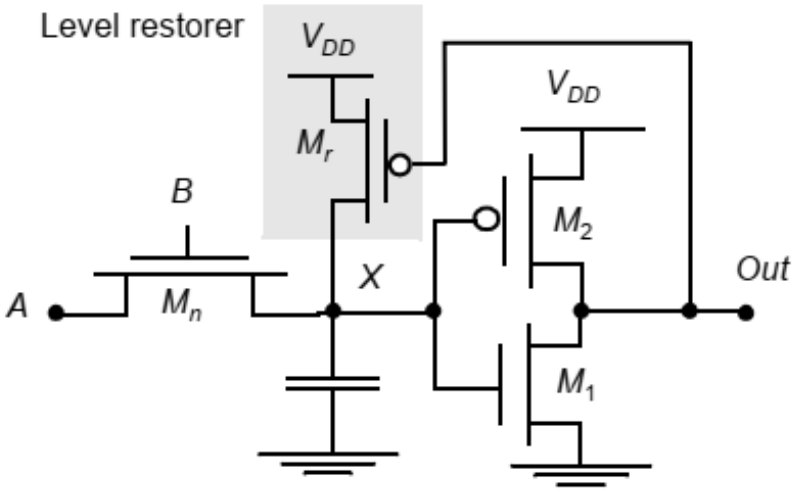
NAND Gate (4 Input CPL)





Robust and Efficient Pass-Transistor Design

- Solution for robust and efficient PTL
  - Level Restoration
  - Multiple Threshold Transistors
  - Transmission Gate Logic



Level Restoration

Robust and Efficient Pass-Transistor Design

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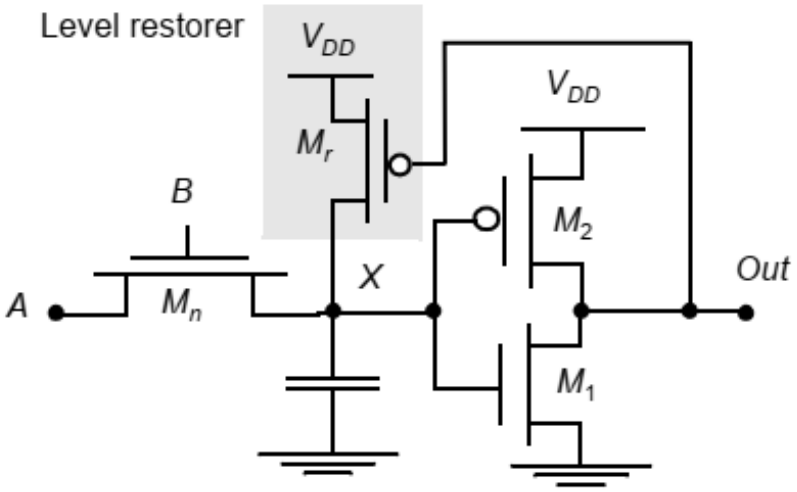
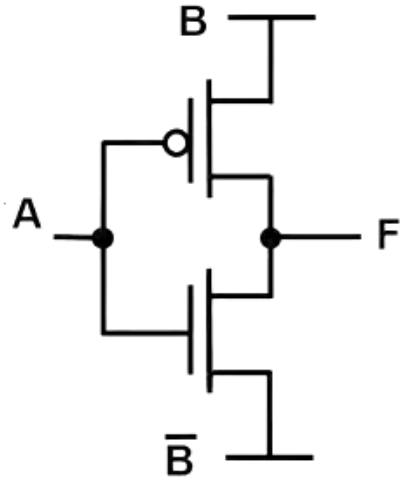
  - Multiple Threshold Transistors
  - Transmission Gate Logic

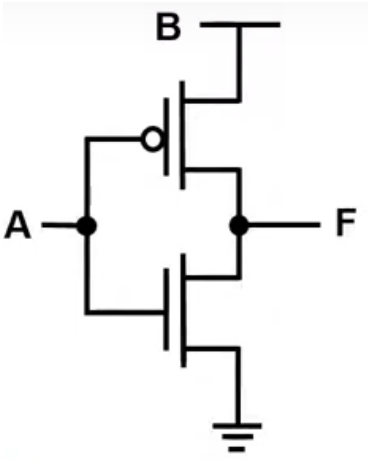


Level Restoration

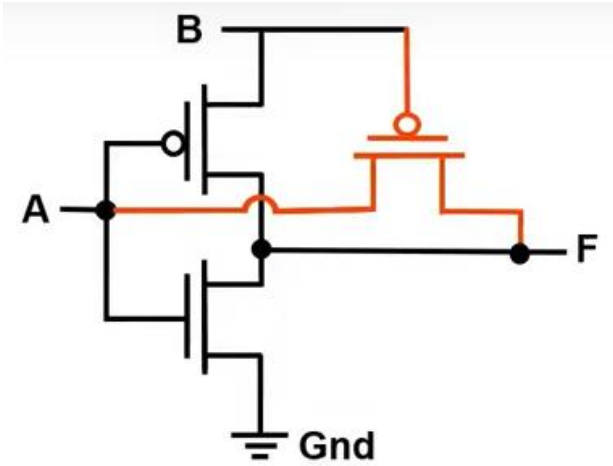
Pass Transistor Logic Design



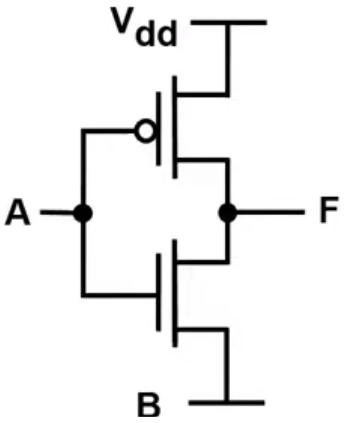
Controlled Inverter



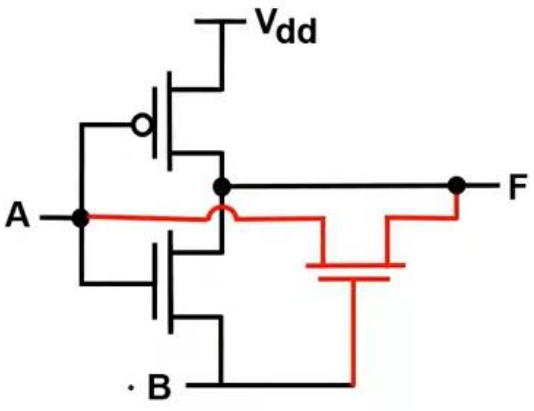
Inverter with Tristate



XOR Gate



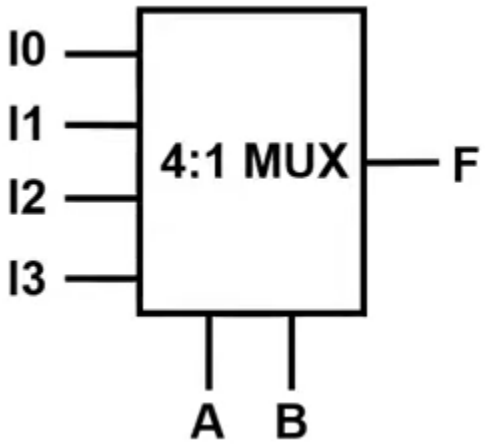
Inverter with Tristate

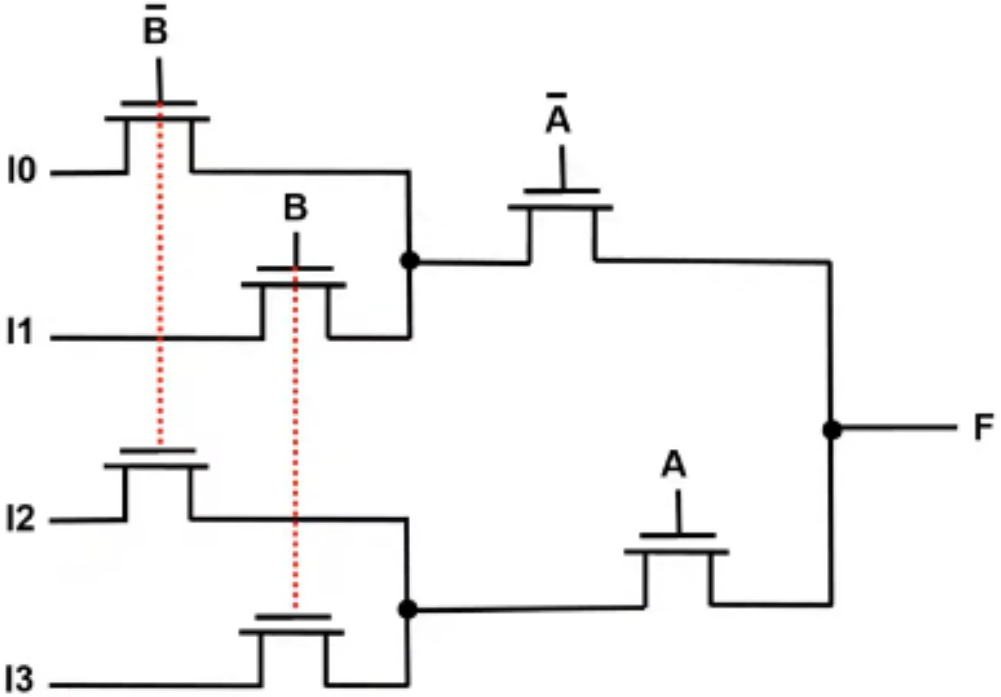


XNOR Gate

PTL Based Mux

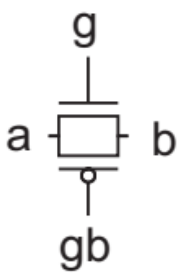
$$F = \bar{A}\,\bar{B}I0 + \bar{A}BI1 + A\bar{B}I2 + ABI3$$

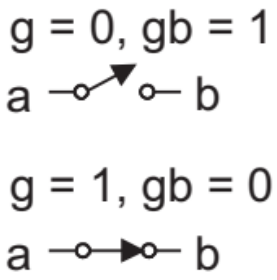


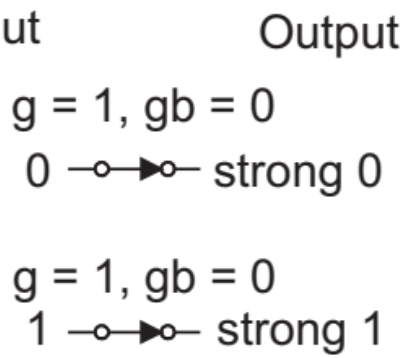


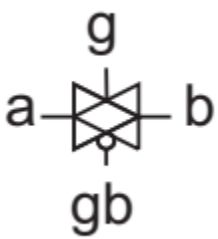
Transmission Gate Logic

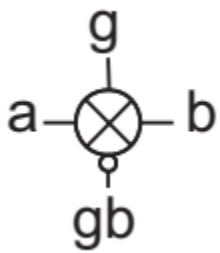
- CMOS transmission gates overcome the weak logic levels of single-pass transistors.
- Use two complementary transistors (nMOS + pMOS) to ensure robust logic levels.

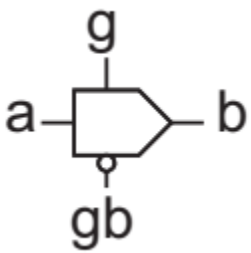




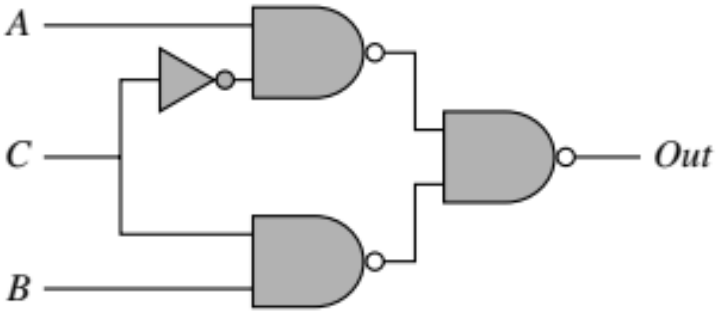






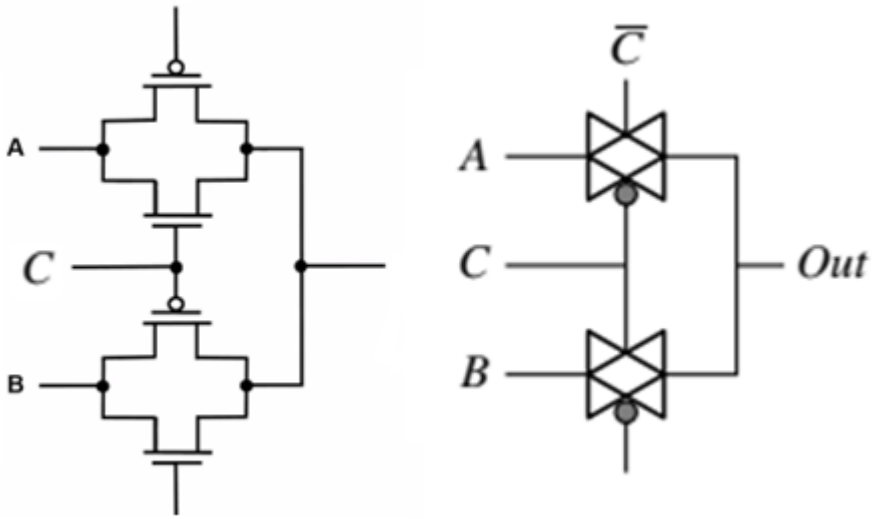


Mux using Transmission Gate Logic



Transistor count: 14

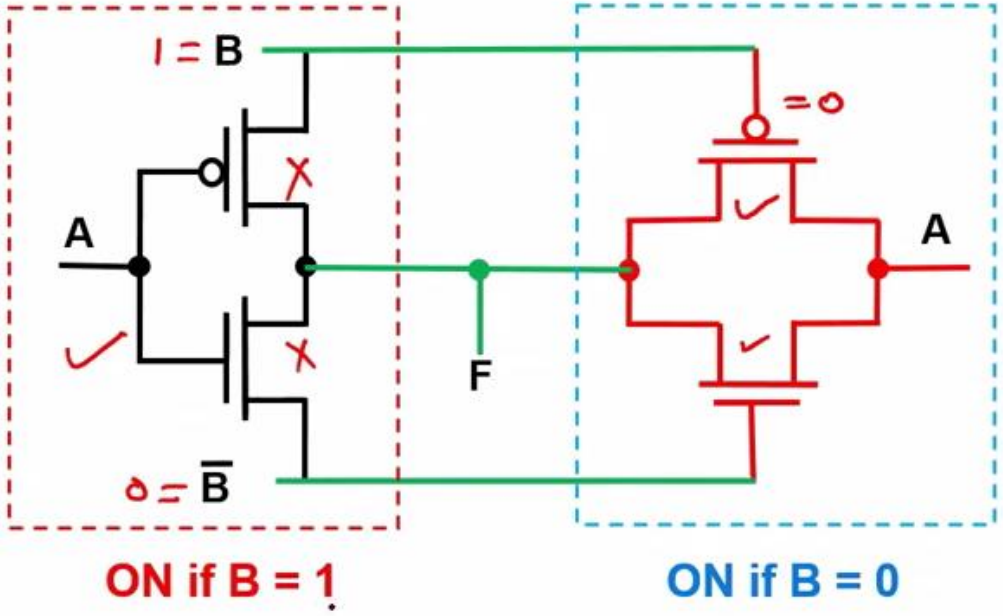
- 4 transistors per NAND gate,
- 2 for the inverter

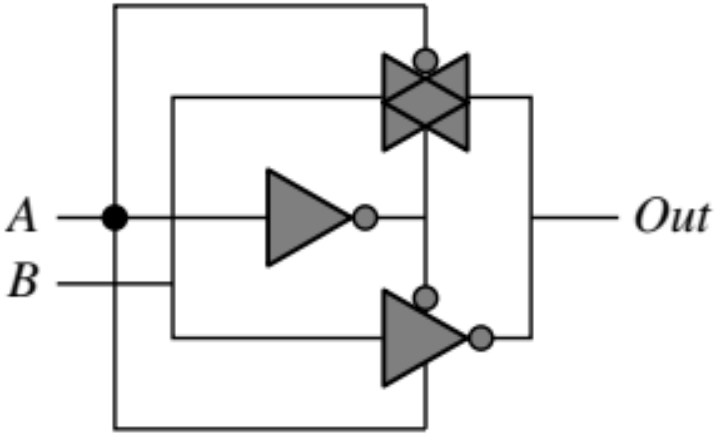


Transistor count: 6

- 4 for transmission gates
- 2 for inverter

XOR Gate using Transmission Gate Logic





Transistor Counts :

- 12 transistors for conventional CMOS
- 6 or 8 Transistors for TG

Thank you !

Happy Learning