Aspects of ASIC Design

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Outline

Introduction to ASIC Design

- **Application-Specific Integrated Circuit (ASIC)**, customized for a particular use, rather than intended for general-purpose use
- Semiconductor industry evolved from first IC in early 1970 and matured rapidly (SSI, LSI, VLSI , ULSI)
- We select some ICs from the catalog and data sheets and purchase them from distributors as **Standard IC**s.
- With the advent of VLSI technology , engineers realize the advantages of **Customized or tailored** particular system or application rather than Standard IC
- Microelectronic systems are combination of **standard function (Std. ICs)** with one or more **custom ICs**

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Examples of ASICs

- **Cryptography Chips**: Designed for encryption and decryption algorithms, such as AES, RSA hardware accelerators.
- **Graphics Processing Units (GPUs)**: Custom-designed ASICs for rendering images and graphics (though some GPUs can be general-purpose, many include ASIC elements).
- **Networking Chips**: Switches and routers often contain ASICs optimized for handling data packets.
- **Digital Signal Processors (DSPs)**: ASICs used in audio, video, and communication processing applications.
- **Automotive Control Units**: ASICs specifically designed for controlling various functions in vehicles like ABS, engine management, and infotainment systems.
- **Bitcoin Mining Chips (e.g., SHA-256 ASICs)**: Used in cryptocurrency mining, these ASICs are optimized for solving cryptographic hash functions.

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- **Microcontrollers (MCUs)**: General-purpose ICs used in a wide range of embedded applications.
- **Field-Programmable Gate Arrays (FPGAs)**: Reconfigurable ICs that can be programmed after manufacturing for various applications.
- **General-Purpose CPUs**: Central Processing Units used in personal computers, servers, and mobile devices.
- **Memory Chips (RAM/ROM)**: ICs used for storing data, with no specific application beyond storage.
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- **Energy Efficiency**: Reduces power consumption by eliminating unnecessary components.
- **Compact Size**: Custom design leads to smaller, lighter chips.
- **High Speed**: Streamlined architecture enables faster operation.
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Where ASIC is Not Preferred

- **High Development Costs**: Expensive to design and manufacture, impractical for low-volume production.
- **Limited Flexibility**: Cannot be reprogrammed once manufactured, unlike FPGAs.
- **Long Time to Market**: Lengthy design, testing, and manufacturing process.
- **Design Complexity**: Requires specialized expertise and tools, increasing development effort.
- **Risk of Obsolescence**: Market or technology changes can render the ASIC obsolete after completion.
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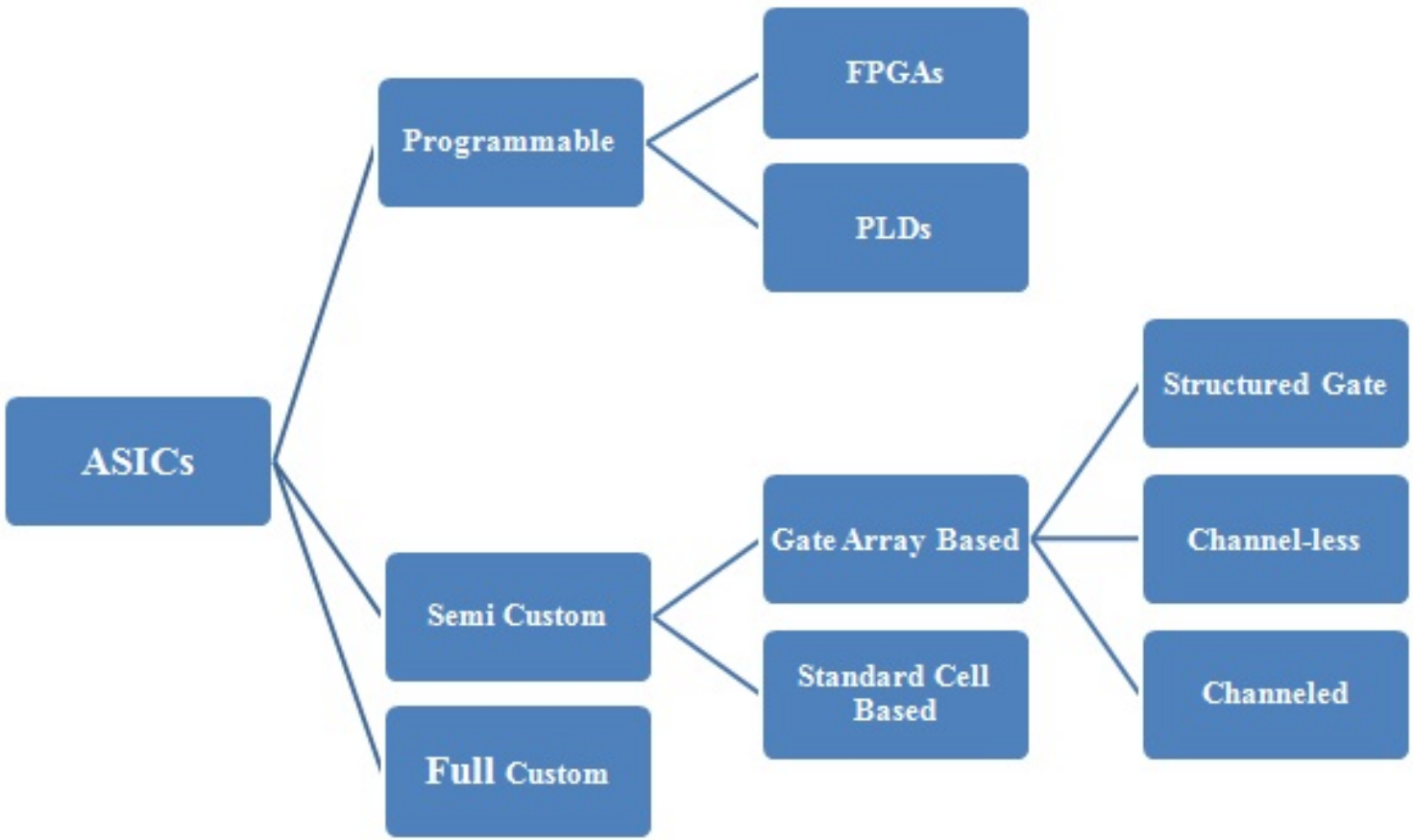
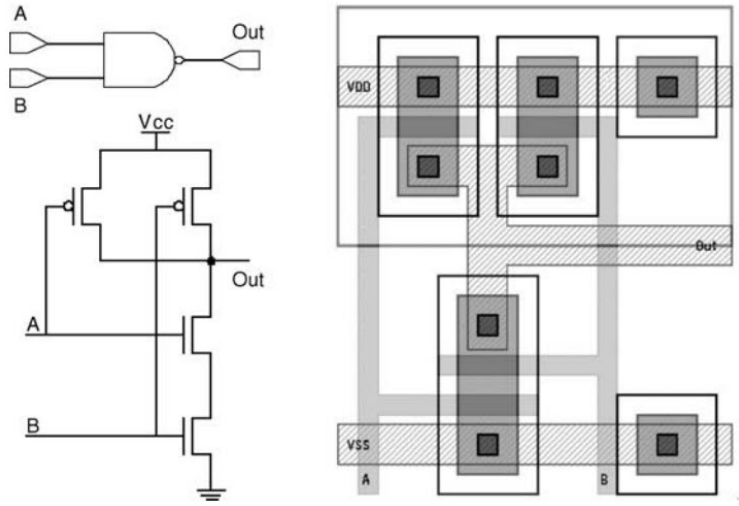
ASIC Classification



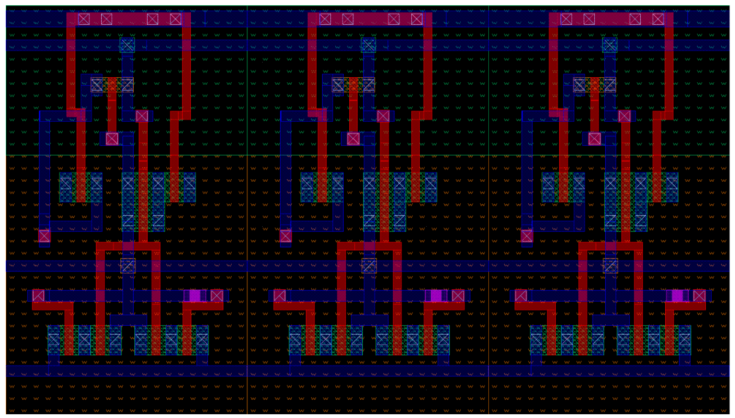
Full-Custom ASIC

Salient Features:

- Every transistor and component is custom-designed for the specific application.
- Offers maximum performance and efficiency.
- Extremely high design cost and complexity.
- Longer time-to-market due to detailed design.
- Used in high-performance applications where power, speed, and area need to be optimized.



NAND Gate

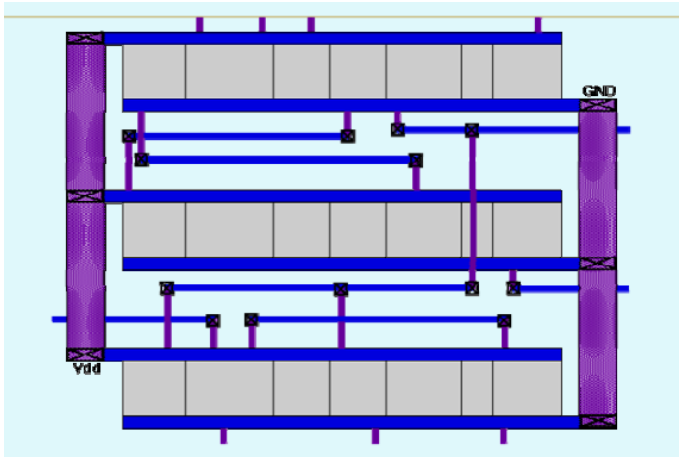


Memory Layout

Semi-Custom ASIC

Salient Features:

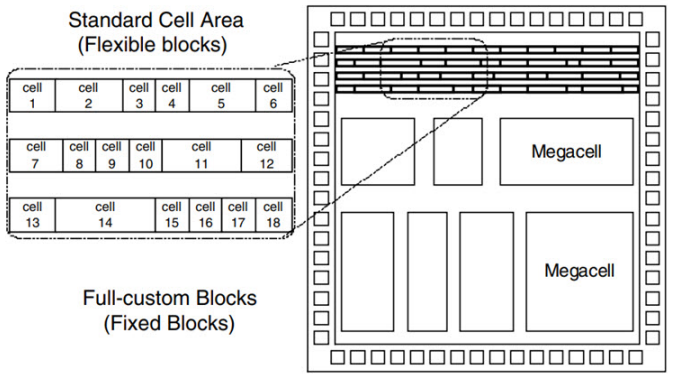
- Combines custom-designed components with pre-built standard cells.
- Offers a balance between customization and design time.
- Faster and less expensive to develop compared to full-custom ASICs.
- Standard cells handle common logic functions, while custom blocks handle application-specific tasks.
- Commonly used in industrial and consumer electronics.



DSP Processor

Standard Cell Based (CBIC

- It used predesigned logic cells (AND gates, OR gates, muxes, FF etc..)
- The standard cell areas are built of rows of std. cells like wall built of brick.
- Std. cells may be large predefined cells, (microcontroller) known as megacells/ megafunctions.
- Each cell can be optimized individually.
- Designer save time, money, and reduce risk by using a predefined, pretested, precharacterized std. cell library



Gate Array Based ASICs

- In gate-array based ASICs, the transistors are predefined on the silicon wafer.
- Designers cannot alter the placement of the transistors,
- Designer can change the interconnections between transistors using the die's initial metal layers.
- Following are three types of Gate Array based ASICs
  - Channeled Gate Arrays
  - Channel-less Gate Arrays
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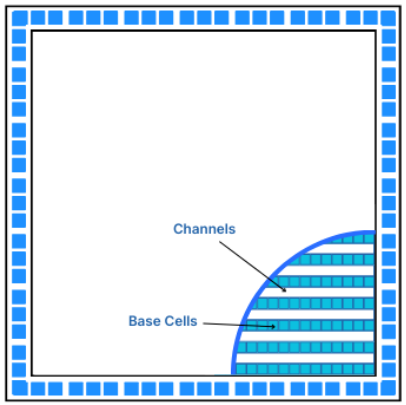
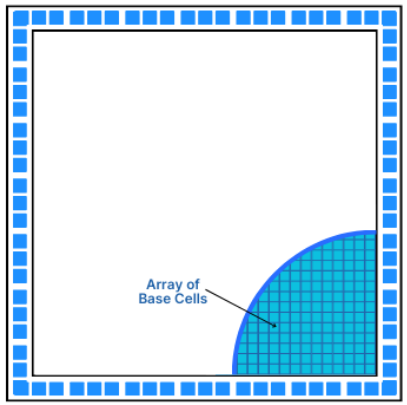
Gate Array Based ASIC

- **Channeled Gate Arrays:** Utilize predefined routing channels between logic cells for wire connections, suitable for standardized designs needing flexible interconnect pathways.
- **Channel-less Gate Arrays:** Lack predefined routing channels, allowing more compact designs by placing interconnects directly over cells, enhancing chip density.
- **Structured Gate Arrays:** Combine predefined logic blocks with customizable interconnect layers, offering a balance between design flexibility and rapid development.



Channeled Gate Arrays



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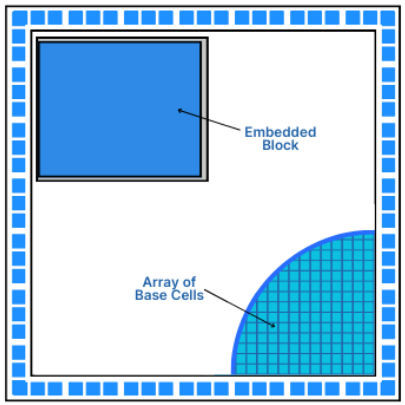

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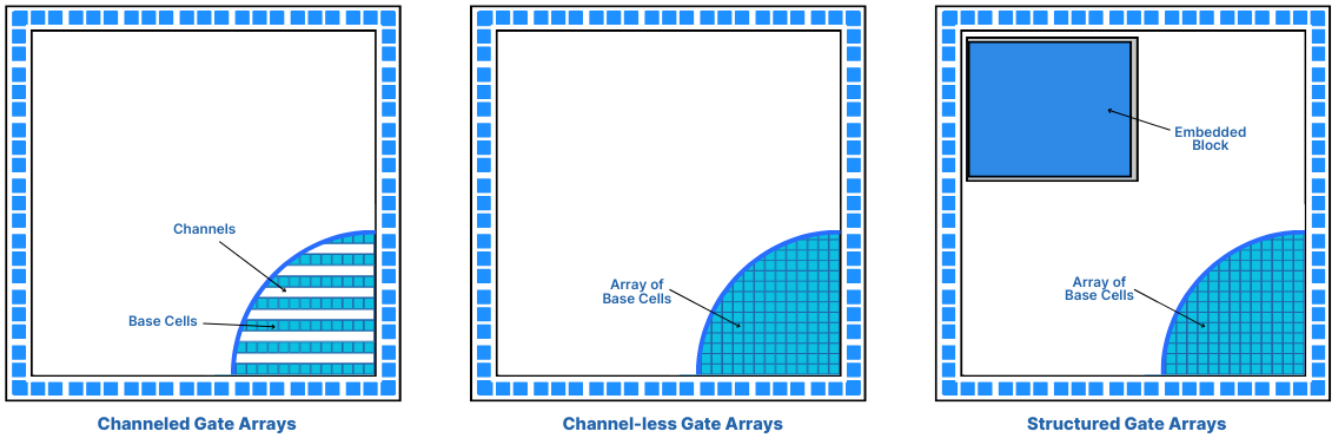

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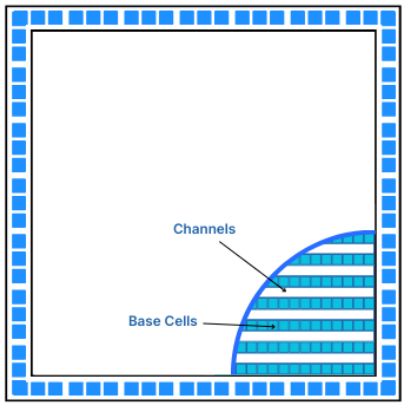

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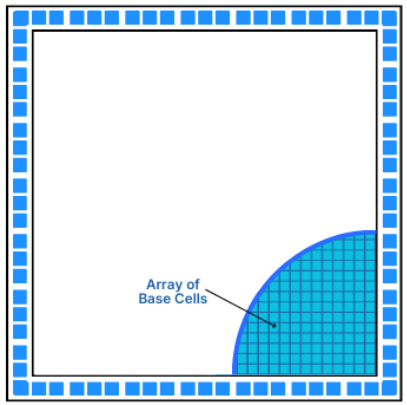

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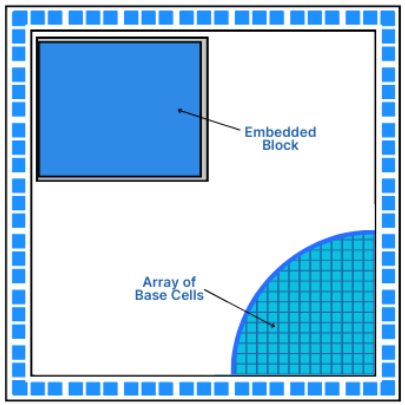

Structured Gate Arrays

Application-Specific Standard Products (ASSP)

Salient Features:

- Standardized ASIC designed for a specific application but not for a single customer.
- Pre-designed for large-scale commercial use.
- Limited customization options but highly cost-effective for mass production.
- Faster to market due to standardized design.
- Commonly used in consumer electronics, networking devices, and automotive systems.

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Programmable ASICs

- ASICs that allow for configuration and reconfiguration after manufacturing.
- **Types:**
  - **FPGAs (Field-Programmable Gate Arrays):**
    - Highly flexible and can be programmed multiple times.
  - **CPLDs (Complex Programmable Logic Devices):**
    - Suitable for simpler logic functions with quicker configuration times.
- **Advantages:**
  - Rapid prototyping and design iterations.
  - Flexibility to update designs post-production.
  - Cost-effective for low to medium volume applications.
- **Typical Applications:**
  - Prototyping and testing of digital circuits.
  - Telecommunications and networking.
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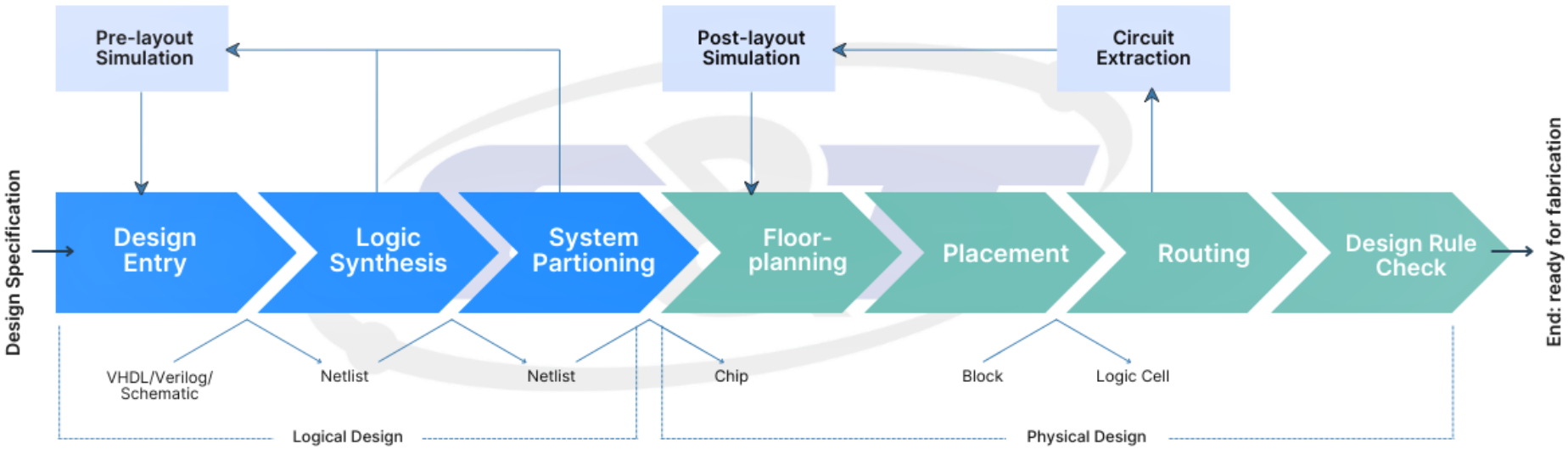
ASIC Design Flow



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[1] source: https://www.candtsolution.com

Comparison of FPGA and ASIC

Table 1: Comparison of FPGA and ASIC Features

Feature	**FPGA**	**ASIC**
Flexibility	High (reprogrammable)	Low (not reprogrammable)
Performance	Lower than ASIC	Higher performance for specific tasks
Power Consumption	Higher compared to ASIC	Lower (optimized for efficiency)
Development Cost	Low (no NRE cost)	High (high NRE cost)
Production Cost per Unit	Higher compared to ASIC	Lower (optimized for efficiency)
Time to Market	Shorter (reprogrammable, adaptable)	Longer (due to design and fabrication)
Reprogrammability	Yes (can change algorithms post-production)	No (fixed design)
Suitable Production Cycle	Small to medium scale	High volume (to offset NRE costs)
Design Cycle	Shorter	Longer


Consumer Electronics
Telecommunications
VLSI Technology
Automotive Industry
Healthcare

Thank You