Fabrication of MOSFET

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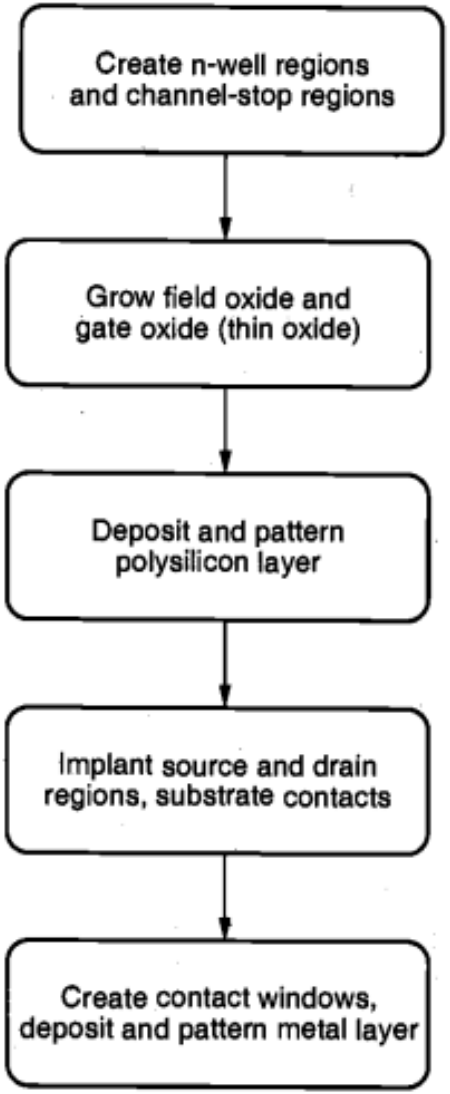
Introduction

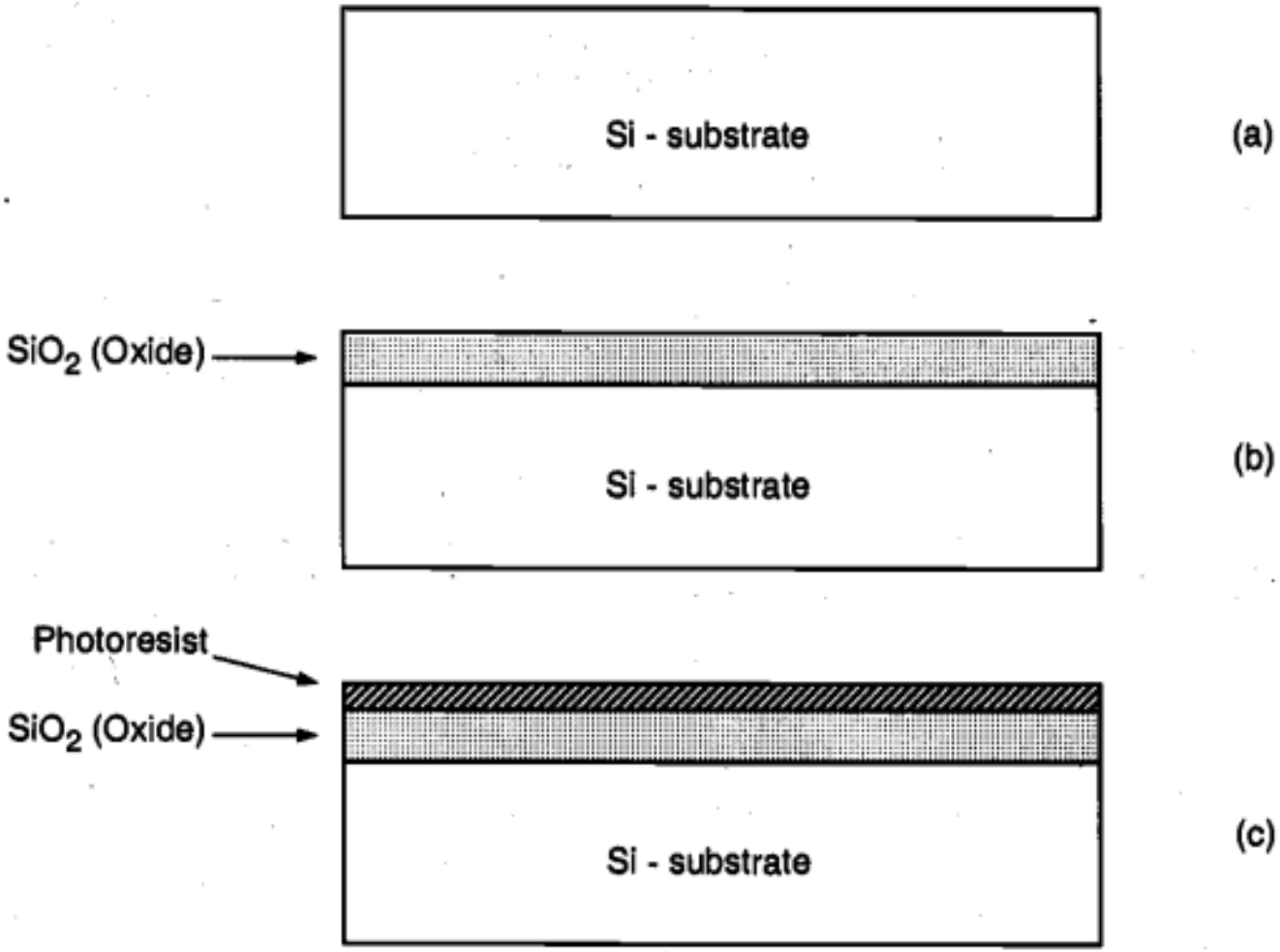
- CMOS Fabrication technology, requires both n-channel (nMOS) and (pMOS) transistor built on same substrate
- Special regions are required to accommodate nMOS and pMOS
- These regions are called as wells or tubs.
- A p-well is created in an n-type substrate , alternatively, an n-well is created in a p-type substrate

CMOS Fabrication Flow

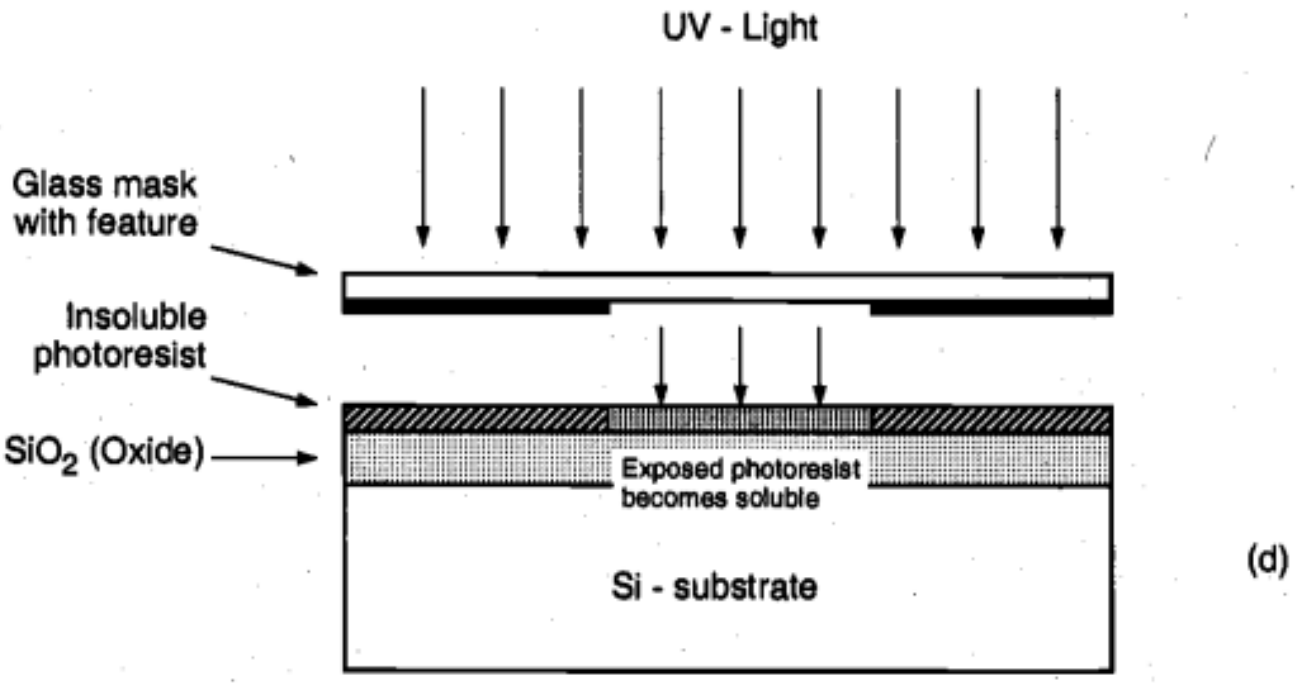


- Creation of the n-well regions for pMOS transistors, by impurity implantation into the substrate
- Thick oxide is grown in the regions surrounding the nMOS and pMOS active regions
- Thin gate oxide is subsequently grown on the surface through thermal oxidation
- followed by the creation of n+ and p+ regions (source, drain, and channelstop implants) and by final metallization (creation of metal interconnects).

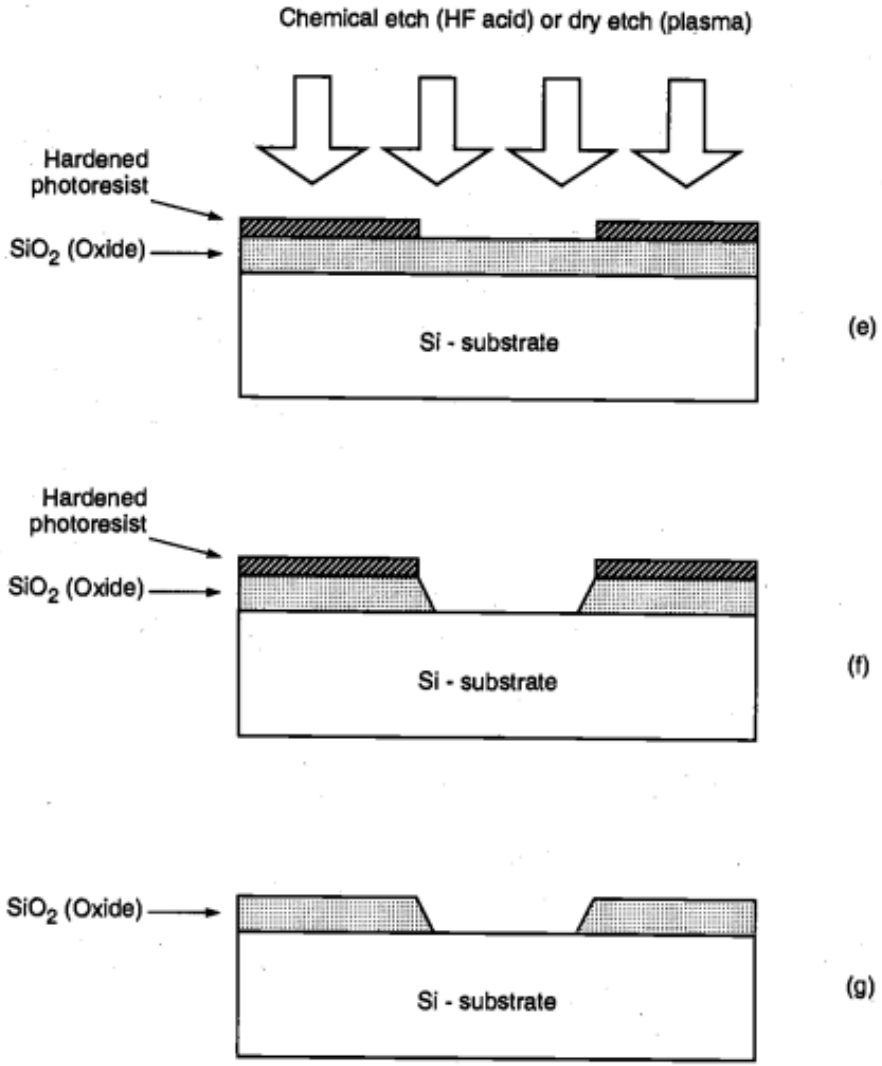
CMOS Fabrication Steps 1/



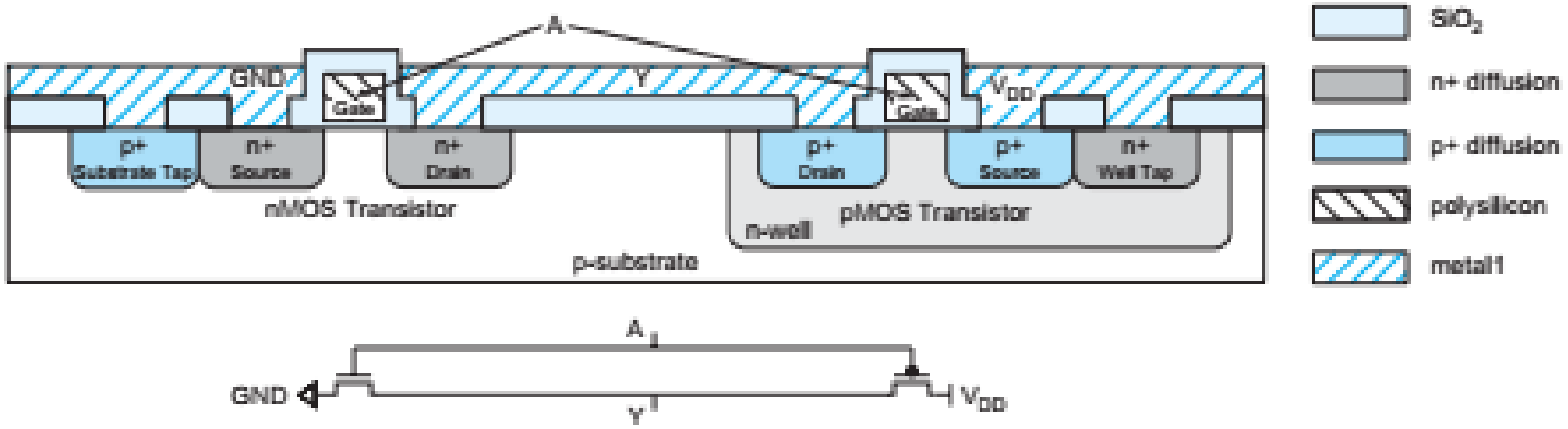
CMOS Fabrication Steps 2/



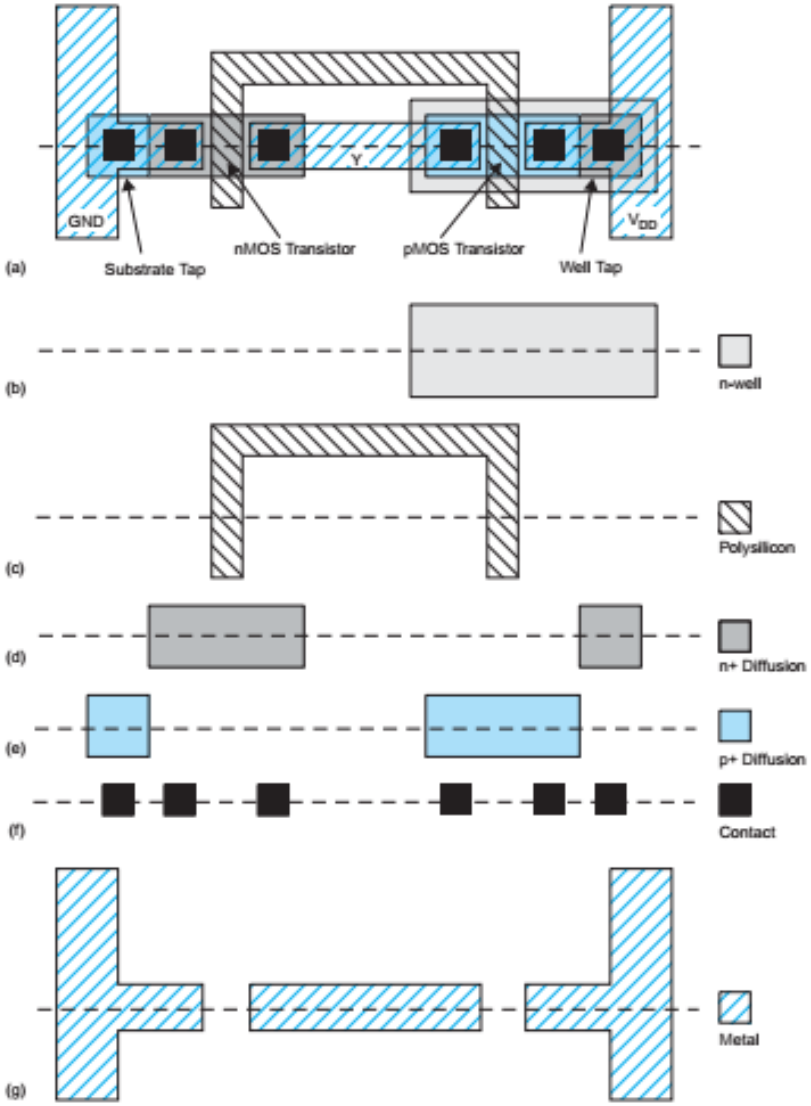
CMOS Fabrication Steps 3/



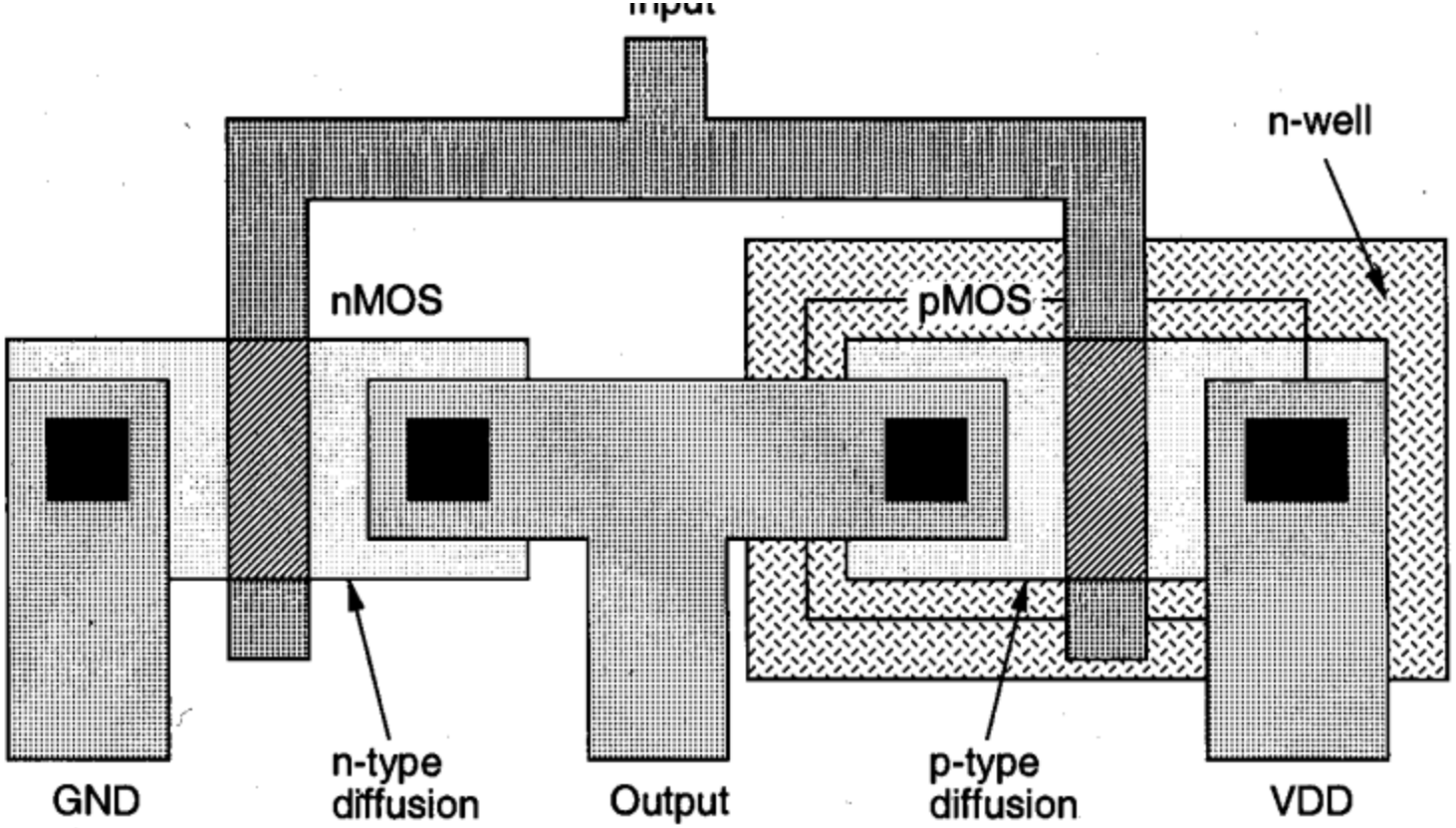
Inverter Cross Section



Mask Set for Inverter

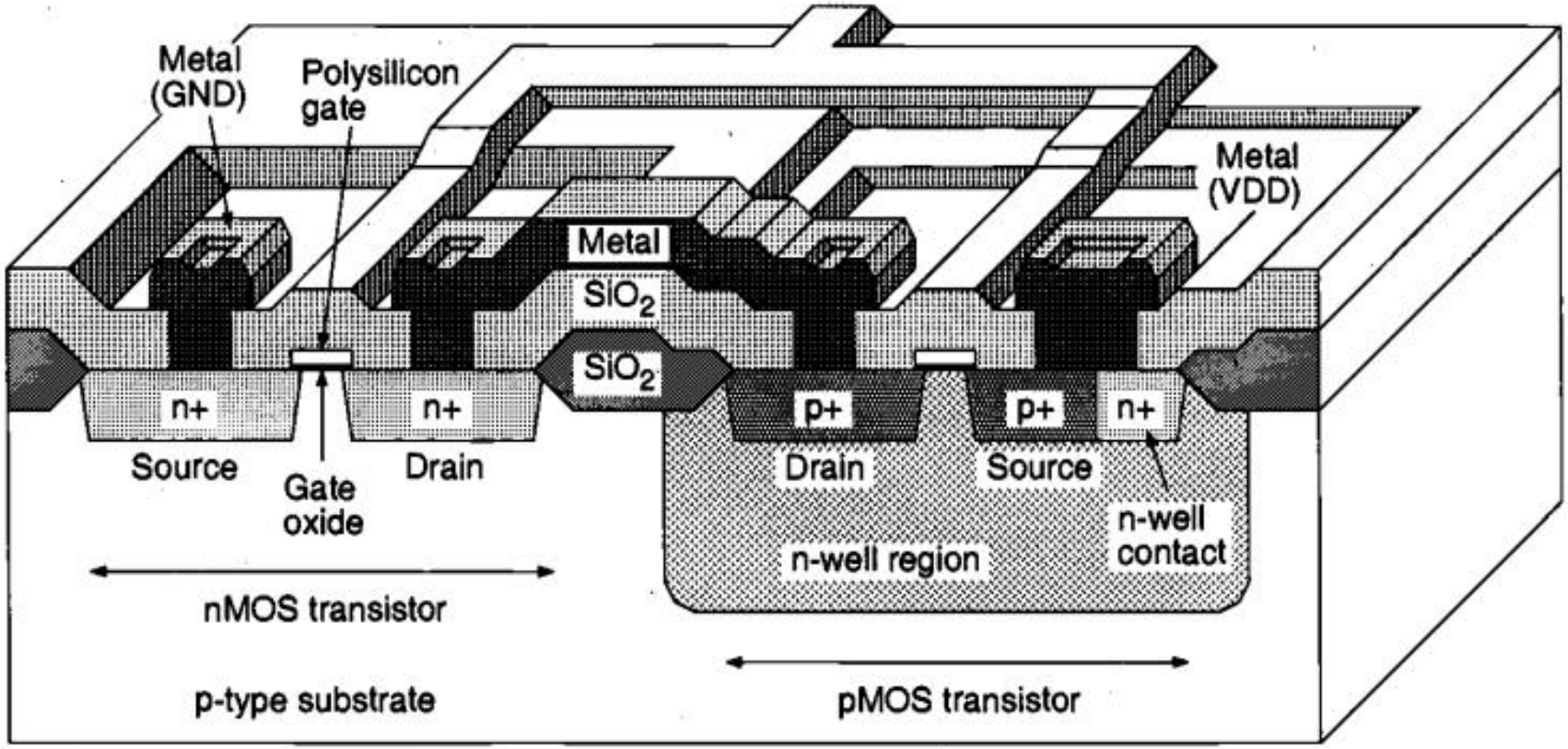


Layout of Inverter



Layout of Inverter

Cross Section Inverter



Cross section view of Inverter

Design Rules

- Design rules are a set of geometrical specifications that dictate the design of the layout
- **Layout is top view of a chip.**
- Design process are aided by stick diagram and layout
- Stick diagram gives the placement of different
- components and their connection details
- But the dimensions of devices are not mentioned
- Circuit design with all dimensions is Layout

Design Rules

- Design Fabrication process needs different masks, these masks are prepared from layout
- Layout is an Interface between circuit designer and fabrication
- Engineer
- Layout is made using a set of design rules.
- Design rules allow translation of circuit (usually in stick diagram or symbolic form) into actual geometry in silicon wafer
- These rules usually specify the minimum allowable line widths for physical objects on-chip
- Example: metal, poly, interconnects, diff. areas, min feature dimensions, and minimum feature.

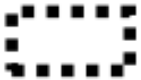
Need for Design Rules

- Better yield
- Better reliability
- Increase the probability of fabricating a successful
- product on Si wafer

If design rules are not followed:

- Functional or non-functional circuit.
- Design consuming larger Si area.
- The device can fail during or after simulation

Color Codes for Design Rules

Layer	Color	Representation
N+ Active	Green	
P+ Active	Yellow/Brown	
PolySi	Red	
Metal 1	Blue	
Metal 2	Magenta	
Contact	Black	X
Buried contact	Brown	X
Via	Black	X
Implant	Dotted yellow	
N-Well	Dotted Green/Black	

Stick Diagrams

- A stick diagram is a symbolic representation of a layout.
- In stick diagram, each conductive layer is represented by a line of distinct color.
- Width of line is not important, as stick diagrams just give only wiring and routing information.
- Does show all components/vias, relative placement.
- Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick Diagrams : Basic Rules

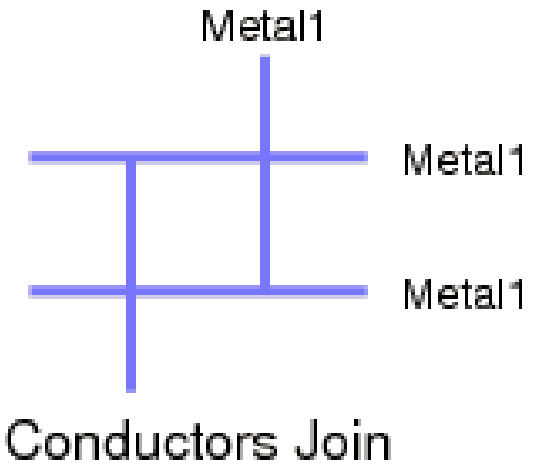
- Poly crosses diffusion forms transistor
- Red (poly) over Green(Active), gives a FET

nFET/
nMOS

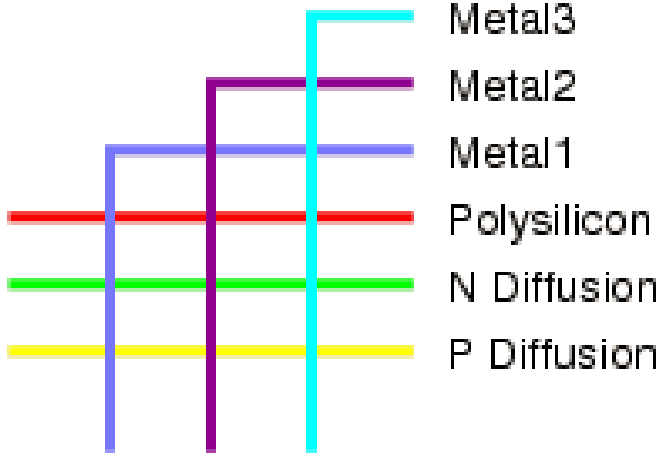
pFET/pMOS

Stick Diagrams : Implied Connections & Crossover

- Where two sticks of the same color meet or cross there is always a connection
- Where two sticks of different colors meet or cross there is no implied connection.



Conductors Join



Conductors Cross
(No Connection)

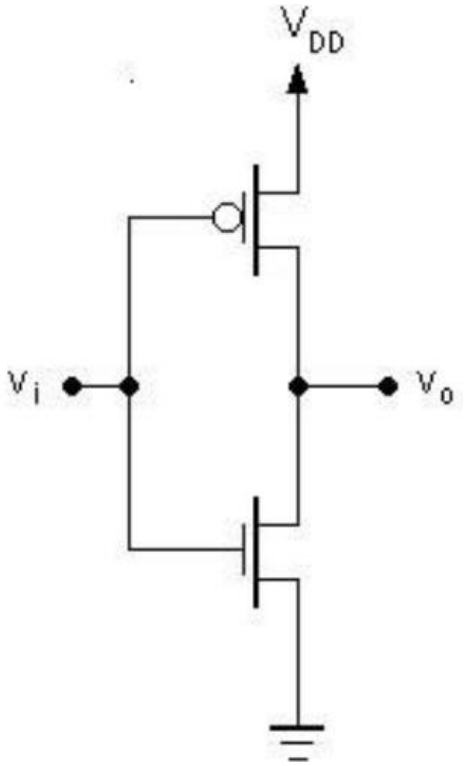
Stick Diagrams (CMOS): Basic Steps

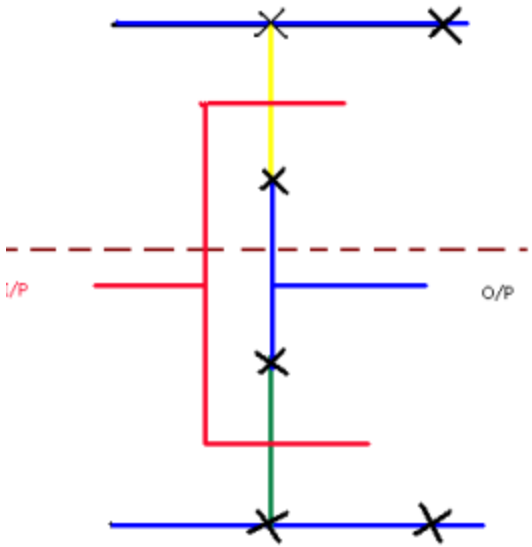
- Normally, the first step is to draw two parallel metal (blue) VDD and GND rails.
- There should be enough space between them for other circuit elements.
- Draw Demarcation line (Brown) at center of VDD and GND rails. This line represents the well (n/p-well).
- Next, Active (Green/yellow) paths must be drawn for required PU & PD transistors above & below DL.
- Draw vertical poly crossing both diffusions (Green & yellow)
- Remember, Poly (Red) crosses Active (Green/yellow), where transistor is required.

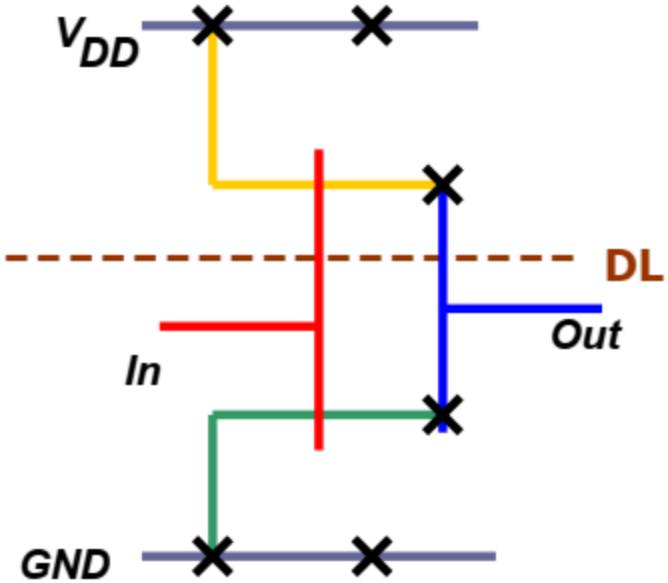
Stick Diagrams (CMOS): Basic Steps

- No Diffusion can cross demarcation line.
- Only poly and metal can cross demarcation line
- N-diffusion and p-diffusion are joined using a metal wire.
- Place all PMOS above and NMOS below demarcation line.
- Connect them using wires (metal).
- Blue may cross over red or green, without connection.
- Connection between layers is specified with X.
- Metal lines on different layer can cross one another, connections are done using via

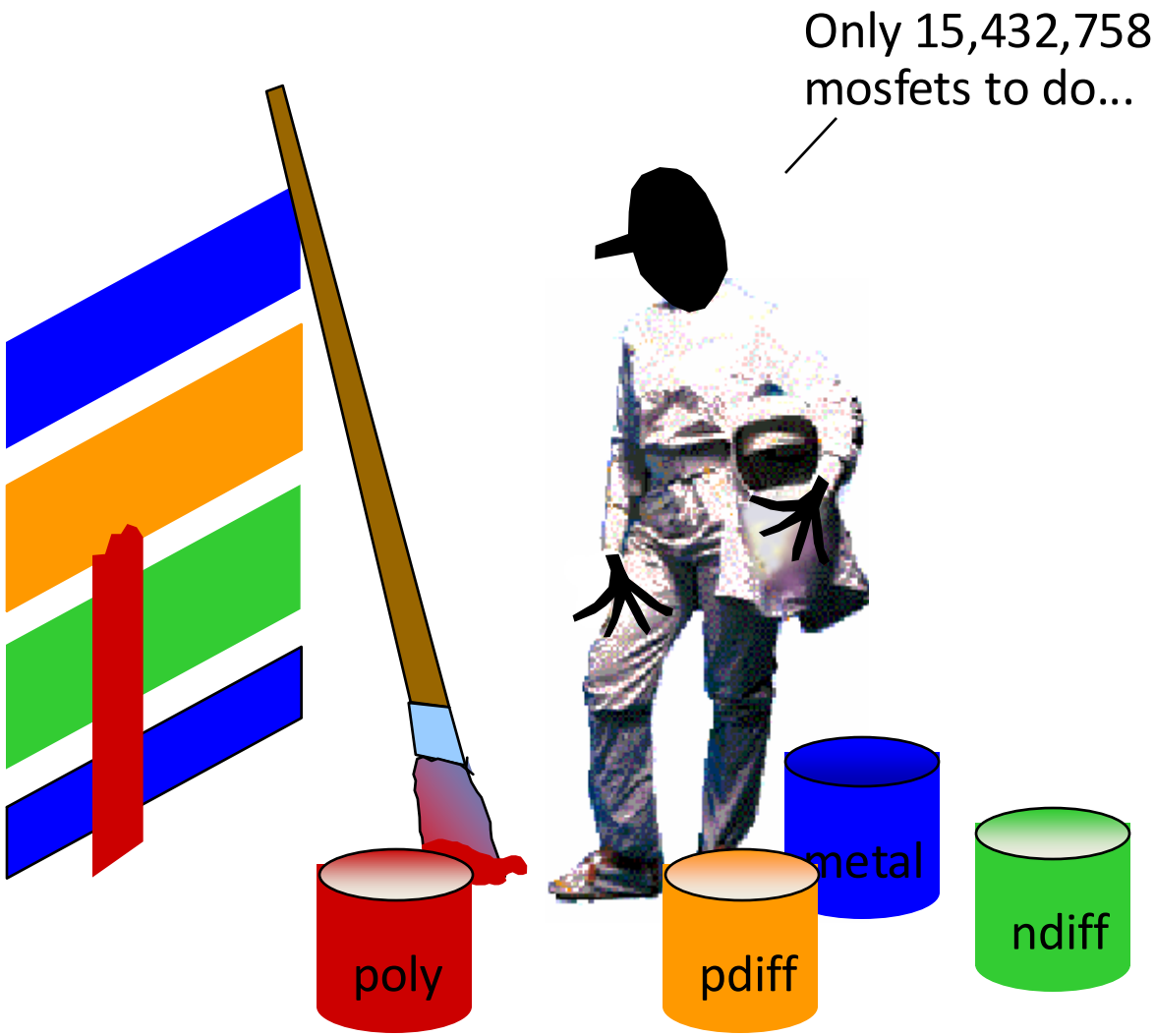
Stick Diagrams : Inverter



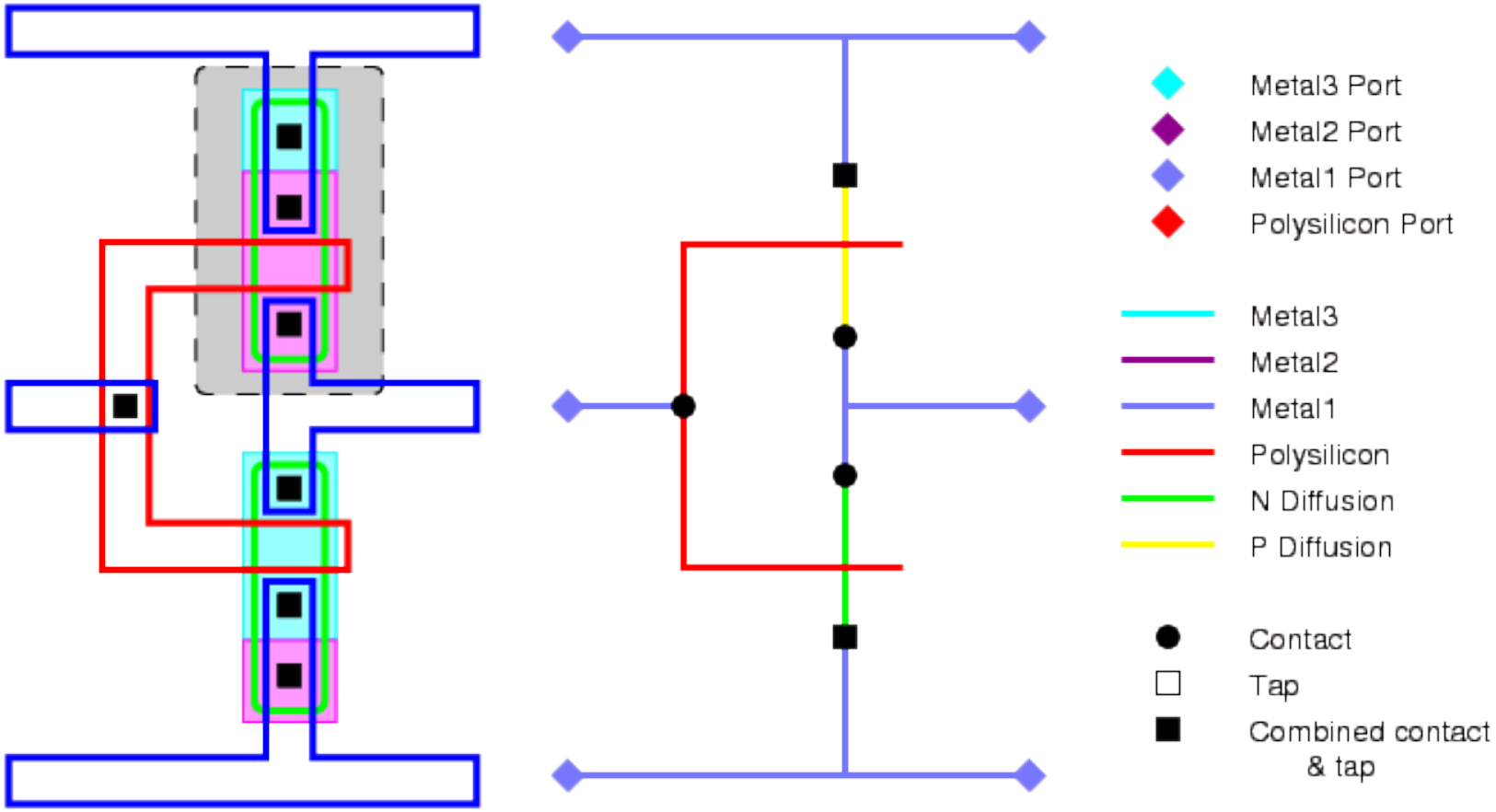




Layout

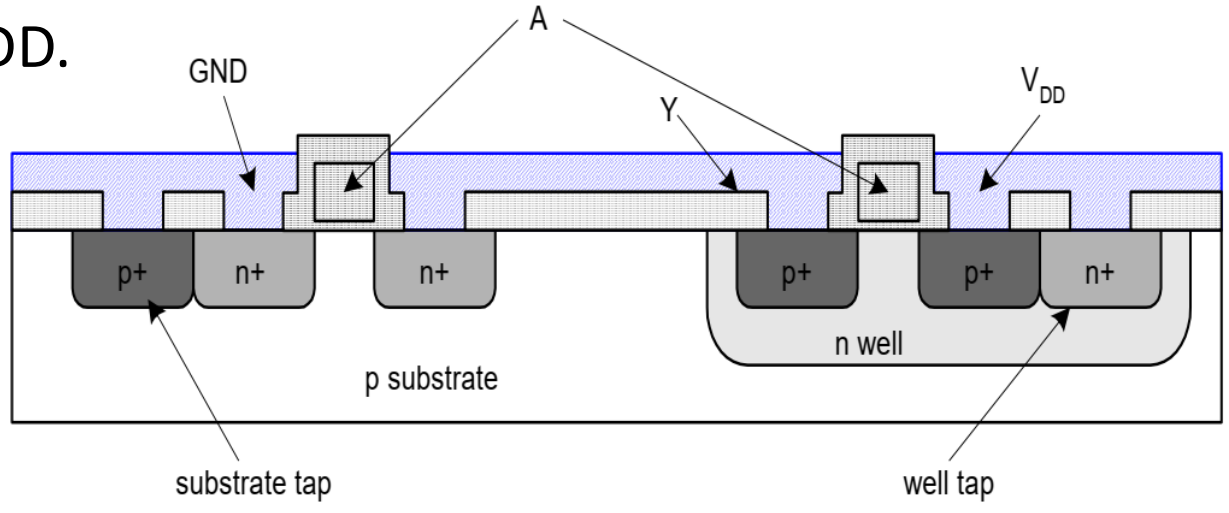


Stick Diagrams : Inverter



Stick Diagrams : Inverter

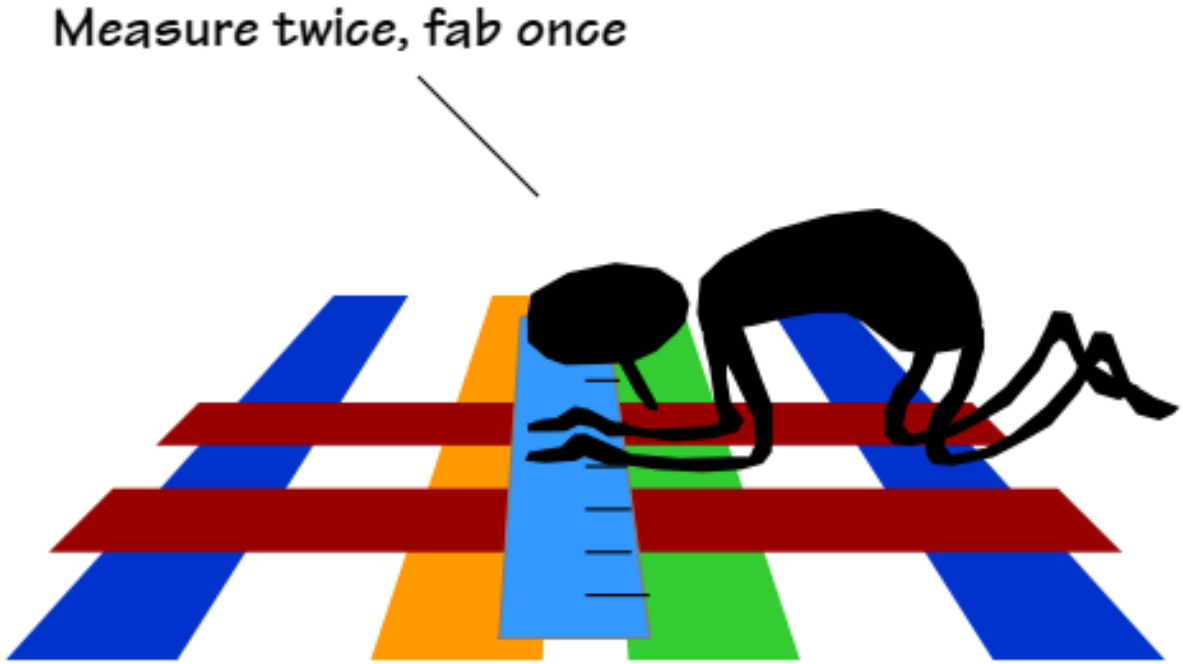
- The various N and P diffusions must be reverse biased to ensure that those wells are insulated from each other.
- This requires that the N- wells are connected to the most positive voltage, VDD
- The P- substrate must be connected to the most negative voltage, ground.
- This assumes that all other nets are at a voltage between 0V and VDD.



Layout Design Rules

Two types of Design rules

- Industry Standard: Micron Rule
  - All device dimensions are expressed in terms of absolute dimension(µm/nm)
  - These rules will not support proportional scaling
- Based Design Rules
  - All device dimensions are expresses in terms of a scalable parameter λ
  - λ = L/2; L = The minimum feature size of transistor, L = 2 λ
  - These rules support proportional scaling



Thank you !

Happy Learning