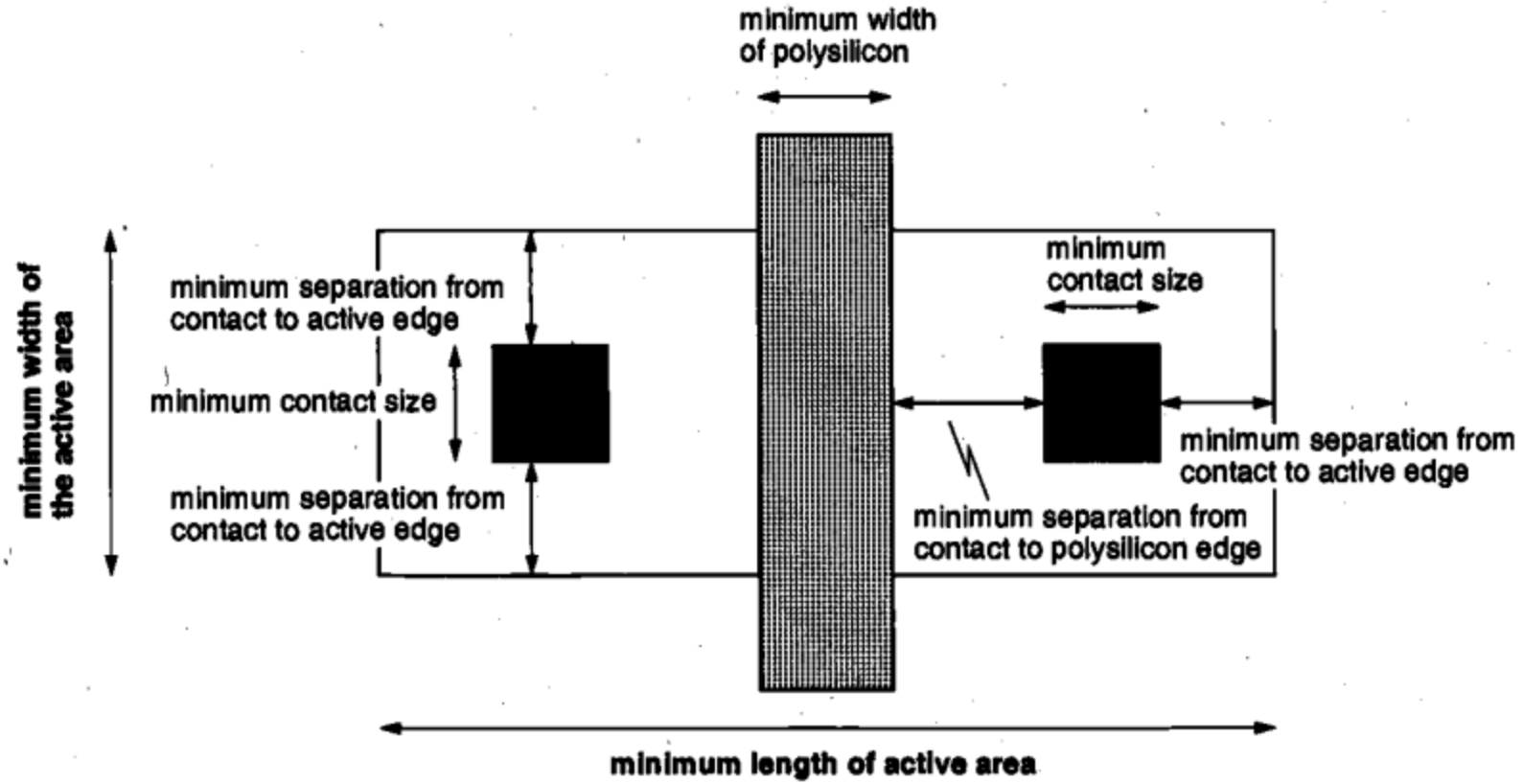
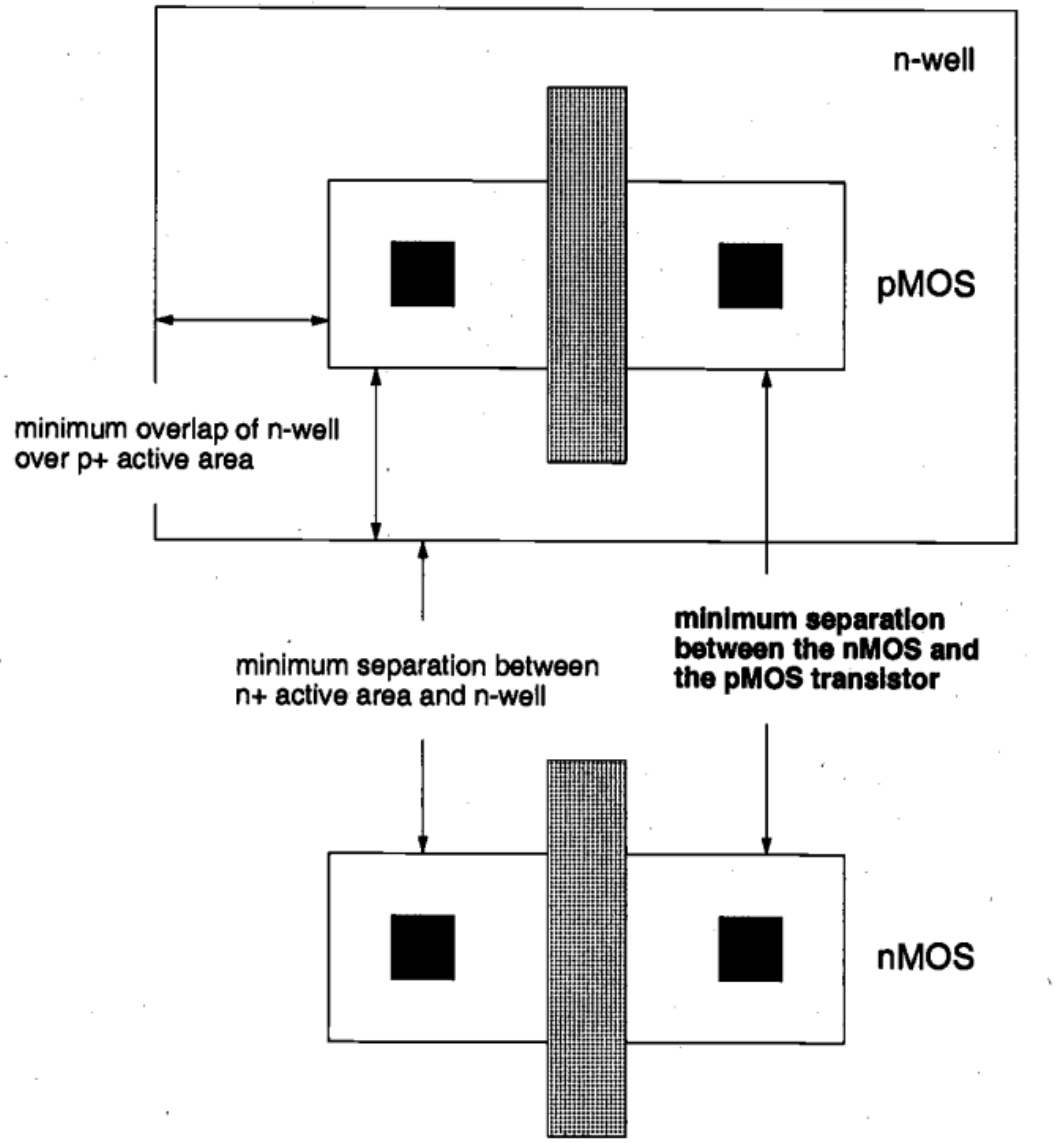
Design Rules

Pravin Zode

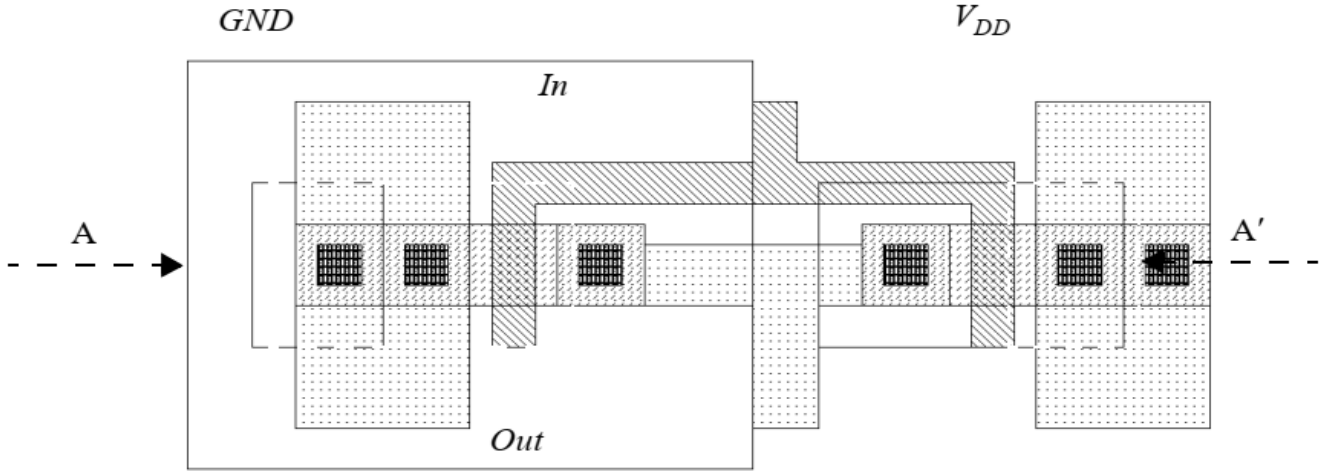
Minimum Size Transistor



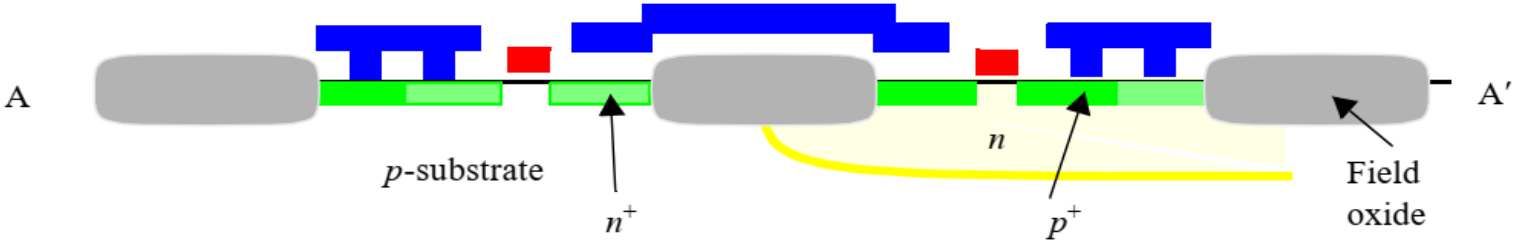
Minimum Size NMOS and PMOS

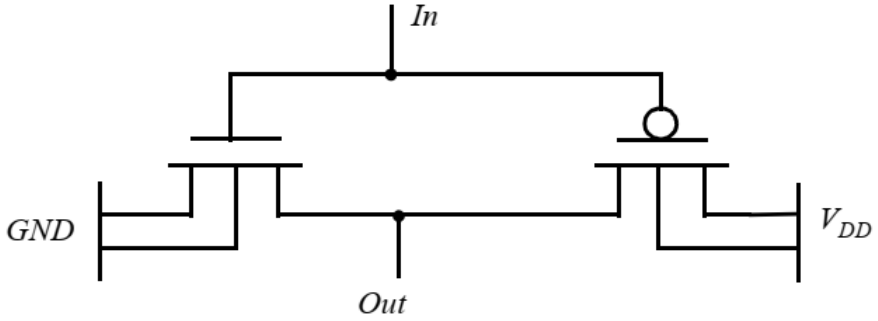


Cross Section and Layout

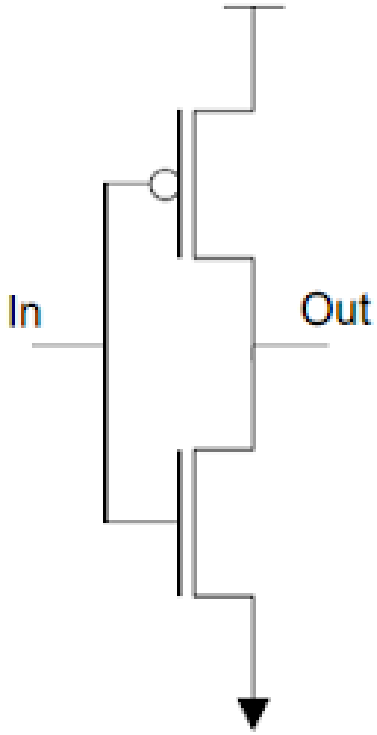


(a) Layout





Inverter Layout



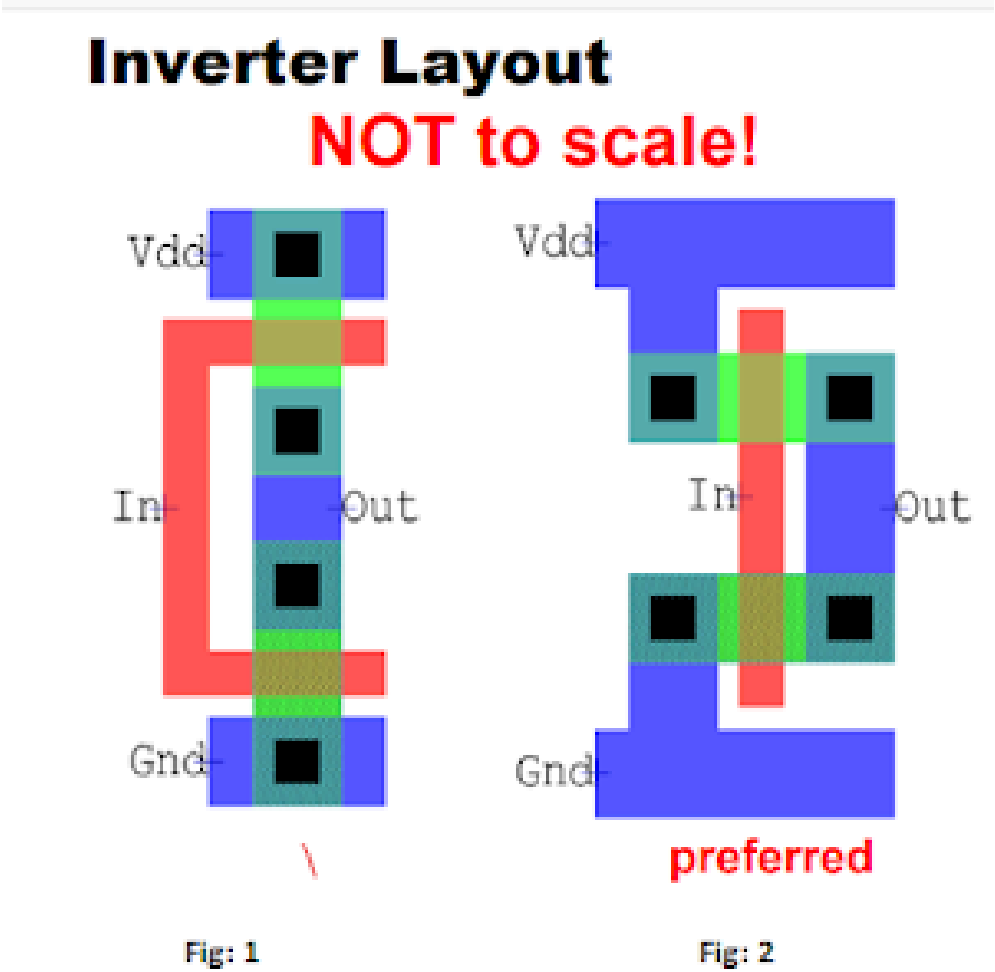
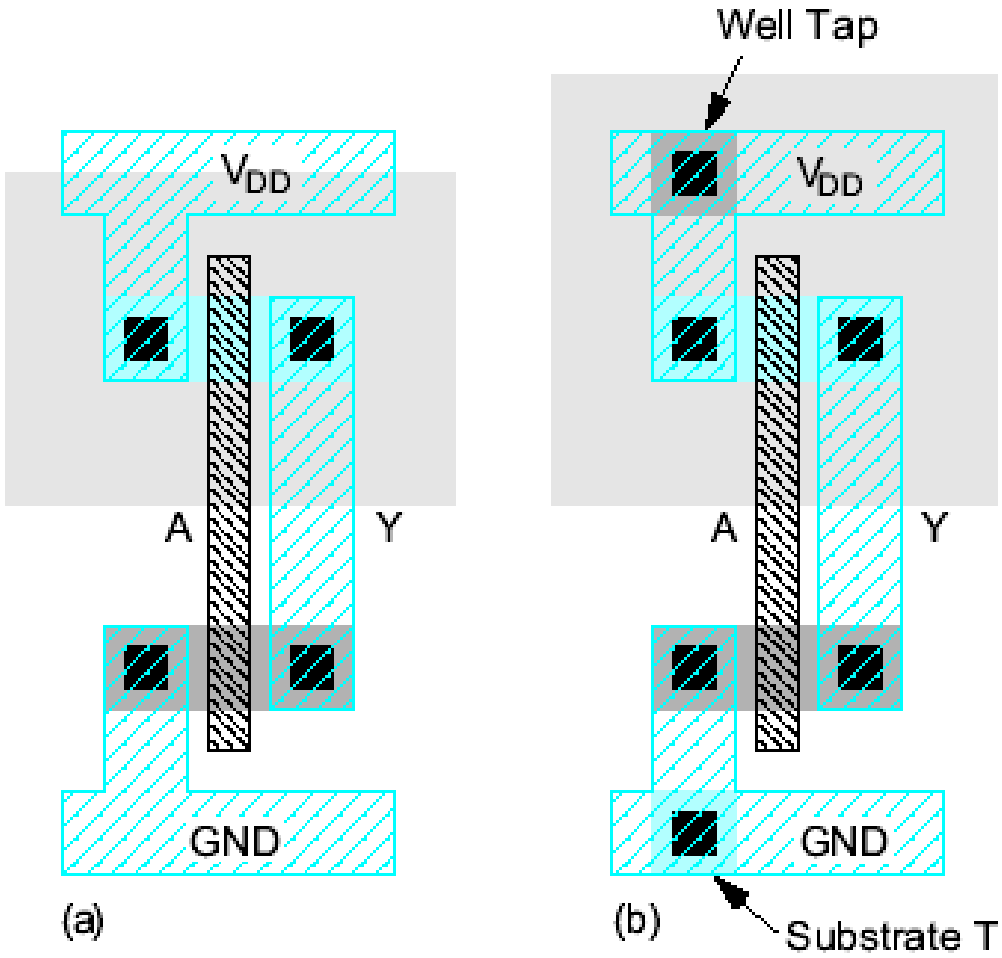


Fig: 1

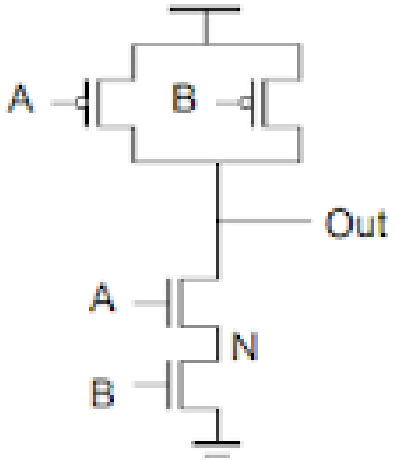
Fig: 2

Inverter Layout



NAND Gate Layout

NAND Gate Layouts



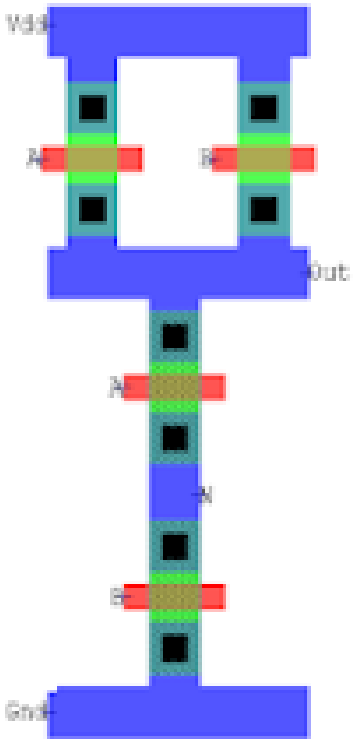


FIG :3

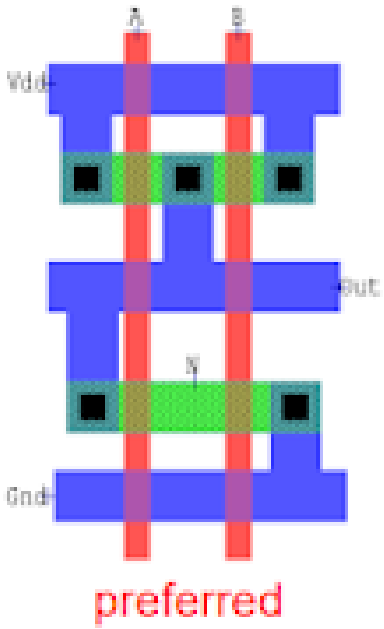
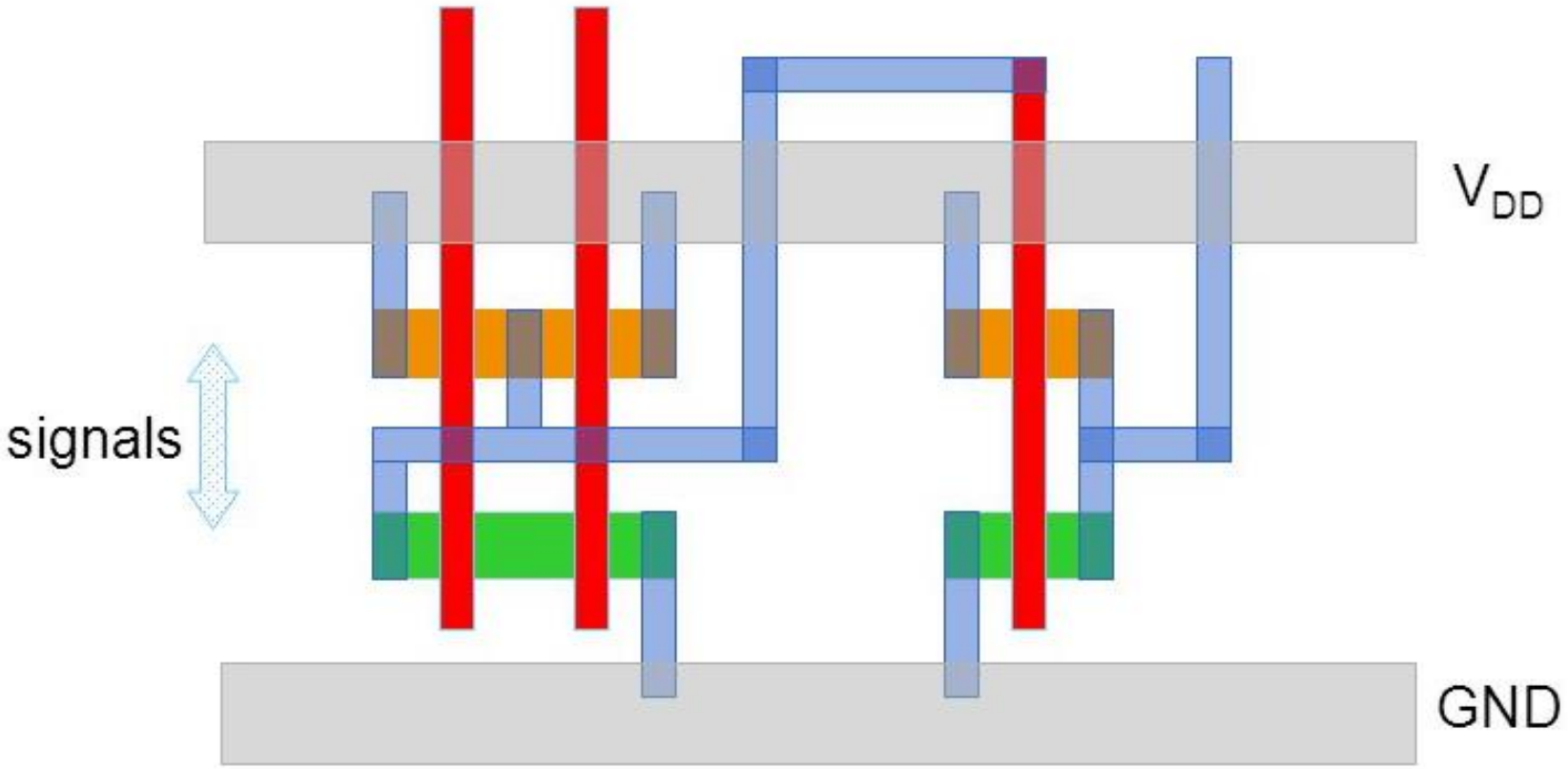
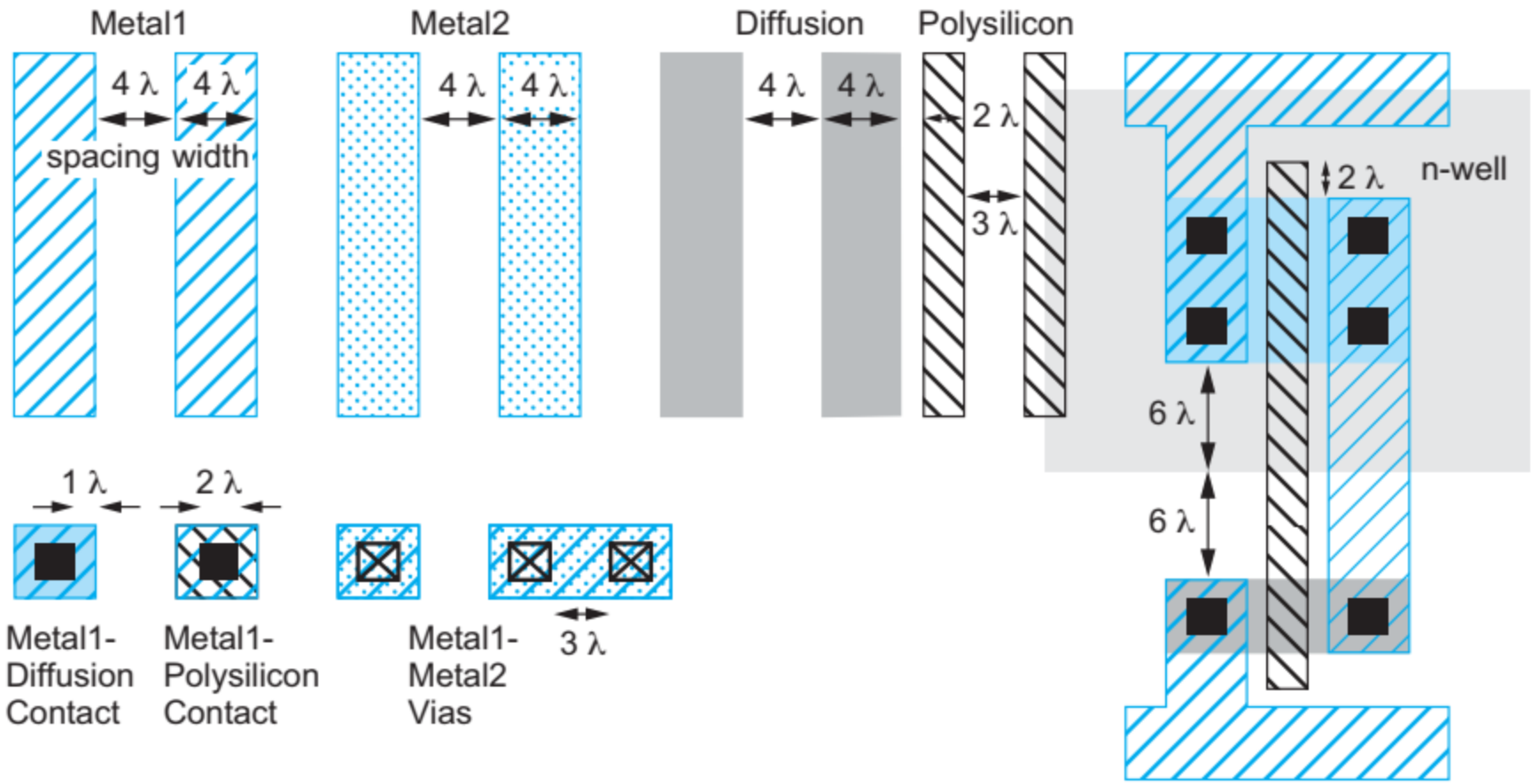


FIG :4

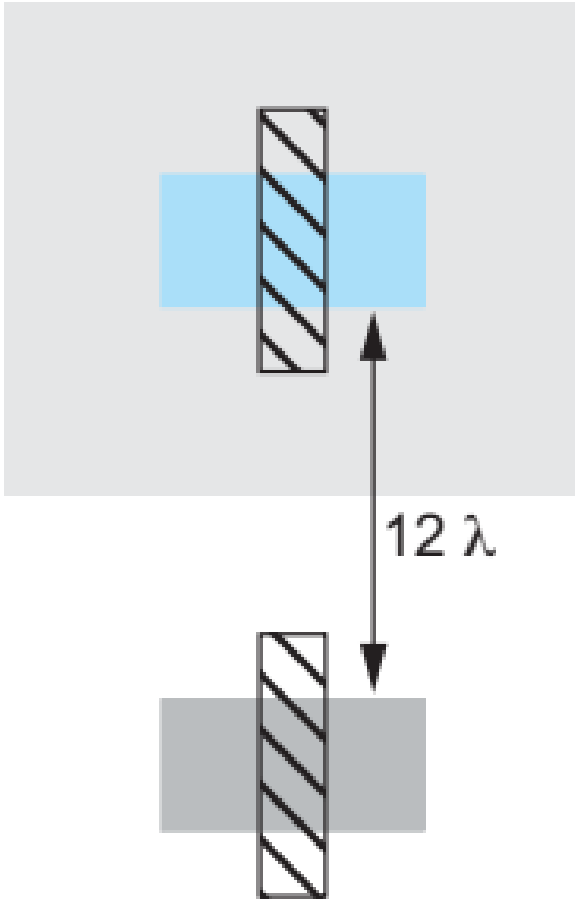
Example

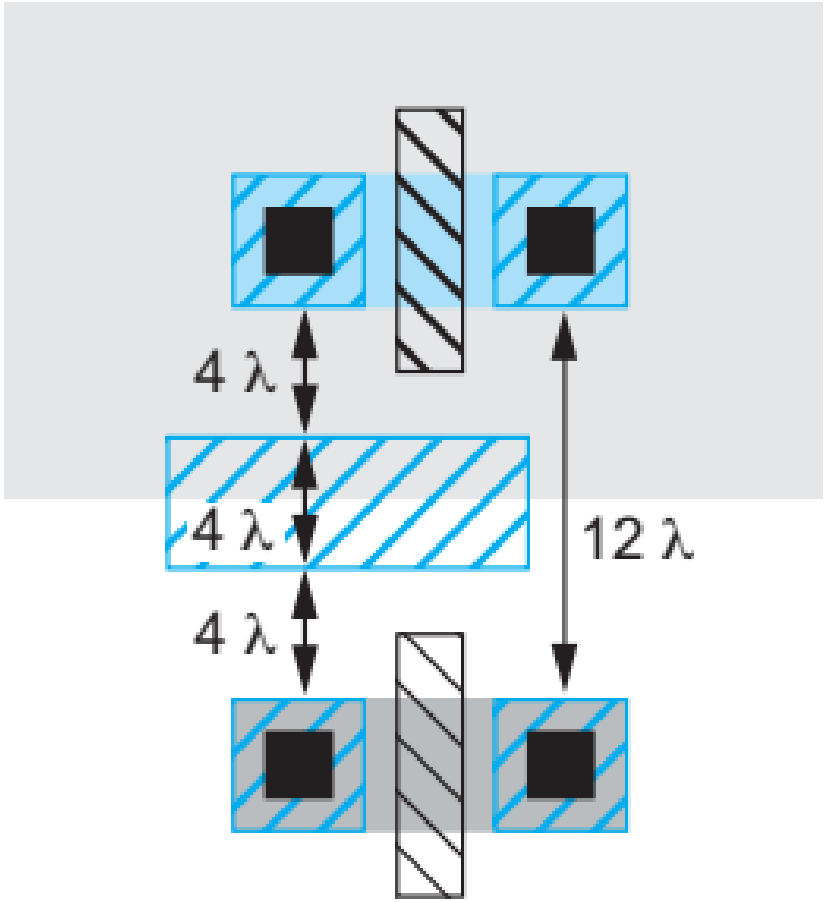


Simplified Lambda Rules

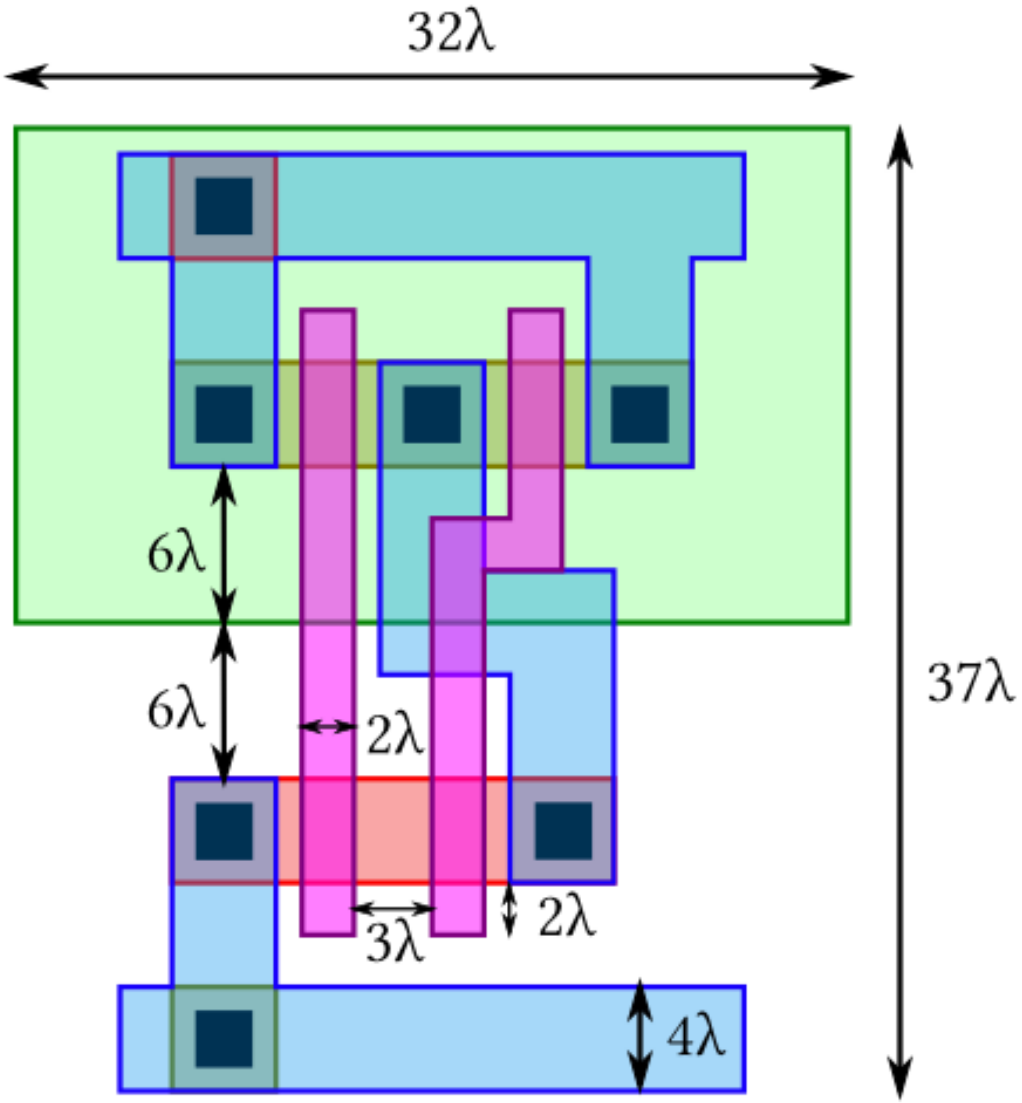


Spacing between NMOS & PMOS

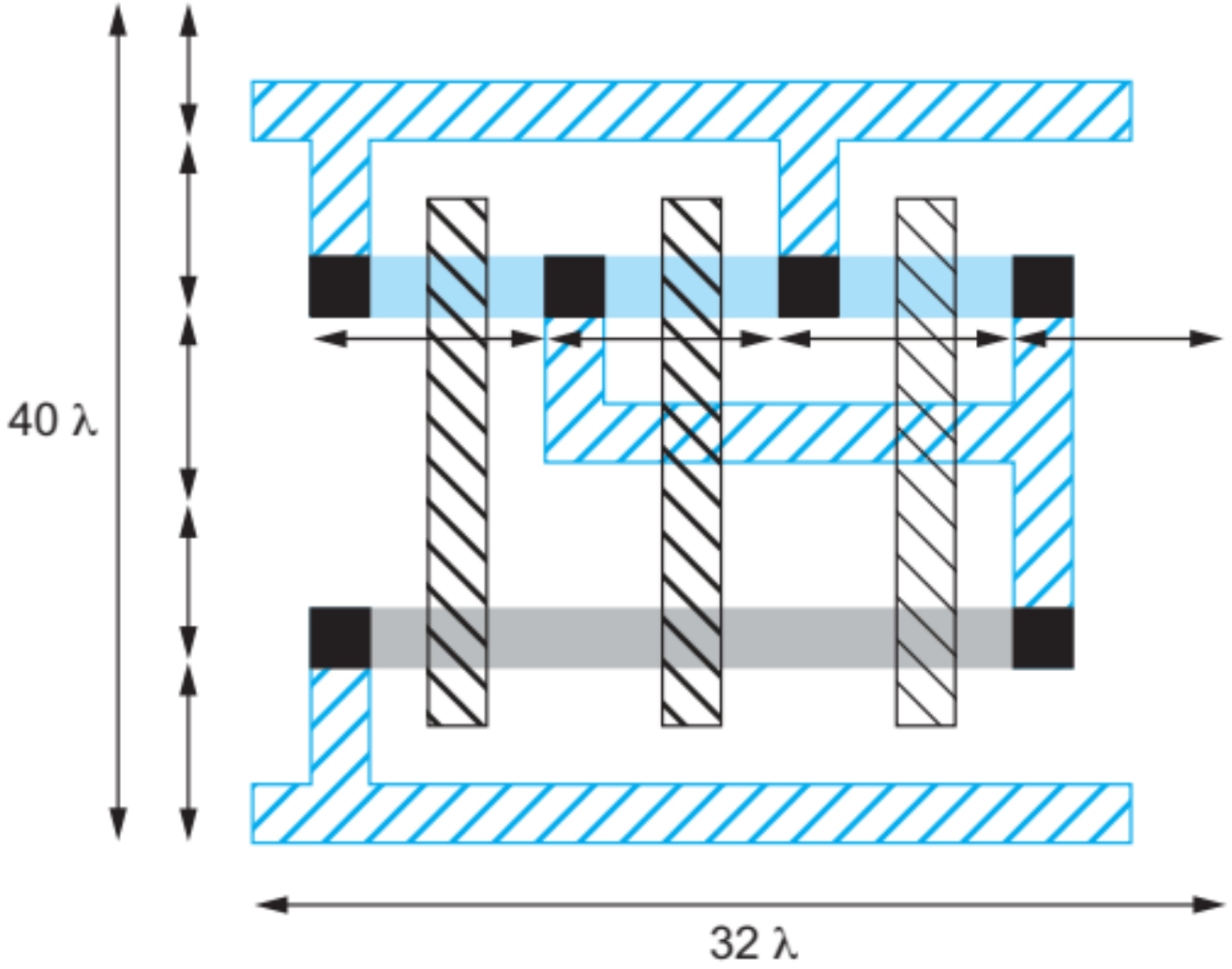




Spacing between NMOS & PMOS



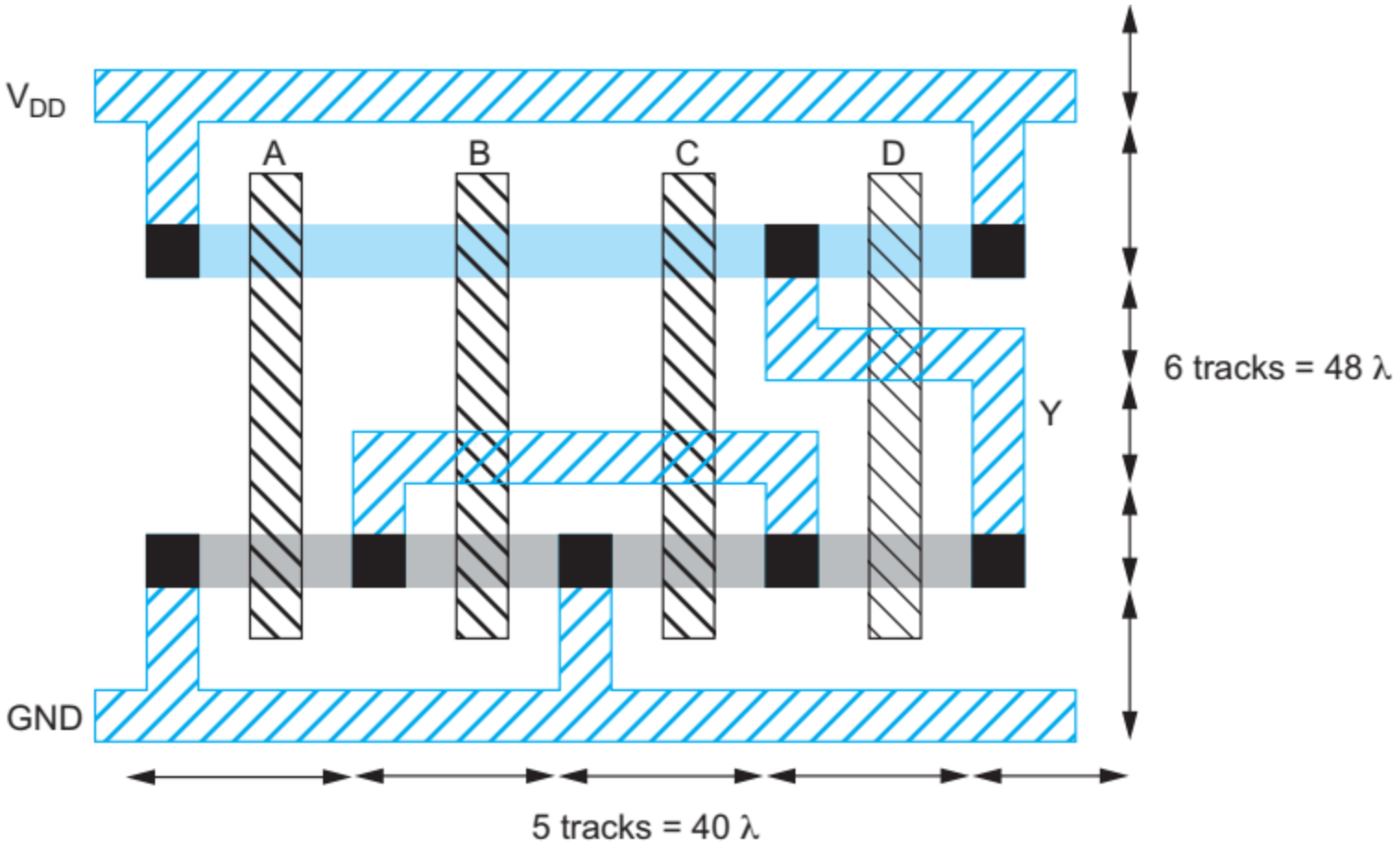
3-Input NAND Gate Layout

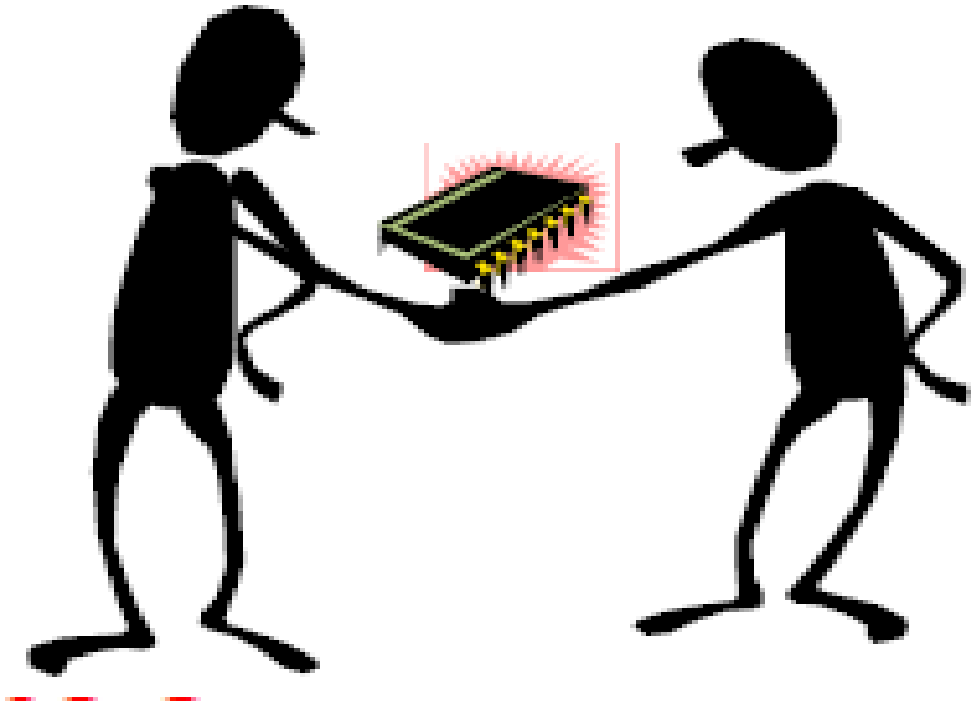


Compound Gate Layout

Example : O3AI Sketch a stick diagram for O3AI and estimate area

$$Y = \overline{(A + B + C) \cdot D}$$





Thank you !

Happy Learning