VLSI Testing

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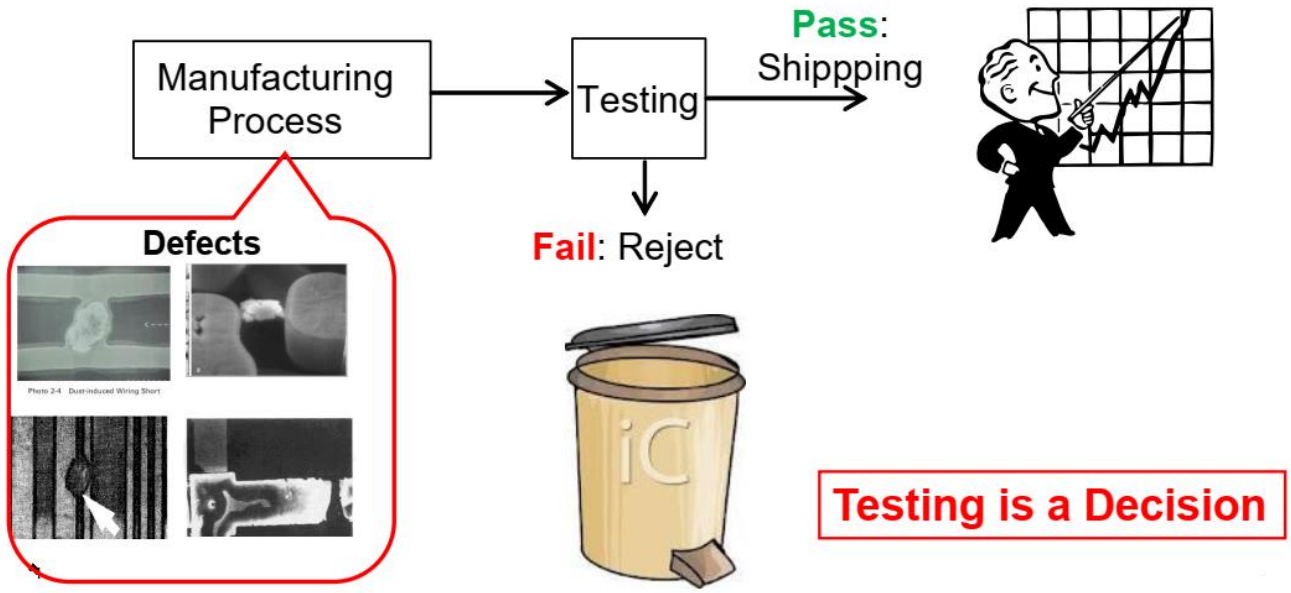
Outline

- Testing Basics
- Stages of Product Design
- Difference Verification and Testing
- Challenges in testing
- Design for Testability (DFT)
- DFT Guidelines and Techniques

What is testing ?

- Testing is process of determining whether a piece of hardware
  - Functioning correctly (**PASS**) or defective **(FAIL**)
- Why do we need to test ICs ?
  - Because defect occur in manufacturing process .

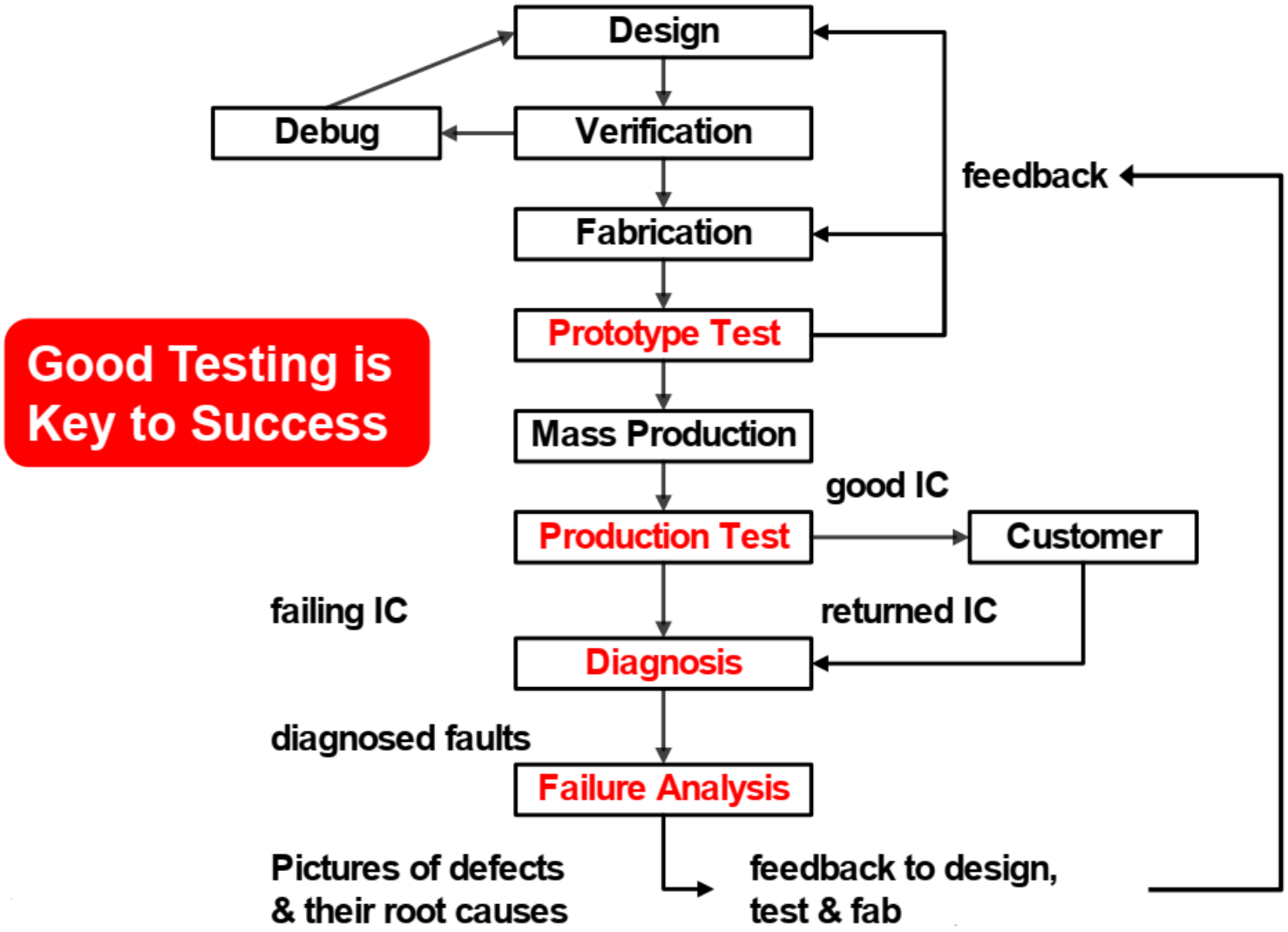


Four Possible Outcomes of testing

- True pass and true reject are correct decision
- Test escapes = defective chips that pass test
- Yield loss = good chips that fail the tests
- Goal of good testing : reduce both test escape and yield loss
- Trade off between test cost and test quality
  - Quality test reduces test escapes but increase yield loss
  - low-cost test reduces yield loss but increase test escape

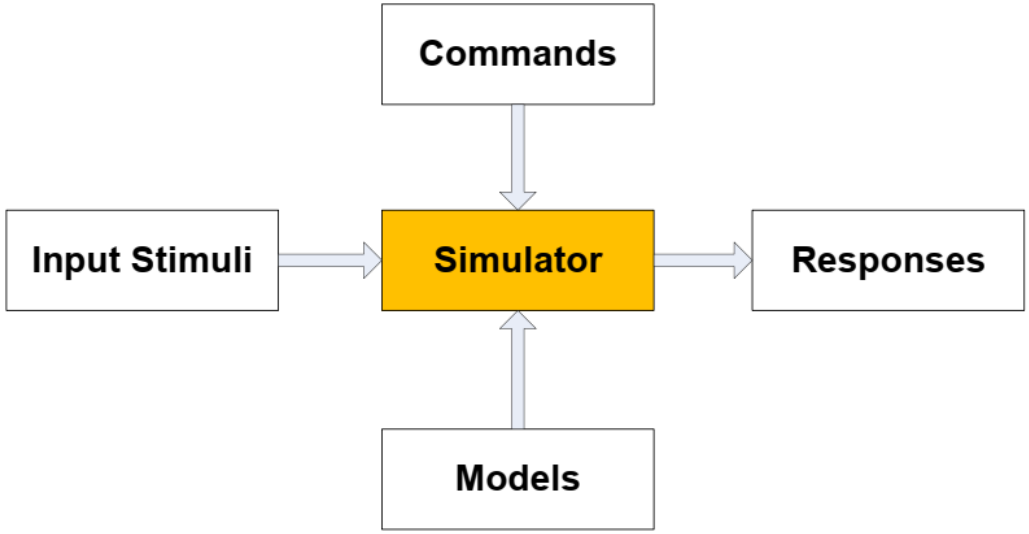
	Good IC	Defective IC
Pass tests	True PASS	Test Escapes (less is better)
Fail tests	Yield Loss (less is better)	True Reject

Stages of IC Product



Simulation

- Given input stimuli, models and command run software to produce output responses
- For digital circuits
  - Input stimuli are test patterns
  - Models can be functional /logic/transistor



Verification Vs Test

Verification

- Verifies correctness of design.
- Performed by simulation, hardware emulation, or formal methods.
- Performed once prior to manufacturing.
- Responsible for quality of design.

Testing

- Verifies correctness of manufactured hardware.
- Two-part process:
  1. Test generation: software process executed once during design
  2. Test application: electrical tests applied to hardware
- Test application performed on every manufactured device.
- Responsible for quality of devices.

Roles of Testing

- Detection: Determination whether or not the device under test (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.

Circuits Testing

- Combinational circuits can be tested effectively using deterministic or random test sets
- Sequential circuits are harder to test due to the presence of memory elements and internal states
- The output response of a sequential circuit depends on its current state and input
- Combinational circuits can be tested using truth tables for output comparison
- For sequential circuits, testing by comparing with a state table is theoretically possible but impractical.

Challenges in Sequential Circuit Testing

- Challenges in sequential testing include:
  - Difficulty in setting or observing the internal state
  - Inability to verify if the circuit has reached the correct destination state
- Verifying every state transition is not feasible for large designs
- A more practical solution is to design sequential circuits to be easily testable, i.e., **Design for Testability (DFT)**.

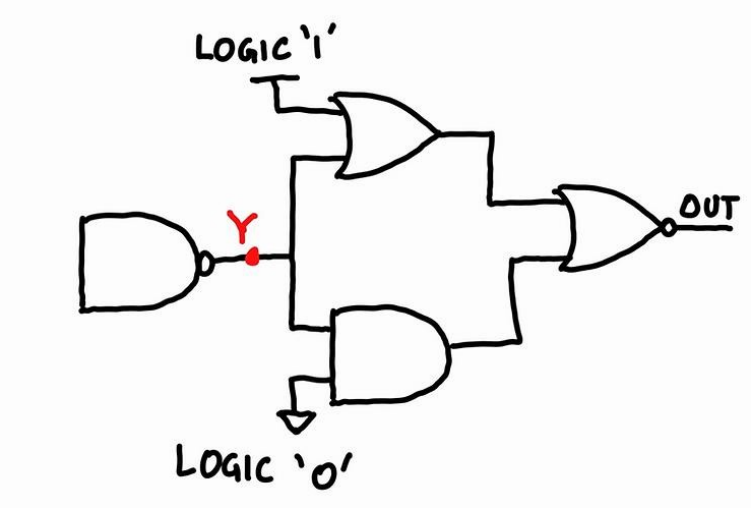
Design for Testability

- Design for testability (DFT) refers to those design techniques that make test generation and test application cost-effective.
- DFT methods for digital circuits:
  - Ad-hoc methods
  - Structured methods:
    - Scan
    - Partial Scan
    - Built-in self-test (BIST)
    - Boundary scan
- DFT method for mixed-signal circuits:
  - Analog test bus

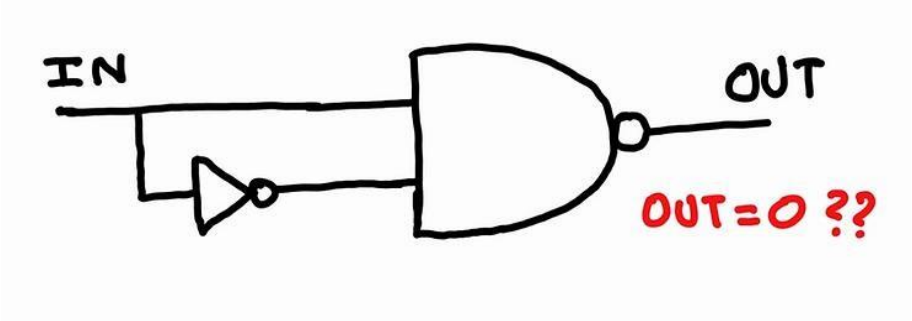
Observability & Controllability

- **Observability** : Ease of observing a node by watching external output pins of chip
- **Controllability** : Ease of forcing a node to 0 or 1 by driving input pins of the chip

Observability & Controllability



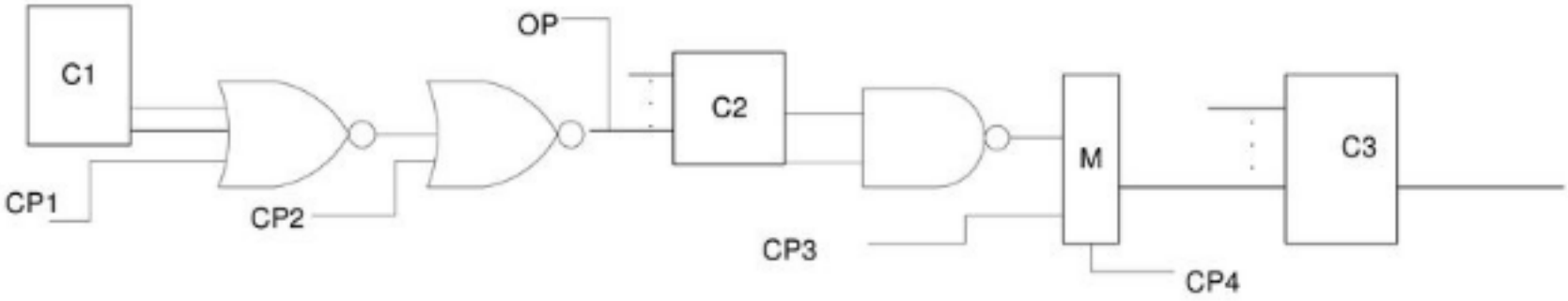
Node ‘Y’ cannot be observed at ‘OUT’ pin



Node ‘OUT’ cannot be controlled to ‘logic 0’

Ad Hoc Testing

- Employ test point to enhance controllability and observability (testpoints : Control points (CPs) & Observation points (OPs)



Guidelines : Ad hoc testing

Good design practices learnt through experience are used as guidelines:

- Avoid asynchronous (unclocked) feedback.
- Make flip-flops initializable.
- Avoid redundant gates. Avoid large fanin gates.
- Provide test control for difficult-to-control signals.
- Avoid gated clocks.
- Consider ATE requirements (tristates, etc.)

Disadvantages of ad-hoc DFT methods:

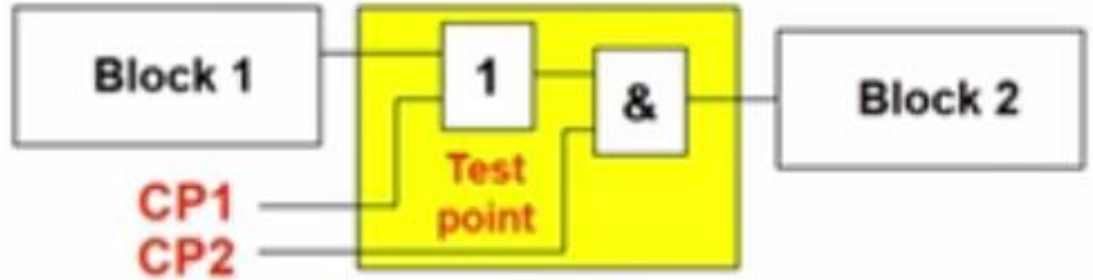
- Experts and tools not always available.
- Test generation is often manual with no guarantee of high fault coverage.
- Design iterations may be necessary.

Ad hoc testing

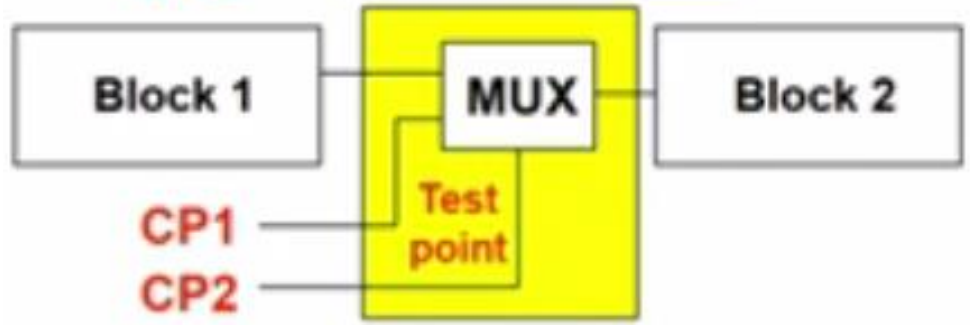
Method of Test Points:

Block 1 is not observable,
Block 2 is not controllable

Improving controllability:



Normal working mode:
CP1 = 0, CP2 = 1
Controlling Block 2 with 1:
CP1 = 1, CP2 = 1
Controlling Block 2 with 0:
CP2 = 0



Normal working mode:
CP2 = 0
Controlling Block 2 with 1:
CP1 = 1, CP2 = 1
Controlling Block 2 with 0:
CP1 = 0, CP2 = 1

Ad hoc testing

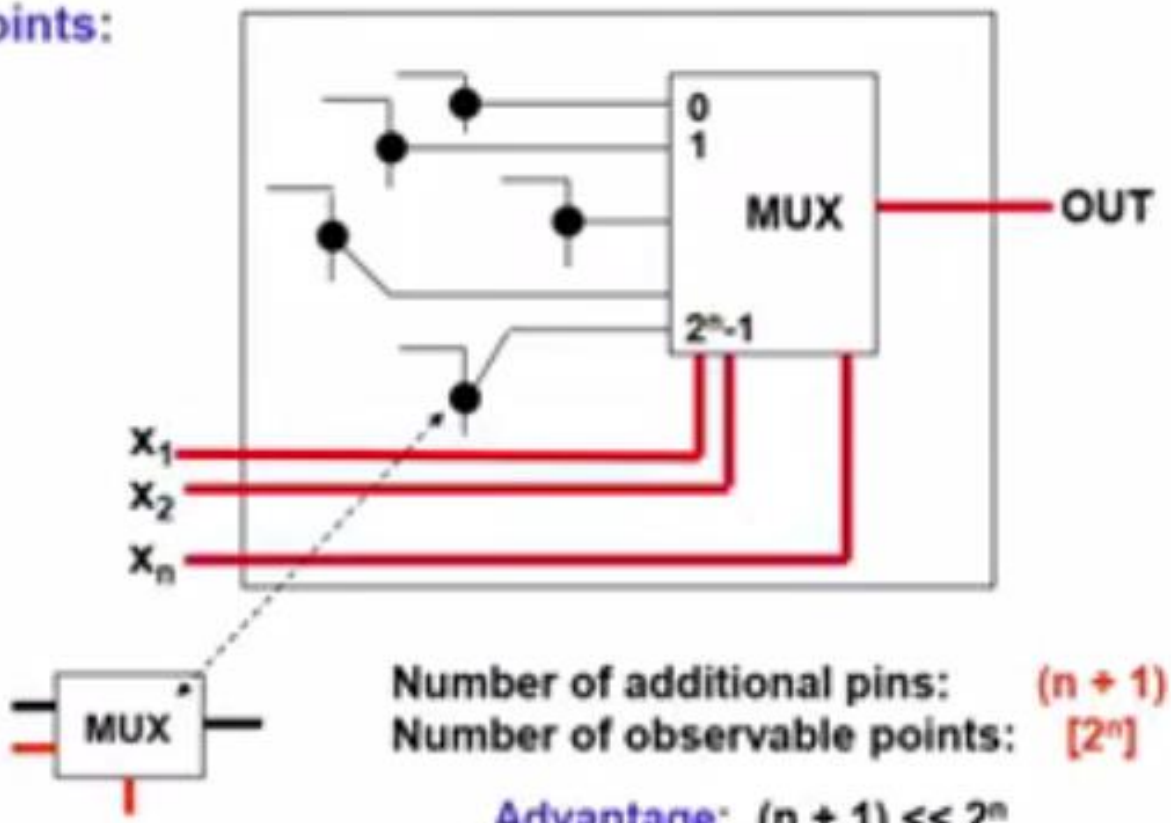
Multiplexing monitor points:

To reduce the number of output pins for observing monitor points, multiplexer can be used:

2^n observation points are replaced by a single output and n inputs to address a selected observation point

Disadvantage:

Only one observation point can be observed at a time



Number of additional pins: (n + 1)
Number of observable points: [2^n]

Advantage: (n + 1) << 2^n

Ad hoc testing

Multiplexing monitor points:

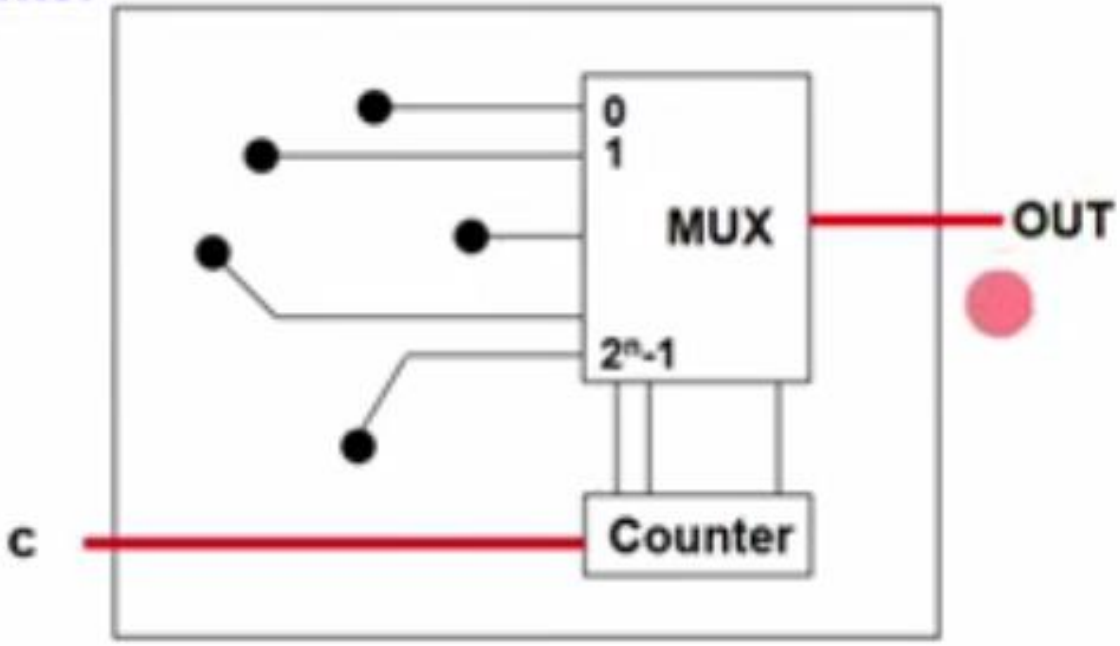
To reduce the number of output pins for observing monitor points, multiplexer can be used:

To reduce the number of inputs, a counter (or a shift register) can be used to drive the address lines of the multiplexer

Disadvantage:

Only one observation point can be observed at a time

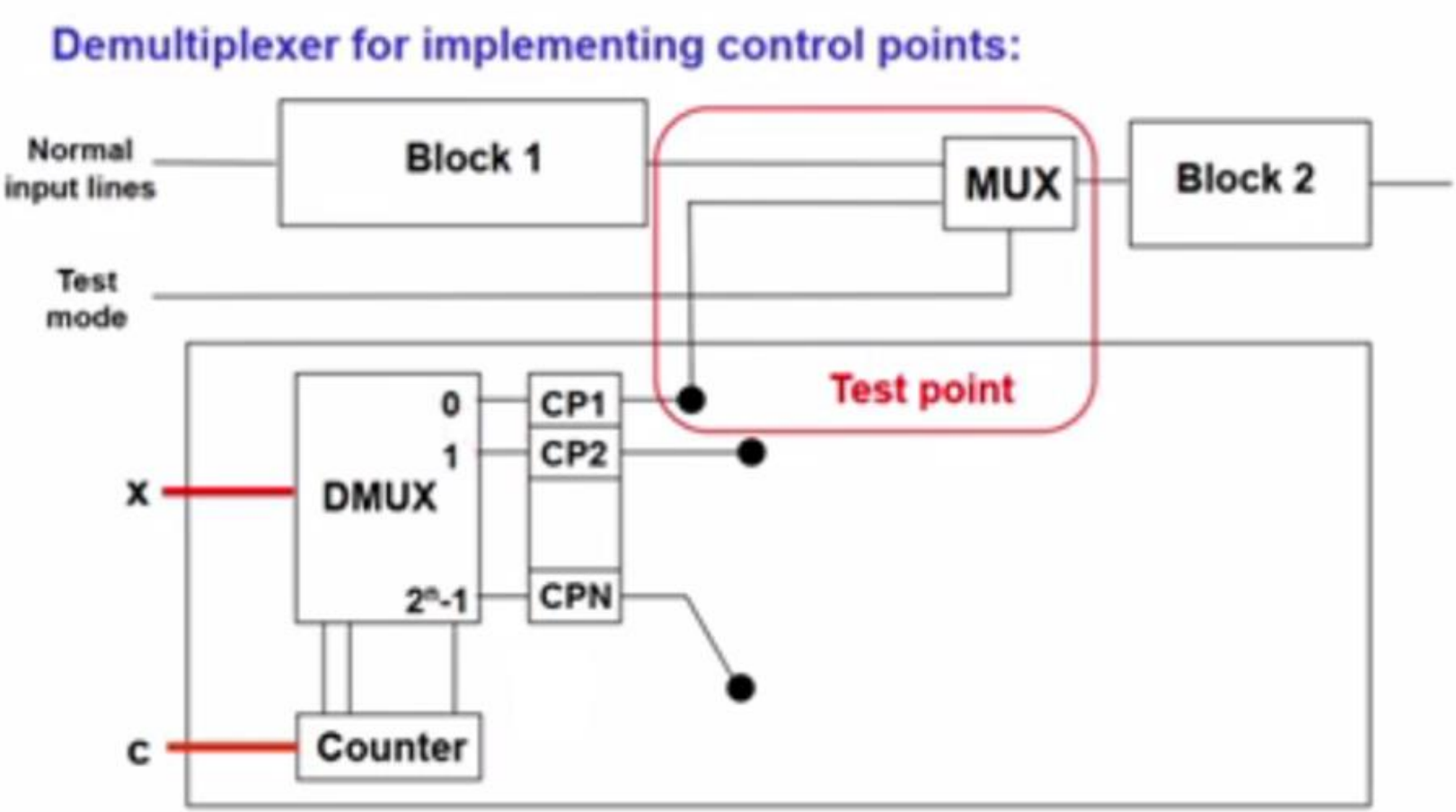
Reset for counter?



Number of additional pins: 2
Nmber of observable points: [2^n]

Advantage: $2 < n << 2^n$

Ad hoc testing (DeMux Control Input)

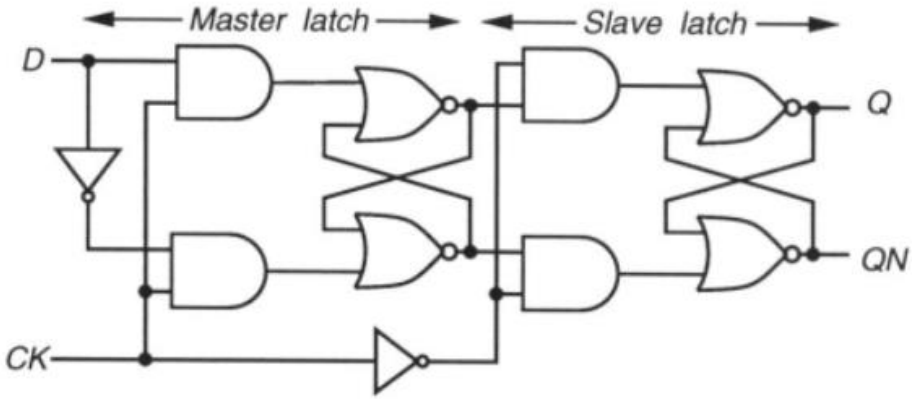


Scan

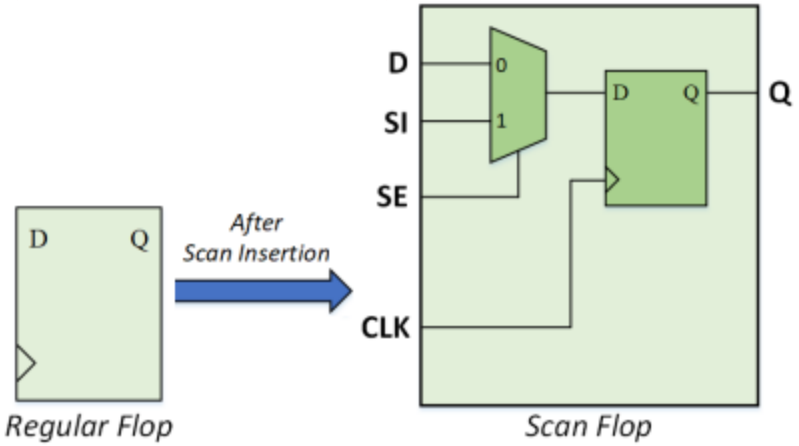
- The main idea in scan design is to obtain control and observability for flip-flops
- This is achieved by adding a test mode to the circuit
- In test mode, all flip-flops form one or more shift registers (also called scan registers)
- The inputs and outputs of these shift registers are treated as primary inputs and outputs
- Flip-flops can be set to any desired states by shifting in the test vector
- Flip-flop states can be observed by shifting out the contents of the scan register

Scan

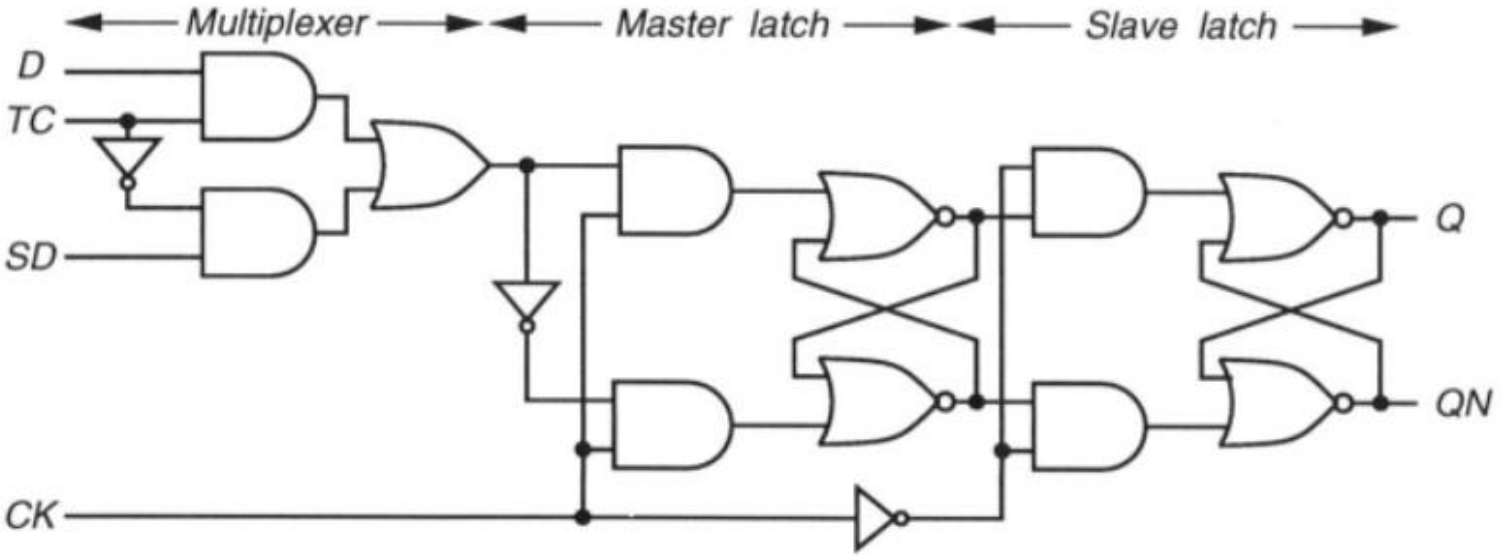
D-Flip Flop



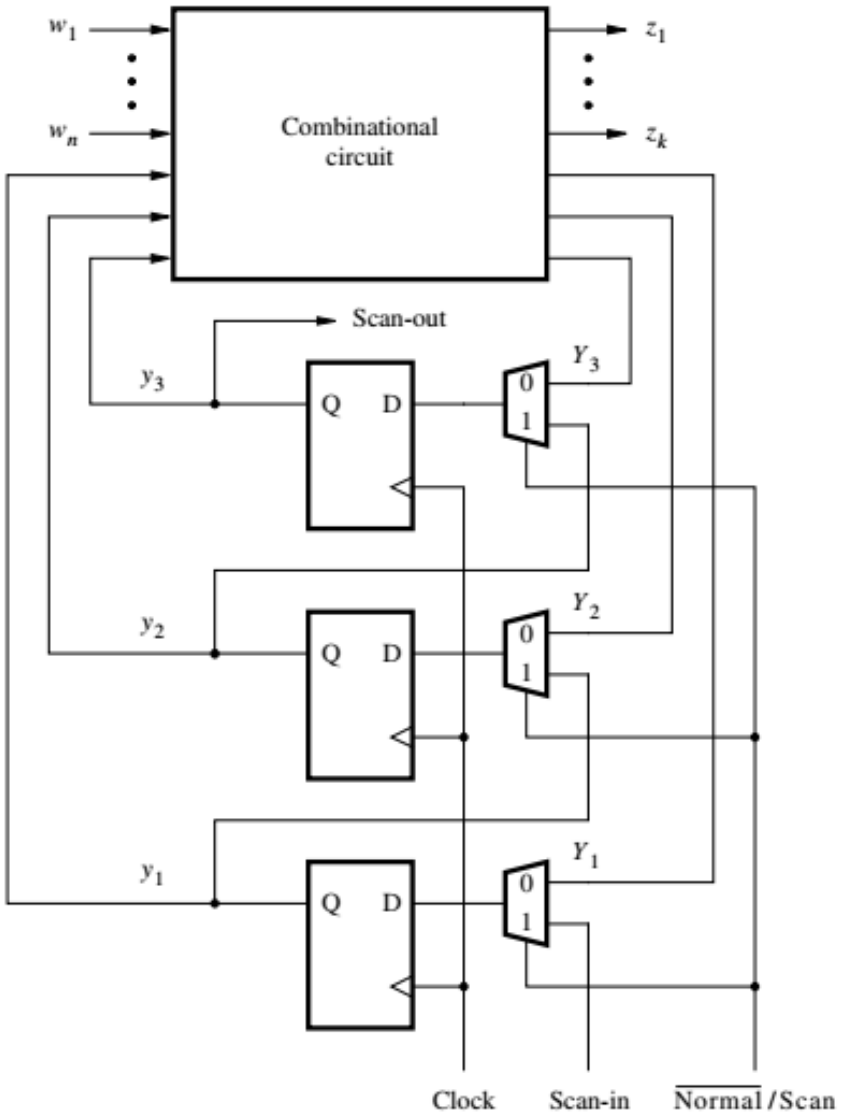
Single Clock Scan D-Flip Flop

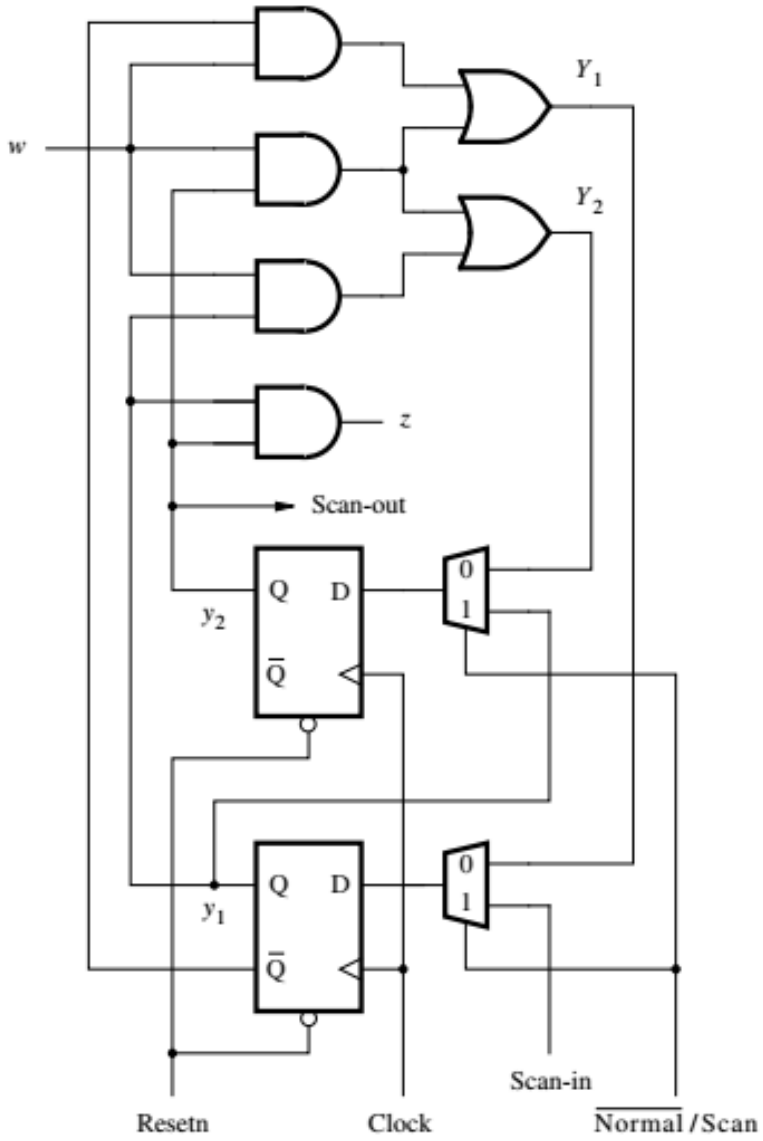


Single Clock Scan D-Flip Flop



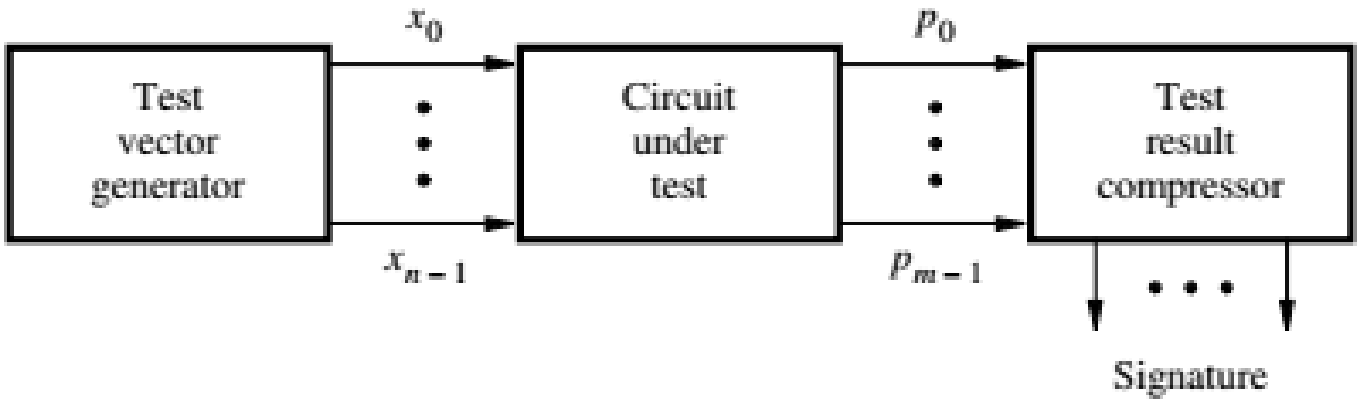
Example : Scan Design





BIST (Built In Self Test)

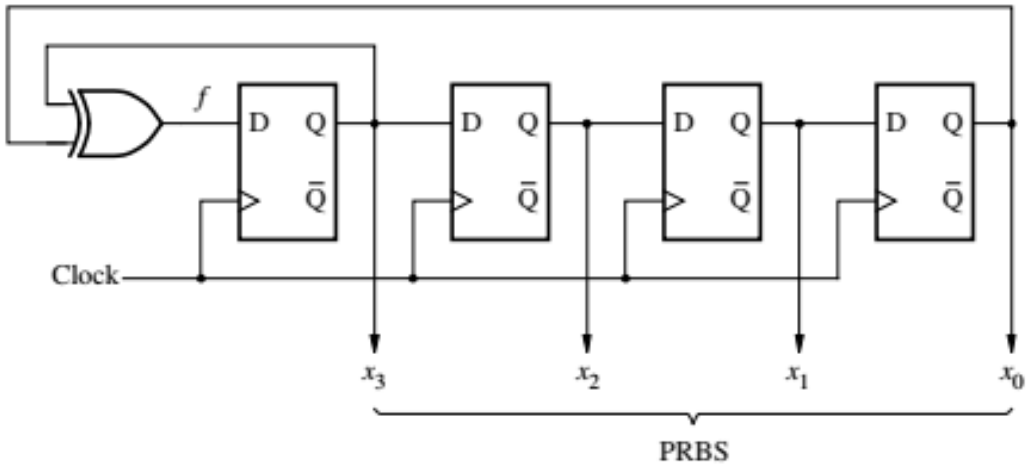
- BIST is a DFT technique that enables a circuit to test itself
- Adds test generation and output analysis circuitry on-chip
- Removes the need for external Automatic Test Equipment (ATE)
- Improves test speed, accessibility, and fault coverage



BIST (Built In Self Test)

- Useful for field test and diagnosis (less expensive than a local automatic test equipment)
- Software tests for field test and diagnosis:
  - Low hardware fault coverage
  - Low diagnostic resolution
  - Slow to operate
- Hardware BIST benefits:
  - Lower system test effort
  - Improved system maintenance and repair
  - Improved component repair
  - Better diagnosis

Pseudorandom Generator



Pseudorandom Binary Sequence Generator (PRBSG) (LFSR)

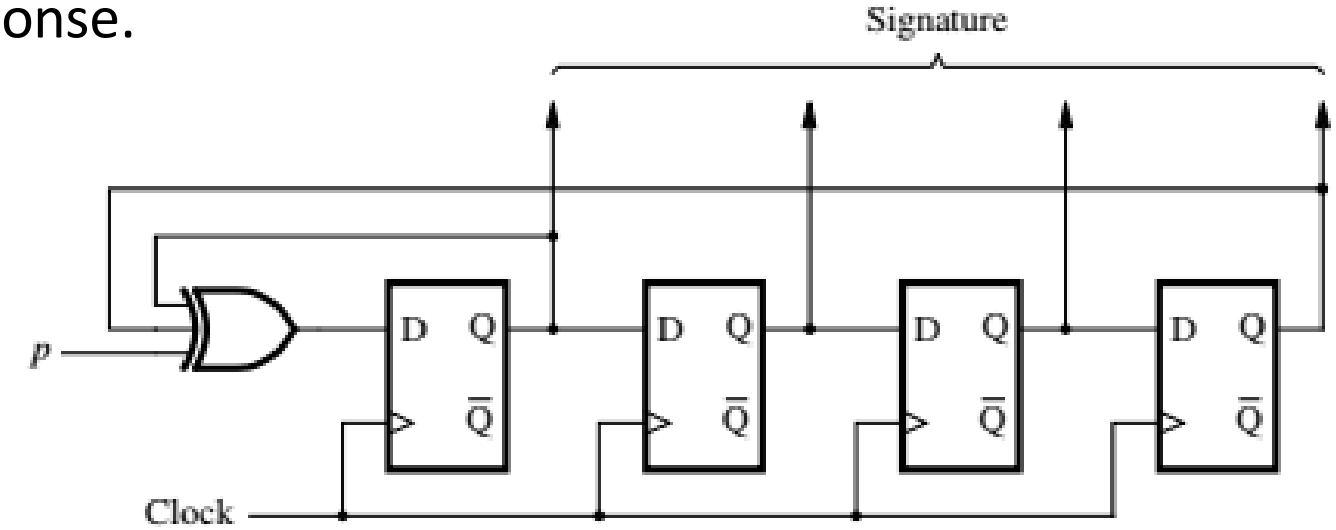
x_3	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0	1	...
x_2	0	1	1	1	1	0	1	0	1	1	0	0	1	0	0	0	...
x_1	0	0	1	1	1	1	0	1	0	1	1	0	0	1	0	0	...
x_0	0	0	0	1	1	1	1	0	1	0	1	1	0	0	1	0	...
f	1	1	1	0	1	0	1	1	0	0	1	0	0	0	1	1	...

Generated Sequence

- Used to generate test patterns internally in BIST.
- Based on Linear Feedback Shift Registers (LFSRs).
- Eliminates need for storing large test vectors.
- Provides good fault coverage due to randomness.

Single Input Compressor (SIC)

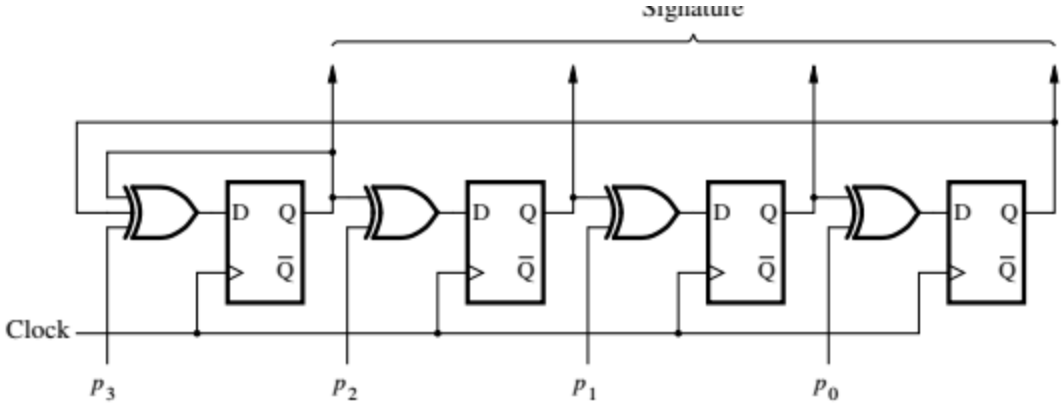
- A Single Input Compressor is essentially a Linear Feedback Shift Register (LFSR) that:
- Takes the test response from a single output line of the circuit.
- Serially shifts these values into the LFSR.
- Produces a compact signature (n-bit) summarizing the entire response.



Single Input Compressor

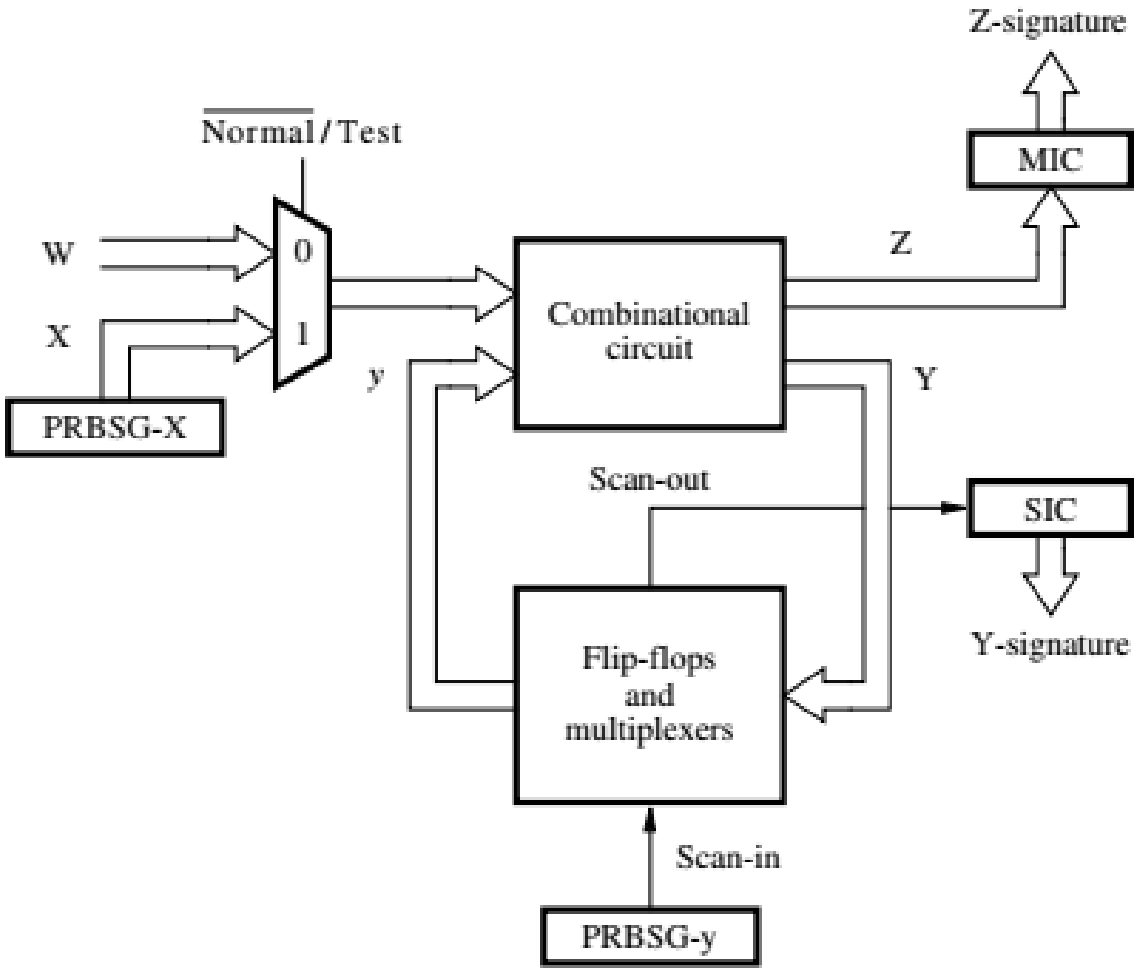
Multiple Input Compressor (SIC)

- A Multiple Input Compressor is a Linear Feedback Shift Register (LFSR) that:
- Accepts multiple output lines from the CUT (e.g., $p0$,$p1$,…,pnp 0 ,p 1 ,…,p n)
- XORs these values into selected stages of the LFSR
- Generates a compact n-bit signature summarizing the overall response.



Multiple Input Compressor

BIST in Sequential Circuits

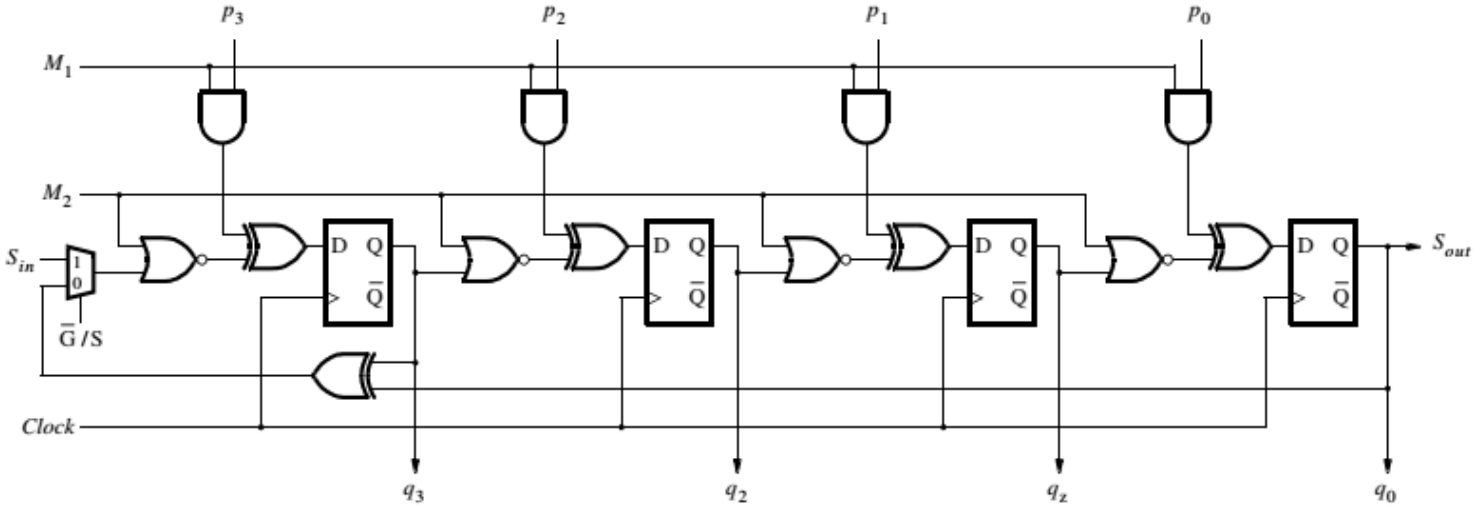


BILBO (Built-in Logic Block Observer)

- The essence of BIST is to have internal capability for generation of tests and for compression of the results.
- Instead of using separate circuits for these two functions, it is possible to design a single circuit that serves both purposes
- **BILBO** is a register that can operate in multiple modes
- **Normal mode** – behaves as a regular register in the circuit
- **Scan mode** – behaves like a shift register for test access
- **Pattern generation mode** – acts like a pseudo-random pattern generator (PRPG)
- **Signature analysis mode** – acts like a signature analyzer or LFSR to compress outputs.

BILBO (Built-in Logic Block Observer)

- **M1M2 = 11**— Normal system mode in which all flip-flops are independently controlled by the signals on inputs p0 through p3
- **M1M2 = 00** — Shift-register mode in which the flip-flops are connected into a shift register
- **M1M2 = 10** — Signature mode in which a series of patterns applied on inputs p0 through p3 are compressed into a signature
- **M1M2 = 01** — Reset mode in which all flip-flops are reset to 0



4 bit Built In Logic Block Observer

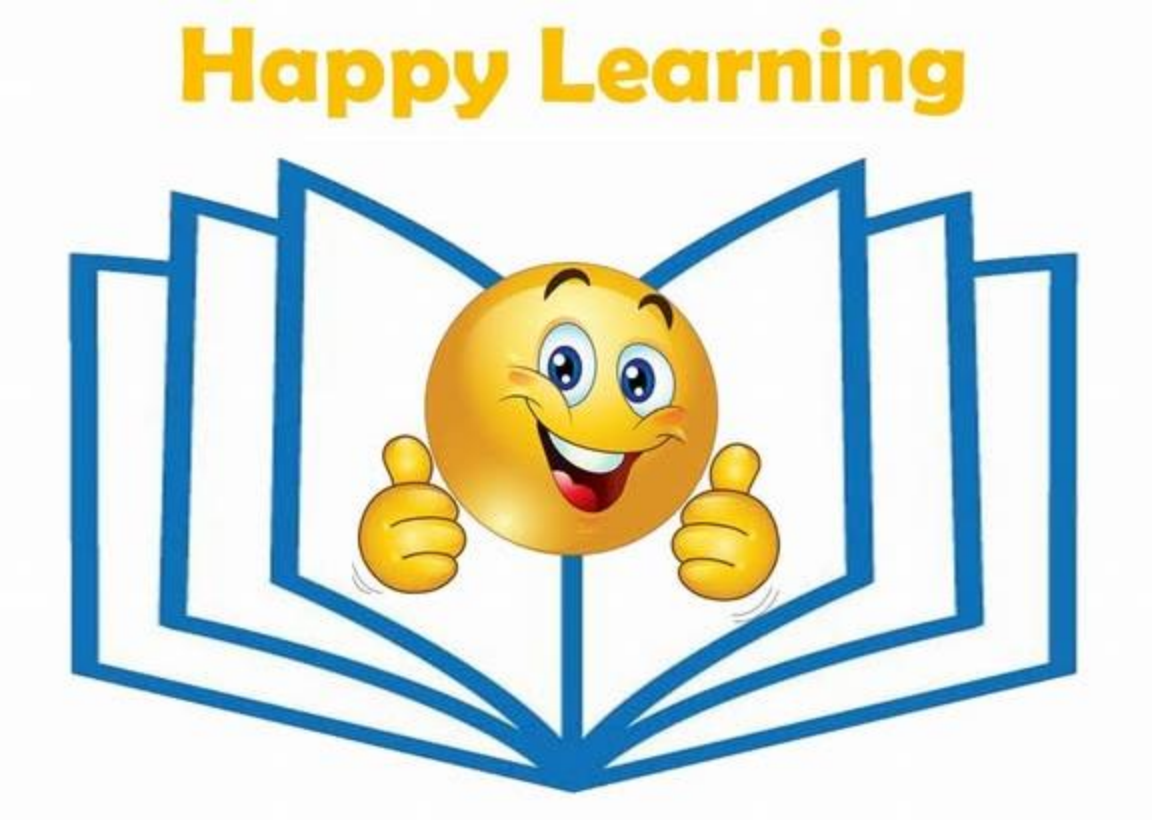
Summary

- Types of Testing
- Manufacturing Testing: Detects physical defects (e.g., stuck-at faults).
- Design Verification: Ensures the logic design matches functional requirements
- Challenges:
- Sequential circuits are harder to test due to internal states
- Large designs can't be tested exhaustively — smart strategies are needed
- Limited observability and controllability of internal nodes.
- Key Techniques:Scan Design (DFT): Adds shift registers to access flip-flops; BIST (Built-In Self-Test): Circuit tests itself using pattern

Summary

Key Techniques:

- **Scan Design (DFT):** Adds shift registers to access flip-flops
- **BIST (Built-In Self-Test):** Circuit tests itself using pattern generation and response compression
- **PRBSG + LFSR:** Generate test patterns and compress output into a signature
- **Test Compression:** Reduces test data volume using single or multiple input signature analysis



Thank You !!!!