

Technology Scaling

Pravin Zode

Outline

- Moore's Law
- Why Scaling in CMOS?
- Types of Scaling
- Scaling Influence

Moore's Law



Gordon Moore
1929-2023

- Moore's Law is an empirical observation made by Gordon Moore, co-founder of Intel
- He noted that the number of transistors on a microchip was doubling approximately every two years
- Predicting an exponential increase in computing power and a decrease in relative cost over time

Why Scaling in CMOS?

The only constant in VLSI is constant change

- Increased Computational Power
- Reduced Power Consumption
- Improved Performance and Speed
- Cost Efficiency
- Increased Device Functionality
- Enhanced Portability and Miniaturization
- Support for Emerging Technologies

Scaling Types

Constant-Field Scaling

Reduces device dimensions (channel length, oxide thickness, etc.) and supply

Constant-Voltage Scaling

Reduces device dimensions while keeping the supply voltage constant

Generalized Scaling

flexible approach that scales device dimensions, supply voltage, and other parameters independently, aiming to balance performance, power, and reliability



Constant-Field Scaling

- Constant-field scaling, often called "Dennard Scaling" after Robert Dennard
- Involves scaling down the dimensions of transistors while keeping the electric field across them constant
- Scaling assumptions
 - All dimensions ($x, y, z \Rightarrow W, L, t_{ox}$)
 - Voltage (V_{DD})
 - Doping levels

Improve device speed, reduce power consumption, and increase integration density

Constant-Voltage Scaling

- Device dimensions are reduced while keeping the supply voltage constant
- This approach is used to improve transistor performance (switching speed) without reducing the supply voltage
- Leads to higher power density, increased leakage currents, and thermal issues

Scaling Influence

Parameter	Sensitivity	Dennard Scaling	Constant Voltage	Lateral Scaling
Scaling Parameters				
Length: L		$1/S$	$1/S$	$1/S$
Width: W		$1/S$	$1/S$	1
Gate oxide thickness: t_{ox}		$1/S$	$1/S$	1
Supply voltage: V_{DD}		$1/S$	1	1
Threshold voltage: V_{tn}, V_{tp}		$1/S$	1	1
Substrate doping: N_A		S	S	1

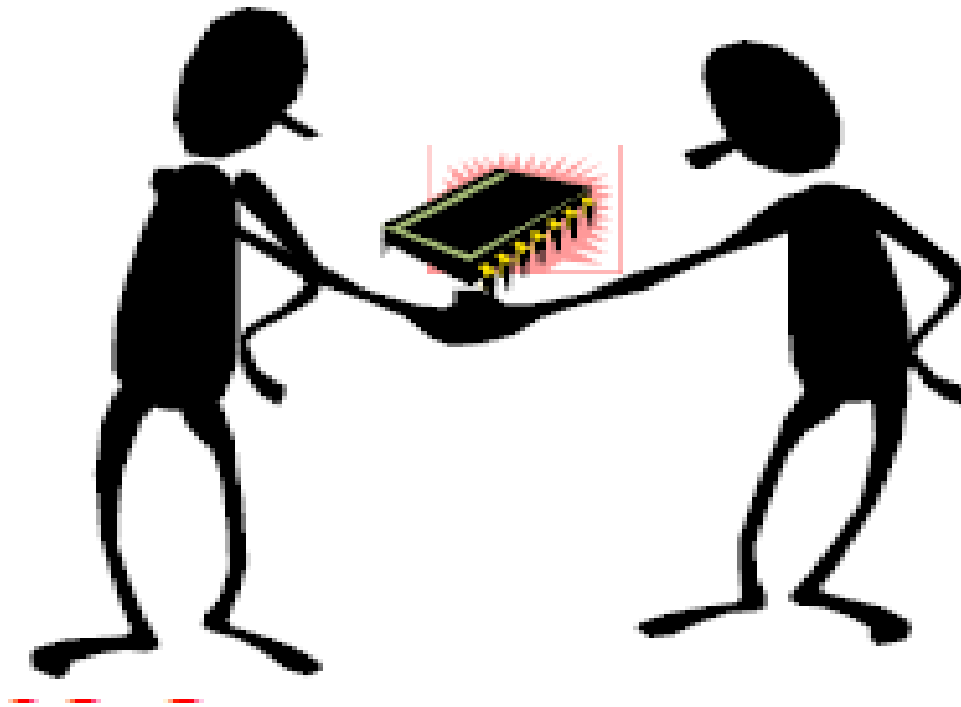
[Detail with \$\alpha\$](#)

Scaling Influence

Device Characteristics				
β	$\frac{W}{L} \frac{1}{t_{ox}}$	S	S	S
Current: I_{ds}	$\beta(V_{DD} - V_t)^2$	$1/S$	S	S
Resistance: R	$\frac{V_{DD}}{I_{ds}}$	1	$1/S$	$1/S$
Gate capacitance: C	$\frac{WL}{t_{ox}}$	$1/S$	$1/S$	$1/S$
Gate delay: τ	RC	$1/S$	$1/S^2$	$1/S^2$
Clock frequency: f	$1/\tau$	S	S^2	S^2
Switching energy (per gate): E	CV_{DD}^2	$1/S^3$	$1/S$	$1/S$
Switching power dissipation (per gate): P	Ef	$1/S^2$	S	S
Area (per gate): A		$1/S^2$	$1/S^2$	1
Switching power density	P/A	1	S^3	S
Switching current density	I_{ds}/A	S	S^3	S

Scaling Influence

- **Diminishing Returns:** Power and thermal limitations challenge further scaling
- **End of Dennard Scaling:** Shift towards multi-core and architectural optimizations
- **Rising Fabrication Complexity and Cost:** Increases both economic and technical barriers
- **Physical and Quantum Limits:** Atomic-scale challenges (e.g., tunneling, heat) signal CMOS nearing its limits.



Thank you !

Happy Learning

Scaling Influence

TABLE 4.12 Influence of Scaling on MOS-Device Characteristics			
PARAMETER	SCALING MODEL		
	Constant field	Constant voltage	Lateral
Length (L)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Width (W)	$1/\alpha$	$1/\alpha$	1
Supply voltage (V)	$1/\alpha$	1	1
Gate-oxide thickness (t_{ox})	$1/\alpha$	$1/\alpha$	1
Current ($I = (W/L)(1/t_{ox})V^2$)	$1/\alpha$	α	α
Transconductance (g_m)	1	α	α
Junction depth (X_j)	$1/\alpha$	$1/\alpha$	1
Substrate doping (N_A)	α	α	1
Electric Field across gate oxide (E)	1	α	1
Depletion layer thickness (d)	$1/\alpha$	$1/\alpha$	1
Load Capacitance ($C = WL/t_{ox}$)	$1/\alpha$	$1/\alpha$	$1/\alpha$
Gate Delay (VC/I)	$1/\alpha$	$1/\alpha^2$	$1/\alpha^2$
RESULTANT INFLUENCE			
DC power dissipation (P_s)	$1/\alpha^2$	α	α
Dynamic power dissipation (P_d)	$1/\alpha^2$	α	α
Power-delay product	$1/\alpha^3$	$1/\alpha$	$1/\alpha$
Gate Area ($A = WL$)	$1/\alpha^2$	$1/\alpha^2$	$1/\alpha$
Power Density (VI/A)	1	α^3	α^2
Current Density	α	α^3	α^2

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