

Steps for LVS Design Flow

Note:- save .cir files in same folder where generated netlist are saved / Else specify the path in .cir files.

For Schematic Side

1. Install netgen
2. Generate netlist from Xschem
3. Create a new .cir file as given example below (in text editor) by filtering out the simulation related command and voltage sources from netlist (ex. Voltage sources, simulation commands like .dc, .tran etc.)

Follow the example given below:-

```
** inv_xschem.cir

x1 a y vp vn inv          // create a instance of following subcircuit and follow same port order as
below

.subckt inv a y VP VN      // add the ports here according to the circuit (for inverter, like a , y ,
vdd, gnd)

XM1 y a VN VN sky130_fd_pr__nfet_01v8 L=0.15 W=1 nf=1 ad='int((nf+1)/2) * W/nf * 0.29'
as='int((nf+2)/2) * W/nf * 0.29'
+ pd='2*int((nf+1)/2) * (W/nf + 0.29)' ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 /
W' nrs='0.29 / W'
+ sa=0 sb=0 sd=0 mult=1 m=1
XM2 y a VP VP sky130_fd_pr__pfet_01v8 L=0.15 W=2 nf=1 ad='int((nf+1)/2) * W/nf * 0.29'
as='int((nf+2)/2) * W/nf * 0.29'
+ pd='2*int((nf+1)/2) * (W/nf + 0.29)' ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 /
W' nrs='0.29 / W'
+ sa=0 sb=0 sd=0 mult=1 m=1

.ends
.end
```

For layout side

1. Generate spice file from magic (*.spice).
2. Create a new .cir file as follows (in text editor).

```
-- .cir file
** inv_magic.cir

.include magic_inv.spice    // include name of file spice file create by magic

Xinv A Y VP VN magic_inv    //create instance and follow ports as per given order in spice netlist
generated by magic.

.end
```

Spice netlist generated by magic example:-

* NGSPICE file created from magic_inv.ext - technology: sky130A

.subckt magic_inv A Y VP VN

X0 Y A VN VN sky130_fd_pr__nfet_01v8 ad=4.5e+11p pd=2.9e+06u as=4.5e+11p ps=2.9e+06u
w=1e+06u l=150000u

X1 Y A VP VP sky130_fd_pr__pfet_01v8 ad=9e+11p pd=4.9e+06u as=9e+11p ps=4.9e+06u
w=2e+06u
l=150000u

.ends

Netgen flow:-

1. Open new terminal in folder where the .cir files are saved.
2. Type in command:-

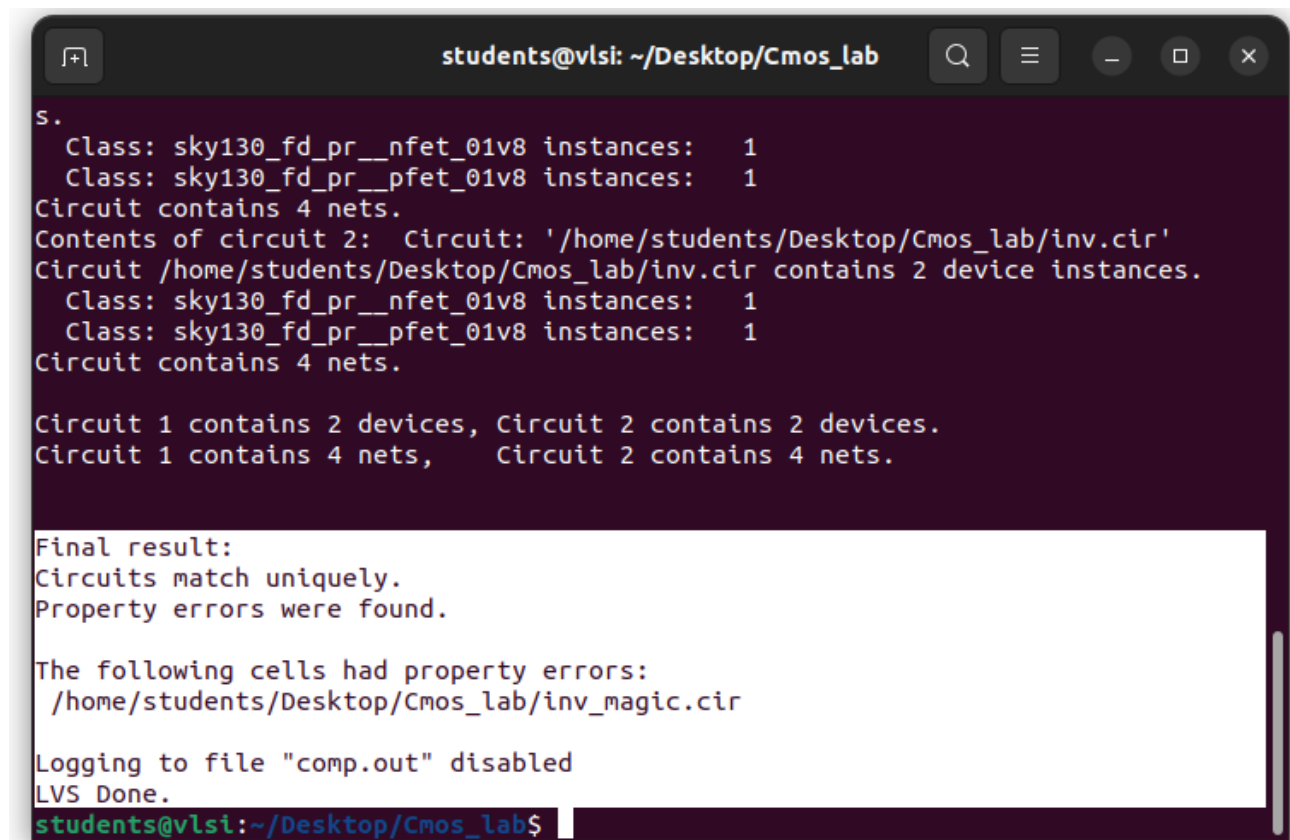
```
netgen -batch lvs <name of schematic cir file.cir> <name of layout cir file.cir> <Environment  
setup file.tcl>
```

Example :-

```
netgen -batch lvs /home/students/Desktop/Cmos_lab/inv_magic.cir  
/home/students/Desktop/Cmos_lab/inv.cir  
/usr/local/share/pdk/sky130A/libs.tech/netgen/sky130A_setup.tcl
```

Note:- In above example the .cir files where stored in another directory so the paths are mentioned instead of names.

After execution of above steps, the results would be as follows if the circuits are matching at the end of :-



```
students@vlsi: ~/Desktop/Cmos_lab
s.
  Class: sky130_fd_pr__nfet_01v8 instances:  1
  Class: sky130_fd_pr__pfet_01v8 instances:  1
Circuit contains 4 nets.
Contents of circuit 2:  Circuit: '/home/students/Desktop/Cmos_lab/inv.cir'
Circuit /home/students/Desktop/Cmos_lab/inv.cir contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances:  1
  Class: sky130_fd_pr__pfet_01v8 instances:  1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets,   Circuit 2 contains 4 nets.

Final result:
Circuits match uniquely.
Property errors were found.

The following cells had property errors:
/home/students/Desktop/Cmos_lab/inv_magic.cir

Logging to file "comp.out" disabled
LVS Done.
students@vlsi:~/Desktop/Cmos_lab$
```