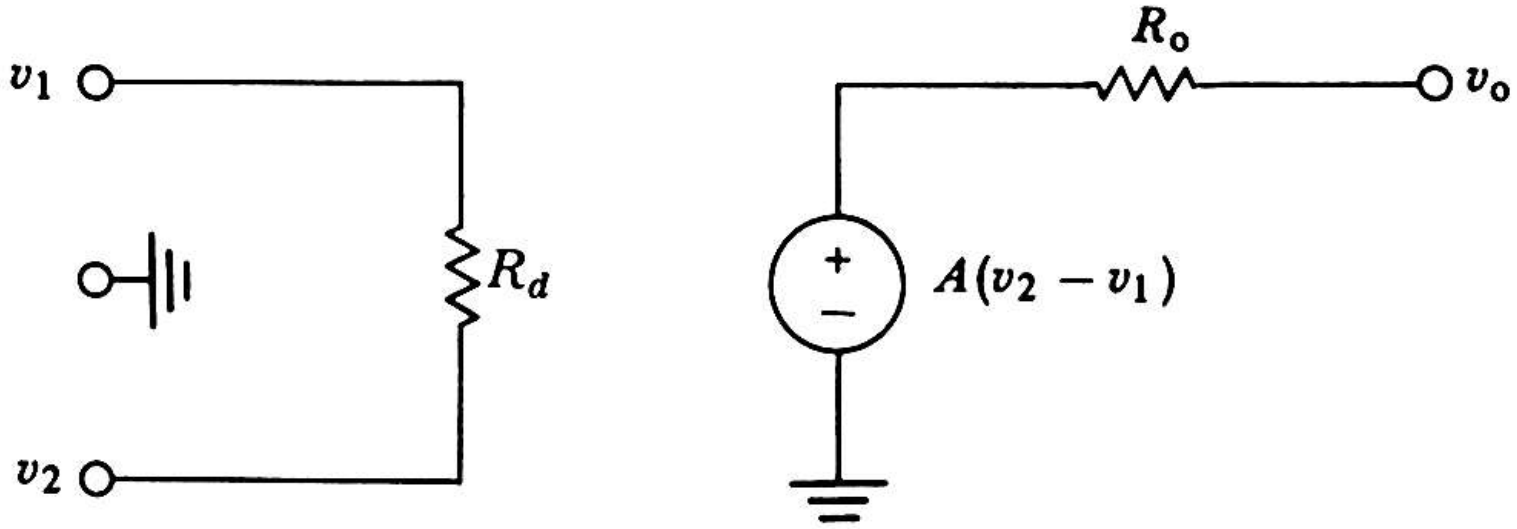


Figure 3.1 Op-amp equivalent circuit. The two inputs are υ_1 and υ_2. A differential voltage between them causes current flow through the differential resistance R_d. The differential voltage is multiplied by A, the gain of the op amp, to generate the output-voltage source. Any current flowing to the output terminal vo must pass through the output resistance R_o.

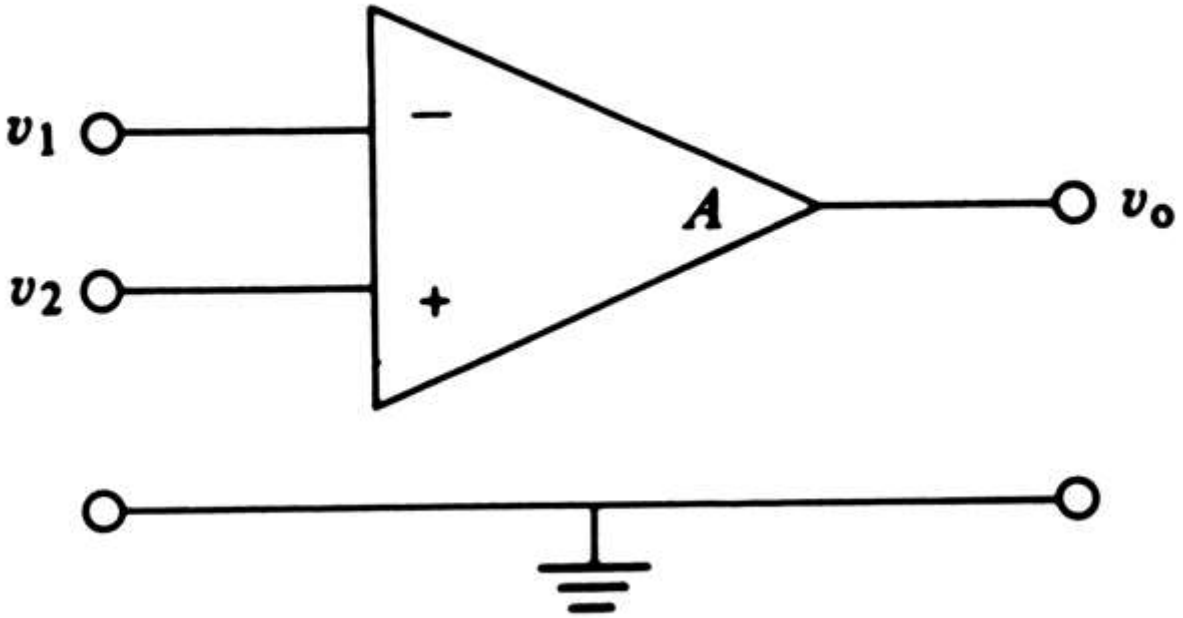


Figure 3.2 Op-amp circuit symbol. A voltage at v_1, the inverting input, is greatly amplified and inverted to yield υ_o. A voltage at υ_2, the noninverting input, is greatly amplified to yield an in-phase output at υ_o.

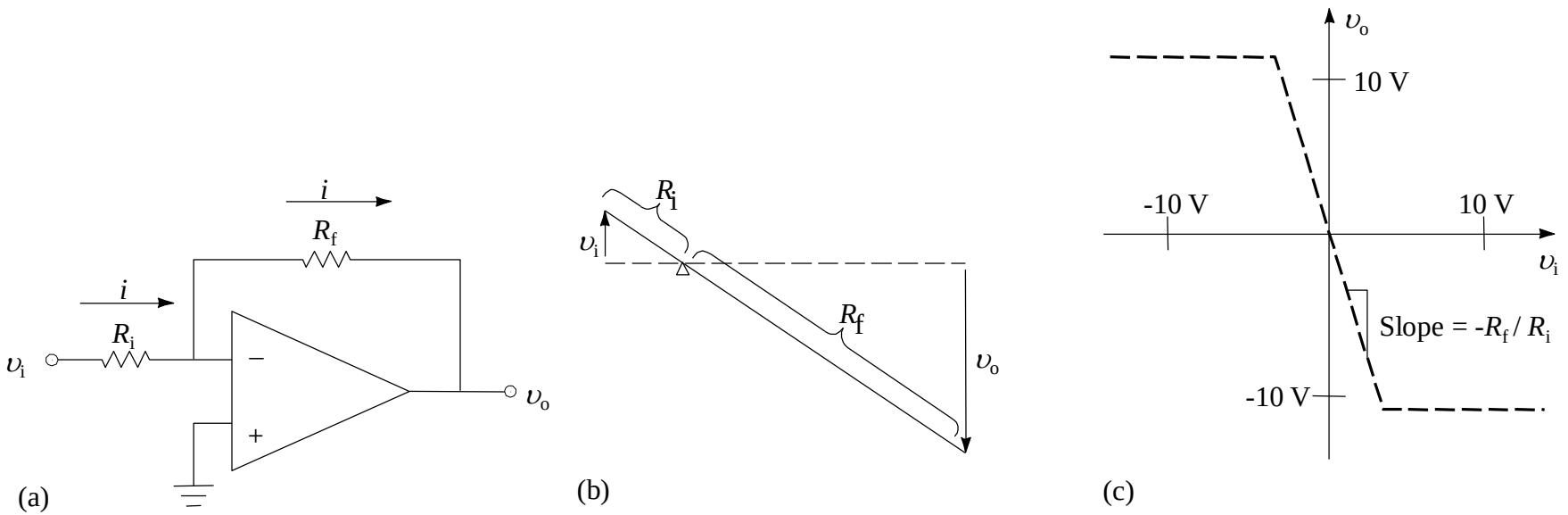


Figure 3.3 (a) An inverting amplified. Current flowing through the input resistor R_i also flows through the feedback resistor R_f. (b) A lever with arm lengths proportional to resistance values enables the viewer to visualize the input-output characteristics easily. (c) The input-output plot shows a slope of $-R_f / R_i$ in the central portion, but the output saturates at about ±13 V.

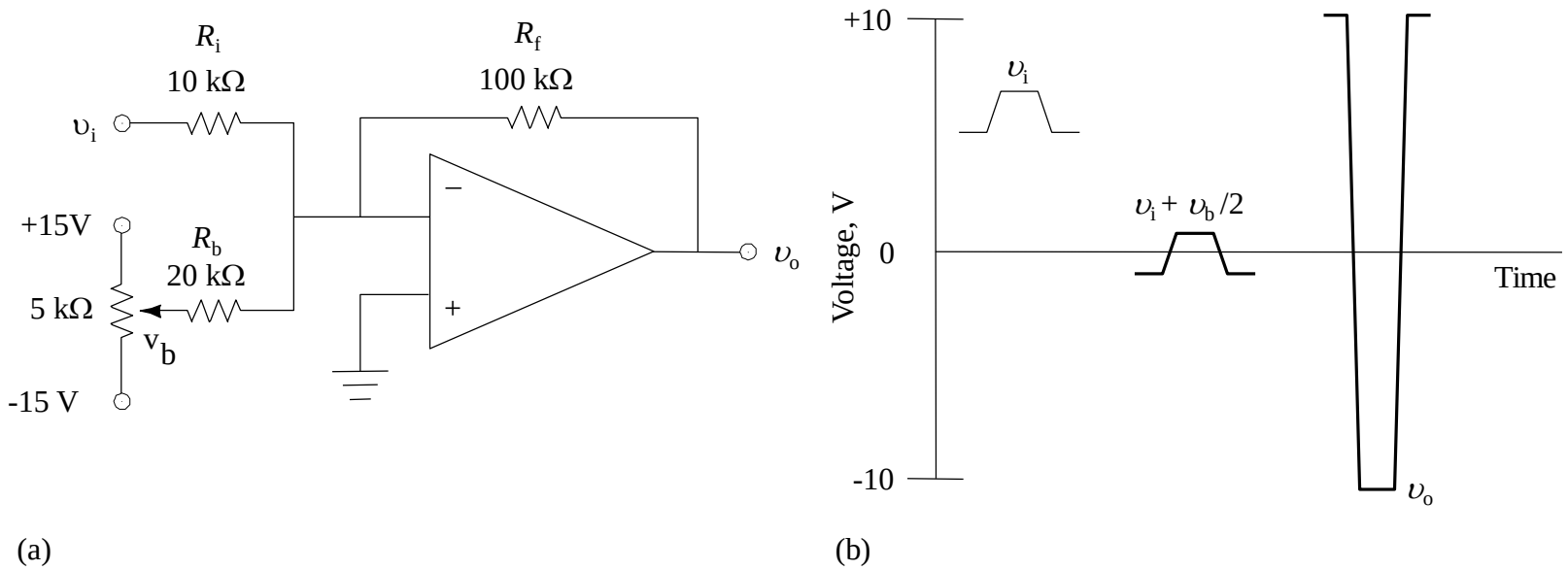


Figure E3.1 (a) This circuit sums the input voltage υ_i plus one-half of the balancing voltage υ_b. Thus the output voltage υ_o can be set to zero even when υ_i has a nonzero dc component. (b) The three waveforms show υ_i, the input voltage; $(\upsilon_i + \upsilon_b/2)$, the balanced-out voltage; and υ_o, the amplified output voltage. If υ_i were directly amplified, the op amp would saturate.

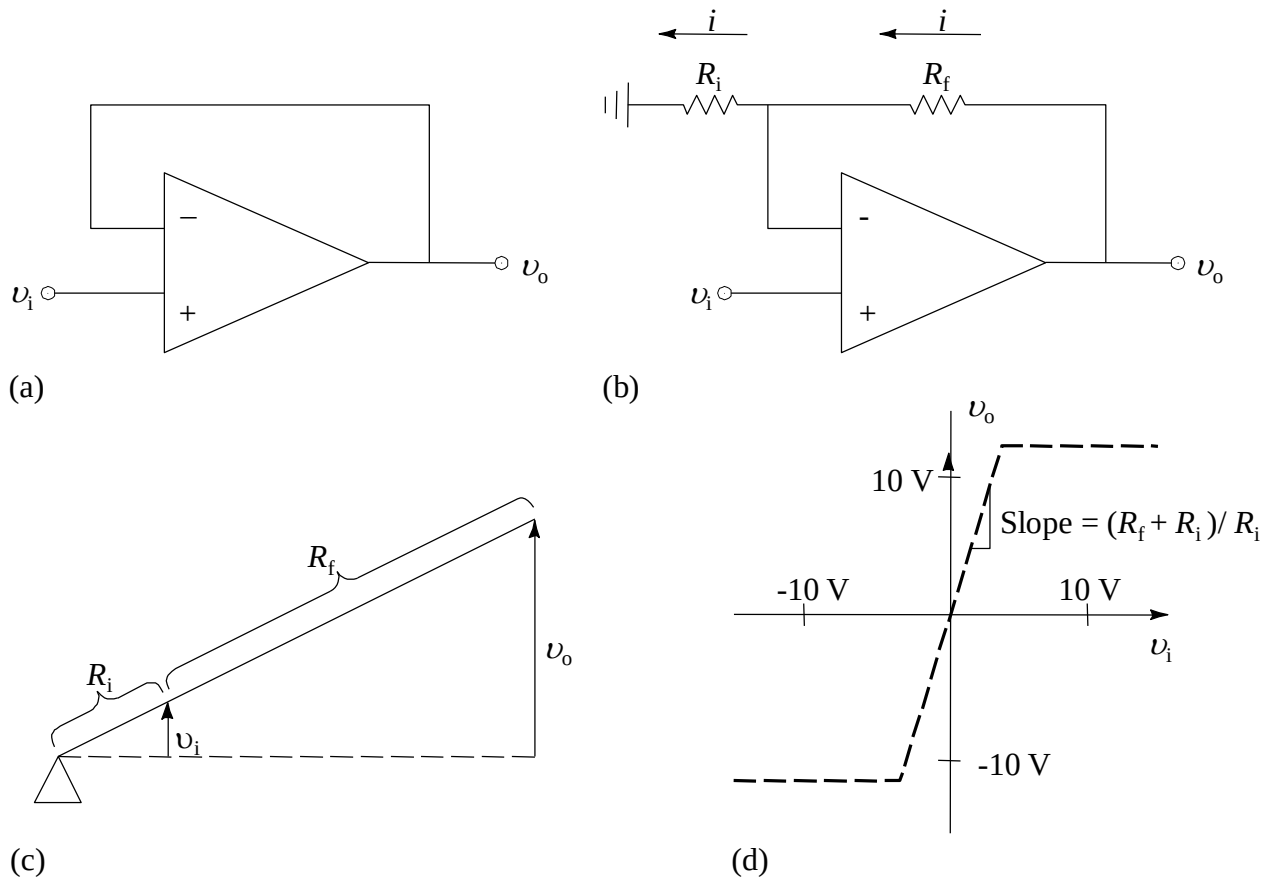


Figure 3.4 (a) A follower, $\upsilon_o = \upsilon_i$. (b) A noninverting amplifier, υ_i appears across R_i , producing a current through R_i that also flows through R_f. (c) A lever with arm lengths proportional to resistance values makes possible an easy visualization of input-output characteristic. (d) The input-output plot shows a positive slope of $(R_f + R_i)/R_i$ in the central portion, but the output saturates at about ±13 V.

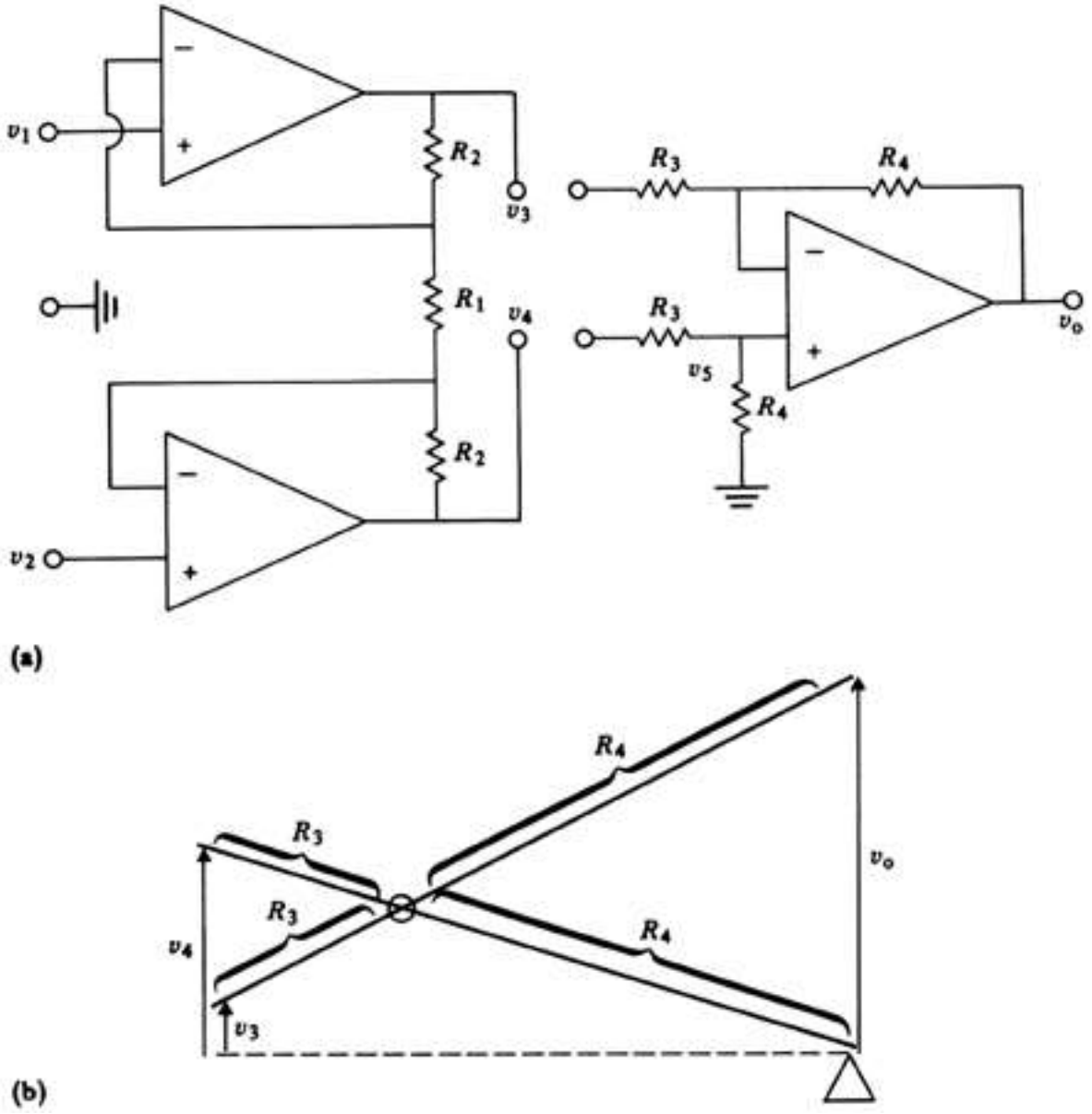


Figure 3.5 (a) The right side shows a one-op-amp differential amplifier, but it has low input impedance. The left side shows how two additional op amps can provide high input impedance and gain. (b) For the one-op-amp differential amplifier, two levers with arm lengths proportional to resistance values make possible an easy visualization of input-output characteristics.

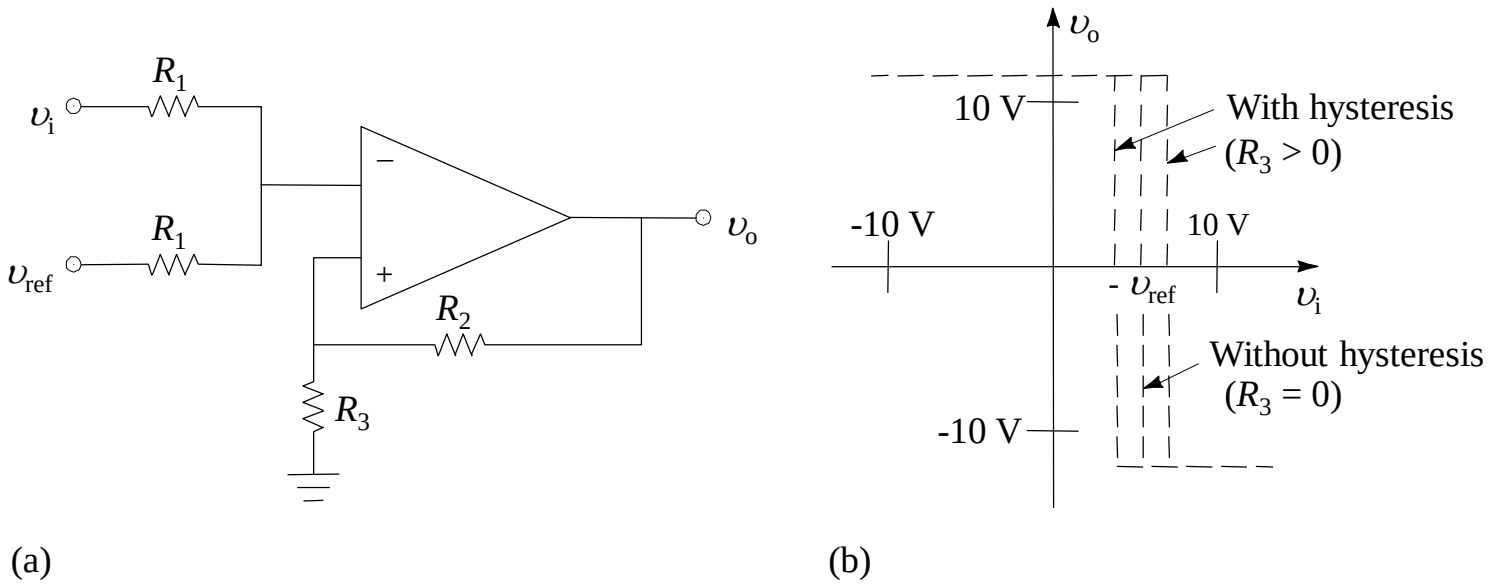


Figure 3.6 (a) Comparator. When $R_3 = 0$, υ_o indicates whether ($\upsilon_i + \upsilon_{Ref}$) is greater or less than 0 V. When R_3 is larger, the comparator has hysteresis, as shown in (b), the input-output characteristic.

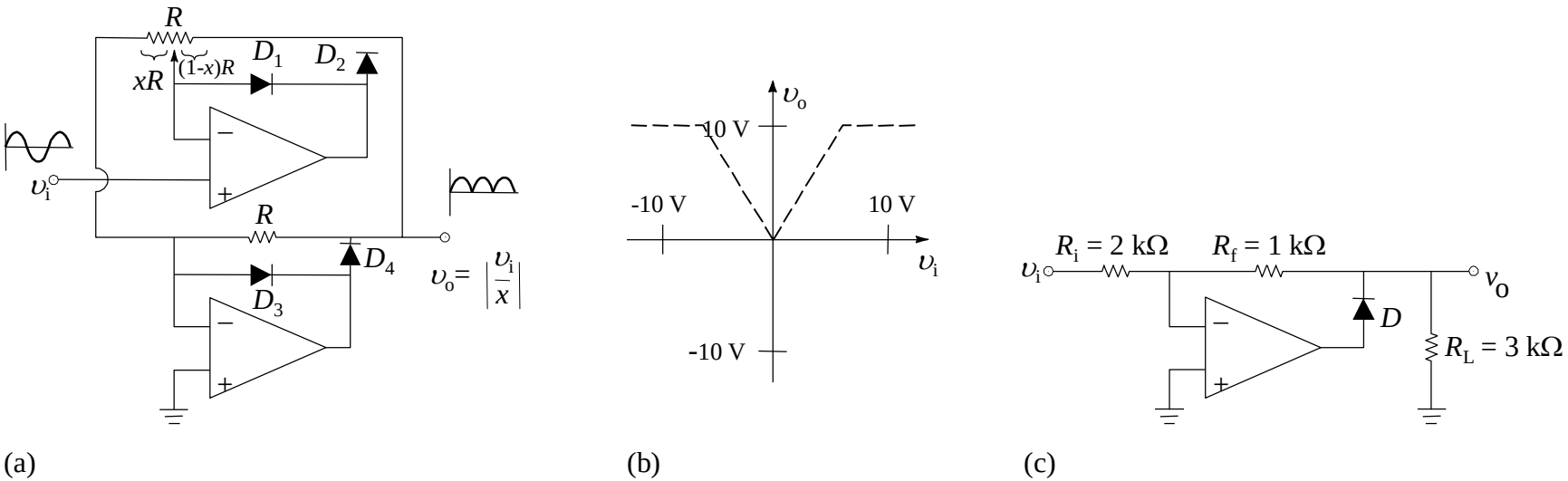


Figure 3.7 (a) Full-wave precision rectifier. For $\upsilon_i > 0$, the noninverting amplifier at the top is active, making $\upsilon_o > 0$. For $\upsilon_i < 0$, the inverting amplifier at the bottom is active, making $\upsilon_o > 0$. Circuit gain may be adjusted with a single pot. (b) Input-output characteristics show saturation when $\upsilon_o > +13$ V. (Reprinted with permission from Electronics Magazine, copyright © December 12, 1974; Penton Publishing, Inc.) (c) One-op-amp full-wave rectifier. For $\upsilon_i < 0$, the circuit behaves like the inverting amplifier rectifier with a gain of +0.5. For $\upsilon_i > 0$, the op amp disconnects and the passive resistor chain yields a gain of +0.5.

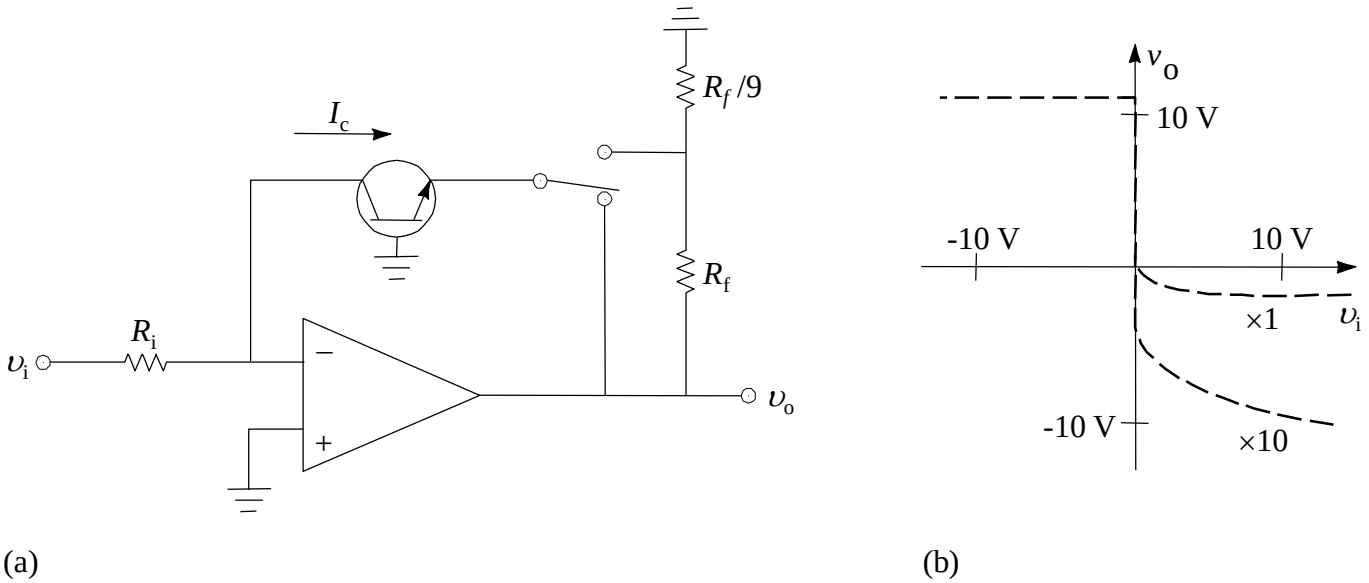


Figure 3.8 (a) A logarithmic amplifier makes use of the fact that a transistor's V_{BE} is related to the logarithm of its collector current. With the switch thrown in the alternate position, the circuit gain is increased by 10. (b) Input-output characteristics show that the logarithmic relation is obtained for only one polarity; ×1 and ×10 gains are indicated.

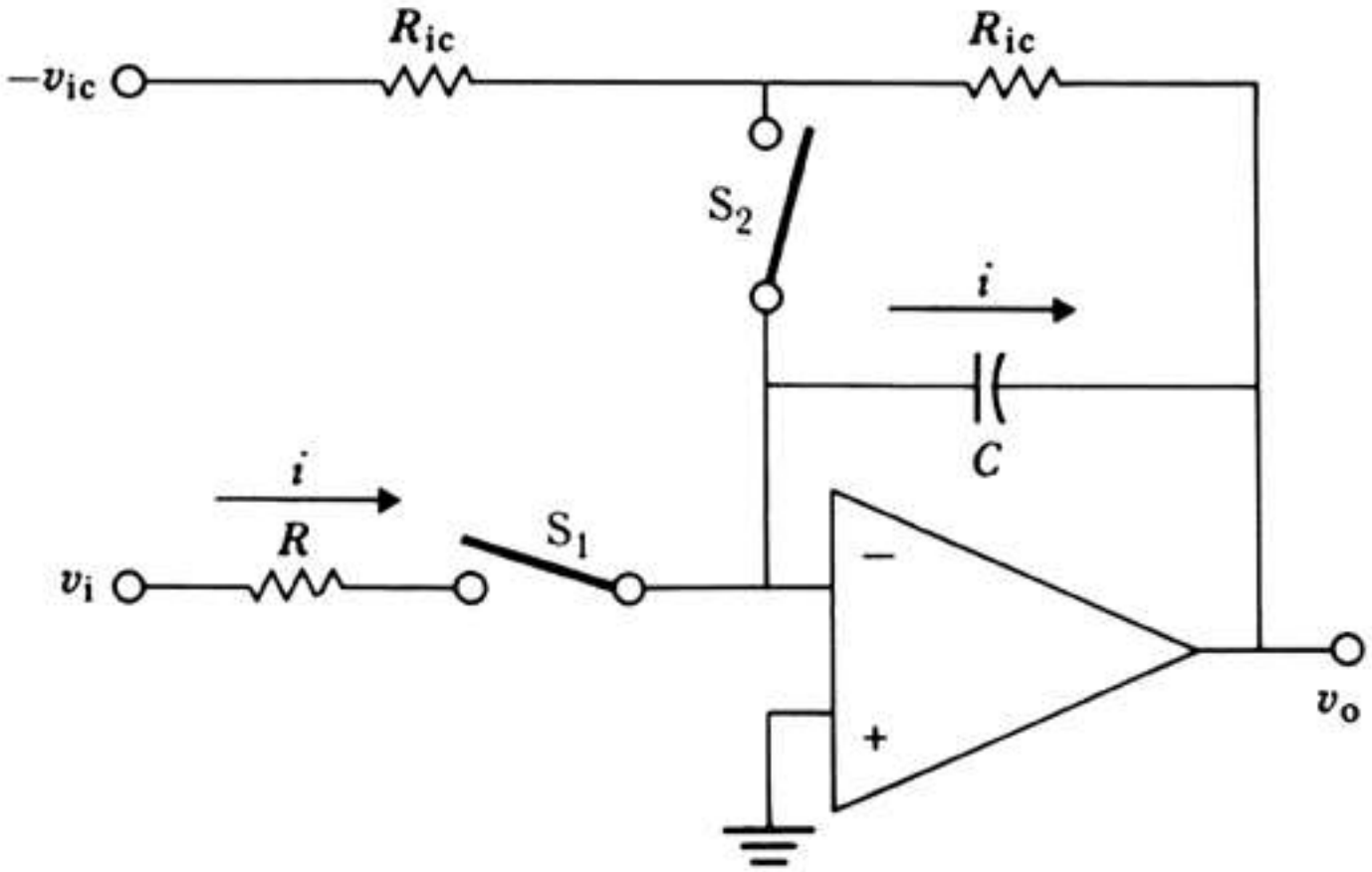


Figure 3.9 A three-mode integrator With S_1 open and S_2 closed, the dc circuit behaves as an inverting amplifier. Thus $\upsilon_o = \upsilon_{ic}$ and υ_o can be set to any desired initial conduction. With S_1 closed and S_2 open, the circuit integrates. With both switches open, the circuit holds υ_o constant, making possible a leisurely readout.

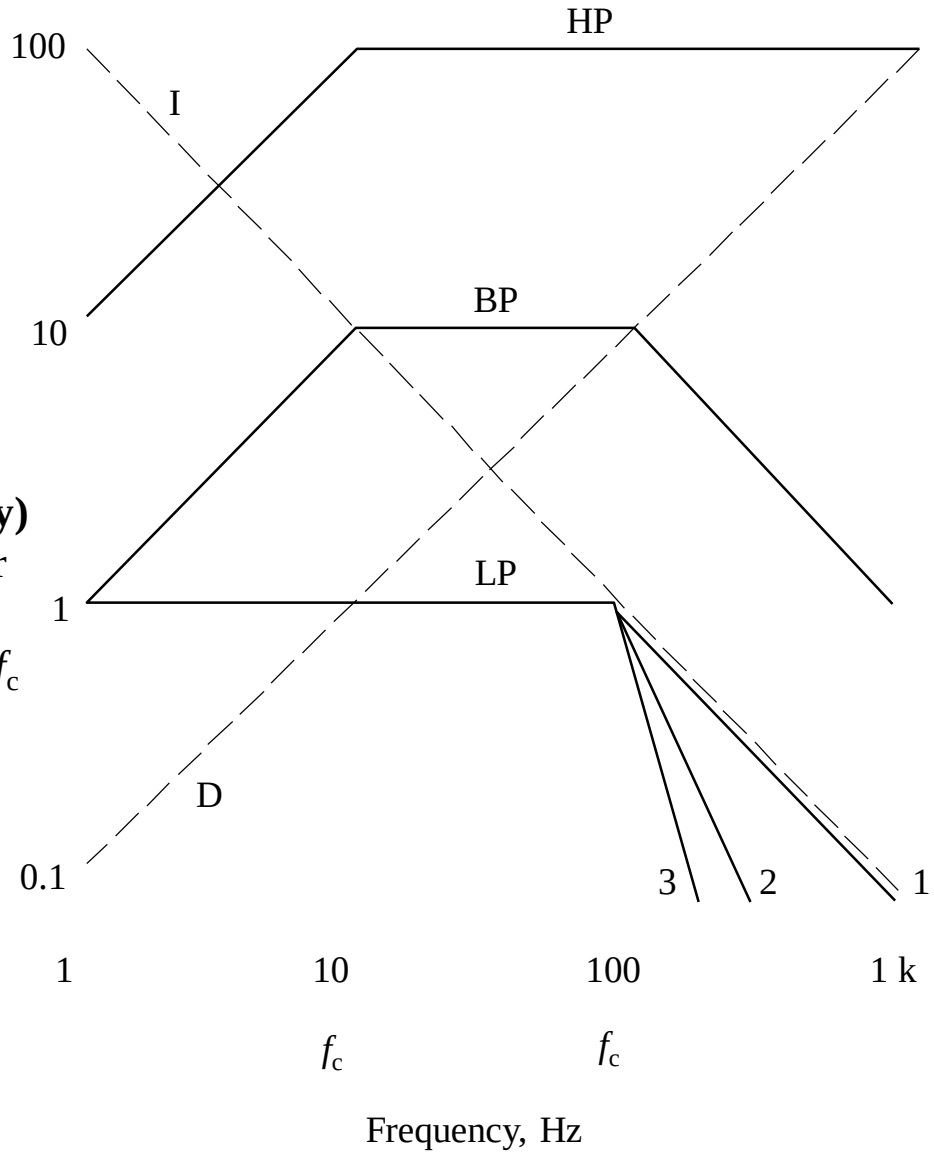


Figure 3.10 Bode plot (gain versus frequency) for various filters. Integrator (I); differentiator (D); low pass (LP), 1, 2, 3 section (pole); high pass (HP);bandpass (BP). Corner frequencies f_c for high-pass, low-pass, and bandpass filters.

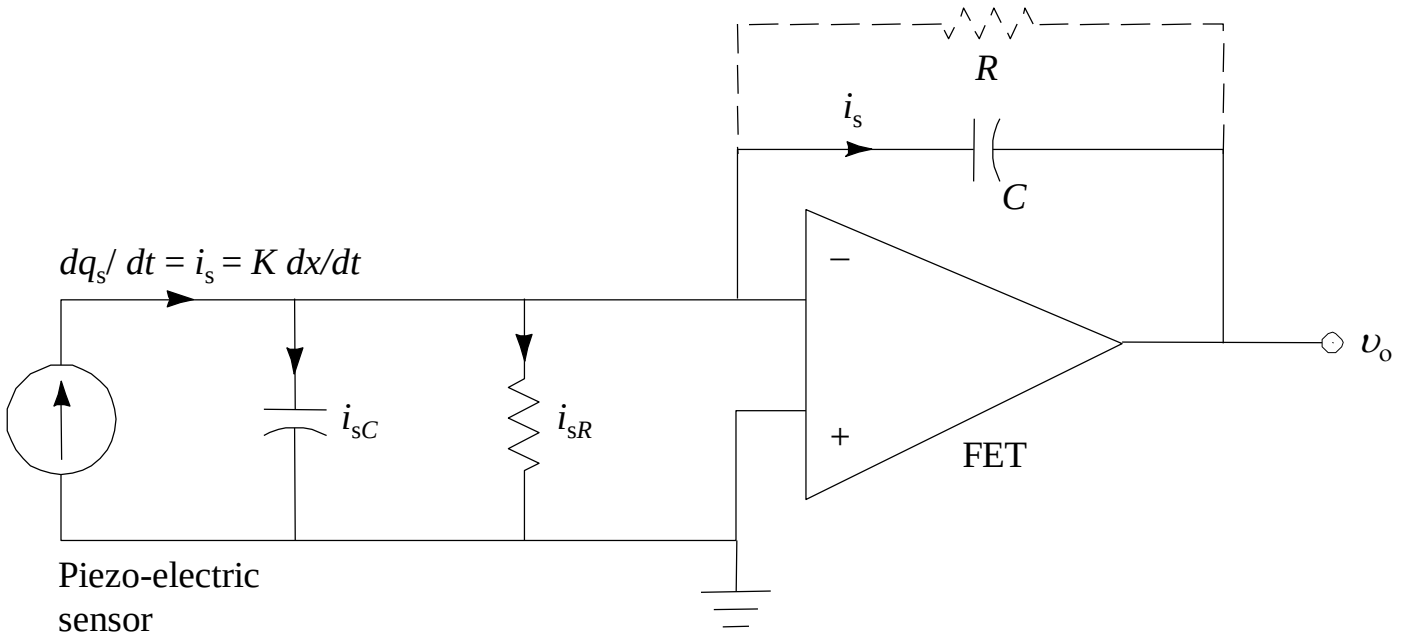


Figure E3.2 The charge amplifier transfers charge generated from a piezo-electric sensor to the op-amp feedback capacitor *C*.

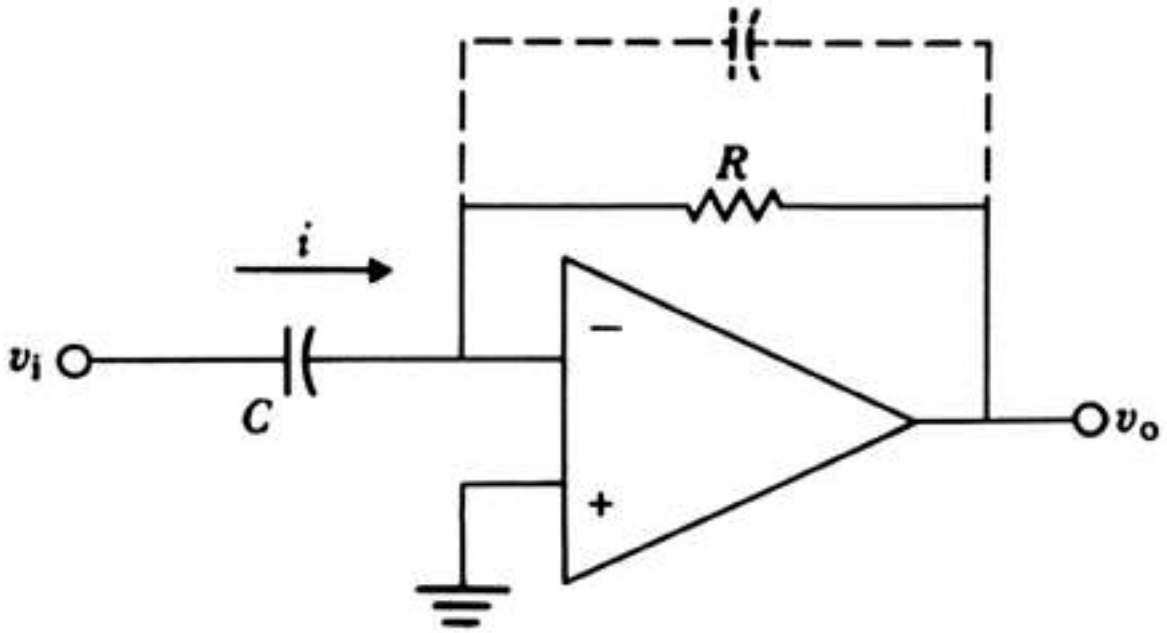


Figure 3.11 A differentiator The dashed lines indicate that a small capacitor must usually be added across the feedback resistor to prevent oscillation.

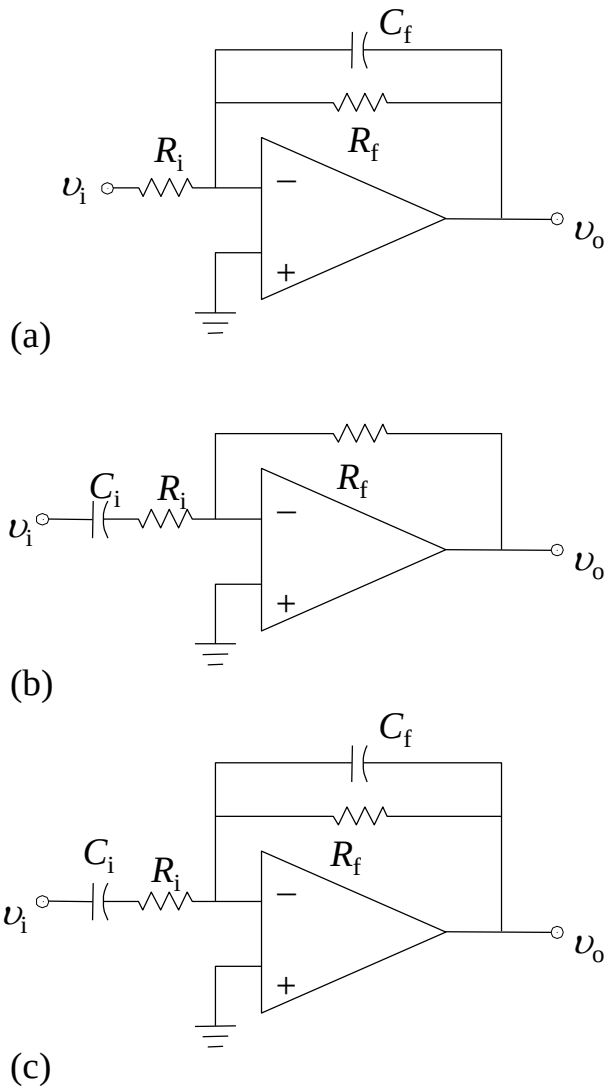
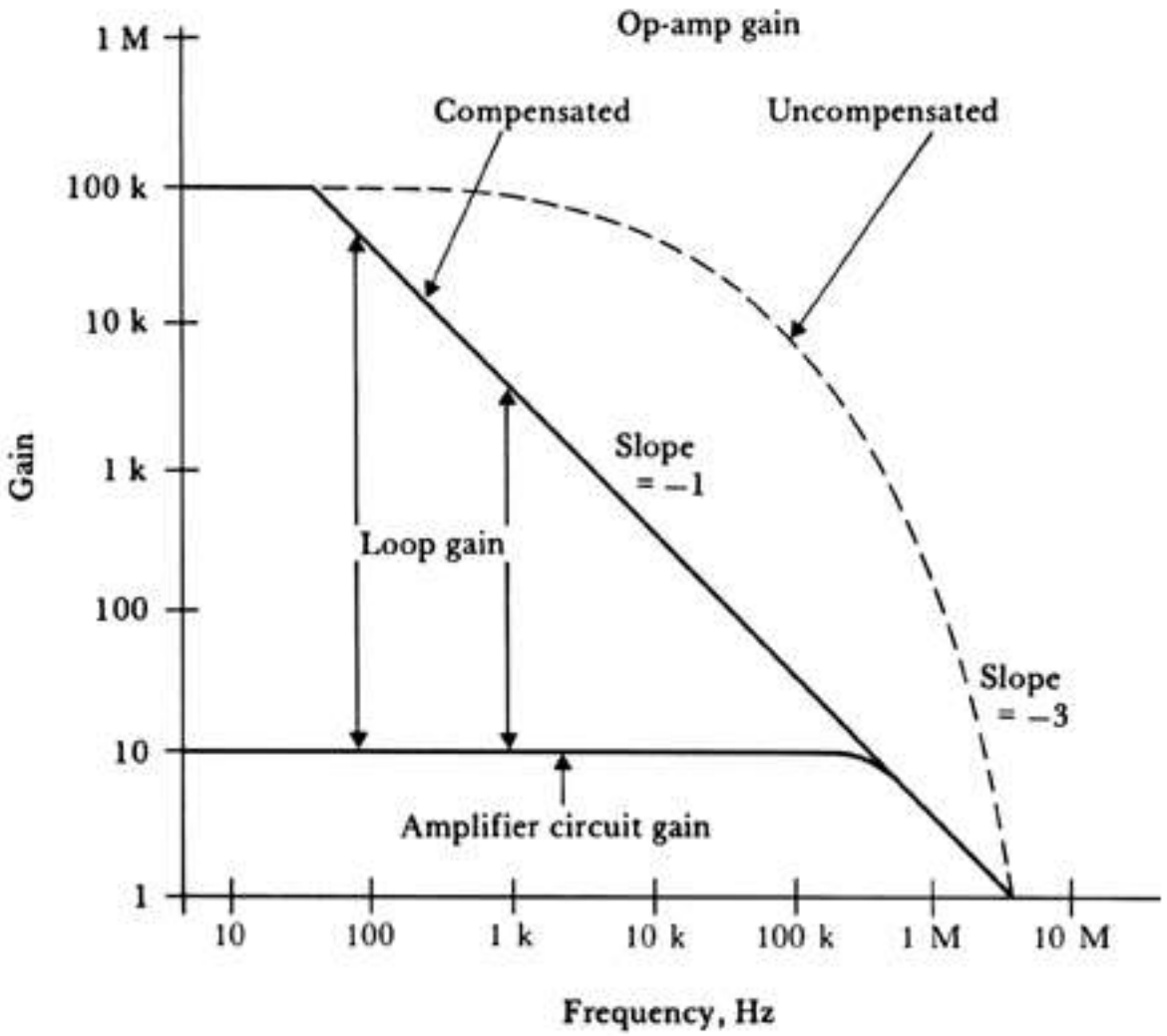


Figure 3.12 Active filters (a) A low-pass filter attenuates high frequencies (b) A high-pass filter attenuates low frequencies and blocks dc. (c) A bandpass filter attenuates both low and high frequencies.

Figure 3.13 Op-amp frequency characteristics early op amps (such as the 709) were uncompensated, had a gain greater than 1 when the phase shift was equal to –180º, and therefore oscillated unless compensation was added externally. A popular op amp, the 411, is compensated internally, so for a gain greater than 1, the phase shift is limited to –90º. When feedback resistors are added to build an amplifier circuit, the loop gain on this log-log plot is the difference between the op-amp gain and the amplifier-circuit gain.



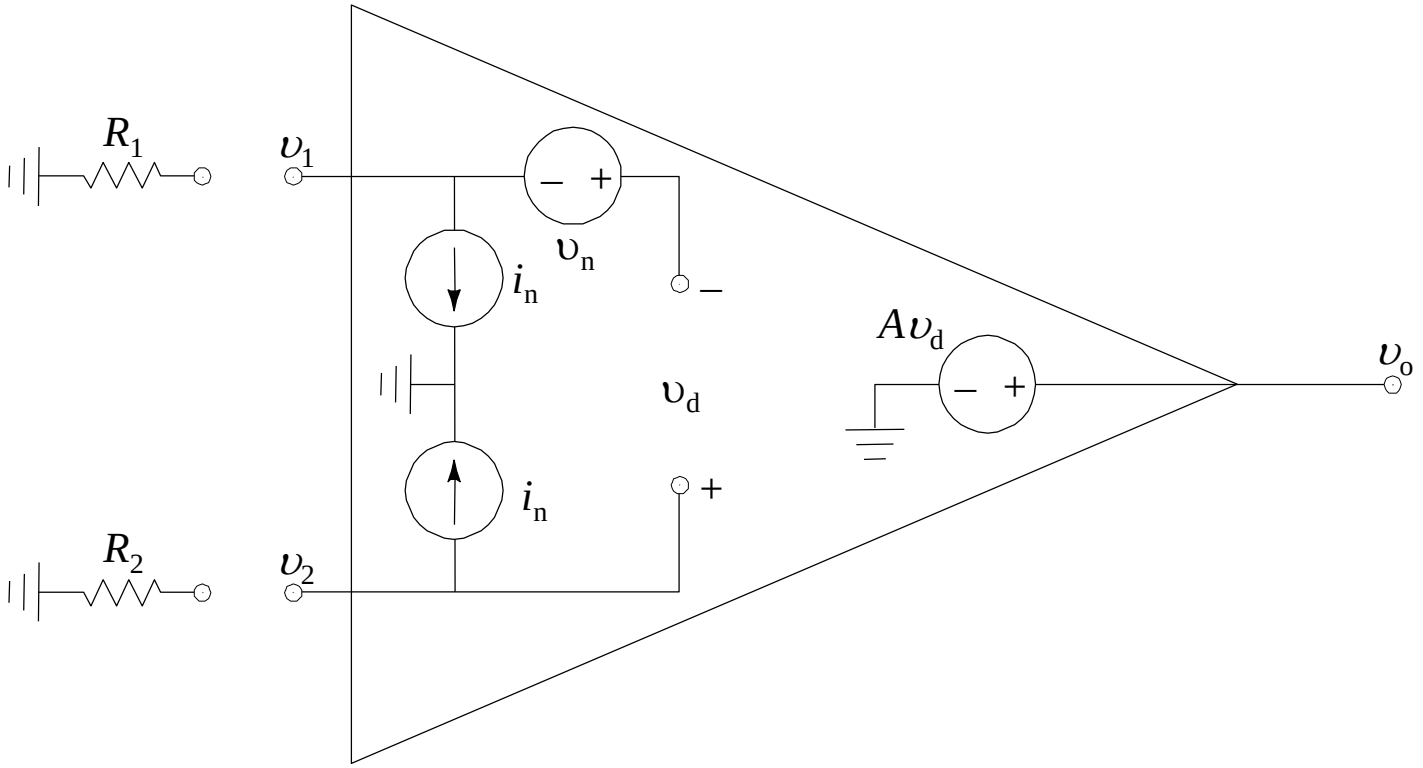


Figure 3.14 Noise sources in an op amp The noise-voltage source v_n is in series with the input and cannot be reduced. The noise added by the noise-current sources In can be minimized by using small external resistances.

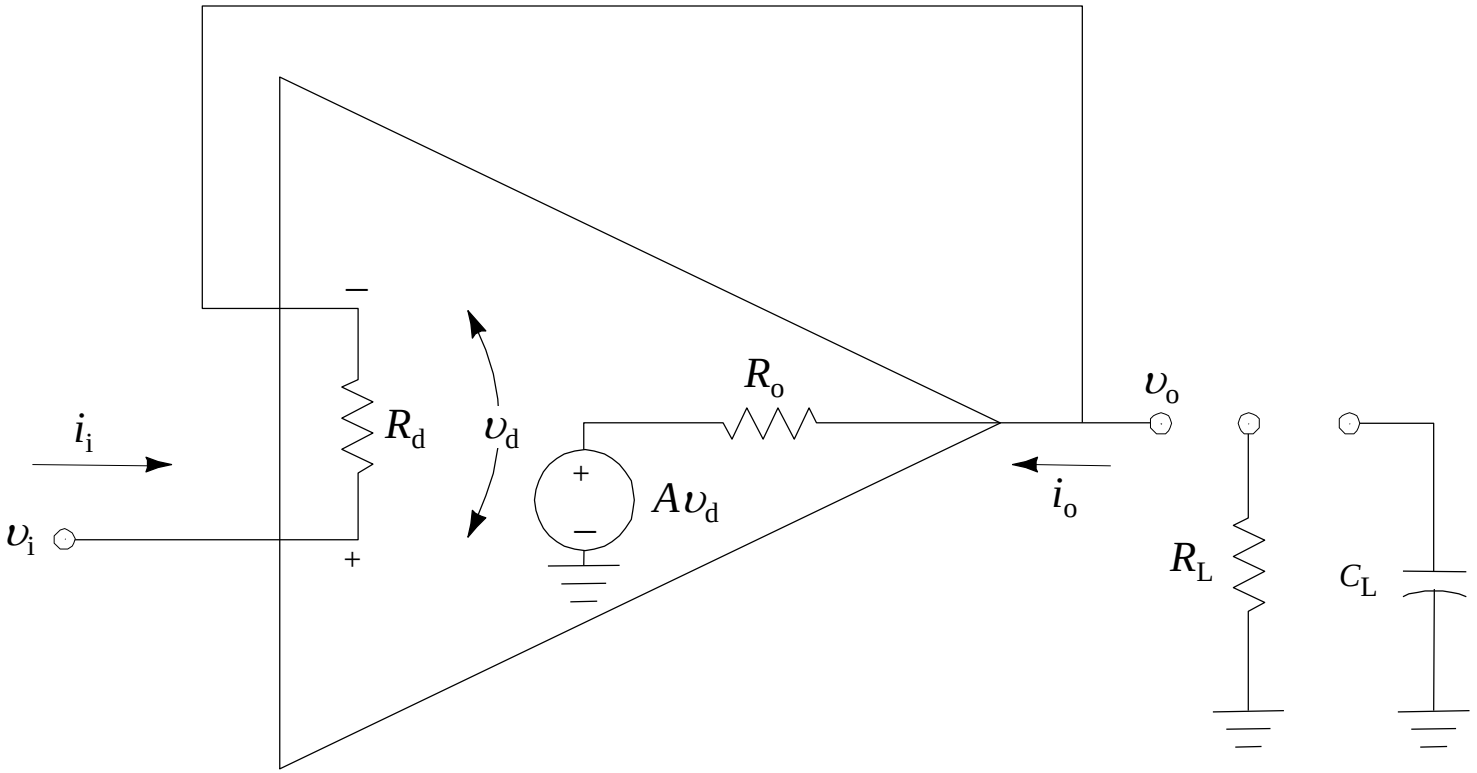


Figure 3.15 The amplifier input impedance is much higher than the op-amp input impedance R_d. The amplifier output impedance is much smaller than the op-amp output impedance R_o.

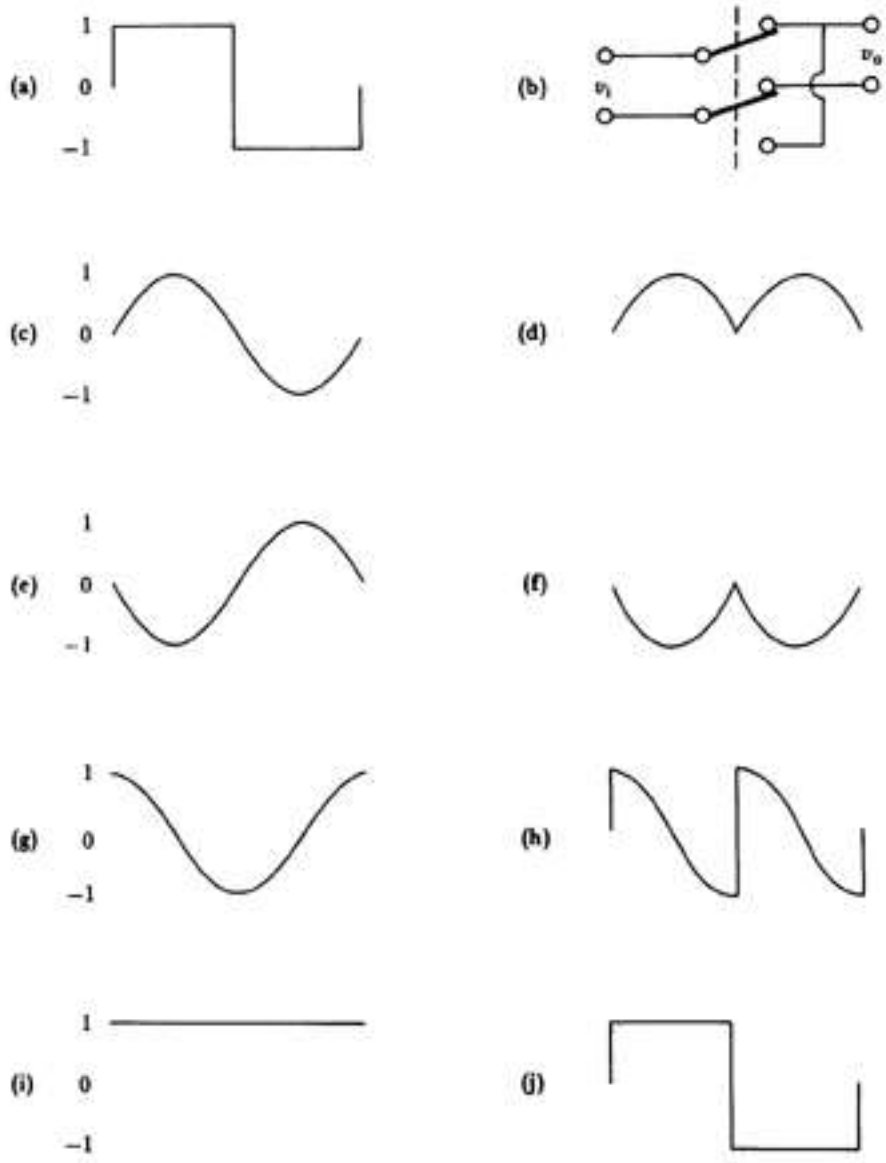


Figure 3.16 Functional operation of a phase-sensitive demodulator (a) Switching function. (b) Switch. (c), (e), (g), (i) Several input voltages. (d), (f), (h), (j) Corresponding output voltages.

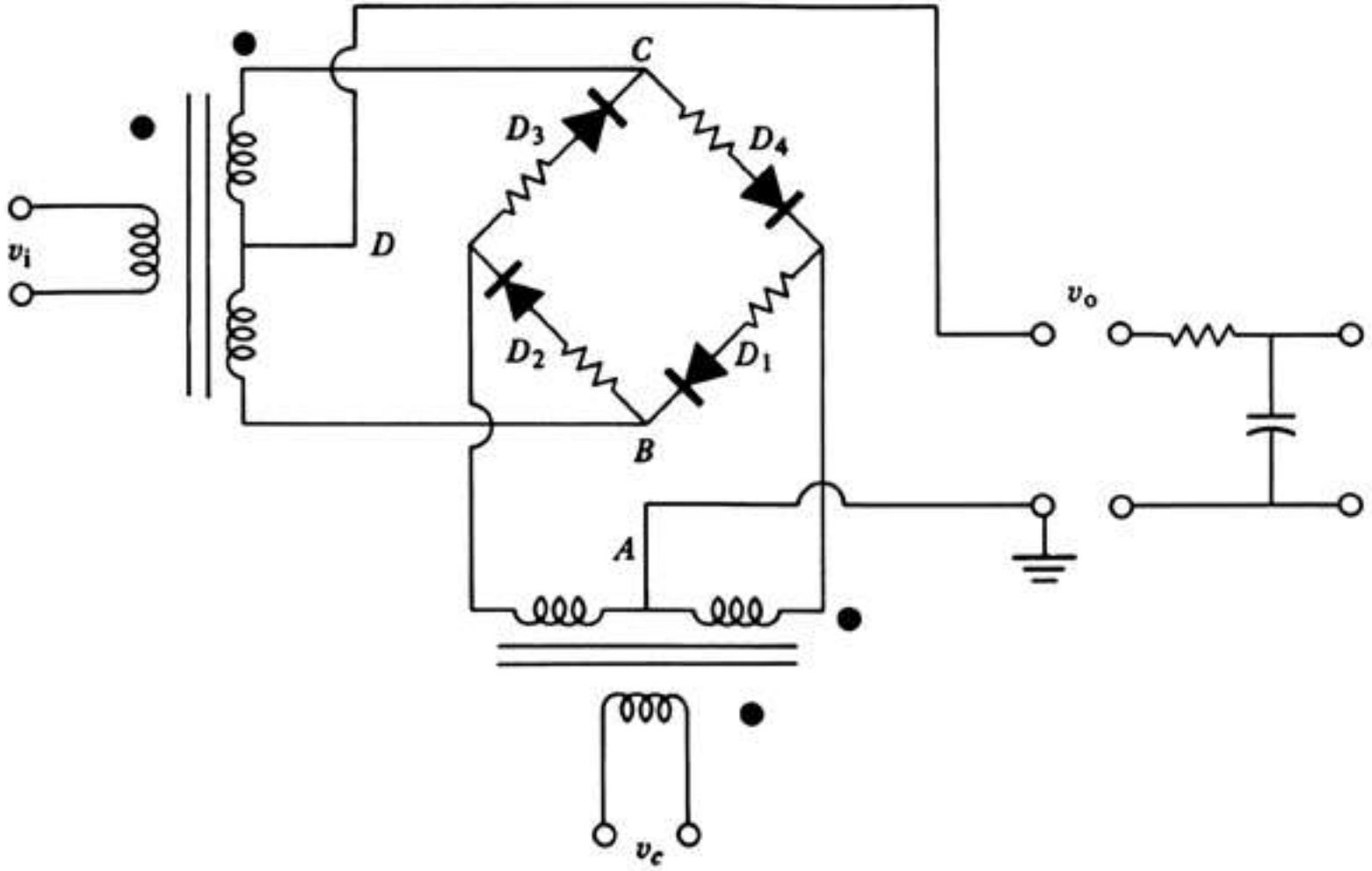


Figure 3.17 A ring demodulator This phase-sensitive detector produces a full-wave-rectified output υ_o that is positive when the input voltage υ_i is in phase with the carrier voltage υ_c and negative when υ_i is 180° out of phase with υ_c .