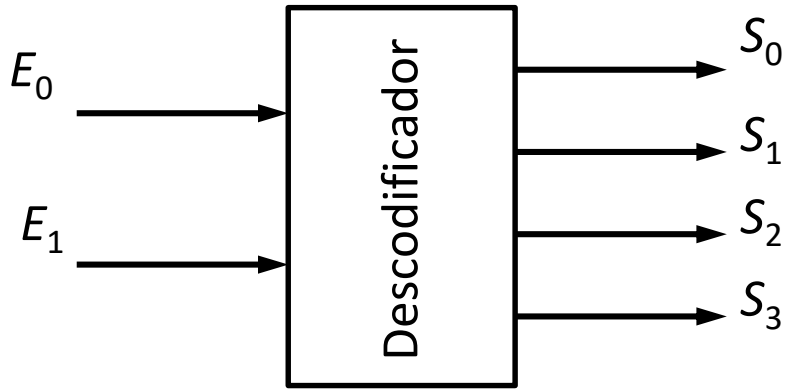
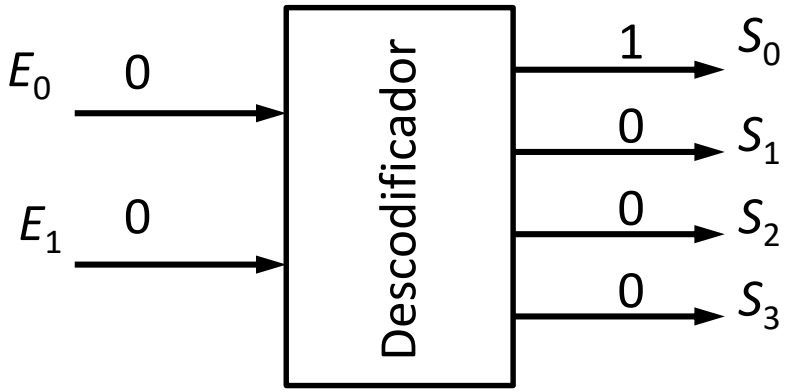
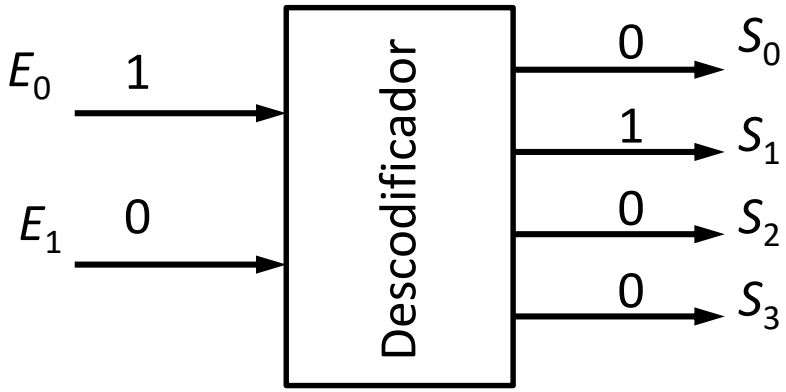
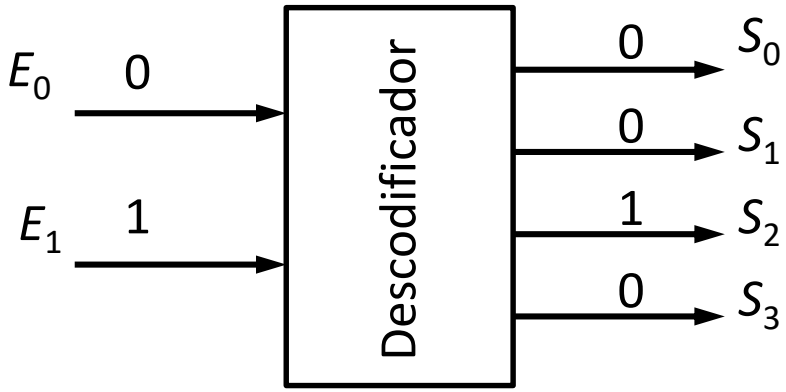
Um “descodificador” é um circuito combinacional que a partir de um uma palavra binária de *n* bits activa uma de 2^n saídas (colocando-a p. ex. a “1”). Um “descodificador de 2 para 4” (ou 2 x 4), p. ex, possui 2 entradas e 4 saídas e produz um “1” lógico na saída S_2 quando a entrada é “10” (e um “0” lógico para todas as outras combinações de entradas (ver fig. abaixo).

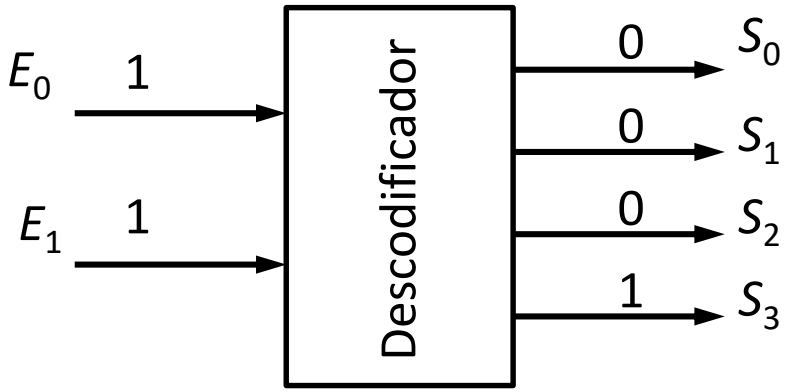


Apresente o diagrama lógico de um circuito que implemente um decodificador 2 x 4.

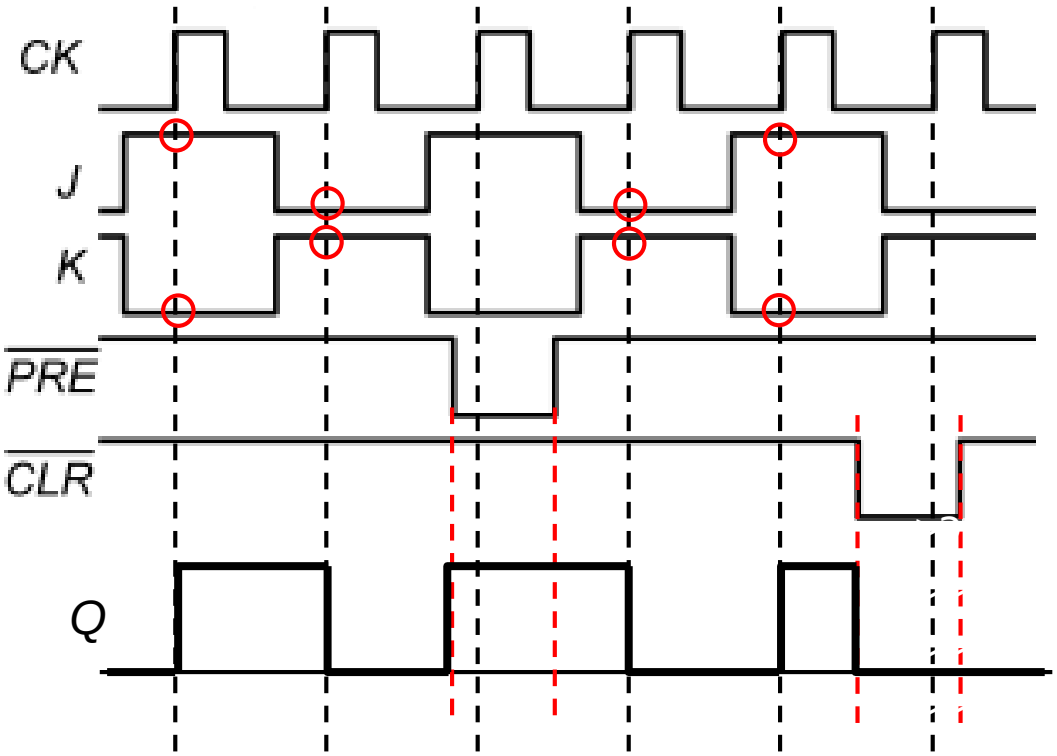

E_0
0
E_1
0
Descodificador
1
S_0
0
S_1
0
S_2
0
S_3

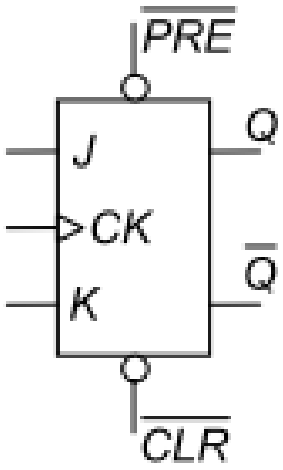

E_0
1
E_1
0
Descodificador
0
S_0
1
S_1
0
S_2
0
S_3


E_0
0
E_1
1
Descodificador
0
S_0
0
S_1
1
S_2
0
S_3


E_0
1
E_1
1
Descodificador
0
S_0
0
S_1
0
S_2
1
S_3

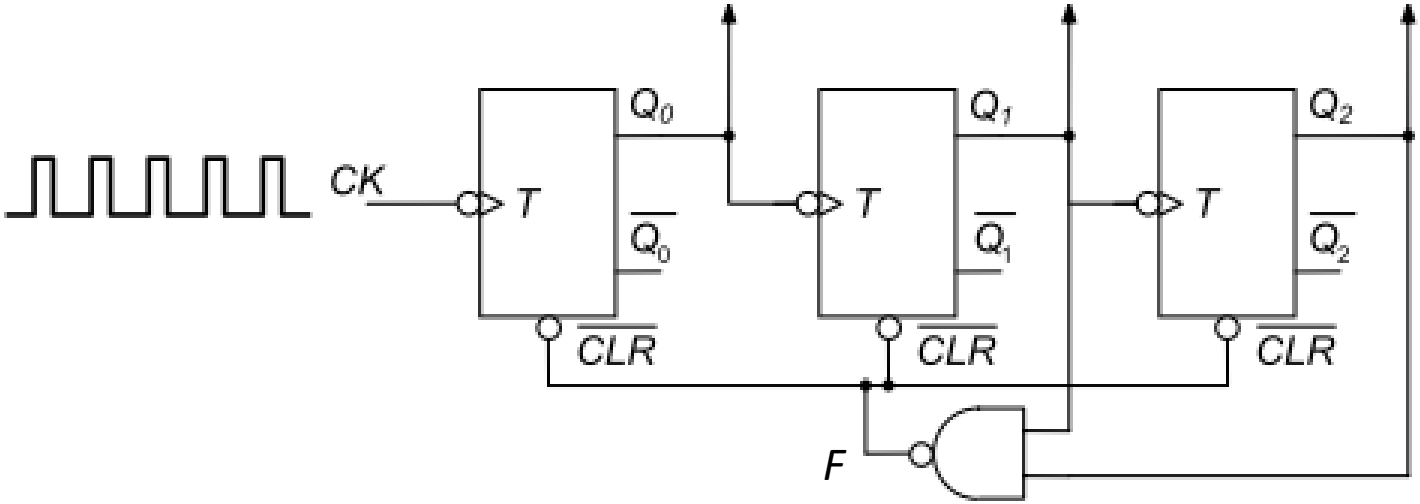
Exercício 55

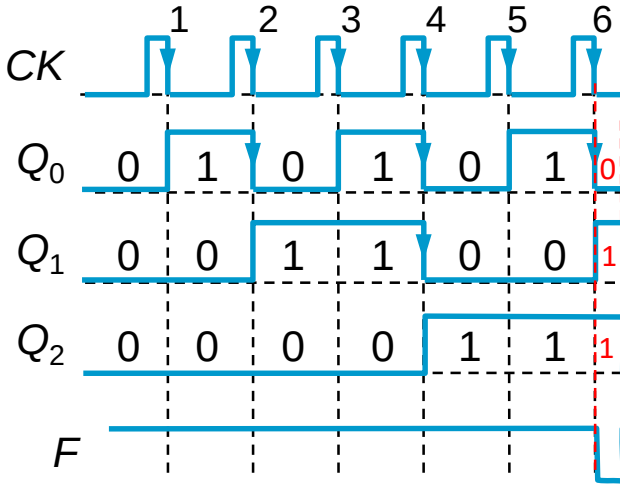




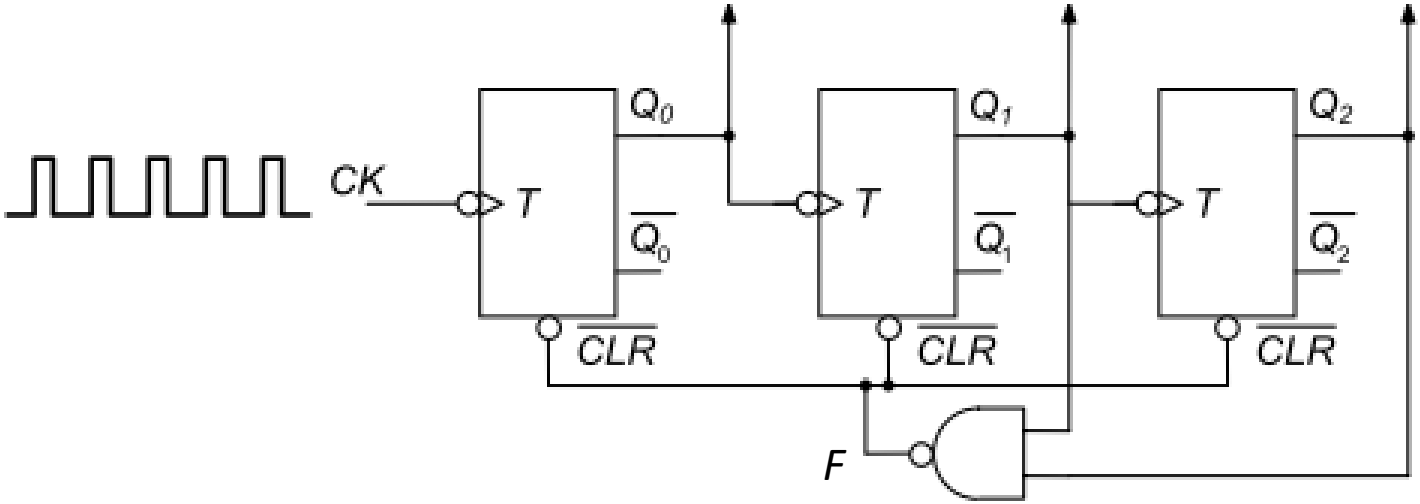
J	***K***	***Q*** após um impulso ***CK***
0	0	*Q* (mantém-se)
0	1	0 (“reset”)
1	0	1 (“set”)
1	1	$\overline{Q}$ (comuta)

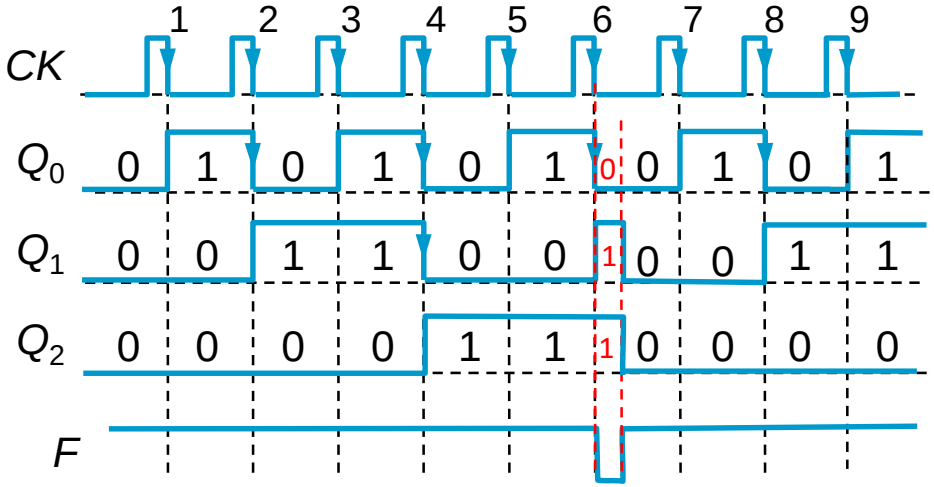
Exercício 58



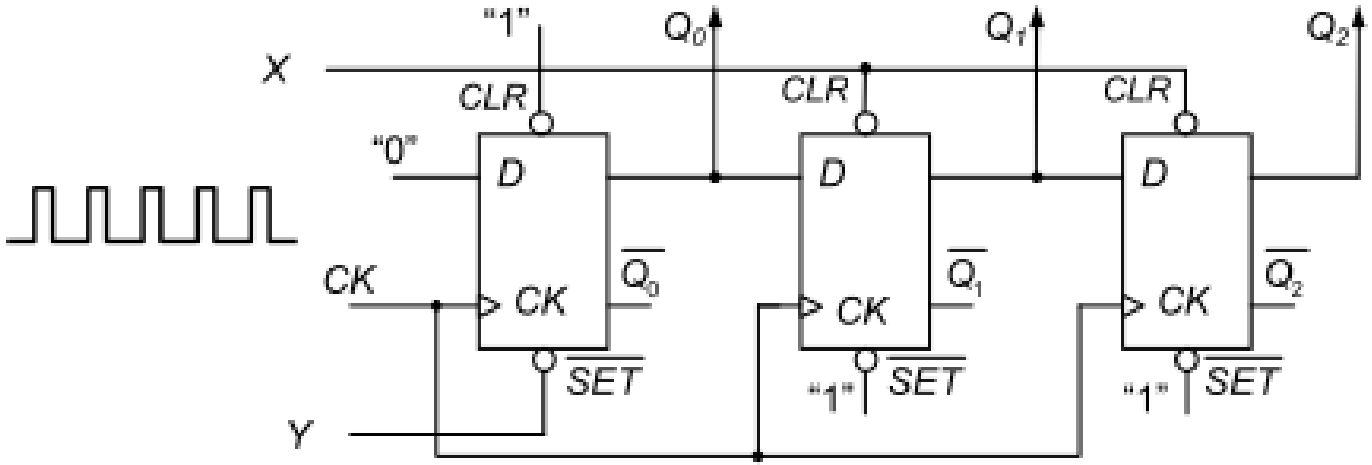


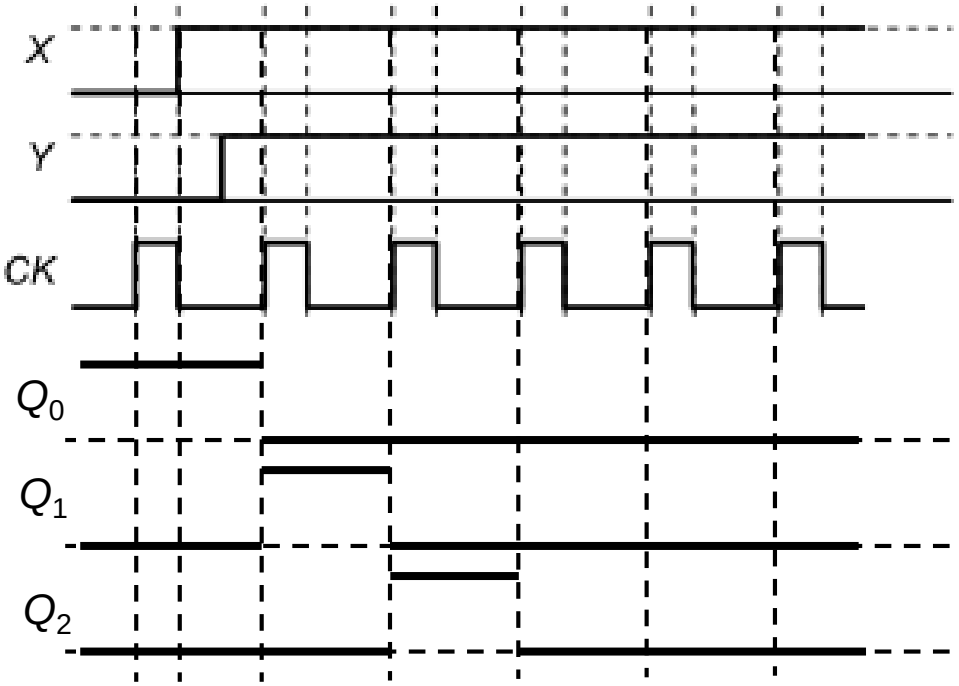
Exercício 58





→ Contador crescente de 0 a 5





→ Registo de deslocamento (*shift-register*)