Implementation of Programmable Data Plane for Media Applications

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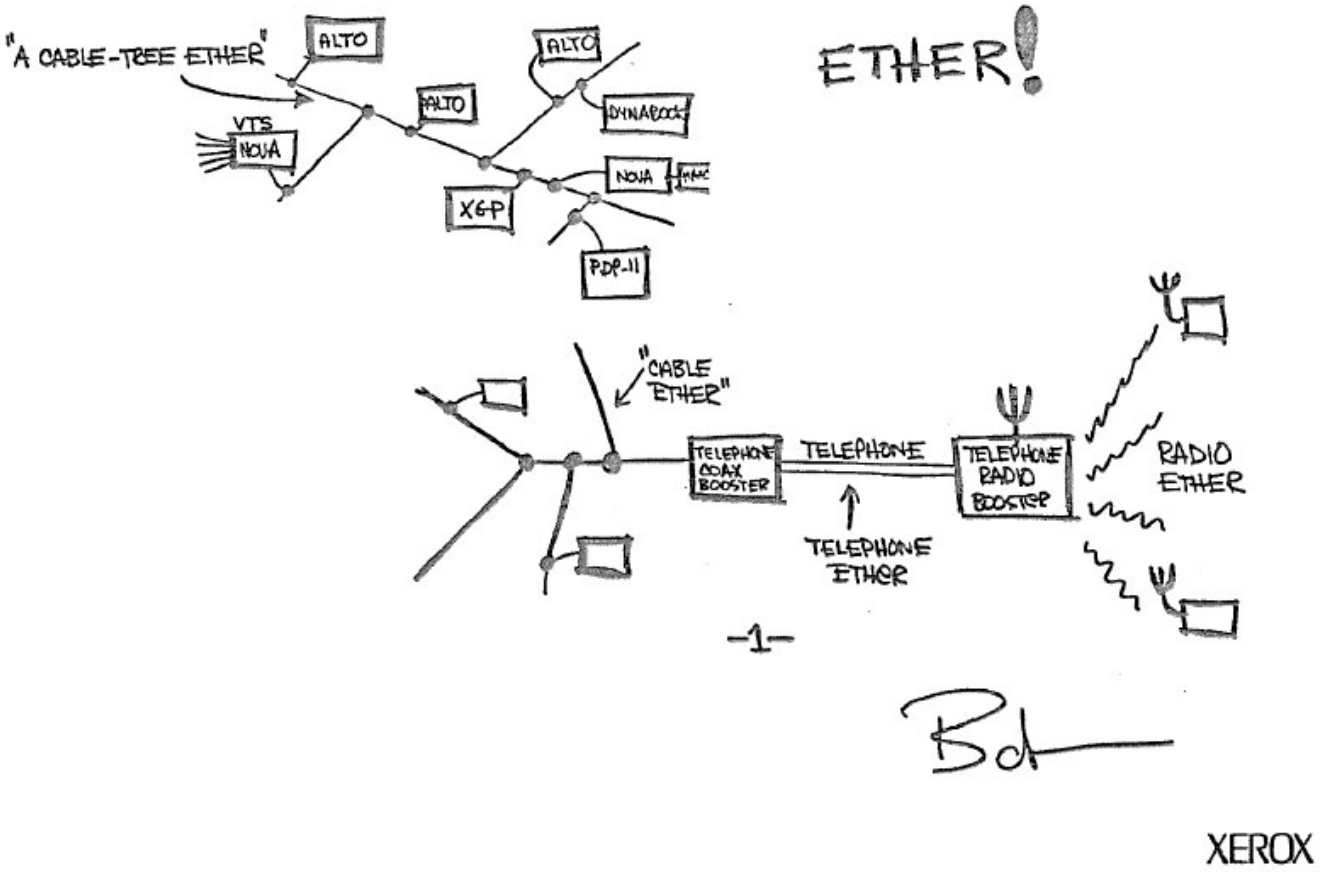
FOX Networks Engineering & Operations

Evolution of Switching: 1972



Inspired by ALOHAnet
“Alto Aloha Network”
CSMA/CD:
Carrier Sense
Collision Detect
Exponential backoff
2.94 Mbps

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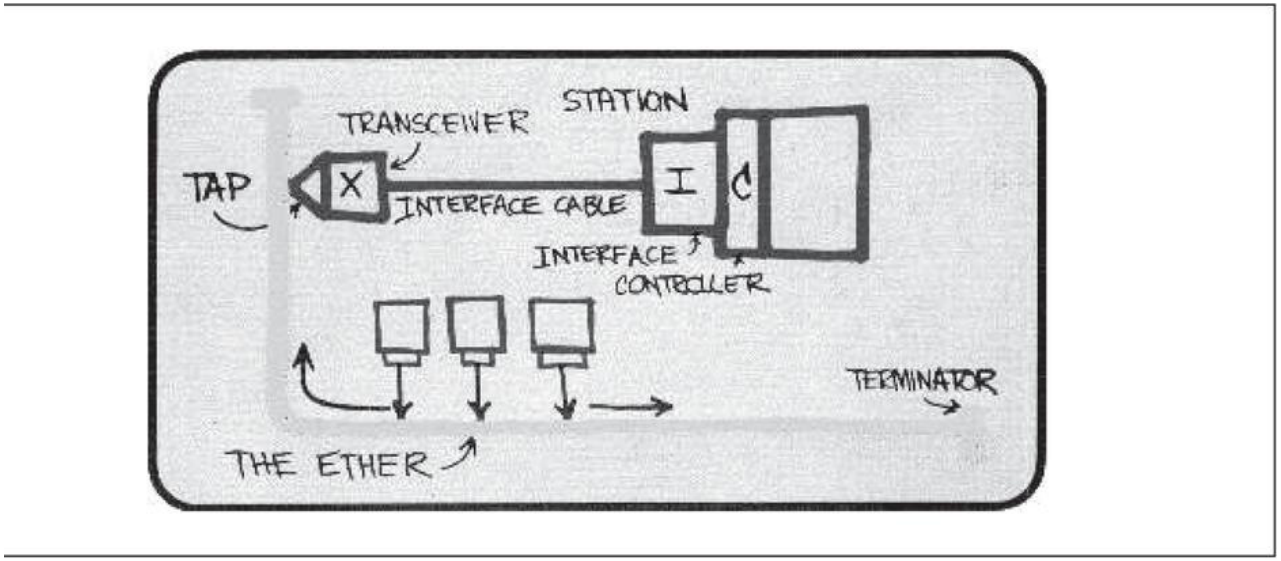
Shared Media



1980: “The Ethernet” - Digital/Intel/Xerox developed 10 Mbps standard
1984: IEEE 802.3 - 10BASE5 vampire taps on RG-8/U
Transceivers attached at n*2.5m intervals so reflections from multiple taps are not in phase

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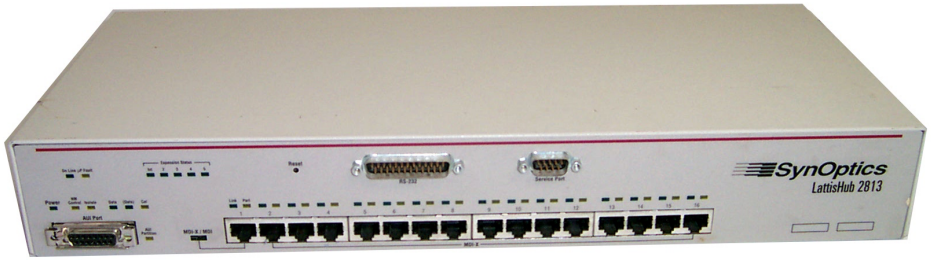
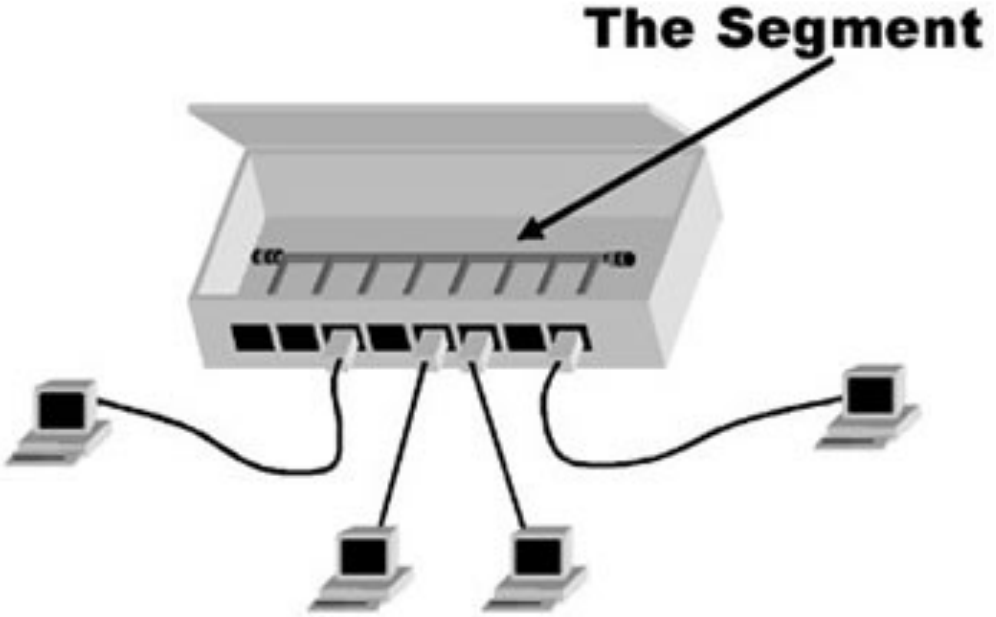
Hubs: Early 1980's

10 Mbps AUI – DEC DELNI 1983



10BASE-T – SynOptics 1985



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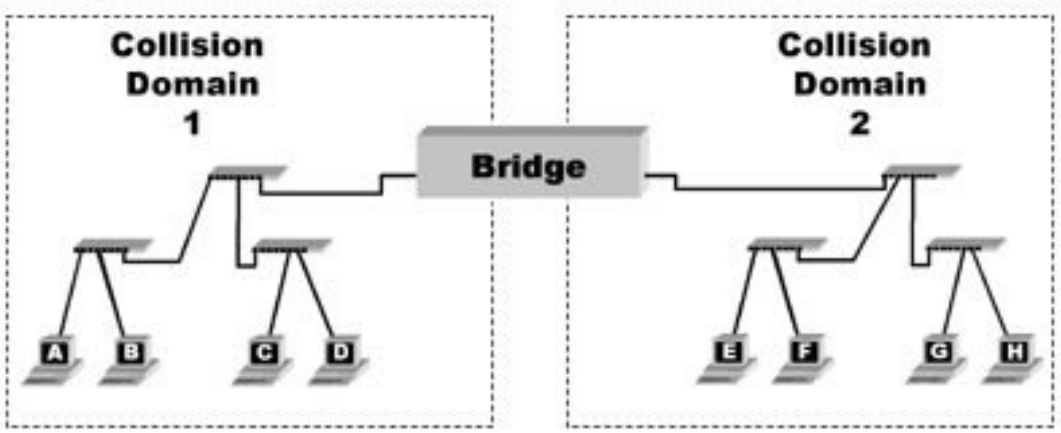
Bridges – Mid 1980's



Learn MAC addresses on different ports
Only forward frames whose MAC dst is on a segment

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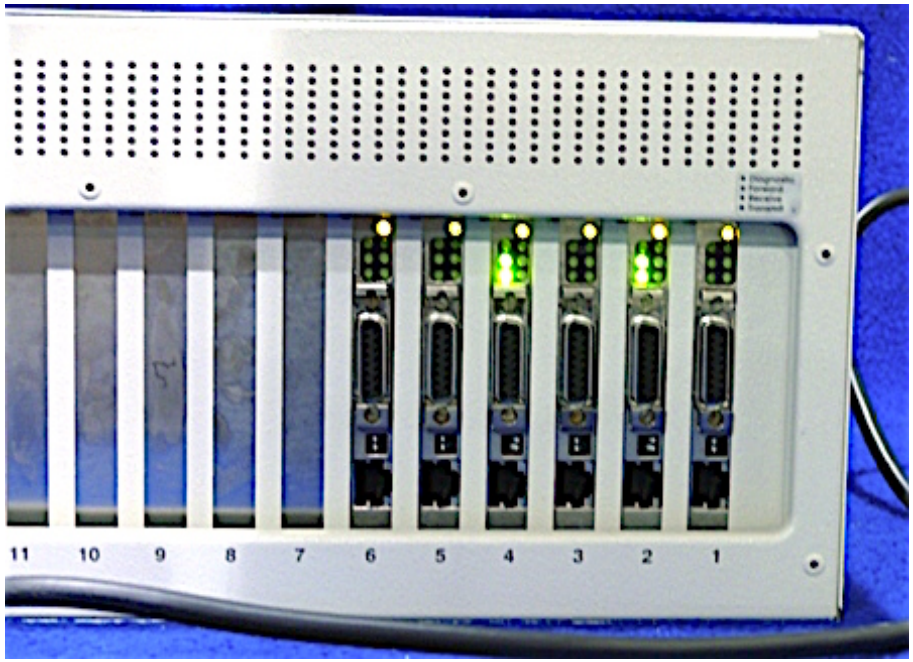
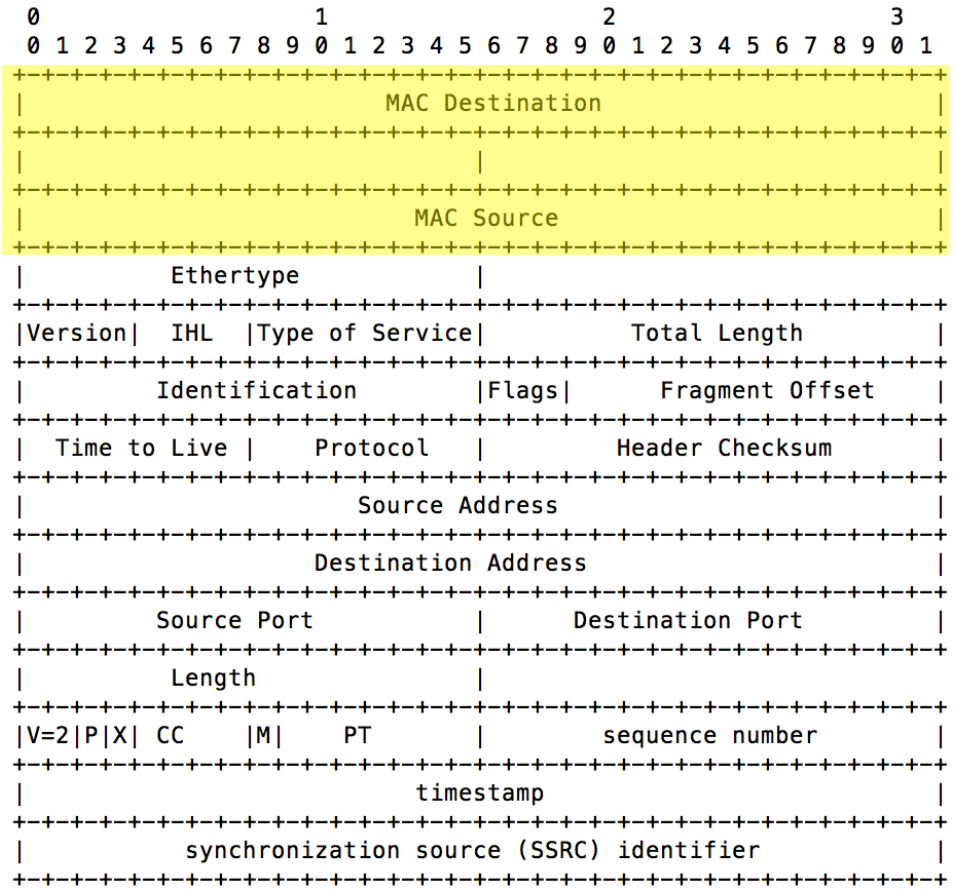
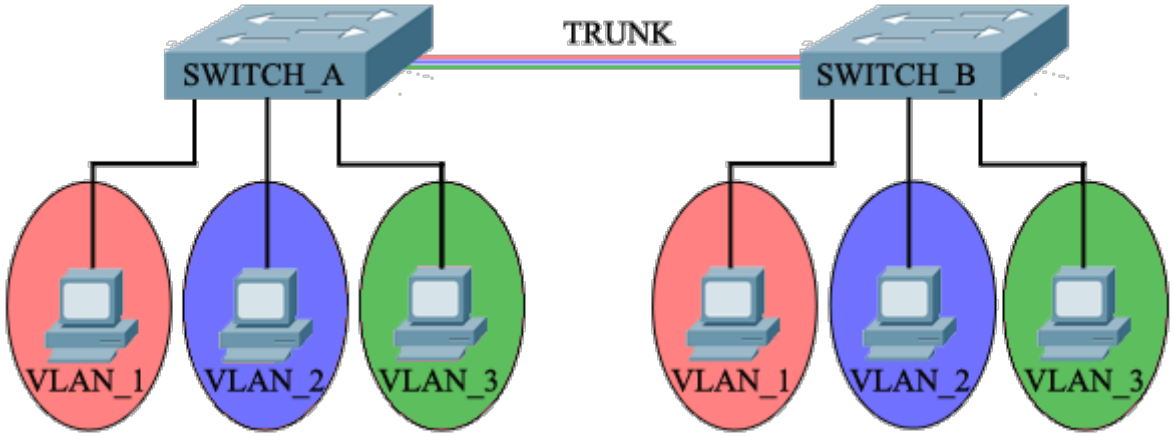
Switching: 1989

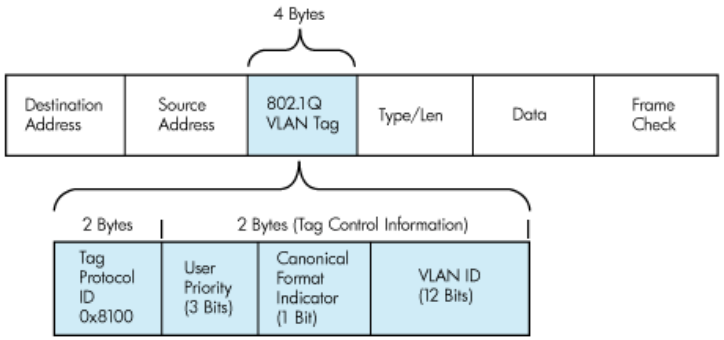


Ethernet switch from Kalpana
Layer 2 Switching based on MAC address



VLANs – Mid 1990's





Available in Cisco Catalyst switches by 1995
Standardized as 802.1Q 1999

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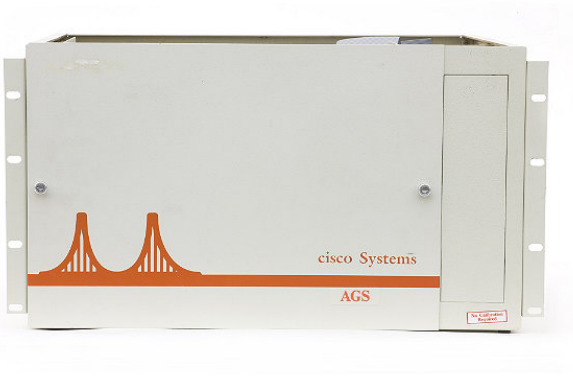
Layer 3 Routing

ARPANET IMP
1822 Protocol - 1969

Fuzzball
(DEC LSI-11)
IP Protocol - 1977



Cisco AGS
IP Protocol - 1986

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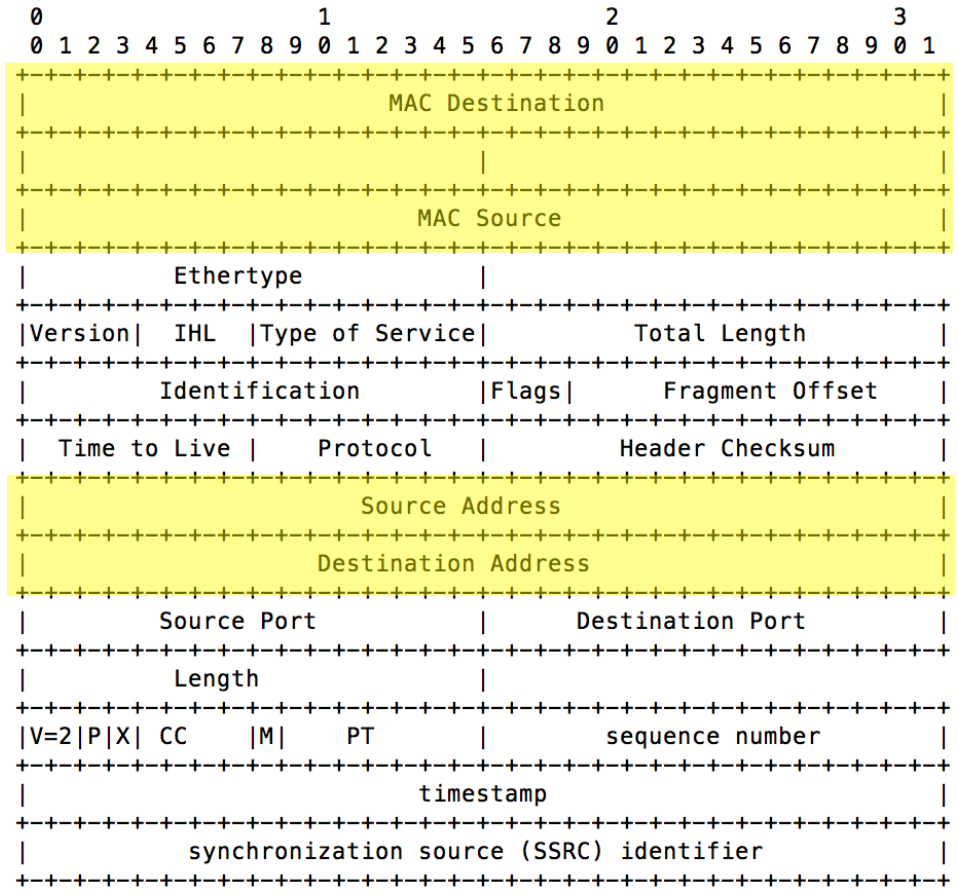
~1997: The “Layer 3 Switch”



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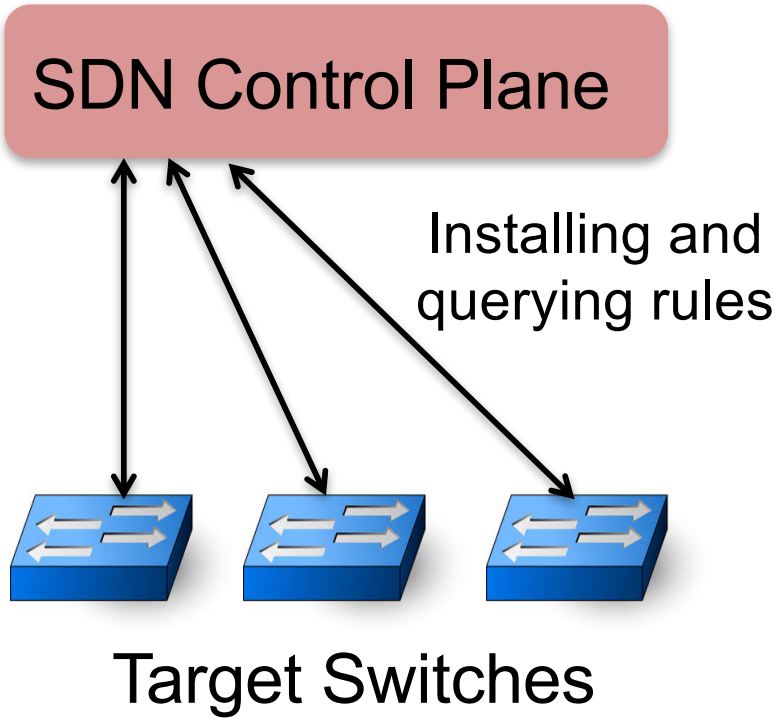
Software-Defined Networking: 2008



- SDN gives programmatic control over networks
- Control plane physically separate from the forwarding plane
- One control plane can control multiple forwarding devices
- OpenFlow is one SDN API

OpenFlow Match/Action Rule Examples

```
Match: in_port=1
Action: output port 2

Match: ip,nw_dst=10.0.0.3
Action: output port 3

Match: nw_dst=10.*.*.*,udp_dst=2000
Action: drop
```

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Proliferation of OF Header Fields

Version	Date	# Headers
OF 1.0	Dec 2009	12 (Ethernet, TCP/IPv4)
OF 1.1	Feb 2011	15 (+MPLS)
OF 1.2	Dec 2011	36 (+ARP, ICMP, IPv6)
OF 1.3	Jun 2012	40
OF 1.4	Oct 2013	41

But still not enough (e.g., VXLAN, NVGRE, STT, …)

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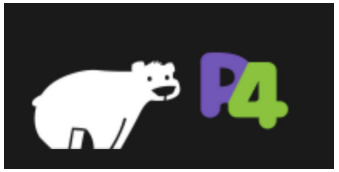
Programmable Data Plane:

P4: Programming Protocol-Independent Packet Processors **2014**



- **Programming Language**
- **Protocol independent**
- **Configurable packet parser**
- **Flexible set of typed match+action tables**
- **Target independence**
  - Program at high level without knowledge of switch details
  - Rely on compiler to configure the target switch
- **Reconfigurability**
  - Change parsing and processing in the field
- **http://p4.org**

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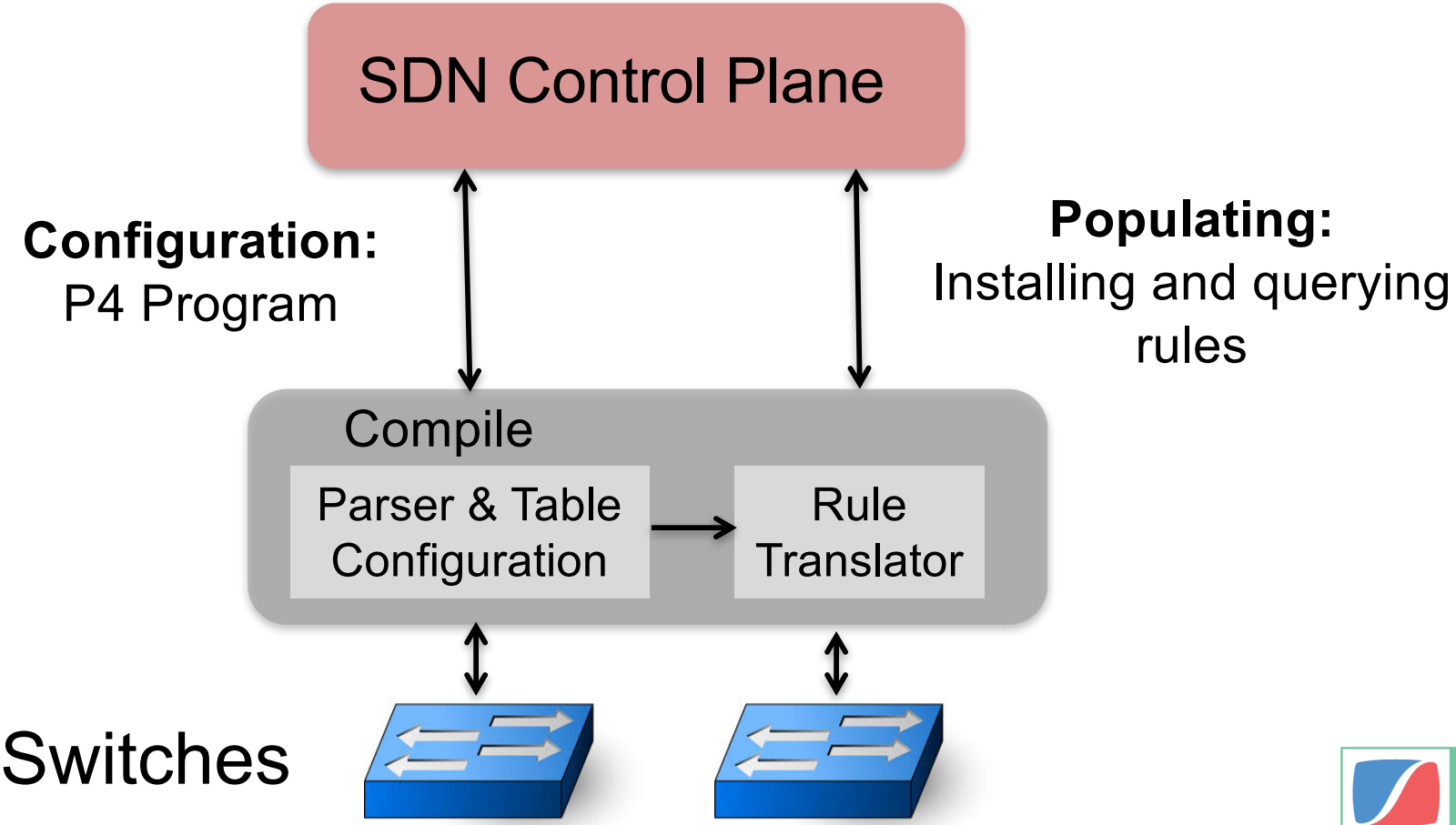
P4 Model



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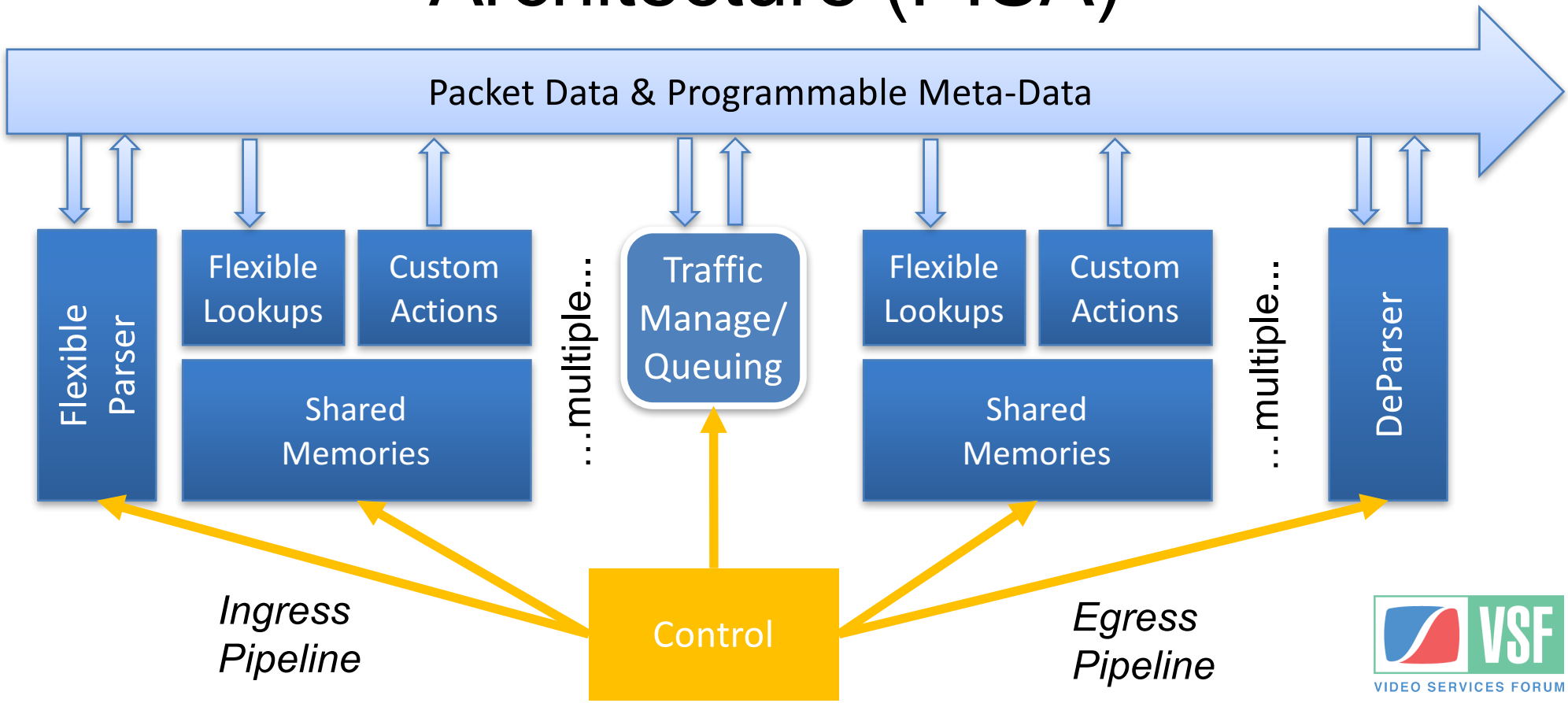
Protocol-Independent Switching Architecture (PISA)



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2022-6 versus 2110-20 timestamps

No. ▲	Time	Source	Destination	Protocol	Timestamp	seq#
1	0.000000	10.10.10.51	239.0.0.1	RTP	2013337987	39902
2	0.000007	10.10.10.51	239.0.0.1	RTP	2013338188	39903
3	0.000015	10.10.10.51	239.0.0.1	RTP	2013338389	39904
4	0.000022	10.10.10.51	239.0.0.1	RTP	2013338588	39905
5	0.000030	10.10.10.51	239.0.0.1	RTP	2013338789	39906
6	0.000037	10.10.10.51	239.0.0.1	RTP	2013338989	39907
7	0.000045	10.10.10.51	239.0.0.1	RTP	2013339190	39908
8	0.000052	10.10.10.51	239.0.0.1	RTP	2013339390	39909
9	0.000059	10.10.10.51	239.0.0.1	RTP	2013339590	39910

2022-6: The timestamp reflects the sampling instant of the first octet in the RTP datagram.

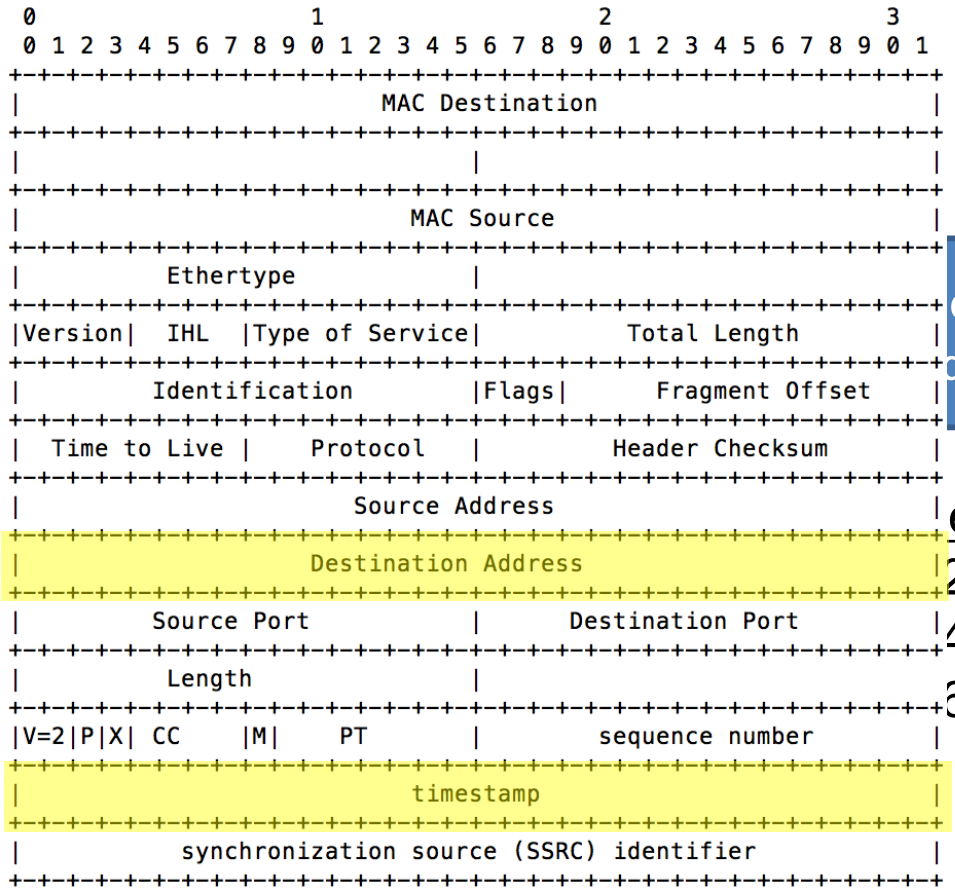
No.	Time	Source	Destination	Protocol	Timestamp ▲	seq#	Mark	Line #
203	0.001120872	10.10.10.12	239.0.0.3	RTP	88538753	21182	False	719
204	0.001125192	10.10.10.12	239.0.0.3	RTP	88538753	21183	False	719
205	0.001801823	10.10.10.12	239.0.0.3	RTP	88538753	21184	False	719
206	0.001806151	10.10.10.12	239.0.0.3	RTP	88538753	21185	True	719
207	0.001810463	10.10.10.12	239.0.0.3	RTP	88540254	21186	False	0
208	0.001814767	10.10.10.12	239.0.0.3	RTP	88540254	21187	False	0
209	0.001824071	10.10.10.12	239.0.0.3	RTP	88540254	21188	False	0
210	0.001828391	10.10.10.12	239.0.0.3	RTP	88540254	21189	False	0

2110-20 Timestamp is video alignment point of entire field or frame

Switching on RTP Timestamp

Source 1
nw_dst: 239.0.0.1

Source 2
nw_dst: 239.0.0.2



estination
dst: 239.0.0.3

e	Source
2	1
4	2
6	1

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Header Definition Examples

```
header_type ethernet_t
{
fields {
        dstAddr : 48;
        srcAddr : 48;
        etherType : 16;
        }
}
```

```
header_type udp_t
{
fields {
        srcPort : 16;
        dstPort : 16;
        hdr_length : 16;
        checksum : 16;
        }
}
```

```
header_type rtp_t
{
fields {
        version : 2;
        padding : 1;
        extension : 1;
        CSRC_count : 4;
        marker : 1;
        payload_type : 7;
        sequence_number : 16;
        timestamp : 32;
        SSRC : 32;
        }
}
```

Parser Example

```
parser ethernet {
    extract(ethernet);
    return select(ethernet.etherType) {
        0x800:   parse_ipv4;
        0x8100: parse_vlan;
        0x88F7: parse_ptp;
        0xF000: parse_my_protocol;
        default: ingess;
      }
   }
}
```

```
parser parse_ipv4 {
   extract(ipv4);
   return select(ipv4.protocol) {
      0x11 : parse_udp;
      default: ingress;
    }
}
```

```
parser parse_udp {
   extract(udp);
   return parse_rtp;
}
```

```
parser parse_rtp {
   extract(rtp);
   return ingress;
}
```

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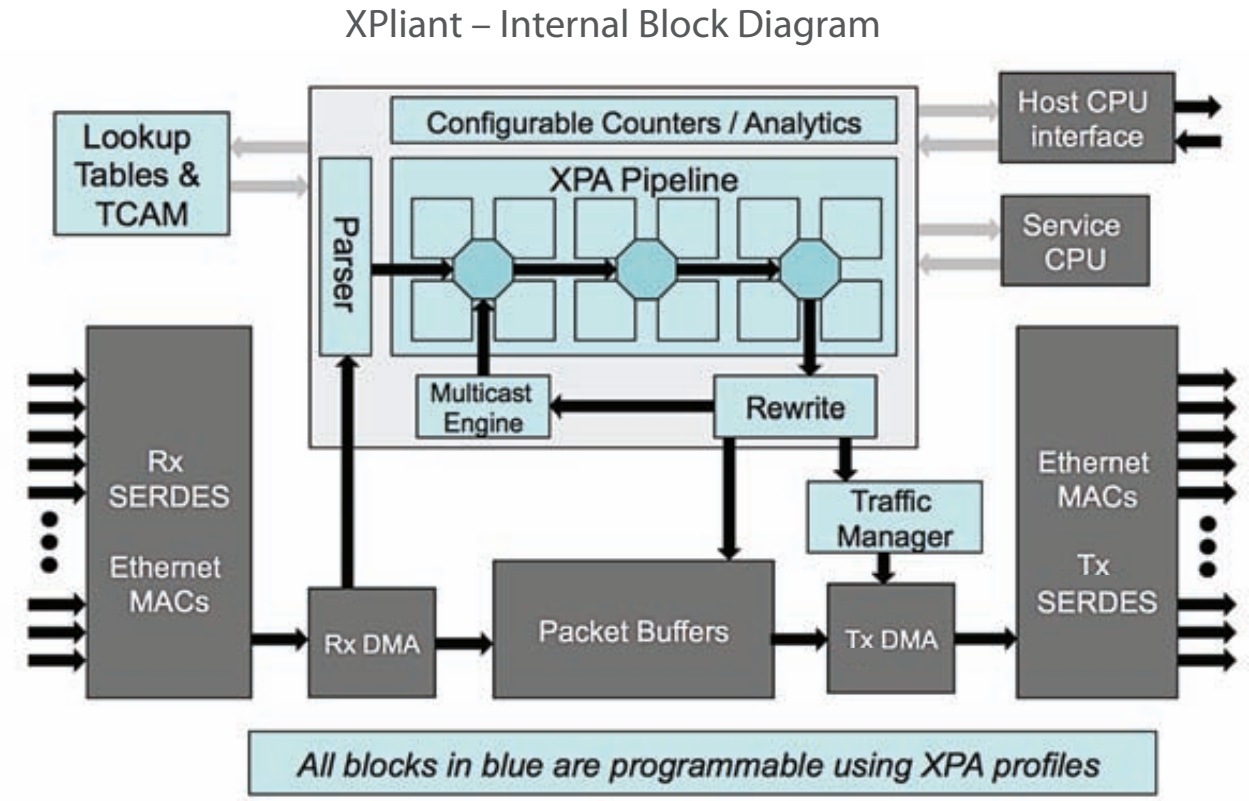
Typed Tables & Action Functions

```
table schedule_table {
reads {
        ipv4.dstAddr: exact;
        rtp.timestamp: range;
        }
actions {
          take_video;
          _drop;
          }
size : 16384;
}
```

Ipv4.dstAddr	rtp.timestamp	action	Dst_ip
239.0.0.1	0x0000->0x0002	take_video	239.0.0.3
239.0.0.2	0x0003->0x0004	take_video	239.0.0.3
239.0.0.1	0x0005->0x0006	take_video	239.0.0.3
default	default	_drop	

```
action take_video(dst_ip) {
    modify_field(standard_metadata.egress_spec,1);
    modify_field(ipv4.dstAddr,dst_ip);
}
```

XPliant CNX88091



- 3.2 Tbps switching
- Up to 128 x 25Gbps SERDES
- XPliant Packet Architecture (XPA) programmability

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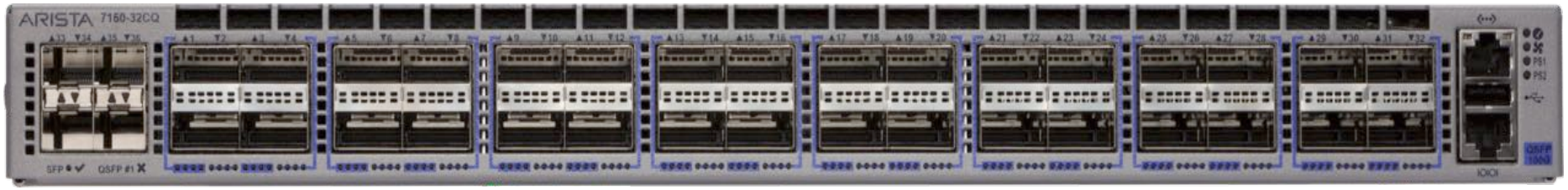
Arista 7160-32CQ



- 32 x 100G QSFP
- + 4 x 10G SFP+ / used in the demo
- 24MB Fully shared packet buffer

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XPliant Implementation

Following fields extracted from the UDP + RTP header

- **FIELD metadata :32;**
- **FIELD reserved :32; // SSRC**
- **FIELD timestamp :32;**
- **FIELD sequenceNum :16;**
- **FIELD rtpHeader :16;**
- **FIELD dstPort :16;**
- **FIELD srcPort :16;**

All fields available for lookup or possibly re-write

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Development

- Modify the Arista profile code to issue lookup in the RTP TCAM for RTP packets
- TCAM bank set aside with key defined as {DIP, RTP-TS}
- Result is {Target-DIP, pktCmd}, where pktCmd is DROP/FORWARD/TRAP
- Process lookup result to provide rewrite instructions to rewrite the DIP with New-DIP or drop as per the hit.

```
./xpRtpTcamProgramer.py --dip='239.0.0.1' --timestamp=0
        --tsmask=4294443007 --target_dip='239.0.0.3‘
./xpRtpTcamProgramer.py --dip='239.0.0.2' --timestamp=524288
        --tsmask=4294443007 --target_dip='239.0.0.3'
```

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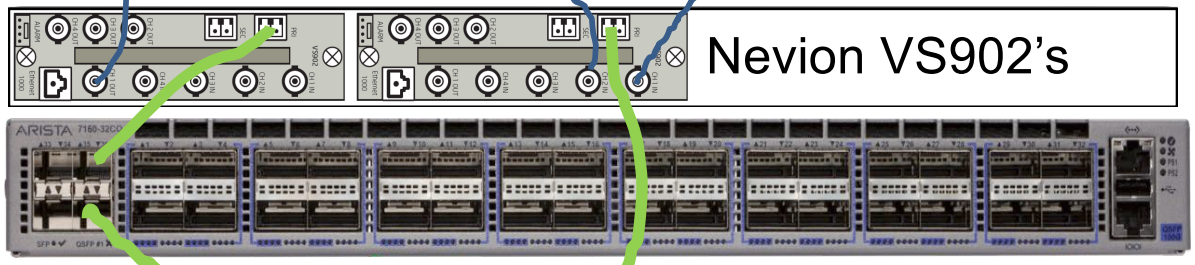
Demo Setup

HDMI Monitor



- SDI Inputs genlocked
- VS902 gateways powered up at same time for same seq# & TS

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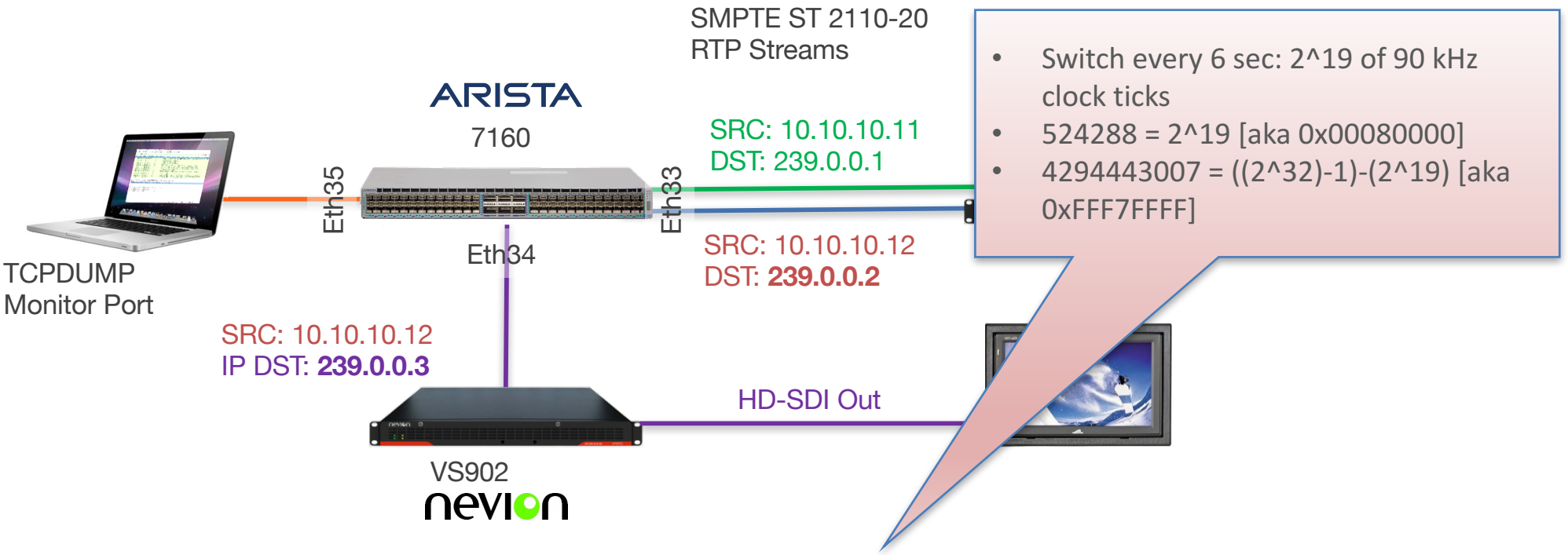
RTP Time Switching DemonstrationTest Case



./xpRtpTcamProgramer.py --dip='239.0.0.1' --timestamp=0 --tsmask=4294443007 --target_dip='239.0.0.3'
Map 239.0.0.1 to the 239.0.0.3 stream at designated RTP time
./xpRtpTcamProgramer.py --dip='239.0.0.2' --timestamp=524288 --tsmask=4294443007 --target_dip='239.0.0.3'
Map 239.0.0.2 to the 239.0.0.1 stream at designated RTP time

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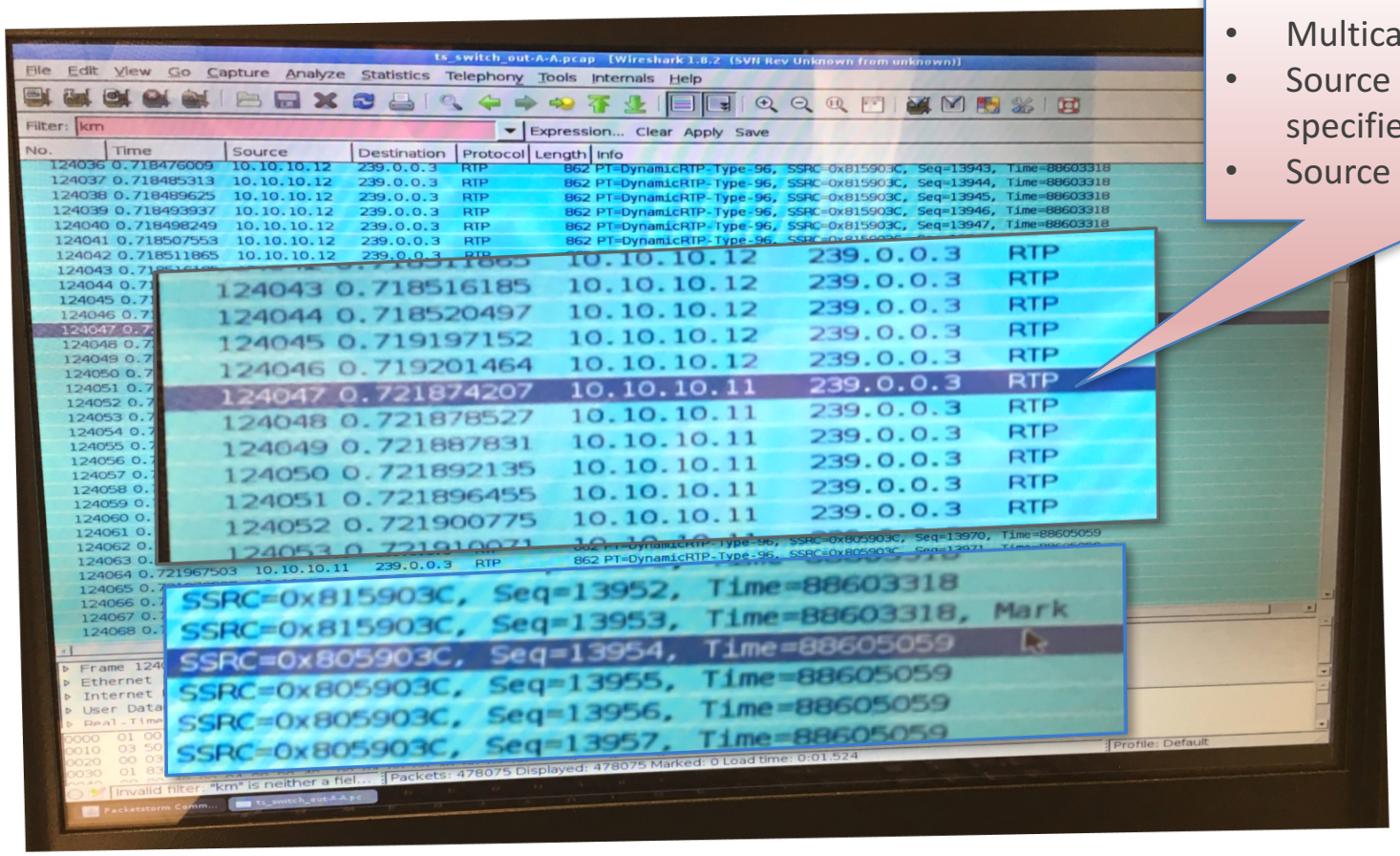
RTP Time Switching Demonstration



- Multicast DST consistent
- Source streams switched at specified RTP timestamp
- Source IP Address change

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It worked*…

* After the 2110-20 decoder was adjusted to not reset on a change of SSRC!

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Next Steps…

- **Test scale up – how many flows can be switched**
- **Port to Barefoot Tofino chip**
- **“Lower Thirds” based on 2110-20 line #?**

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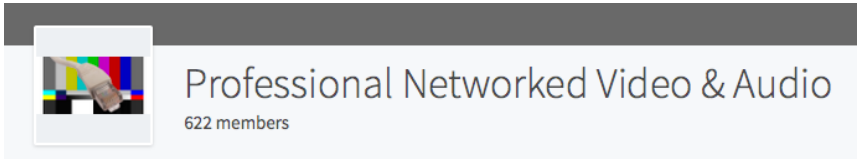
P4 examples at: https://github.com/FOXNEOAdvancedTechnology

Thanks for your Attention!

Feel free to join LinkedIn Group:



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