Design and Simulation of a CMOS-Based Memristive Crossbar Array with Analog Tanh Activation Function

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***Abstract*—This report presents the design and simulation of a CMOS-based static random-access memory (SRAM) cell, employing a six-transistor (6T) configuration for efficient data storage and retrieval. The circuit features access transistors that enable connection to the bit line during read and write operations, while a cross-coupled inverter pair maintains the stored data. Utilizing Xschem for schematic design and ngspice for simulation, we evaluate the performance of the SRAM cell through transient analysis, focusing on critical metrics such as data stability, power consumption, and operational speed. The findings demonstrate the effectiveness of the 6T SRAM cell design in contemporary memory applications.**

I. Introduction

Static random-access memory (SRAM) is a crucial component in modern digital systems, offering high-speed data access and stability compared to dynamic random-access memory (DRAM). This report discusses the design of a CMOS-based SRAM cell, specifically a 6T configuration, which is widely used in memory arrays. The design integrates access transistors and cross-coupled inverters to facilitate robust data storage and retrieval capabilities. We aim to explore the operational characteristics of the SRAM cell through detailed circuit analysis and simulation, highlighting its potential applications in various computing environments.

II. Hardware description

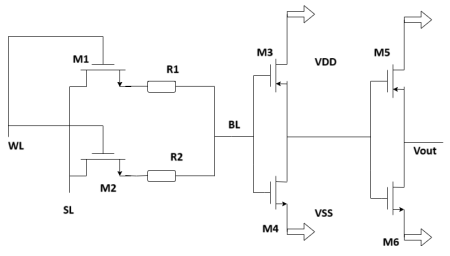

Fig. 1. Memristive Crossbar Array with Tanh Activation Function

The proposed SRAM cell consists of six transistors (M1 to M6) configured to form a stable memory unit. The access transistors (M1 and M2) connect the memory cell to the bit line (BL) when activated by the word line (WL), allowing data to be written or read. The cross-coupled inverter pair, comprising NMOS (M4, M6) and PMOS (M3, M5) transistors, creates a feedback loop that maintains the stored state, ensuring reliable data retention. Resistors (R1, R2) provide additional stability, while a supply voltage of 1.8V powers the circuit. The transient simulation setup in ngspice allows for the observation of circuit behavior over time, with parameters defined for a 10-nanosecond duration and a 100-picosecond time step.

The memristor crossbar array enables efficient parallel computation by performing matrix-vector multiplications directly within memory, minimizing data movement between the processor and memory. This architecture incorporates the ReLU activation function, a simple non-linear function that introduces essential non-linearity, aiding in the learning of complex patterns. By integrating memristor crossbar technology, researchers can achieve faster and more energy-efficient training and inference in neural networks. While the memristor crossbar handles linear operations, ReLU manages transformations, making this combination particularly advantageous for applications like image and speech recognition.

III. CONCLUSION

The simulation of the CMOS SRAM cell demonstrates its effectiveness in maintaining stable data storage and retrieval. The 6T configuration successfully leverages the advantages of CMOS technology, providing reliable performance in high-speed applications. Results from the transient analysis indicate that the SRAM cell operates efficiently under varying input conditions, affirming its suitability for integration into memory arrays. Future work may focus on optimizing the design for lower power consumption and improved scalability to meet the demands of advanced computing systems.

References

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