HP85 Disk Project v1.0 by ©Mike Gore Feb 2015

Schematics and Pin-out information for HP85 Disk Project

PIN	CPU Function	Role	CPU to component connection notes	GPIB Name	GPIB Pin
1	PB0	GPIB	**120R to 5 GPIB pin, GPIB pin 10K to VCC** 2 HC32 Parallel Poll Circuit	**EOI**	**5**
2	PB1		**120R to 6 GPIB pin, GPIB pin 10K to VCC**	**DAV**	**6**
3	PB2	PP	12 RCLK HC595 Parallel Poll Circuit Latch		
4	PB3	/CS	/CS 1 Micro SD		
5	PB4(SS SPI)	NC			
6	PB5(MOSI SPI)	SPI	1K to 3 'MOSI Micro SD 4 ISP 14 SER HC595 Parallel Poll Circuit		
7	PB6(MISO SPI)	SPI	1K to 4 'MISO Micro SD 1 ISP		
8	PB7(SCK SPI))	SPI	1K to 2 'SCK Micro SD 11 SRCLK HC595 Parallel Poll Circuit 3 ISP		
9	/RESET		1K to VCC 5 ISP Reset button		
10	VCC	5V	4 VCC 5V FT232RL 5 VCC Micro SD 2 VCC ISP 5 VCC DS1307 RTC BOARD 16 VCC HC 595 Parallel Poll Circuit 14 VCC HC 32 Parallel Poll Circuit 14 VCC HC 05 Parallel Poll Circuit 0.1uf GND 22uf GND		
11	GND	GND	6 GND FT232RL 6 GND Micro SD 6 ISP 4 GND DS1307 RTC BOARD 8 GND HC 595 7 GND HC 32 7 GND HC 05 **12,18,19,20,21,22,23,24 GPIB GND**	**GND**	**12** **18** **19** **20** **21** **22** **23** **24**
12	XTAL2		20MHZ 22pf GND		
13	XTAL1		20MHZ 22pf GND		
14	PD0 (RXD0)	RS232	3 TXD FT232RL		
15	PD1 (TXD0)	RS232	2 RXD FT232RL		
16	PD2	GPIB	**120R to 7 GPIB pin, GPIB pin 10K to VCC**	**NRFD**	**7**

17	PD3	GPIB	**120R to 8 GPIB pin, GPIB pin 10K to VCC**	**NDAC**	**8**
18	PD4	GPIB	**120R to 9 GPIB pin, GPIB pin 10K to VCC** 10 /SRCLR HC595 Parallel Poll Circuit	**IFC**	**9**
19	PD5	GPIB	**120R to 10 GPIB pin, GPIB pin 10K to VCC**	**SRQ**	**10**
20	PD6	GPIB	**120R to 11 GPIB pin, GPIB pin 10K to VCC** 3 HC32 Parallel Poll Circuit	**ATN**	**11**
21	PD7	GPIB	**120R to 17 GPIB pin, GPIB pin 10K to VCC**	**REN**	**17**
22	PC0(SCL)	**I2C**	1 SDA DS1307 RTC BOARD		
23	PC1(SDA)	**I2C**	2 SCL DS1307 RTC BOARD		
24	PC2(TCK JTAG)	NC			
25	PC3(TMS JTAG)	NC			
26	PC4(TD0 JTAG)	NC			
27	PC5(TDI JTAG)	NC			
28	PC6(TOSC1)	**NC**			
29	PC7(TOSC2)	**NC**			
30	AVCC		**VCC 10**		
31	GND		**GND 11**		
32	AREF	0.1uf	0.1uf to GND 11		
33	PA7	GPIB	**120R to 16 GPIB pin, GPIB pin 10K to VCC**	**D8**	**16**
34	PA6	GPIB	**120R to 15 GPIB pin, GPIB pin 10K to VCC**	**D7**	**15**
35	PA5	GPIB	**120R to 14 GPIB pin, GPIB pin 10K to VCC**	**D6**	**14**
36	PA4	GPIB	**120R to 13 GPIB pin, GPIB pin 10K to VCC**	**D5**	**13**
37	PA3	GPIB	**120R to 4 GPIB pin, GPIB pin 10K to VCC**	**D4**	**4**
38	PA2	GPIB	**120R to 3 GPIB pin, GPIB pin 10K to VCC**	**D3**	**3**
39	PA1	GPIB	**120R to 2 GPIB pin, GPIB pin 10K to VCC**	**D2**	**2**
40	PA0	GPIB	**120R to 1 GPIB pin, GPIB pin 10K to VCC**	**D1**	**1**

AVR ATMEGA1284P pin assignments for HP85 Disk

- **GPIB**: Each GPIB pin (8 data and 8 control lines) attach to CPU with a 120 ohm current limit resistor .
    - Each GPIB pin (8 data and 8 control lines) have a 10K pull-up resistor to VCC.
- **ISP header:** MOSI,MISO,SCK,/Reset connects directly to ISP header
- **Micro SD Interface:** MOSI,MISO,SCK attach to CPU function via a 1k series resistor.
    - **Micro SD interface has level shifters and internal 5V to 3.3V regulator**
- **RS232 TTL:** connect to FTDI232 **USB** board which also provides **5V VCC** power to all circuits..
- **I2C:** SCL,SDA connect to optional DS1307 RTC board with each line having a 2k2 pull-up

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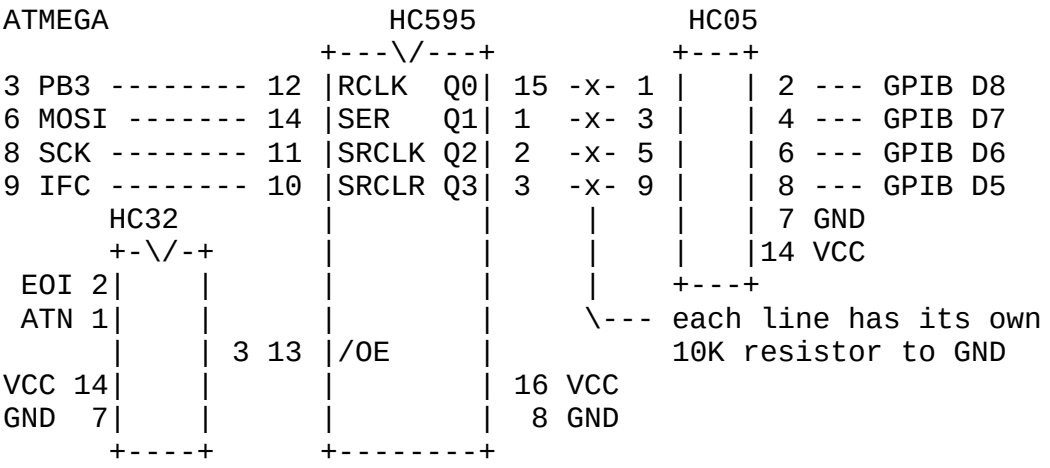
                    ATMEGA1284P (and ATMEGA644P)
                    +---\/---+
 5 EOI INT0  PB0  1|        |40  PA0      D1  1
 6 DAV INT1  PB1  2|        |39  PA1      D2  2
   PP  INT2  PB2  3|        |38  PA2      D3  3
SD /CS  PWM  PB3  4|        |37  PA3      D4  4
   NC   PWM  PB4  5|        |36  PA4      D5 13
SD     MOSI  PB5  6|        |35  PA5      D6 14
SD     MISO  PB6  7|        |34  PA6      D7 15
SD      SCK  PB7  8|        |33  PA7      D8 16
10K pullup  /RST  9|        |32  AREF     0.1uf
   +5        VCC 10|        |31  GND      GND
   GND       GND 11|        |30  AVCC     +5
20MHZ      XTAL2 12|        |29  PC7      NC
20MHZ      XTAL1 13|        |28  PC6      NC
   RX   RX0  PD0 14|        |27  PC5  TDI JTAG
   TX   TX0  PD1 15|        |26  PC4  TDO JTAG
 7 NRFD RX1  PD2 16|        |25  PC3  TMS JTAG
 8 NDAC TX1  PD3 17|        |24  PC2  TCK JTAG
 9 IFC  PWM  PD4 18|        |23  PC1  SDA I2C
10 SRQ  PWM  PD5 19|        |22  PC0  SCL I2C
11 ATN  PWM  PD6 20|        |21  PD7  PWM REN 17
                    +--------+
```

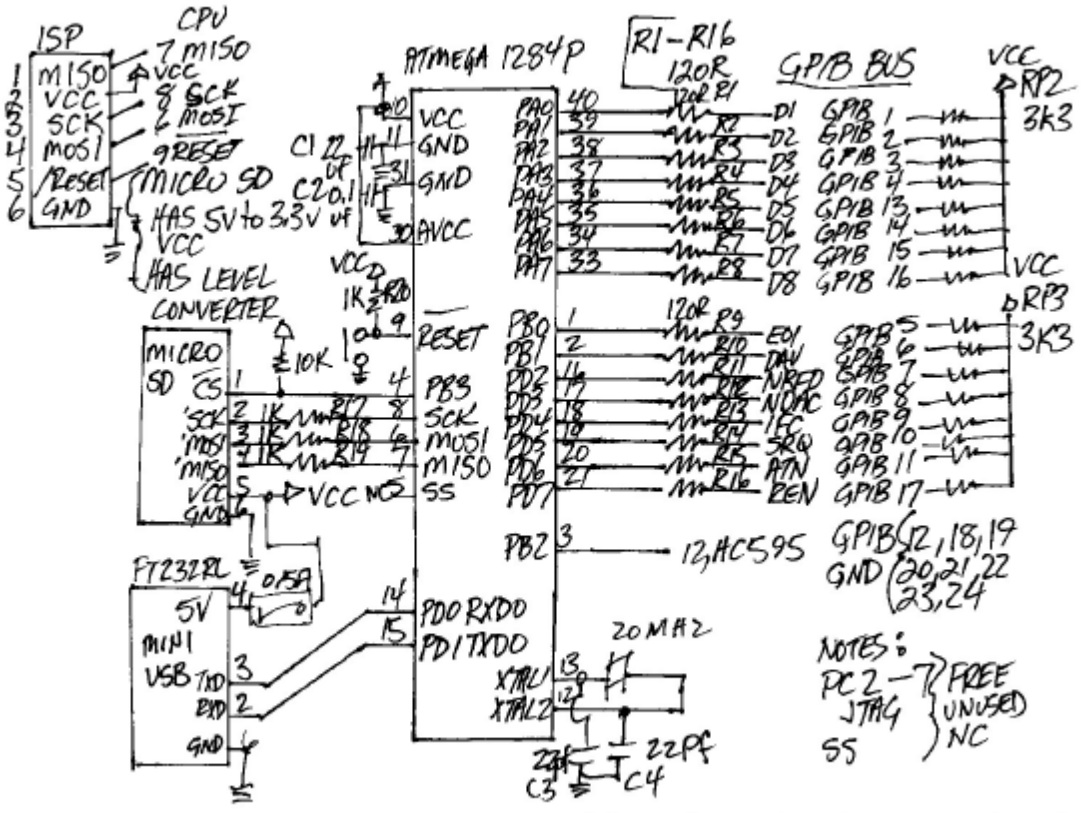
Parallel Poll Response circuit

- Uses: Three chips 74HC05, 74HC32, 74HC595
- Parallel Poll Response must be less then 2 Microseconds therefore we use hardware to do it!



Notes: When both EOI and ATN are low the HC32 enables HC595 outputs

- If any HC595 output is high the GPIB bus bit will be pulled low
- IFC low resets the outputs low



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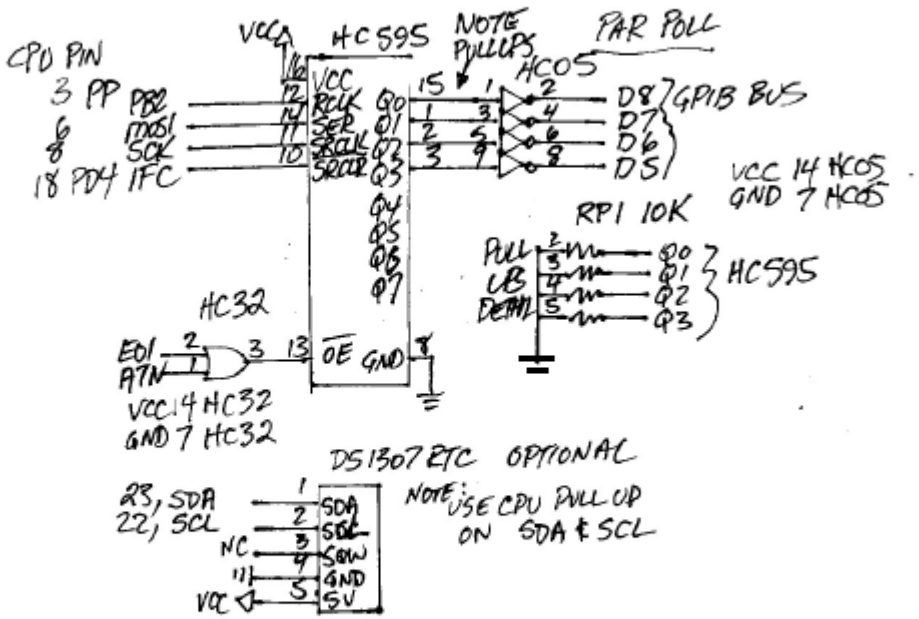

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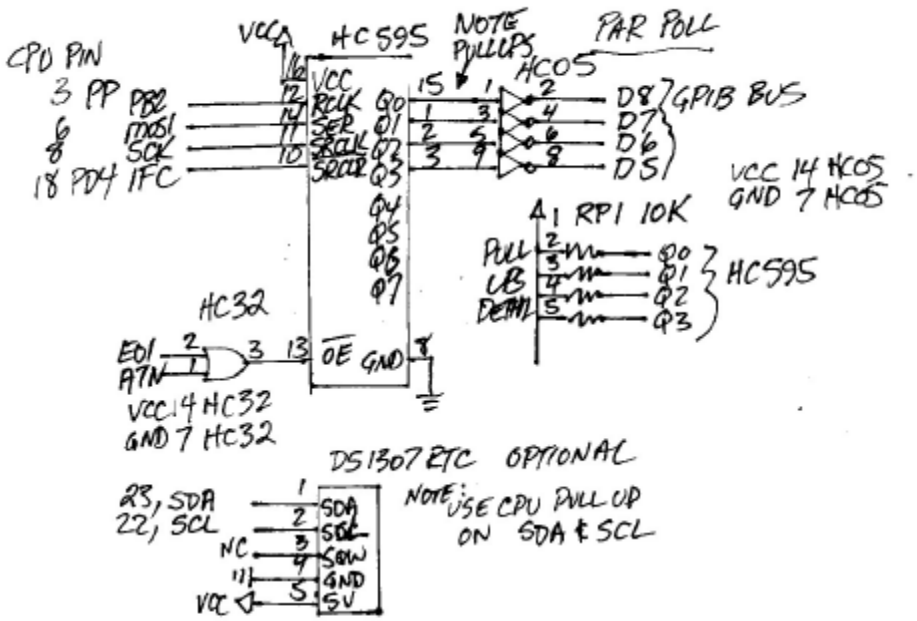

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