HEWLETT-PACKARD

HP-IB

INSTALLATION AND THEORY OF OPERATION MANUAL

HP 82937A

HP-IB Installation and Theory of Operation Manual

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Contents

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Section 1

General Information

Introduction

The 82937A Interface connects the HP-85 Personal Computer to the HP Interface Bus. The interface conforms to IEEE Standard 488-1978 and supports a wide variety of operations.

This manual provides general information about the interface, how to install it and a theory of operation section.

I/O ROMs

This interface requires one of three available ROMs to perform input-output operations. The type of ROM used determines which bus operations can be performed. The available ROMs include:

- I/O ROM (P/N 00085-15003)
- Plotter/printer ROM (P/N 00085-15002)
- Mass storage ROM (P/N 00085-15001)

The I/O ROM is a general purpose ROM and is used in a wide variety of applications. The plotter/printer ROM simplifies interfacing plotter and printer devices and the mass storage ROM was developed to interface a floppy disc.

These ROMs fit into a ROM drawer which plugs into any of the four I/O slots on the HP-85. Ensure that you have the proper ROM for your system.

Technical Specifications

Pertinent specifications of the interface are listed in this section. If complete details of HP-IB electrical, mechanical and timing requirements are desired, refer to IEEE Standard 488-1978.

Select Code Switches

The interface is preset at the factory to select code "7". Switches located on the interface circuit board allow the select code to be changed. The procedure for changing the switch settings is discussed in Section 2.

Parallel Poll Jumper

A provision which allows the interface to respond to a parallel poll is implemented with a jumper wire on the interface circuit board. The interface is delivered with the jumper wired to assign data line DIO1 as the parallel poll response line. The procedure for changing the parallel poll response line is discussed in Section 2.

Bus Signal Lines

The bus consists of 16 signal lines. These are listed in Table 1-1. A more detailed description of these lines is given in Section 3.

Table 1-1. HP-IB Signal Lines

DIO1	Data Input/Output 1
•	•
•	•
•	•
DIO8	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels

The interface and HP-IB bus use the standard +5V TTL logic level. The I/O backplane on the HP-85 uses a +6V logic level. A custom integrated circuit, called the Translator IC, has been developed to provide level shifting between these two levels. The Translator also provides buffering for information flow between the CPU in the HP-85 and the 8049 microcomputer on the interface. There are also four non-overlapping clock signals (Φ1, Φ2, Φ12, Φ21) appearing on the I/O backplane that have a +12V logic level. The interface uses two of these clock signals (Φ1 and Φ2).

The +5V TTL, +6V and +12V logic levels required for the low and high states are listed in Table 1-2.

Table 1-2. Logic Level Requirements

Signal States	HP-85 I/O Backplane Level Requirements	TTL Level Requirements	Clock Levels
Output High	≥4V	≥2.4V	≤11.0V
Output Low	≤.4V	≤.4V	≥0.4V
Input High	≥3.6V	≥2.0V	
Input Low	≤.8V	≤.8V	

Dimensions (Not including cable)	Approximately 16.7 x 12.7 x 1.5 cm (6.59 x 5 x .59 in)
Weight	0.5 kg (1.1 lb)

Line Drivers/Receivers

Each signal line connecting to the HP-IB bus has a driver and receiver circuit with the following characteristics:

Drivers		Receivers	
Type:	Open Collector		
Output Voltage Low State:	≤0.5V	Input Voltage Low State:	≤0.8V
Output Voltage High State:	≥2.5V (HP-IB Bus requires ≥2.4V)	Input Voltage High State:	≥2.0V

Cable Length

The length of the cable supplied with the interface is two metres. Also, see "Cable Length Restrictions" in Section 2.

Operating Temperature

0° to 55° C (32° to 131° F)

Power Requirements

The HP-85 mainframe supplies all power for the interface via the I/O backplane.

Data Transfer Rate

The HP-IB interface is capable of transferring data at a rate of 25k bytes per second in the Fast Handshake mode. Normal rates can be considerably slower and are determined by the program and the devices on the bus at a given time. The slowest device determines the data transfer rate.

Bus Functions

Interface functions are those elements which provide the capability for a bus device to send, receive and process messages if the device has the functional capability to do so.

Table 1-3 lists the HP-IB functions implemented by the 82937A interface. A complete description of these interface functions can be found in IEEE Standard 488-1978. Some of the terms used in the table are defined below.

Handshake	A technique used by devices to synchronize data byte transfers.
Source	An originator of data or commands.
Acceptor	A receiver of data or commands.
Listener	A device with Listen capability becomes Listener Active when it receives its Listen Address from the Controller Active device. As such, it is prepared to receive data bytes sourced by the Talker Active device.
Talker	A device with Talker capability becomes Talker Active when it receives its Talk Address from the Controller Active device. As such, it is prepared to source data bytes to one or more Listener Active devices. There can never be more than one device as a Talker at a given time.
System Controller	At power on, one (and only one) device on the HP-IB bus assumes the roll of System Controller. The HP-85 can be configured to be the System Controller by a switch on the interface circuit board. The System Controller resets the bus at power on and becomes Controller Active. Also, the System Controller may reset the bus and become Controller Active at any time, even if control has been passed to another bus device.
Controller Active	The Controller Active device configures the bus for the exchange of data by sourcing commands that designate one talker and one or more listeners. It can also send commands to cause specific actions to occur within a device, such as trigger, clear, etc. The Controller Active device can pass control to any other bus device capable of receiving control.
Serial Poll	The Controller Active device may serially poll another device to obtain it's status byte. This is usually done in user's software in response to a request for service. A device's status byte denotes the device's present status and whether or not it requested service.
Parallel Poll	The user can program the Controller Active device to conduct a parallel poll to obtain a status bit from devices on the HP-IB bus that are properly configured.

Table 1-3. Interface Functions and Allowed Capability

Mnemonic	Function/Allowed Capability
SH1	Source Handshake, complete capability. Provides the interface with the capability to send message bytes.
AH1	Acceptor Handshake, complete capability. Provides the interface with the capability to guarantee the proper reception of message bytes.
T6	Talker. Provides the interface with the capability to send device dependent data over the HP-IB bus to other devices. T6 implements: Basic Talker Serial Poll Unaddress if my listen address (MLA)
L4	Listener. Provides the interface with the capability to receive device dependent data from the HP-IB bus from other devices. L4 implements: Basic Listener Unaddress if my talk address (MTA)
SR1	Service Request, complete capability. Permits the interface to asynchronously request service from the Controller Active device.
RL1	Remote/Local, complete capability. Provides the interface with the capability to allow the HP-85 to select between either keyboard control (local) or program control (remote) if provided for in the user's program. The use of the RL function is totally program dependent.
PP2	Parallel Poll. Implemented by a jumper wire on the interface circuit board. Permits the interface to return a 1-bit status to the controller in response to a parallel poll.
DC1	Device Clear, complete capability. Gives the user access to the Device Clear state; use is program dependent.
DT1	Device Trigger, complete capability. Gives the user access to the Device Trigger state; use is program dependent.
C1,2,3,4,5	Controller. This implements: C1 – System Controller C2 – Send Interface Clear (IFC) and Take Charge C3 – Send Remote Enable (REN) C4 – Respond to Service Request (SRQ) C5 – Send Interface Message, Receive Control, Pass Control, Pass Control to Self, Parallel Poll, Take Control Synchronously

HP-IB Messages

The interface and I/O ROM determine how the preceding functions are implemented for passing messages over the bus. Following is a complete list of single line and multi-line messages. The manner in which some of these messages are responded to is device dependent and/or user defined. The controller is the primary source of messages that causes some specified action to take place on another bus device. Some of these messages are also discussed in more detail in Section 3.

Programming techniques for implementing these messages are not discussed in this manual. Refer to the I/O ROM manual for programming techniques.

Table 1-4. HP-IB Messages

Mnemonic	Message Name	Response
		Single Line Messages
ATN	Attention	The Controller Active places ATN true to source commands on the bus or in conjunction with EOI, to do a parallel poll. When ATN is false, data may be sent over the bus by a designated talker.
IFC	Interface Clear (Abort)	The System Controller uses this to place talkers and listeners in an unaddressed state. If control has been passed, the System Controller again becomes Controller Active when it sends IFC.
REN	Remote Enable	Removes all devices from Local Lockout mode and causes all devices to revert to manual control.
SRQ	Service Request	Indicates a device's need for interaction with the controller.
EOI	End or Identify	Terminates a flow of data, and can be used with ATN to do a parallel poll.
		Single Line Handshake Messages
DAV	Data Valid	Allows source to validate DIO lines.
NRFD	Not Ready For Data	Used to inform the source that all devices are ready for data.
NDAC	Not Data Accepted	Used by devices to inform the source that data has been accepted.

Table 1-4. HP-IB Messages

Mnemonic	Message Name	Response
		Multi-Line Messages
GTL	Go To Local	Causes selected devices to switch to local (front or rear panel) control.
LAG	Listen Address Group	A group of 31 listen addresses, one of which corresponds to the listen address of the interface.
UNL	Unlisten	Device becomes unaddressed to listen.
TAG	Talk Address Group	A group of 31 talk addresses.
UNT	Untalk	Causes a talker to become unaddressed to talk.
LLO	Local Lockout	Prevents local (front or rear panel) control of device functions.
DCL	Device Clear	Causes all devices to be initialized to a predefined or power-up state.
SDC	Selected Device Clear	Causes a device to be initialized to a predefined or power-up state.
SPD	Serial Poll Disable	Devices exit serial poll mode and are not allowed to send their status byte.
SPE	Serial Poll Enable	Devices enter serial poll mode and are allowed to send their status byte when addressed to talk.
GET	Group Execute Trigger	Signals one or more devices to simultaneously initiate a set of device dependent actions.
TCT	Take Control	Passes bus controller responsibilities from the current controller to a device which can assume the bus supervisory roll.
SCG	Secondary Command Group	A group of 32 commands which are only recognized if they immediately follow a talk or listen address.
DAB	Data Byte	Transfers device dependent information between a talker and one or more listeners. This may be programming information or data.

Note: Pressing the Reset key will reset the interface and return keyboard control to the operator. If the HP-85 is System Controller, pressing the Reset key will output the IFC message and set REN true.

Section 2
Installation

Unpacking and Inspection

If the shipping carton is damaged, ask the carrier's agent to be present when the interface is unpacked. If the interface is damaged or fails to meet electrical specifications, immediately notify the carrier and the nearest HP sales and service office. Retain the shipping carton for the carrier's inspection. The sales and service office will arrange for the repair or replacement of your interface without waiting for the claim against the carrier to be settled.

Installation

The select code switches, talk/listen address switches, system controller switch and the parallel poll jumper are preset at the factory as follows:

- Select Code 7
- Talk/Listen Address 21
- System Controller Enabled
- Parallel Poll Wired from E1 to E2 (DIO1)

Verifying or changing any of the above requires disassembly of the interface housing. If this is necessary, use the following disassembly procedure and disassemble the interface. Then refer to the discussion of the function requiring change.

If it isn't necessary to change or verify the factory settings, refer directly to "Installing the Interface and Connecting Peripherals" on page 20.

Disassembly

Refer to Figure 2-1 to see how the interface parts fit together. Place the interface on a flat surface with the side having the six screws facing upward and the cable coming out to the left. Then use the following steps to disassemble the interface.

1. Using a Pozidriv screwdriver, remove the six screws and set them aside.
2. Hold the interface parts together and turn the interface over so that the six screw holes are facing downward and the cable is still coming out to the left.
3. Hold the cable strain relief in place and remove the top half of the interface housing.

If you have followed the above steps, switch S1 should be oriented as shown in the following figures. If it isn't, orient it as illustrated before identifying the switch segments.

When you re-assemble the interface, reverse the above procedure, making sure the ground clip is in place. The ground clip should be under the circuit board when the component side is up.

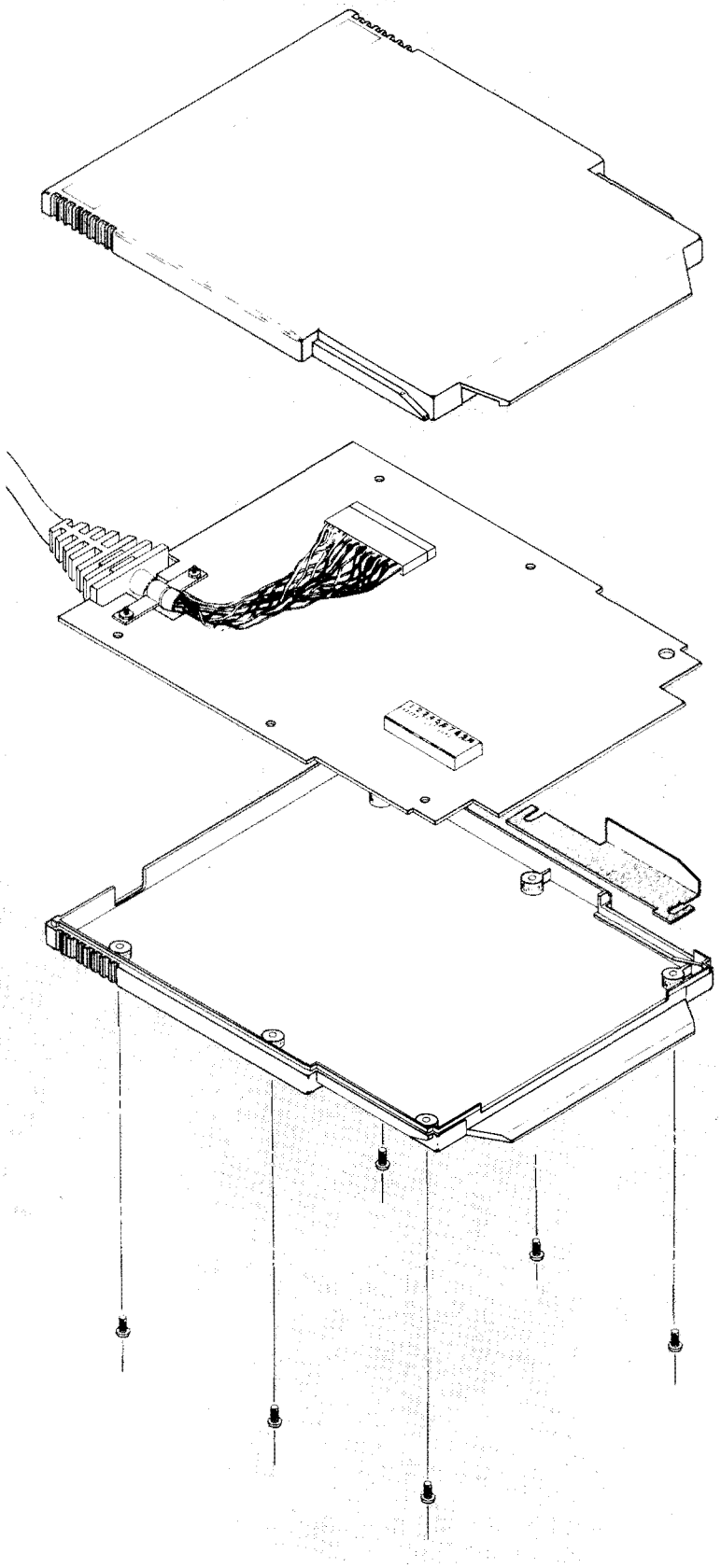


Figure 2-1. Disassembly

Switch Settings

As previously noted, the select code, talk/listen address and system controller functions are preset at the factory. Switch segments 2 through 10 of switch S1 on the interface circuit board are used for this purpose. Switch segment 1 is not used and may be in either position.

Once the interface is disassembled, any of the factory settings may be verified or changed by referring to the following discussions of the individual functions.

The interface may be equipped with either slide or rocker type switches. Both types are illustrated in the factory preset positions.

CAUTION

If you change any of the factory settings, make sure that you change the proper switch segments. Do not disturb the settings of adjoining switches. The small tip of a pencil or similar object is recommended for this purpose.

Select Code Switches

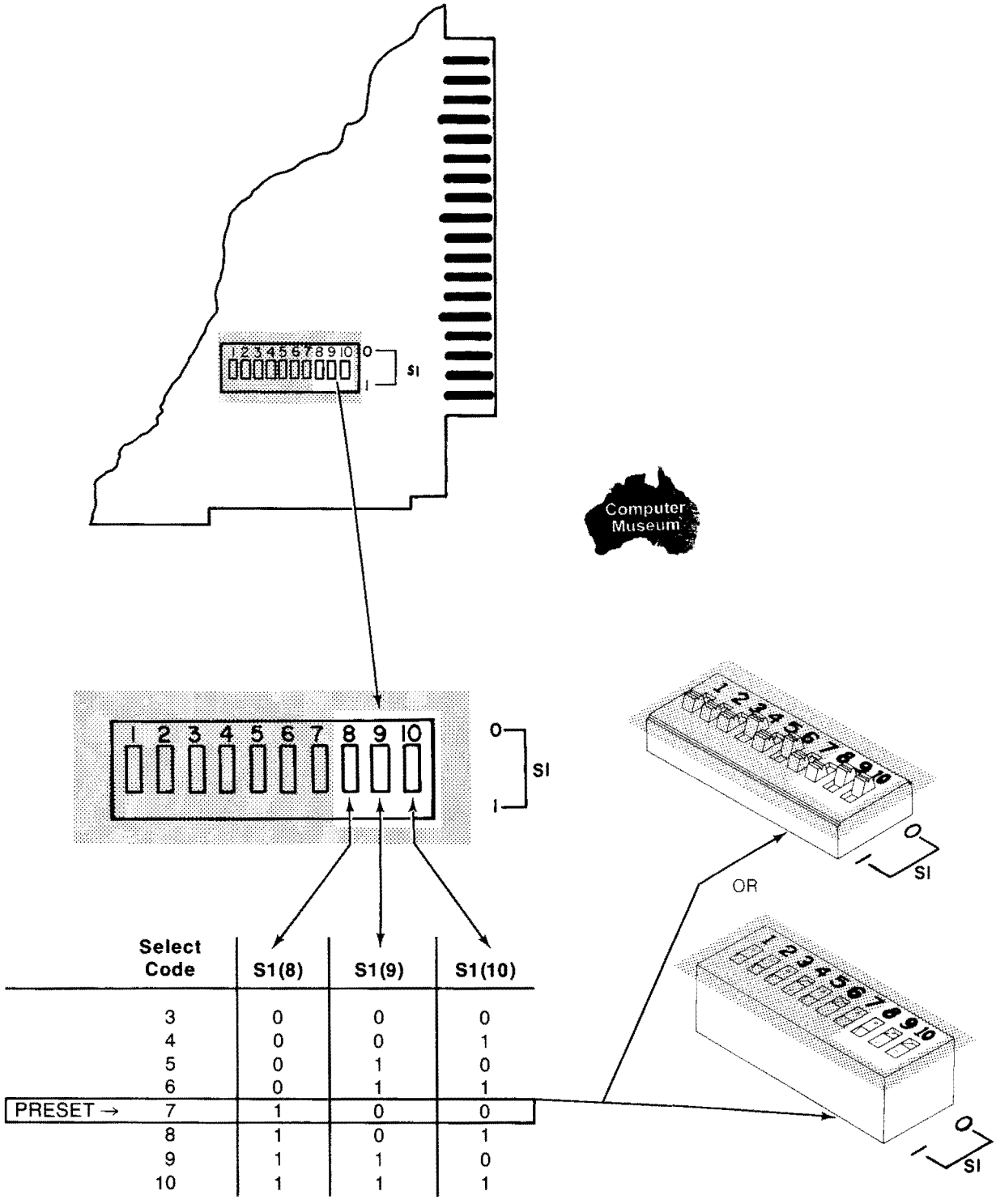
Switch segments 8, 9 and 10 of switch S1 are preset at the factory for select code "7" as follows:

- Switch segment 8 set to "1"
- Switch segment 9 set to "0"
- Switch segment 10 set to "0"

The "0" and "1" positions are labeled on the circuit board.

Select codes 3 through 10 may be set with these three switch segments. To change or verify the factory setting, orient the circuit board as shown in Figure 2-2 and locate switch segments 8, 9 and 10. **Next identify the "0" and "1" switch positions on the circuit board.** You may verify that select code "7" is properly set by comparing the actual positions of switch segments 8, 9 and 10 with those illustrated. They should be the same.

To change the select code, refer to the table and set switch segments 8, 9 and 10 as required for the select code chosen. For example, if select code "3" is to be set, the three switch segments must all be set to "0". In this case, if the switches are the slide type, slides 8, 9 and 10 must all be set to the "0" position; if they are the rocker type, all three rockers must be pressed down toward the "0" position.



Select Code	S1(8)	S1(9)	S1(10)
3	0	0	0
4	0	0	1
5	0	1	0
6	0	1	1
PRESET → 7	1	0	0
8	1	0	1
9	1	1	0
10	1	1	1

Figure 2-2. Select Code Switches

Note: Select codes 1 and 2 are the CRT and printer select codes, respectively.

Talk/Listen Address Switches

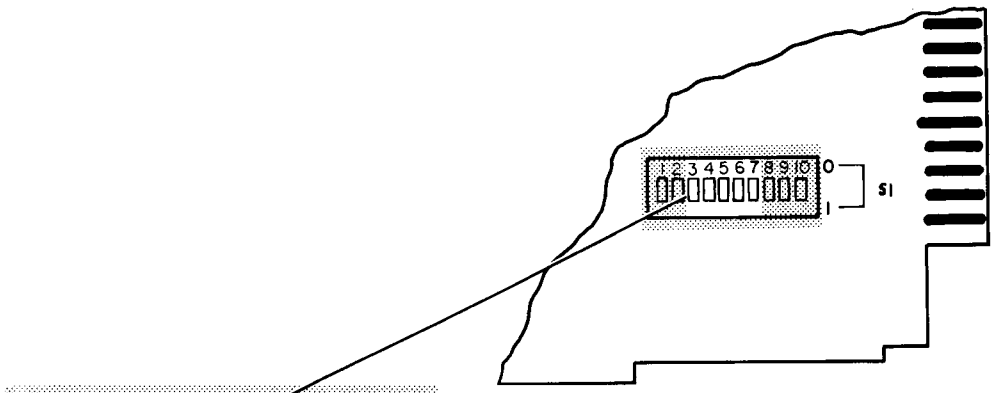
Switch segments 3 through 7 of switch S1 are preset at the factory for talk/listen address "21" as follows:

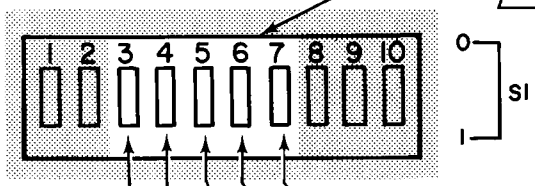
- Switch segment 3 set to "1"
- Switch segment 4 set to "0"
- Switch segment 5 set to "1"
- Switch segment 6 set to "0"
- Switch segment 7 set to "1"

The "0" and "1" positions are labeled on the circuit board.

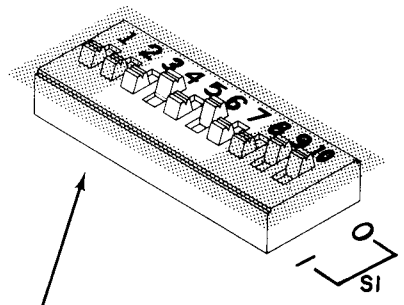
Any talk/listen address from 0 through 30 may be set with these five switch segments. To change or verify the factory setting, orient the circuit board as shown in Figure 2-3 and locate switch segments 3 through 7. **Next identify the "0" and "1" switch positions on the circuit board.** You may verify that talk/listen address "21" is properly set by comparing the actual positions of switch segments 3 through 7 with those illustrated. They should be the same.

To change the factory setting, refer to the table and set switch segments 3 through 7 as required for the talk/listen address chosen. For example, if talk/listen address "30" is chosen, switch segments 3, 4, 5 and 6 must be set to "1" and switch segment 7 set to "0". In this case, if the interface is equipped with slide switches, move the slides for segments 3, 4, 5 and 6 to the "1" position and the slide for segment 7 to the "0" position. If they are rocker switches, press the rockers down toward the "1" position for segments 3, 4, 5 and 6 and down toward the "0" position for segment 7.





Address	S1(3)	S1(4)	S1(5)	S1(6)	S1(7)
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	0	0	0	0
17	1	0	0	0	1
18	1	0	0	1	0
19	1	0	0	1	1
20	1	0	1	0	0
PRESET → 21	1	0	1	0	1
22	1	0	1	1	0
23	1	0	1	1	1
24	1	1	0	0	0
25	1	1	0	0	1
26	1	1	0	1	0
27	1	1	0	1	1
28	1	1	1	0	0
29	1	1	1	0	1
30	1	1	1	1	0



OR

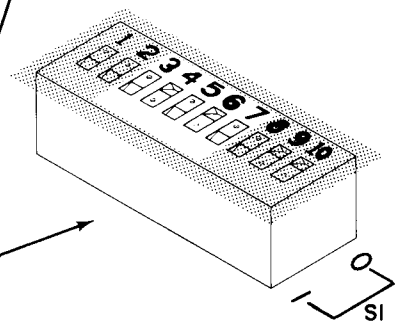


Figure 2-3. Talk/Listen Address Switches

System Controller Switch

Switch segment 2 of switch S1 is preset to "1" at the factory to enable the host HP-85 as system controller. One (and only one) HP-IB bus device can assume system controllers status.

If the host HP-85 is to be the **system controller,** leave switch segment 2 in the factory preset position. To verify the factory setting, orient the circuit board as shown in Figure 2-4 and locate switch segment 2. **Next identify the "0" and "1" switch positions on the circuit board.** Switch segment 2 should be in the "1" position as illustrated.

If the host HP-85 is not to be the system controller, set switch segment 2 to the "0" position. In this case, if the interface is equipped with slide switches, move slide segment 2 to the "0" position. If they are rocker switches, press rocker segment 2 down toward the "0" position.

It is important that one, and only one, bus device be assigned as system controller. Failure to comply with this will result in improper bus operation.

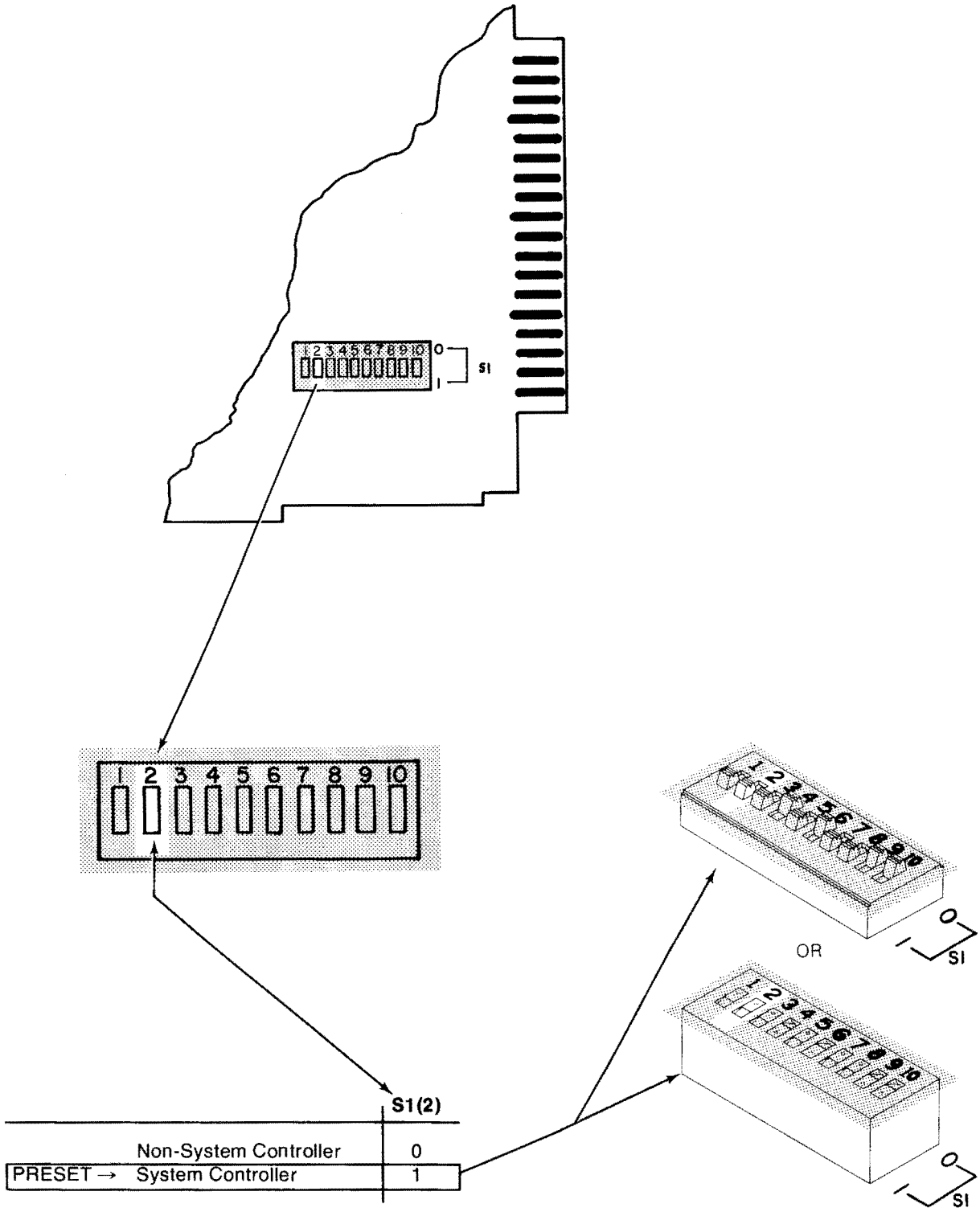


Figure 2-4. System Controller Switch

A jumper wire on the interface circuit board allows the interface to respond to a parallel poll by configuring the interface to one of the DIO lines. The interface is delivered with the jumper installed to assign DIO1 as the parallel poll response line.

The jumper is not necessary when the host HP-85 is the controller directing parallel polls to other HP-IB bus devices. It is necessary when the host HP-85 is being interrogated by another controller for a parallel poll response. In this case, the interface responds to the poll by pulling the DIO line it is configured to if it is requesting service.

The jumper is located underneath the cable wires. If it is necessary to change the DIO response line, first refer to Figure 2-5 and remove the cable connector. Remove the cable connector by prying it away from the circuit board connector as shown; do not pull on the cable wires to remove the connector. To change the parallel poll response line, refer to Table 2-1, locate the DIO line you want to configure and identify the two holes the jumper must be configured between. Then unsolder and remove the jumper wire using a soldering iron with a 25 watt or less rating. Next refer to Figure 2-6 and identify the two holes that you want to configure the jumper to. The odd-numbered holes are labeled on the component side of the circuit board; the even-numbered holes are labeled on the circuit side. Use the jumper you removed and solder in place between the two appropriate holes using rosin core solder. When you are finished, check both sides of the circuit board to ensure there are no bridges between the circuit board traces and re-connect the cable connector.

Table 2-1. Parallel Poll Jumper Placement

	DIO Line	Place Jumper From	To
PRESET →	DIO1	E1	E2
	DIO2	E3	E4
	DIO3	E5	E6
	DIO4	E7	E8
	DIO5	E9	E10
	DIO6	E11	E12
	DIO7	E13	E14
	DIO8	E15	E16

After all the switches are set and the parallel poll jumper is installed to meet your needs, re-assemble the interface before attempting to connect it to the HP-85.

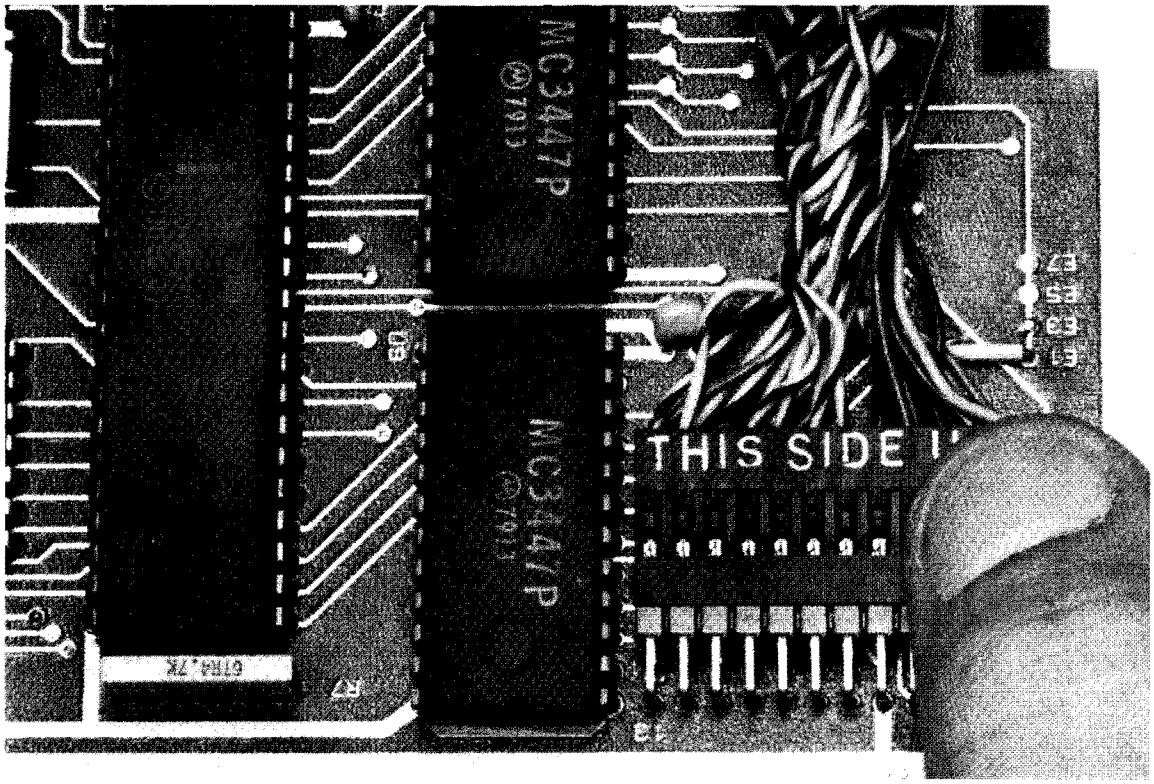


Figure 2-5. Removing Cable Connector

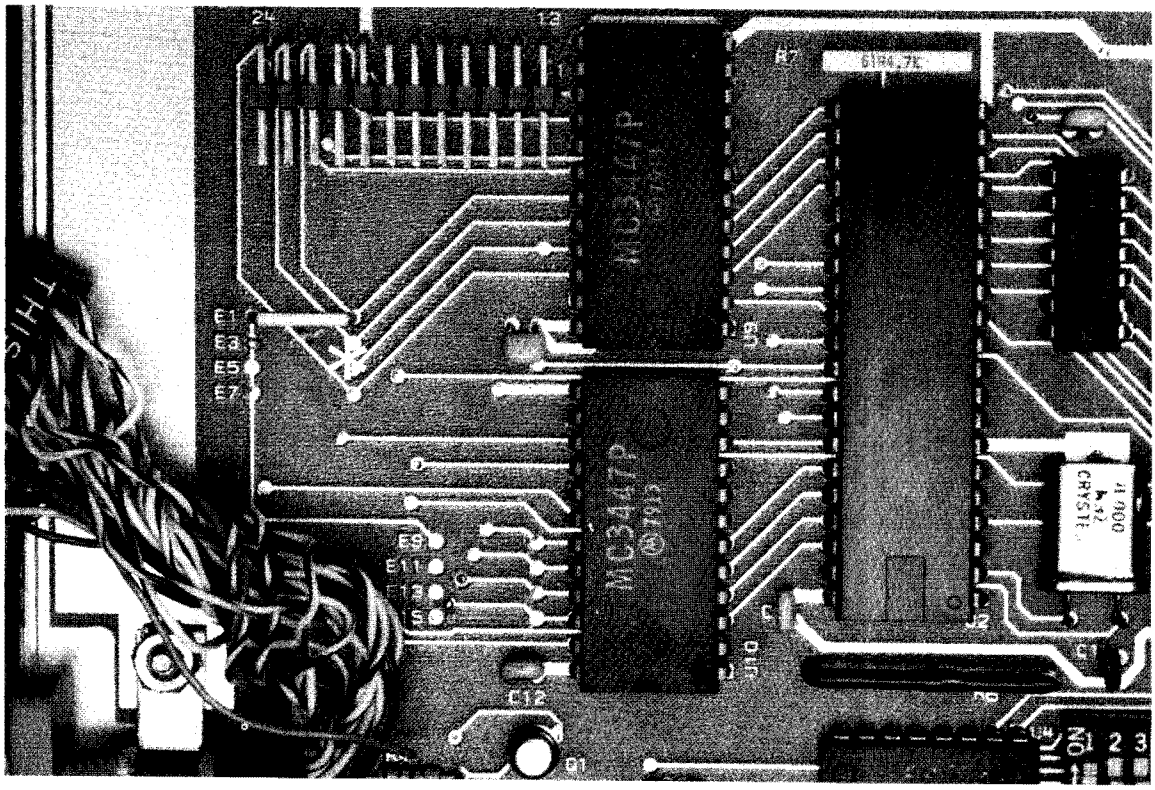


Figure 2-6. Parallel Poll Jumper Wire Placement

Installing the Interface and Connecting Peripherals

Make sure you read and understand this entire procedure before you install the interface or connect a peripheral device to it.

Safety Precautions

Manufacturers of peripheral devices do not all use the same grounding technique. Often, earth ground and logic ground are at different voltage levels. In some instances, this is deliberate in an effort to reduce ground return interference with digital signals.

When the 82937A interface is installed on the HP-85, earth ground and logic ground become connected together. Thus, if logic ground on a peripheral is never connected to earth ground or, if it is defective, it may have a voltage level considerably different than logic ground on the interface. This potential may be high enough to be hazardous unless peripherals are connected to the bus in an exacting manner.

If you don't know the grounding technique used on a peripheral, check with the manufacturer of the device. After verifying that suitable grounding techniques have been used in your peripheral, use the following steps in the order given to install the interface and peripherals to the HP-IB bus.

WARNING

To avoid personal injury and equipment damage, read and understand the preceding safety precautions and do not deviate from the order of the following steps when installing the interface and peripheral(s).

1. Turn the power switch located on the back of the HP-85 to the OFF position. However, make sure the HP-85 power cord is plugged into a grounded (three wire) AC outlet.
2. Remove the protective cover from any unused I/O slot to accommodate the interface and ROM drawer. Any unused I/O slots should be kept covered.
3. Refer to Figure 2-7 and install the interface into one of the I/O slots. Do not force the interface into the I/O slot. Notice that the tracks are keyed to prevent the interface from being inserted upside-down. If you intend to run the functional test, refer to that discussion at the end of this section before proceeding with step 4.

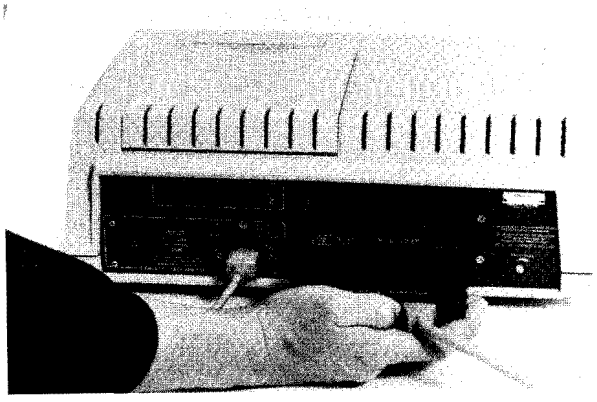


Figure 2-7. Installing the Interface

4. Make sure the power switch on all peripherals to be connected to the HP-IB bus are in the OFF position.
5. Connect the interface cable to the first peripheral. If other peripherals are to be connected at this time, first make sure they all have their power switches in the OFF position. Then, using the accessory cables listed on page 22 , install the cable connectors to the remaining peripherals in a piggy-back fashion, making sure to observe the cable length restrictions given on page 23 .
6. After all the peripherals are connected to the HP-IB bus, turn the power switches on the HP-85 and all peripherals to be operational on the bus to the ON position. A peripheral may be connected to the bus and have its power off without affecting bus operations, as long as more than 50% of the bus devices have their power on. For example, if there are three peripheral devices, two must have their power on; if there are two peripherals, both must have their power on.

Removing Peripherals/Disconnecting the Interface

Use the following steps in the order given to remove peripherals from the HP-IB bus or to disconnect the interface from the HP-85.

CAUTION

Do not remove the interface from the HP-85 with the HP-85 power switch on. Doing this will cause damage to either the interface, HP-85 or both.

1. Turn the power switch of all peripherals connected to the HP-IB bus to the OFF position.
2. Disconnect the HP-IB bus cable from each peripheral you intend to remove from the bus. If all peripherals aren't to be removed from the bus, you may return power to the remaining peripherals after the desired peripherals have been disconnected. If you intend to disconnect the interface from the HP-85, first make sure that all bus devices have their power switches in the OFF position. Then remove the interface cable from the peripheral it is connected to and proceed with step 3.
3. Turn the power switch on the back of the HP-85 to the OFF position. Make sure the interface cable is not connected to a peripheral and proceed with step 4.
4. Remove the interface from the I/O slot.

Interconnecting Cables

WARNING

Before you attempt to use any of the accessory cables, make sure you read and understand the safety precautions on page 20 .

The length of the interface cable is two metres. The end of the cable has a piggy-back connector that connects to a peripheral device. On some peripherals a physical interference problem may exist for the cable connector. Any peripheral that will not directly accept the cable connector will require the adapter. Other peripheral devices may be added to the bus by stacking the piggy-back connectors of the standard bus cables listed below.

Length	Accessory Number
½ metre	10833D
1 metre	10833A
2 metres	10833B
4 metres	10833C
Adapter	10834A

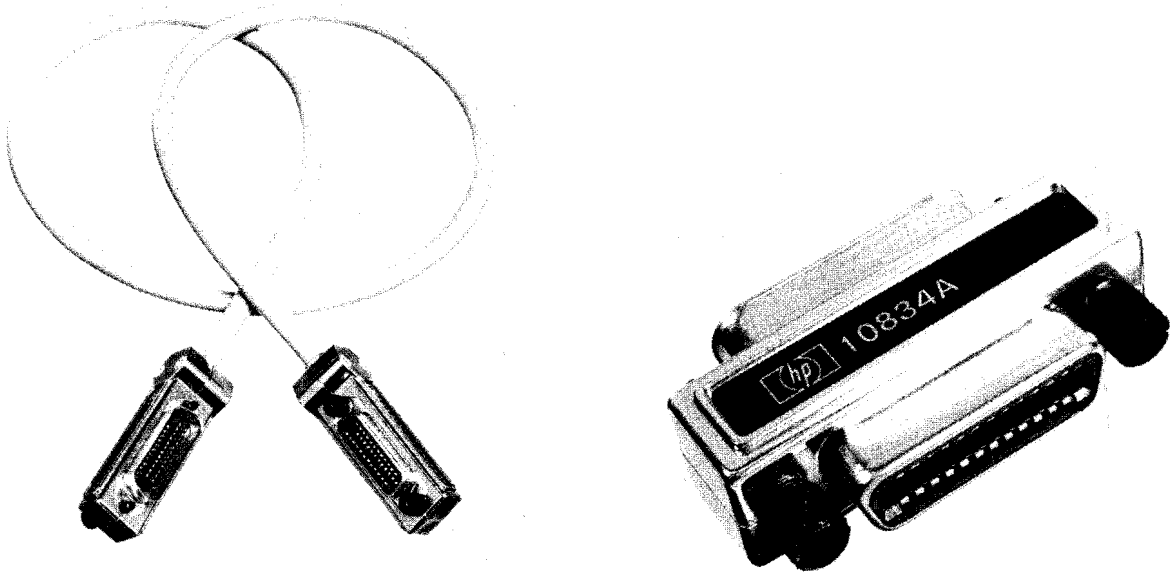


Figure 2-8. Bus Cables

There are no restrictions as to how cables may be connected together. However, it is recommended that no more than three or four piggy-back connectors be stacked together on one device. Doing so could exert enough force on the connector mounting to cause mechanical damage.

Cabling Length Restrictions

In order to ensure proper operation of the bus, two rules must be observed regarding the total length of bus cables when they are connected together:

- The total length of cable permitted with one bus interface must be less than or equal to two metres times the number of devices connected together with their power on (the interface is counted as one device).
- The total length of cable must not exceed 20 metres.

For example, there may be up to 4 metres of cable between the first two devices (2 devices x 2m/device = 4m). Additional devices may be added using 2-metre cables up to a total of 10 devices (10 device x 2m/device = 20 metres) using one 4-metre and eight 2-metre cables (4 + (8 x 2) = 20). If more than ten devices are to be connected together, cables shorter than two metres must be used between some of the devices. For example, 15 devices can be connected together using one 4-metre and thirteen 1-metre cables (4 + (13 x 1) = 17). Other combinations may be used as long as both requirements are met.

Metric Conversion Kit

The interface cable is supplied with mounting fasteners having metric threads. Other HP-IB instruments, however, may have either National Coarse (American) threads or metric threads. The American-threaded fasteners are chromium plated, while the metric-threaded fasteners are black.

Since metric and American threads cannot be connected together, a conversion kit may be needed. This kit will replace the mounting fasteners on any bus cable connector. Conversion kits can be ordered by specifying HP Part Number 5060-0138.

Functional Test

The following program listing may be entered and run to functionally test the interface. In most instances, running this test will indicate whether or not the interface is operational.

> **Note:** Before you run the test, make sure the interface has the System Controller switch segment set to "1" and the I/O ROM is installed.

Use the following steps to enter and run the test from the HP-85 keyboard:

1. Make sure the interface and I/O ROM are installed. If necessary, refer to page 20 and install the interface and I/O ROM.
2. Peripherals may or may not be connected to the interface.
3. Turn the HP-85 power switch to the ON position.
4. Press the [SHIFT] key and, while this key is depressed, press the [AUTO] key. This will cause the program lines to be numbered by ten in ascending order (10, 20, 30, etc.). Then press [END LINE]
5. Refer to the following program listing and enter the first line by pressing these keys:

   [C] [L] [E] [A] [R] then press [END LINE]

   Continue this procedure until the entire program is entered, making sure to press [END LINE] as each numbered program line is entered.

```
 10 CLEAR
 20 DISP "82937A EXERCISER";"ENT
    ER SELECT CODE..." @ PRINT "
    82937A EXERCISER"
 30 INPUT S
 40 DISP "ENTER # OF TIMES TO RU
    N TEST..."
 50 INPUT N
 60 RESET S
 70 GOSUB 130
 80 GOSUB 370
 90 N=N-1
100 IF N>0 THEN GOTO 70
110 DISP "TEST COMPLETE" @ PRINT
     "TEST COMPLETE"
120 END
130 DISP "CHECKING SWITCH SETTIN
    GS AND";"HANDSHAKE"
140 A2=0
150 A1=53
160 WIO S,0;2
170 WIO S,1;230
180 IF RIO (S,0)<128 THEN 220
190 A2=A2+1 @ IF A2>2 THEN GOSUB
     460
200 IF A2=3 THEN 220
210 GOTO 180
220 WIO S,0;0
230 WIO S,1;3
240 IF RIO (S,0)<128 THEN 280
250 A2=A2+1 @ IF A2>4 THEN GOSUB
     460
```

```
260 IF A2=4 THEN 280
270 GOTO 240
280 WIO S,0;2
290 WIO S,1;120
300 WIO S,0;0
310 IF RIO (S,0)<1 THEN 310
320 A1=RIO (S,1)
330 IF RIO (S,0)#0 THEN GOSUB
    480
340 IF A1>192 THEN A1=A1-192
350 IF A1#53 THEN GOSUB 500
360 RETURN
370 DISP "STATUS TEST"
380 STATUS S,0 ; B1,B2,B3,B4,B5,
    B6
390 IF B1#1 THEN GOSUB 540
400 IF B2#0 THEN GOSUB 540
410 IF B3#64 THEN GOSUB 540
420 IF B4#0 THEN GOSUB 540
430 IF B5#A1 THEN GOSUB 540
440 IF B6#160 THEN GOSUB 540
450 RETURN
460 PRINT "HANDSHAKE ERROR-PROBA
    BLE";"PROCESSOR OR XLATOR FA
    ILURE"
470 RETURN
480 PRINT "XLATOR IB NOT CLEAR W
    HEN";"EXPECTED-PROBABLE XLAT
    OR OR";"PROCESSOR FAILURE"


490 RETURN
500 PRINT "SWITCHES DIDN'T READ
    AS EXPECTED DEFAULT"
510 A$=DTB$(A1)
520 PRINT "SWITCHES 2-7 READ AS
    "&A$[11,16]&"      EXPECTED
    110101"
530 RETURN
540 PRINT "STATUS ERROR"
550 PRINT "STS BYTES=";B1;B2;B3;
    B4;B5;B6
560 RETURN
```

6. After the program is entered press (RUN). The printer should print:

```
                              82937A EXERCISER
```

   The screen should display:

```
82937A EXERCISER
ENTER SELECT CODE
?
```

7. Respond by entering the select code the interface is set to. For example, if select code 7 is set, press (7) and then (END LINE). If the wrong select code is entered, one or more error messages will appear on the screen after step 8 is performed. If this happens, press (RUN) and enter the select code again.

8. The screen should then display:

```
ENTER # OF TIMES TO RUN TEST
?
```

9. Enter the number of times you wish to run the short test. To run the test once, press (1) and then (END LINE); to run the test ten times, press (1) (0) and then (END LINE), etc. Running the test several times may be useful if you suspect an intermittent failure.

10. The screen should then display:

```
CHECKING SWITCH SETTINGS AND
HANDSHAKE
```

If this test passes, shortly thereafter the screen will display:

```
STATUS TEST
```

The test names are displayed on the screen the number of times you have specified for the test to run unless there is a failure. If a test fails, an error message is printed for that test. If the first test fails, the printer should print:

```
HANDSHAKE ERROR-PROBABLE
XLATOR OR PROCESSOR FAILURE
```

OR

```
XLATOR IB NOT CLEAR WHEN
EXPECTED-PROBABLE XLATOR OR
PROCESSOR FAILURE
```

If the factory settings of switch segments 2 through 7 have been changed, you can always expect the printer to print:

```
SWITCHES DIDN'T READ AS EXPECTED
DEFAULT

SWITCHES 2-7 READ AS

-EXPECTED 110101
```

(This portion of the printout will be a series of 0's and/or 1's depending on how the HP-85 interprets the switch settings. The first 0 or 1 is for switch segment 2, the second is for switch segment 3, etc. Switch segment 1 and 8 through 10 are not read.)

(These are the factory settings.)

If the above is printed, it does not necessarily mean that the switches are being read improperly. Except for switch segment 2, which must always be 1 to enable the HP-85 as System Controller, the switches may be set to any combination. This feature permits you to set the switches for any talk/listen address given in Figure 2-3 and then verify the switches are being read properly for that address.

If the status test fails, the printer will print:

```
STATUS ERROR
STS BYTES =
```

(This portion of the printout will be a series of numbers indicating which bits are set in status registers SR0 through SR5. SR6 is not read. The first number is for SR0, the second for SR1, etc. These status registers are shown on page 42 .)

An example of a proper status byte would be:

```
1   0   64   0   53   160
```

The only number that may vary in a proper status byte is the one indicating the bits set in SR4. This is shown as 53 in the above status byte and is discussed in more detail in the following discussion.

If a status error is printed, you can identify which bits of a register are set by decoding the decimal number printed into its binary equivalent. Then refer to the status registers on page 42 . The status register bits are shown with bit 0 being the least significant and bit 7 the most significant. The decimal values of the bits are as follows:

SR Bit	Decimal Equivalent
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

The numbers of the proper status byte can therefore be interpreted as follows:

- The first number, 1, indicates that bit 0 in SR0 is set to 1 and all others are 0.
- The second number, 0, indicates that all bits of SR1 are 0.
- The third number, 64, indicates that bit 6 of SR2 is set to 1 and all others are 0.
- The fourth number, 0, indicates that all bits of SR3 are 0.
- The fifth number, 53, indicates that bits 5, 4, 2 and 1 of SR4 are set to 1 and all others are 0.
- The sixth number, 160, indicates that bits 7 and 5 of SR5 are set to 1 and all others are 0.

Now, let us examine the fifth number, 53, which is the only number that may vary in a proper status byte. This number reflects the contents of SR4, the address register. This register should always coincide with how switch segments 2 through 7 are set, which was discussed earlier in this section. The number 53 reflects that the system controller switch and the talk/listen address switches are all in the factory preset positions. The smallest number that should ever appear in this position while running the test is 32, corresponding to the system controller switch being set to 1 and the talk/listen address switches set for address 0. The largest number that should ever appear in the fifth position is 62, corresponding to the system controller switch being set to 1 and the talk/listen address switches set for address 30.

11. After all the tests are run, the printer and screen should display:

```
TEST COMPLETE
```

Section 3

Theory of Operation

Introduction

This section contains a description of the interface circuit operations. This includes a detailed block diagram description of the Translator IC and a schematic diagram description of various interface components and signal lines. Although this information is provided, component level repair is not recommended due to the microcomputer based organization of the interface.

If the interface appears to be malfunctioning, it is recommended that you contact your nearest HP sales and service office for assistance; office locations are listed after the schematic diagram.

Translator IC Description

The interface uses an 8049 microcomputer (μC) which requires the +5V TTL logic level. The microprocessor in the HP-85 uses a +6V logic level. A special IC, known as a Translator, permits communication between the two devices by providing level translation. The +5V and +6V power supplies and two +12V clock signals (Φ1 and Φ2) required by the Translator are located on the HP-85 mainframe. They are brought out to the interface via the I/O backplane when the interface is inserted into one of the four I/O slots.

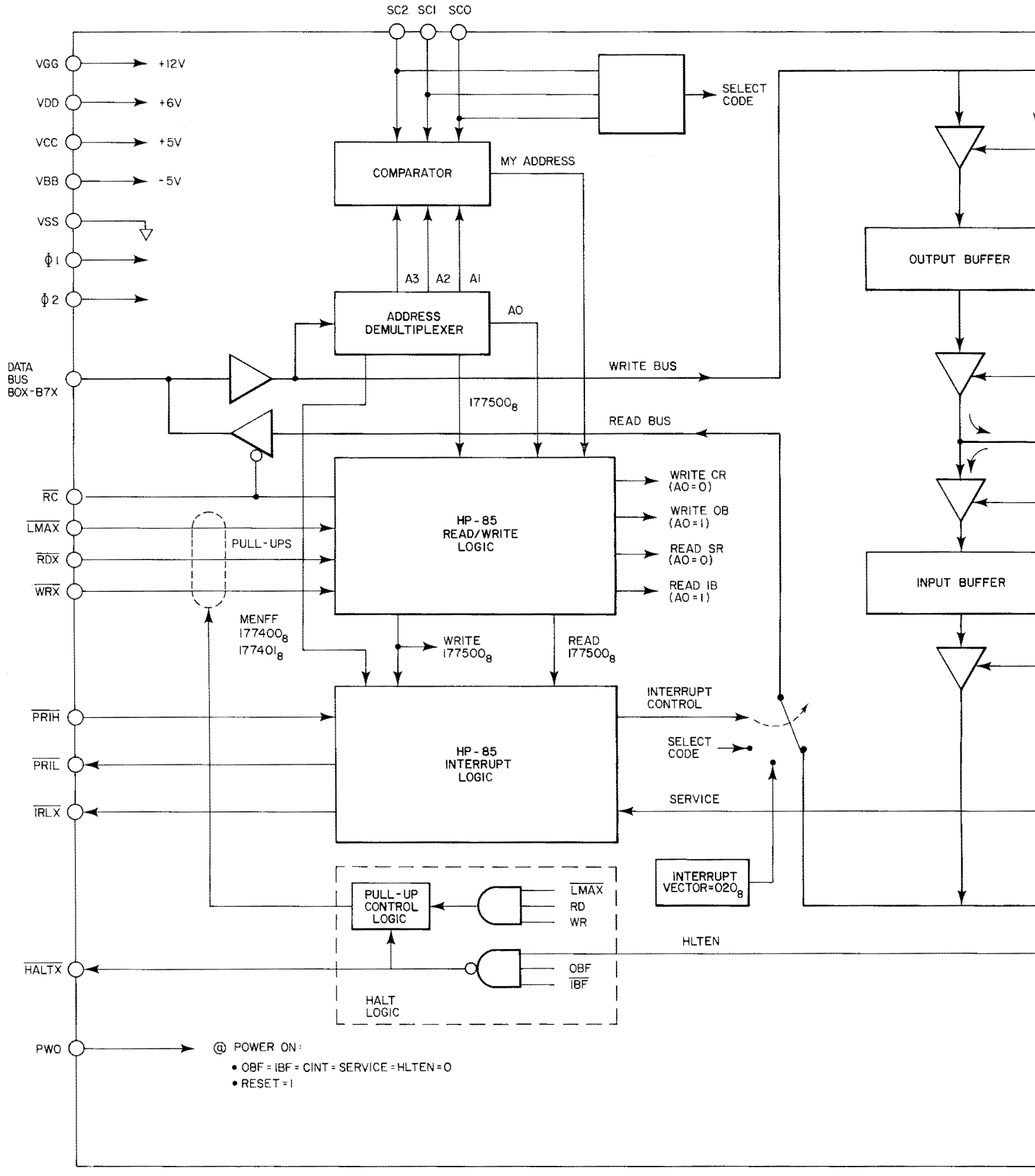
The Translator supports the following operations:

- Handshaking of data and command information from the HP-85 to the μC.
- Handshaking of data from the μC to the HP-85.
- Interrupts issued to the HP-85 by the μC.
- Interrupts issued to the μC by the HP-85.
- Fast handshake operation where the Translator halts the HP-85 with each data byte transfer to synchronize the flow of data.

It may be helpful to refer to the block diagram of the Translator IC (Figure 3-1) and the interface schematic diagram (Figure 3-9) while reading the theory discussed in this section.

Select Codes

Interfaces are memory mapped. When the HP-85 addresses an interface, it provides an address over the address and data bus (B0X – B7X). The Translator demultiplexes the address and then compares address bits (A1, A2, A3) with select code bits (SC0, SC1, SC2). If they match, the interface is addressed. When addressed, another bit (A0) is sent out by the Translator's Address Demultiplexer. If A0 is low, the HP-85 writes to the control register (CR) and reads the status register (SR). When A0 is high, the HP-85 writes to the output buffer (OB) and reads the input buffer (IB). These four registers are discussed next.


SC2 SCI SCO
VGG
+12V
VDD
+6V
VCC
+5V
VBB
-5V
VSS
Φ1
Φ2
SELECT CODE
COMPARATOR
MY ADDRESS
A3 A2 A1
ADDRESS DEMULTIPLEXER
AO
OUTPUT BUFFER
DATA BUS BOX-B7X
WRITE BUS
177500₈
READ BUS
RC
LMAX
RDX
WRX
PULL-UPS
HP-85 READ/WRITE LOGIC
WRITE CR (AO=0)
WRITE OB (AO=1)
READ SR (AO=0)
READ IB (AO=1)
INPUT BUFFER
MENFF
177400₈
177401₈
WRITE 177500₈
READ 177500₈
PRIH
PRIL
IRLX
HP-85 INTERRUPT LOGIC
INTERRUPT CONTROL
SELECT CODE
SERVICE
INTERRUPT VECTOR=020₈
PULL-UP CONTROL LOGIC
LMAX
RD
WR
HLTEN
HALTX
OBF
IBF
HALT LOGIC
PWO
@ POWER ON:
• OBF = IBF = CINT = SERVICE = HLTEN = 0
• RESET = 1

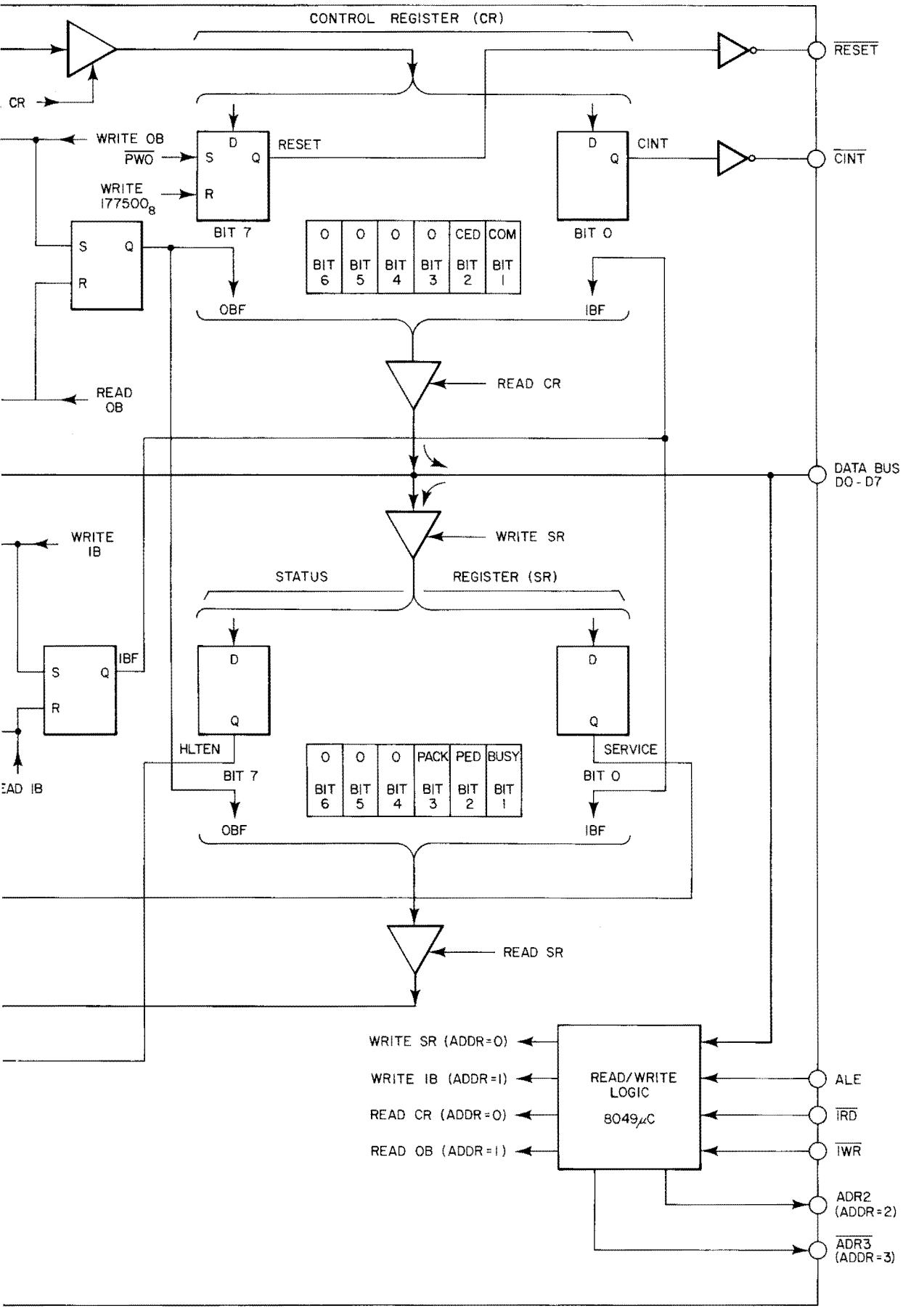


Figure 3-1. Translator IC Block Diagram

Translator I/O Registers

The HP-85 sends data to the μC via the output buffer register (OB) and defines that data by setting appropriate bits in the control register (CR). Both registers are physically located within the Translator IC. The OB is write-only by the HP-85 and read-only by the μC. Except for bit 0 and bit 7, the CR is also write-only by the HP-85 and read-only by the μC. Different status bits are read by the μC for bit 0 and bit 7 of the CR than those written as bits 0 and 7 by the HP-85. This is illustrated in Figure 3-2.

HP-85 Write to CR

7	6	5	4	3	2	1	0
RESET	0	0	0	0	CED	COM	CINT

μC Read CR

7	6	5	4	3	2	1	0
OBF	0	0	0	0	CED	COM	IBF

Figure 3-2. CR Bit Assignments

CINT	Interrupt. This bit is routed to the T1 input of the μC which is used to interrupt.
COM	Command.
CED	End Data. Used by HP-85 to terminate a data transfer to the μC.
RESET	Resets the μC. This bit is routed to the reset input of the μC.
IBF	Input Buffer Full.
OBF	Output Buffer Full.

Two other registers within the Translator are used when the HP-85 receives data from the μC. These registers are the input buffer register (IB) used to handle the data and the status register (SR) which contains status bits to implement communication protocol. The IB is write-only by the μC and read-only by the HP-85. Except for bit 0 and bit 7, the SR is also write-only by the μC and read-only by HP-85. Different status bits are read for bits 0 and 7 by the HP-85 than those written as bits 0 and 7 by the μC. This is illustrated in Figure 3-3.

μC Write to SR

7	6	5	4	3	2	1	0
HLTEN	0	0	0	PACK	PED	BUSY	SERVICE

HP-85 Read SR

7	6	5	4	3	2	1	0
OBF	0	0	0	PACK	PED	BUSY	IBF

Figure 3-3. SR Bit Assignments

SERVICE	The μC sets this bit to initiate an interrupt to the HP-85.
BUSY	Informs the HP-85 the state of the μC. When low, the μC is monitoring OBF to determine when the next command or data byte is available from the HP-85. When OBF is set, the μC sets BUSY to 1, reads the OB and CR, performs the necessary operation then returns BUSY to low.

PED	Processor (μC) End Data. Set high by the μC upon detection of a programmed termination sequence (byte count, end character or EOI).
PACK	Processor (μC) Interrupt Acknowledge. The μC's interrupt service routine sets this bit after being interrupted by the HP-85.
HLTEN	Used by the μC to halt the HP-85 based on the status of OBF and IBF during fast handshake data transfers.
IBF	Input Buffer Full.
OBF	Output Buffer Full.

Interrupts

The interface can interrupt the HP-85 for several reasons. For example, an interrupt may be generated when the interface detects the SRQ line being asserted from the HP-IB bus if the user has programmed the SRQ bit in the interrupt mask register. The interface interrupts the HP-85 as follows:

1. The interface μC sets bit 0 (Service) true in the Translator status register. This causes the interrupt line, $\overline{\text{IRLX}}$, to go low, interrupting the HP-85.
2. The HP-85 acknowledges the interrupt and obtains from the interface an interrupt vector. This tells the HP-85 that this is an I/O interrupt as opposed to an interrupt from the internal keyboard chip.
3. After the interrupt is acknowledged, $\overline{\text{IRLX}}$ is returned high and all other interfaces are locked out from interrupting until re-enabled by the HP-85.
4. The HP-85 then obtains the select code of the interrupting interface and processes the interrupt accordingly.
5. After the interrupting interface is serviced, the other interfaces are re-enabled to interrupt.

Since the HP-85 can accommodate up to three interfaces, there must be a priority scheme if more than one requests service at the same time. This would most likely be a very rare occurrence. Essentially, the HP-85 handles interrupts on a first-come, first-served basis. However, if more than one interface is pulling the $\overline{\text{IRLX}}$ line before the HP-85 acknowledges the interrupt request, the interface that gets serviced first will be the one occupying the upper-most I/O slot.

Refer to the flow chart of Figure 3-4 as you read the following sequence that takes place when the HP-85 interrupts the μC on the interface.

The μC interrupt counter is preset to 255. The interrupt is initiated when the HP-85 pulls $\overline{\text{CINT}}$ of the Translator (T1 of the μC) low. This increments the μC interrupt counter from 255 to 0 (an overflow), and starts the interrupt sequence. Before the μC acknowledges the interrupt, it reads the CR to check the IBF bit. If the IBF bit is set, it indicates the IB contains data. To prevent this data from being lost, the μC sets an input buffer restore flag. This will permit the IB to be restored after the interrupt is serviced.

The μC acknowledges the interrupt by setting the PACK bit in the SR. When PACK is set, the HP-85 reads the IB, which may or may not contain data, and discards it. The HP-85 then sets the COM (command) bit in the CR, writes an instruction into OB and returns $\overline{\text{CINT}}$ high. When $\overline{\text{CINT}}$ goes high, the μC accepts the instruction and performs the operation specified.

After the operation is performed, the HP-85 strobes $\overline{\text{CINT}}$ again, which increments the μC interrupt counter from 0 to 1. When this occurs, the interrupt counter gets reset to 255 and the SR is restored. If the input buffer restore flag is set, the IB is also restored. The μC then returns from interrupt.

Notice in the above sequence that $\overline{\text{CINT}}$ was strobed twice. The first time caused an overflow of the μC interrupt counter (from 255 to 0) which started the interrupt sequence. The second strobe incremented the interrupt counter from 0 to 1 which caused the μC to return from interrupt.

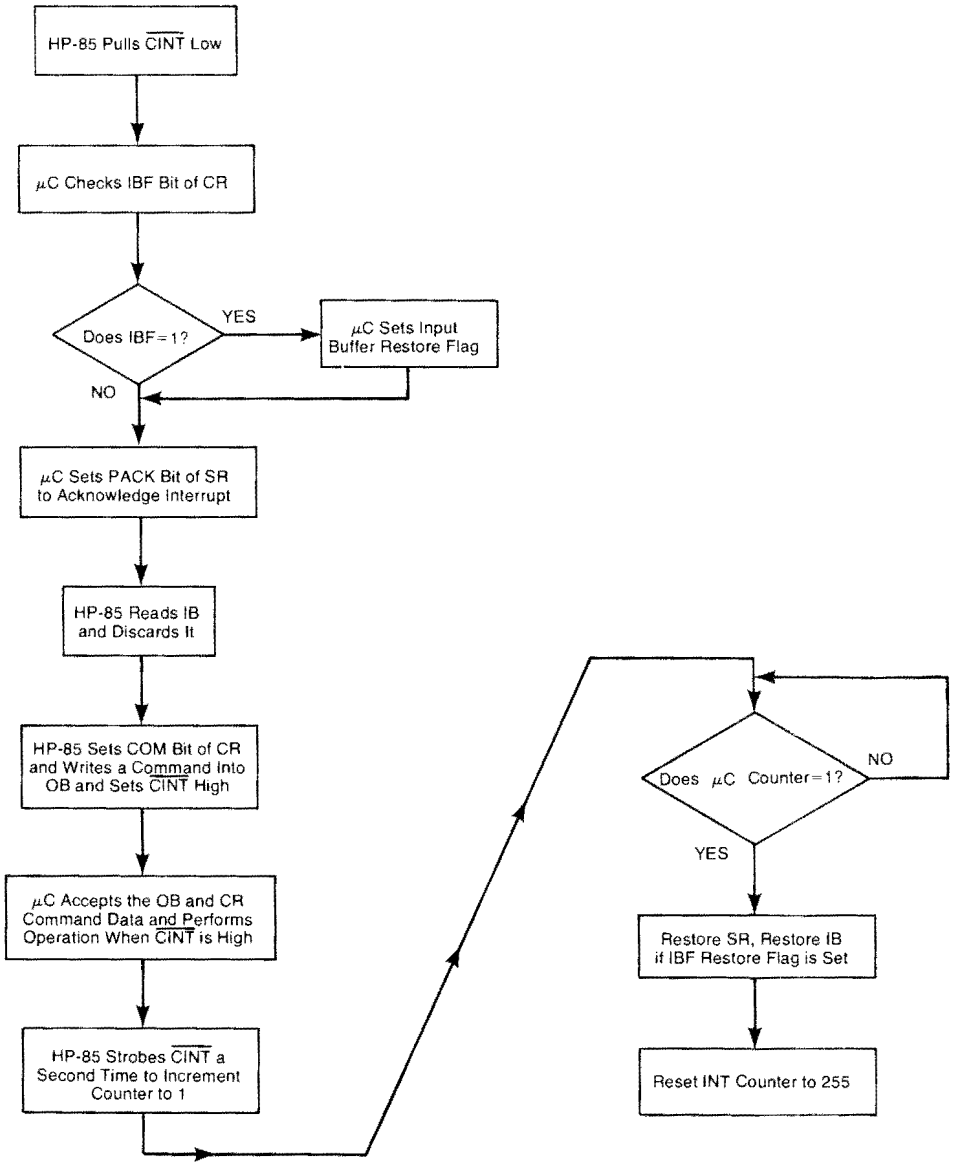


Figure 3-4. Interrupt Flow Chart

HP-85 I/O Backplane Lines

The I/O lines in Table 3-1 appear at each of the four I/O slots on the HP-85. They connect to the interface when it is inserted into any of the slots. Figure 3-5 shows how the I/O slot connector pins are numbered. Each I/O slot is numbered in the same manner.

Table 3-1. HP-85 I/O Backplane Lines

Line	Pin No.	Meaning	Direction HP-85	Direction Interface
Φ21	1	Non-Overlapping Clock (+12V) (not used)	→	
Φ2	2	Non-Overlapping Clock (+12V)	→	
Φ1	3	Non-Overlapping Clock (+12V)	→	
Φ12	4	Non-Overlapping Clock (+12V) (not used)	→	
V_{GG}	5	+12V	→	
$\overline{LMAX}$	6	Load Memory Address	→	
$\overline{IRLX}$	7	Interrupt Request	←	
$\overline{RDX}$	8	Read	→	
$\overline{RC}$	9	Read Control	←	
$\overline{WRX}$	10	Write	→	
V_{CC}	11	+5V	→	
B4X	12	I/O Line	↔	
B5X	13	I/O Line	↔	
B6X	14	I/O Line	↔	
B7X	15	I/O Line	↔	
—	16	Open		
$\overline{PRIH}$	17	Priority High	→	
DIS	18	Disable. +6V Signal Voltage. This is used to keep $\overline{PRIH}$ and $\overline{PRIL}$ from shorting together when an interface is plugged into an I/O slot.		
SPKR	$\overline{1}$	Speaker Output (not used)	→	
—	$\overline{2}$	Open		
—	$\overline{3}$	Open		
L. GND	$\overline{4}$	Logic Ground	→	
L. GND	$\overline{5}$	Logic Ground	→	
L. GND	$\overline{6}$	Logic Ground	→	
$\overline{HALTX}$	$\overline{7}$	Halt	←	
V_{BB}	$\overline{8}$	−5V	→	
—	$\overline{9}$	−12V (not used)	→	
PWO	$\overline{10}$	Power On	→	
V_{CC}	$\overline{11}$	+5V	→	
B0X	$\overline{12}$	I/O Line	↔	
B1X	$\overline{13}$	I/O Line	↔	
B2X	$\overline{14}$	I/O Line	↔	
B3X	$\overline{15}$	I/O Line	↔	
V_{DD}	$\overline{16}$	+6V	→	
—	$\overline{17}$	Open		
$\overline{PRIL}$	$\overline{18}$	Priority Low	←	

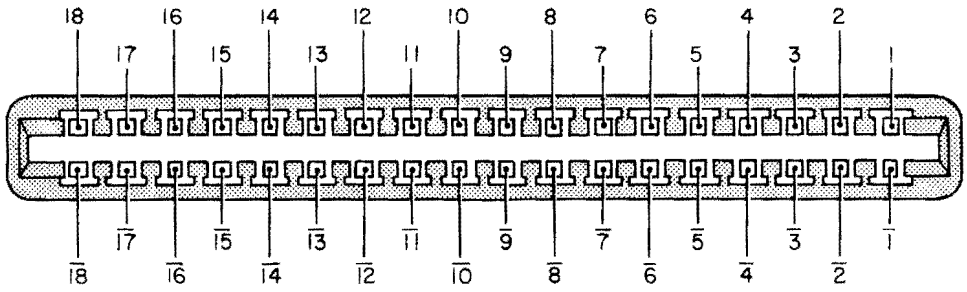


Figure 3-5. HP-85 I/O Slot Connector Pinout

HP-IB Bus Lines

The standard HP-IB signal lines are described next. The function of each line is defined by IEEE Standard 488-1978.

Note: IEEE Standard 488-1978 specifies that the HP-IB bus use negative true logic which is often confusing or misunderstood. This explanation of negative true logic, as it applies to the HP-IB bus and interface, is given so that no misconceptions exist.

All HP-IB bus lines are shown on the schematic without bars over them. Thus, if a bus line is true, it will have a low voltage level. Positive true logic is used on the interface. In positive true logic a line whose mnemonic does not have a bar over it is true when it has a high voltage level. As an example, on the schematic bus line ATN is shown as $\overline{\text{ATN}}$ when it appears as an internal signal on the interface. Thus, the voltage level representing a true ATN on the HP-IB bus is the same as a true $\overline{\text{ATN}}$ on the interface.

Data Lines (DIO1 – DIO8)

The data lines are used to communicate all data including input, output, program codes, status and control information between instruments connected to the bus. One character byte is sent at a time in a byte-serial, bit-parallel fashion. In most instruments, characters are based on the 8-bit ASCII representation. For instance, if the interface is connected to a printer, the 8-bits that represent one character are all sent at once in parallel. Then, the next character is sent and so on. Thus, the 8-bits (one byte) defining a character are all sent at once in parallel (bit-parallel) while each character is sent serially (byte-serial).

Control Lines (ATN, IFC, SRQ, EOI and REN)

The five control lines govern and define the information on the DIO lines.

ATN (Attention) is driven by the active controller. When high, the information on DIO1 through DIO8 is interpreted as data. When low the information is control or address information.

IFC (Interface Clear) is used only by the system controller to initialize the bus. When IFC is held low for at least 100μs, any talker or listener is stopped, the serial poll mode is disabled and control is returned to the system controller, regardless of the device that had control of the bus. When IFC is high, it has no effect on bus operations.

SRQ (Service Request) is pulled low by a device when it wants the attention of the controller. SRQ may be driven low at any time except when IFC is low.

EOI (End or Identify) may be used to indicate the end of a string of characters. For example, if ATN is high to indicate the information on DIO1 through DIO8 is data, the talker may indicate the end of its data transmission by driving EOI low when it places the last byte on the data lines.

REN (Remote Enable) is driven by the system controller and is one of the lines necessary for an instrument to operate under remote control. Only instruments capable of remote operation use REN and they monitor it at all times. Instruments that do not use REN terminate the line into a resistor load. The system controller may change the state of REN at any time.

Transfer Lines (NRFD, NDAC and DAV)

Three transfer (handshake) lines are used to execute the transfer of each byte of information on the data lines. They allow asynchronous data transfer without timing restrictions being placed on any instrument connected to the bus. The transfer speed of each data byte is determined by the speed at which the slowest instrument is capable of sending or receiving data.

NRFD (Not Ready For Data) is high to indicate that all listeners are ready to accept information on the DIO lines. When NRFD is low, at least one listener is not ready for data.

NDAC (Not Data Accepted) is high to indicate that all listeners have accepted the information on the DIO lines. When NDAC is low, at least one listener has not accepted the data.

DAV (Data Valid) is low to indicate the information on the DIO lines is valid for the listener(s). When DAV is high, the information on the DIO lines is not valid.

Data Transfer

Transfer of data on the bus is asynchronous. That is, there are no restrictions placed on the data rates of instruments connected to the bus. The slowest instrument involved in a data transfer on the bus determines the rate of data transfer. As previously mentioned, transfer is under the control of three lines: DAV, NRFD and NDAC. The talker controls the data lines and DAV; the listener(s) controls NRFD and NDAC.

The transfer of a byte of data is initiated by all listeners setting NRFD high, indicating they are ready for data. When the talker recognizes NRFD is high it places data on the lines and validates the data by placing DAV low. The listener(s) senses that DAV is low, accepts the data, then notes the acceptance by setting NDAC high. Notice that the assertive, or action state, of NRFD and NDAC is high. Because all instruments on the bus have their corresponding lines connected together, all listeners must have NRFD and NDAC high before the respective line is high. This is because a low state overrides a high. Thus, a slow listener on the bus that does not accept data and thereby assert NRFD and NDAC as readily as other listeners will slow the rate of data transfer.

The timing diagram in Figure 3-6 shows the relationship of these signal lines during a data byte transfer. At t_1 NRFD is set high to indicate all listeners are ready to accept data. At t_2 the talker places data on the lines and indicates the validity of the data at t_3 by placing DAV low. At some interval between t_3 and t_4 a listener may place NRFD low but it must do so before, or at the same time that NDAC is set high. The talker may return DAV high after it detects NDAC is high, which is shown at t_5. A listener may set NDAC low (shown between t_5 and t_6) but, it must do so before NRFD is set high at t_6. When NRFD goes high at t_6, a new cycle begins equivalent to t_1.

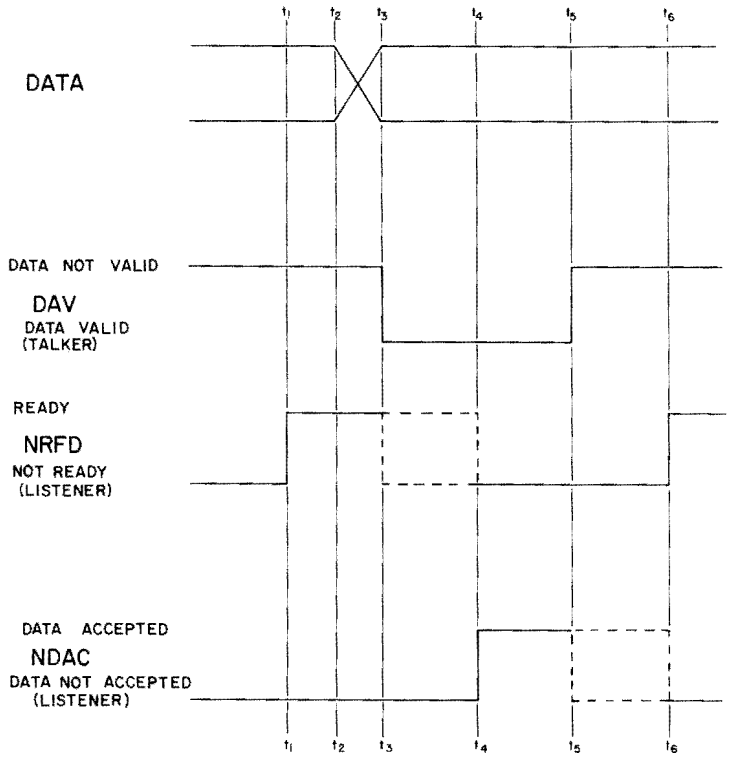


Figure 3-6. Data Transfer Timing Diagram

Polling

Polling is a special bus activity that permits a controller to determine the operating status of other devices. These two processes, serial poll and parallel poll, are an intricate part of the interrupt protocol. However, because software can define whether a serial or parallel poll (or both) is implemented, they are discussed as separate topics to simplify the explanation.

Serial Poll

A serial poll permits the controller active device to obtain a status byte from any bus device that supports the serial poll function. When the controller active device detects that a service request exists (SRQ line is pulled), it may serially poll the bus devices expected to have requested service. When a device is polled, it always returns its status byte. Bit 7 of the status byte will be set to 1 if the device requested service or it will be 0 if it did not. The remainder of the bits in the status byte can be used to indicate the reason for the service request and are totally device dependent.

The programmer has two means of detecting when SRQ is pulled:

- Perform a STATUS read of register SR2 to see if the SRQ bit (bit 5) is set;
- Enable an End-of-Line interrupt when SRQ is pulled.

The bus might have only one bus device capable of requesting service and perhaps for only one purpose. In this case, a serial poll may not be needed. However, if a single device can pull SRQ for various reasons or, if more than one bus device is capable of pulling SRQ, then a serial poll can be used to determine which device(s) requested service and why.

When the HP-85 is controller active and initiates a serial poll, the program specifies the select code and the address of the device to be polled. The 82937A interface then sends the following sequence over the bus:

1. ATN is set true.
2. UNL (Unlisten) command is sent to the device.
3. Interface sends its own listen address and the peripheral talk address commands.
4. SPE (Serial Poll Enable) is sent over the bus, followed by ATN going false. The device being polled then sends its status byte. If it was the only device requesting service, SRQ is removed. If it was not the only device pulling SRQ, or if it didn't request service, SRQ remains, indicating some other device requires service.
5. ATN is set true again followed by the SPD (Serial Poll Disable) command.
6. The UNT (Untalk) command is then sent over the bus causing the peripheral to cease being a talker.

Note in the above sequence that SRQ may or may not be removed when a device is polled. SRQ is removed if the device being polled is the one and only device requesting service. Therefore, the user's program must specify the order in which bus devices are polled and serviced.

If the HP-85 is not the controller active device, the user may allow it to request service with the REQUEST statement followed by a program dependent status byte. Bit 7 of this status byte maps directly to SRQ on the bus. The HP-85 provides this status byte when it is serially polled by the controller active device. If it was requesting service, bit 7 will be set to 1; otherwise, it will be 0. The HP-85 will remove SRQ when it sends its status byte if it was the one and only bus device requesting service. However, if SRQ is removed, bit 7 remains set until changed by the program.

Parallel Poll

In a parallel poll each bus device is assigned one of the DIO lines for identification purposes. This is configured within each bus device. The parallel poll jumper on the interface is used to assign one of the DIO lines for identification of the interface if it is to respond to parallel polls.

A parallel poll can be much faster than a serial poll because the controller reads DIO1 through DIO8 all at once to determine which device(s) requested service.

Switch Buffer (U4)

The switch buffer is a single integrated circuit that isolates switch lines A0 through A4 and SC from the interface address data bus. These lines were discussed in Section 2.

The outputs of U4 connect to the address-data bus and the external control latch (U3). Unless it is enabled, these outputs remain in a high impedance state. When it is enabled via inputs DIS1 and DIS2, the switch settings are reflected on the outputs and therefore appear on D0 through D5 of the address-data bus and the inputs to the external control latch. Thus, the switch buffer is enabled only during initialization or when the 8049 μC is reset to prevent it from interfering with other operations. Once the status of the switches is read by the μC it is not necessary to do so again unless the μC is reset.

To read the switch buffer, the μC sends an address to the Translator read/write logic via the address-data bus and latches it with the address latch enable (ALE) signal. The Translator responds by placing $\overline{\text{ADR3}}$ low. The μC then places $\overline{\text{RD}}$ low. During the period when both these signals are low, the switch buffer is enabled allowing the switch settings to be reflected on D0 through D5 of the address-data bus to be read by the μC.

External Control Latch (U3)

This latch is clocked to accept the information on the address-data bus lines (D0 – D5). This occurs when $\overline{\text{WR}}$ is low and the μC writes an address to the Translator that causes $\overline{\text{ADR3}}$ to go low. This latch is cleared on initialization or when the μC is reset.

The output lines of this latch serve a variety of functions and are discussed separately.

Output	Function
EN NDAC	The IEEE Standard 488-1978 specifies that when ATN goes true, NDAC must go false within 200 ns. This helps ensure that a transfer will proceed in an orderly fashion. The EN NDAC output is gated with IATN to provide a hardware implementation to meet this specification.

EN ATN INT — This line is gated with the IATN line to the interrupt ($\overline{INT}$) input of the μC. When EN ATN INT is set and a peripheral device asserts ATN, the μC recognizes an interrupt request.

EN REN INT — This line is gated with the $\overline{IREN}$ line to the interrupt ($\overline{INT}$) input of the μC. When EN REN INT is true and a peripheral device asserts REN, the μC recognizes an interrupt request.

EN IFC INT — This is gated with the IIFC line to the interrupt ($\overline{INT}$) input of the μC. When EN IFC INT is set and a peripheral device assert IFC, the μC recognizes an interrupt request.

TALKER ACTIVE (TA) — When TA and $\overline{IATN}$ are both true it enables the bi-directional buffers connected to the HP-IB bus (DIO1 through DIO8) in a direction which permits the μC to output information to the bus.

CONTROLLER ACTIVE (CA)* — When this line and IATN are both set the μC is allowed to output information to the HP-IB bus in the same manner described above. Also, the controller can only source commands when ATN is true. The CA line is also used to enable the buffers for the service request (SRQ) and attention (ATN) lines on the HP-IB bus. In the latter, the controller can only source commands when ATN is true; while another talker can only source data when ATN is false.

Bi-directional Bus Transceivers (U9, U10)

Two integrated circuits provide the bi-directional bus transceiver circuitry used to transmit or receive information between the HP-85 and other HP-IB bus devices. The send/receive pairs that connect to bus lines DIO1 through DIO8 are enabled so that all either send or receive bus information in the same direction simultaneously. The handshake and control lines for the bus are enabled as follows:

NRFD and NDAC — Two send/receive pairs are enabled to send or receive the state of these bus lines in the same direction simultaneously.

DAV and EOI — Two send/receive pairs are enabled to send or receive the state of these bus lines in the same direction simultaneously.

ATN — One send/receive pair is enabled by the CA line to permit ATN to be asserted from the controller to other bus devices.

SRQ — One send/receive pair is enabled by the CA line to permit SRQ to be asserted over the HP-IB bus. If CA is high, the HP-85 monitors SRQ from the bus. If CA is low, the HP-85 pulls SRQ when it requests service from another controller.

REN and IFC — Two send/receive pairs are enabled to send or receive the state of these bus lines in the same direction simultaneously.

* CONTROLLER ACTIVE (CA) is synonymous with the term controller-in-charge which is referenced in IEEE Standard 488-1978.

8049 Microcomputer (μC)

Most of the activities carried out by the 8049 μC have already been discussed in this section. This discussion will summarize these activities, give the pin assignment and provide register tables.

The μC is the intermediary between the HP-85 and the HP-IB bus. It implements interface protocol via its own self contained ROM. The μC responds to instructions from the host HP-85 or the bus, depending upon which bus device is assigned controller status. When the host HP-85 is system controller, the μC can recognize an interrupt from an HP-IB bus device, and, depending upon user programmed interrupt conditions, it may service the interrupt or it may in turn interrupt the HP-85.

There are two 8-bit I/O ports that connect the μC to the HP-IB bus. Port 1 connects to the handshake and control lines; port 2 connects to the data lines (DIO1 through DIO8). There are eight other bits (D0 through D7) which go to the address-data bus connecting the μC to the Translator.

The following table lists all the lines used on the 8049 μC.

Table 3-2. 8049 Microcomputer Pin Assignment

Designation	Pin Number	Function
Vss	20	Circuit GND.
V_{DD}	26	+5V.
Vcc	40	+5V.
P10 – P17 (Port 1)	27 – 34	8-bit I/O port that connects to the control and handshake lines on the HP-IB bus.
P20 – P27 (Port 2)	21 – 24 35 – 38	8-bit I/O port that connects to the data lines (DIO1 – DIO8) on the HP-IB bus.
D0 – D7 (Address-Data Bus)	12 – 19	A bi-directional port that connects to the address-data bus from the Translator.
T0	1	An input used to sample ATN. If ATN is true, the μC remains in interrupt service routine and handshakes commands. If ATN is false, the μC leaves the interrupt service routine and returns to the main program.
T1	39	An input which initiates an interrupt of the μC.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt to the HP-85 from the HP-IB bus if interrupt is enabled. Interrupt is disabled after a reset (active low.
$\overline{RD}$	8	Read strobe. When low the μC reads the address-data bus (D0 – D7).
$\overline{WR}$	10	Write strobe. When low the μC writes to the address-data bus (D0 – D7).
$\overline{RESET}$	4	Reset. An active low strobe which is used to initialize the μC.
ALE	11	Address Latch Enable. The negative edge of ALE causes an address the μC has placed on the address-data bus (D0 – D7) to be latched into the Translator.
XTAL 1	2	One side of crystal input for internal oscillator.
XTAL 2	3	Other side of crystal input.
$\overline{PSEN}$	9	Not used.
EA	7	Circuit GND.
$\overline{SS}$	5	Not used.

Internal to the μC are seven 8-bit status registers and twelve 8-bit control registers. The status registers indicate the state of the μC at a given time. The control registers are written to when the state of the interface is to be changed. Register tables of the status and control registers are given in Figures 3-7 and 3-8. If a detailed description of these registers is desired, refer to the I/O ROM manual.

Register Number	Bit Number 7	6	5	4	3	2	1	0	Register Function
SRQ	0	0	0	0	0	0	0	1	Interface Identification
SR1	IFC	LA	CA	TA	SRQ	DCL or SDC	GET	SCG	Interrupt Cause
SR2	IFC	REN	SRQ	ATN	EOI	DAV	NDAC	NRFD	HP-IB Control Lines
SR3	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	HP-IB Data Lines
SR4	0	0	System Controller	A4	A3	A2	A1	A0	HP-IB Address and System Controller
SR5	System Controller	LA	CA	TA	SPE	Parity Error	Remote	Local Lockout	State Register
SR6	0	0	0	SC5	SC4	SC3	SC2	SC1	Secondary Commands

Figure 3-7. μC Status Registers

CAUTION

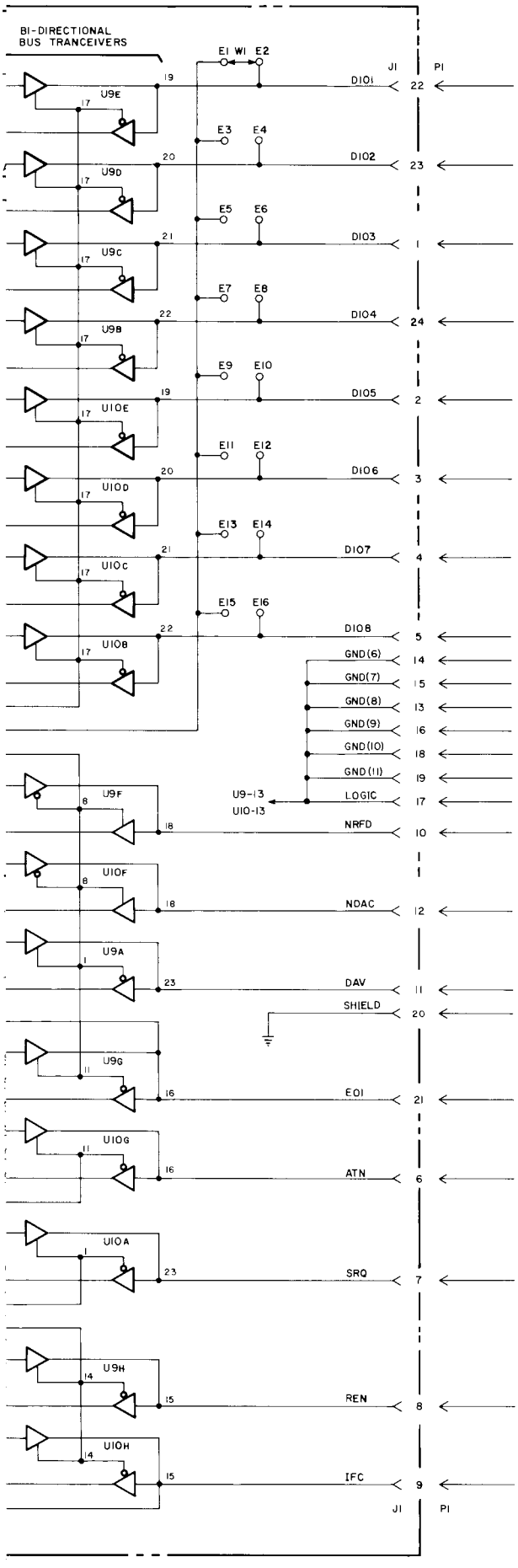
Do not write to Control Registers 0 through 3 unless you have an I/O ROM and you are completely familiar with the function of these registers. In particular, Control Registers 2 and 3 provide direct access to the HP-IB control and data lines. They must be used with care, and used only by persons aware of HP-IB protocols! It is possible to cause a bus malfunction or device damage by improper use of these registers.

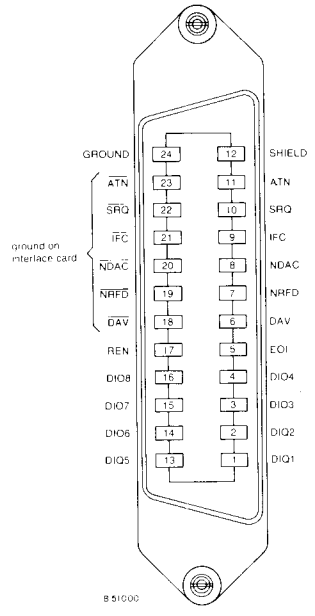
Register Number	Bit Number 7	6	5	4	3	2	1	0	Register Function
CR0	X	X	X	X	Odd Parity	Even Parity	One Parity	Zero Parity	Parity Control
CR1	IFC Mask	LA Mask	CA Mask	TA Mask	SRQ Mask	Clear Mask	Trigger Mask	SCG Mask	Interrupt Mask
CR2	X	REN	SRQ	ATN	EOI	DAV	DAC	RFD	HP-IB Control Lines
CR3	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	HP-IB Data Lines
CR16	EOI Enable	X	X	X	X	EOL2	EOL1	EOL0	EOL Control
CR17				Default = CR					Character #1
CR18				Default = LF					Character #2
CR19									Character #3
CR20									Character #4
CR21									Character #5
CR22									Character #6
CR23									Character #7

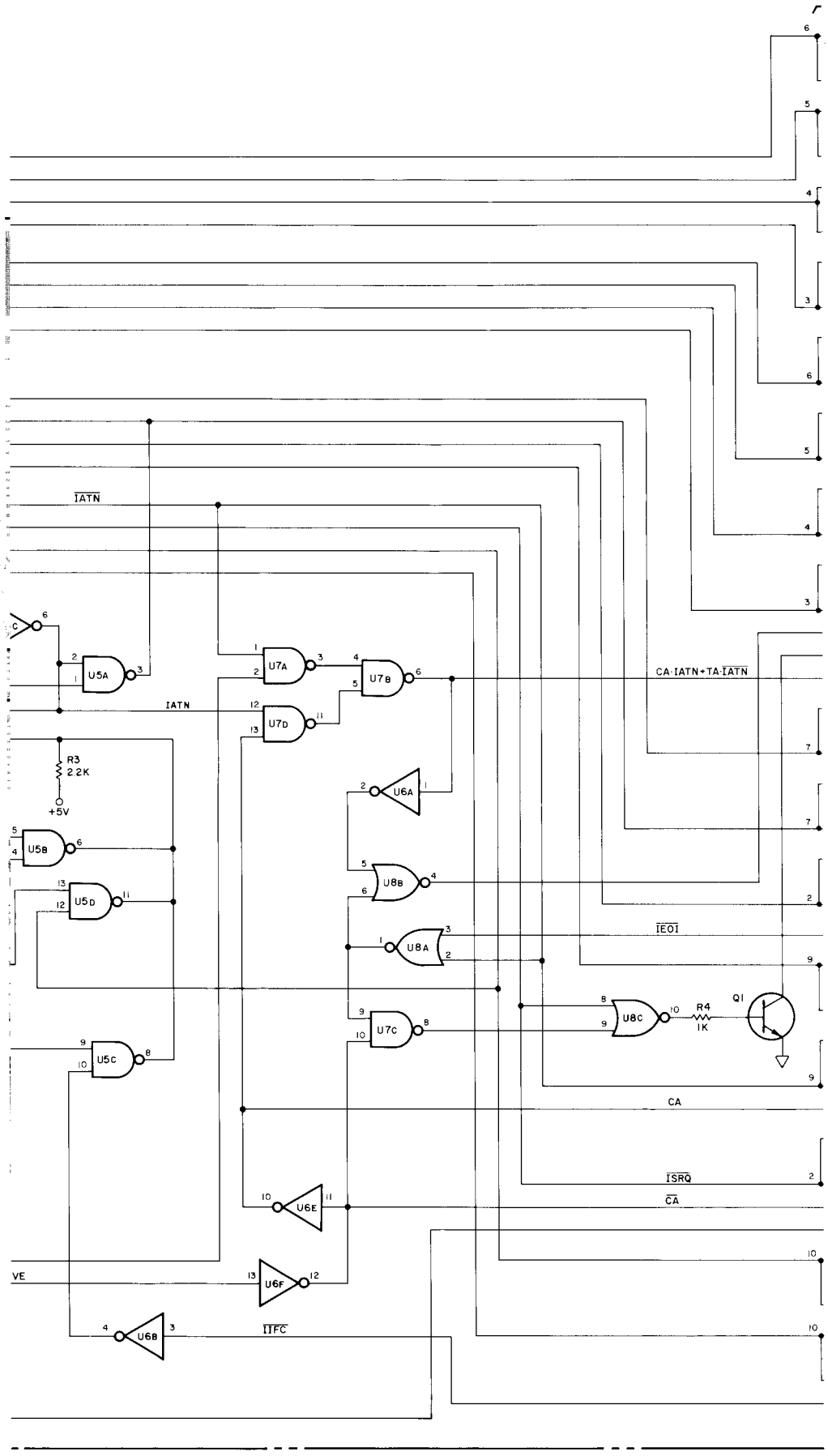
Figure 3-8. μC Control Registers

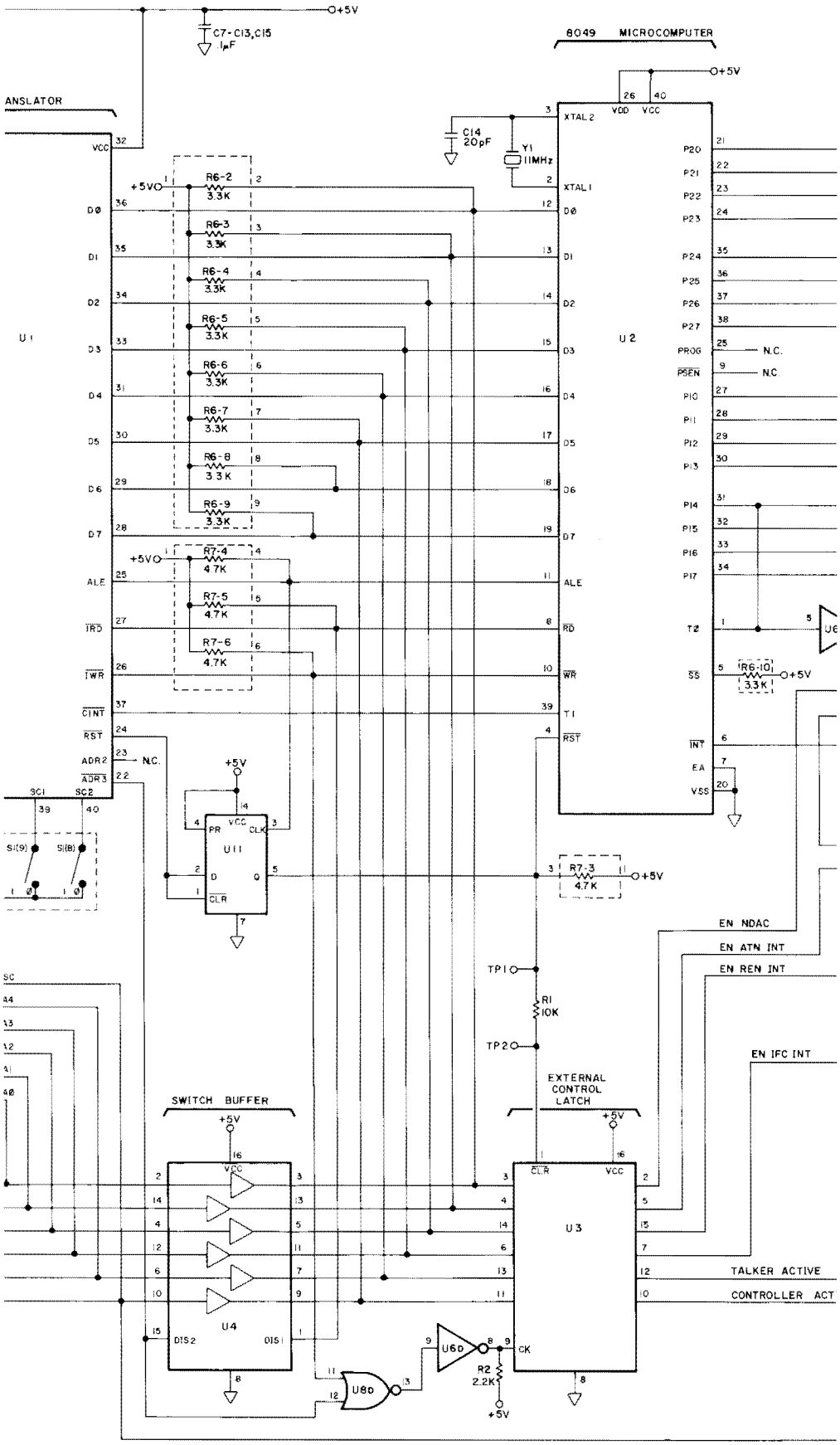
Table 3-3. Replaceable Parts List

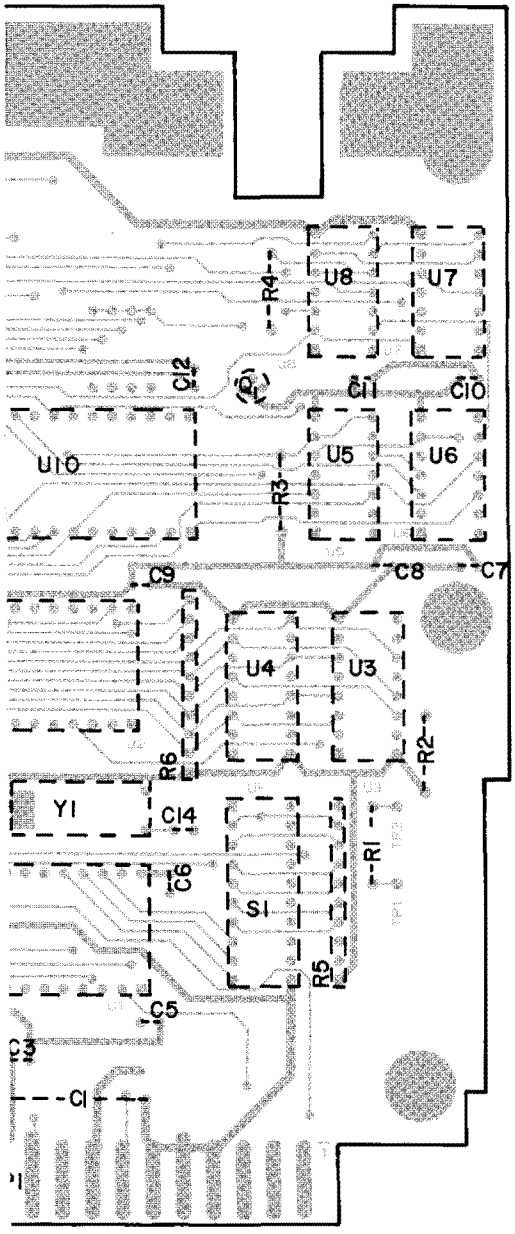
Reference Designator	HP Part No.	TQ	Description
A1	82937-60901	1	PC Assembly
C1, C2	0180-0228	2	C-F: 22μF, 15V
C3-C13	0160-0576	12	C-F: 0.1μF, 50V
C14	0160-4767	1	C-F: 20pF, 200V
C15	0160-0576	0	C-F: 0.1μF, 50V
J1	1251-5266	1	Connector: 24 Pin
MP1	0340-0883	1	Transistor Insulator
Q1	1854-0019	1	Transistor: NPN, Si
R1	0683-1035	1	R-F: 10kΩ, 5%, .25W
R2, R3	0683-2225	2	R-F: 2.2kΩ, 5%, .25W
R4	0683-1025	1	R-F: 1kΩ, 5%, .25W
R5, R6	1810-0278	2	Resistor Network: 3.3kΩ, 2%, 1.25W
R7	1810-0367	1	Resistor Network: 4.7kΩ, 2%, 1.25W
S1	3101-0491	1	Switch: 10 Segment SPDT
U1	1MB5-0101	1	IC: Translator
U2	1820-2437	1	IC: 8049 Microcomputer
U3	1820-1466	1	IC: 74C174, Hex D Flip-Flop
U4	1820-1402	1	IC: 80C95, Hex Buffer
U5	1820-1198	1	IC: 74LS03, Quad 2-Input NAND
U6	1820-1416	1	IC: 74LS14, Hex Schmitt Trigger Inverter
U7	1820-1197	1	IC: 74LS00, Quad 2-Input NAND
U8	1820-1144	1	IC: 74LS02, Quad 2-Input NOR
U9, U10	1820-2424	2	IC: MC3447, Bi-directional Bus Transceivers
U11	1820-1112	1	IC: 74LS74, Quad D Flip-Flop
W1	8150-3773	1	Wire Jumper
Y1	0410-1222	1	11 MHz Crystal
	82937-60902	1	Case
	82937-60004	1	Interface Cable
	0590-0199	2	Hex Nut with Lock Washer
	1400-1063	1	Top Cable Clamp
	1400-1064	1	Bottom Cable Clamp
	2200-0143	6	Screws: 4-40 Machine
	0363-0174	1	Ground Contact

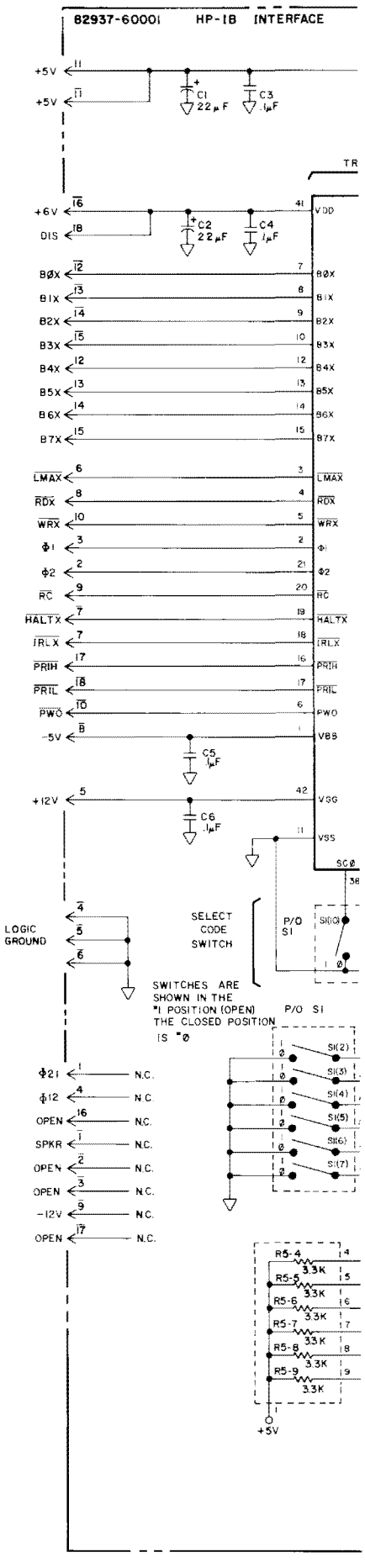

BI-DIRECTIONAL
BUS TRANCEIVERS
E1 W1 E2
J1
P1
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
GND(6)
GND(7)
GND(8)
GND(9)
GND(10)
GND(11)
LOGIC
U9-13
U10-13
NRFD
NDAC
DAV
SHIELD
EOI
ATN
SRQ
REN
IFC
U9E
U9D
U9C
U9B
U10E
U10D
U10C
U10B
U9F
U10F
U9A
U9G
U10G
U10A
U9H
U10H


GROUND
ATN
SRQ
IFC
NDAC
NRFD
DAV
REN
DIO8
DIO7
DIO6
DIO5
SHIELD
ATN
SRQ
IFC
NDAC
NRFD
DAV
EOI
DIO4
DIO3
DIO2
DIO1
ground on
interface card
B 51000


IATN
IATN
R3
2.2K
+5V
U5A
U5B
U5C
U5D
U7A
U7B
U7C
U7D
U6A
U6B
U6E
U6F
U8A
U8B
U8C
R4
1K
Q1
CA·IATN+TA·IATN
IEOI
CA
ISRQ
CA
VE
IIFC


8049 MICROCOMPUTER
ANSLATOR
+5V
C7-C13,C15
.1μF
U1
U2
VCC
VDD
XTAL2
XTAL1
C14
20pF
Y1
11MHz
R6-2
3.3K
R6-3
3.3K
R6-4
3.3K
R6-5
3.3K
R6-6
3.3K
R6-7
3.3K
R6-8
3.3K
R6-9
3.3K
R7-4
4.7K
R7-5
4.7K
R7-6
4.7K
R7-3
4.7K
R6-10
3.3K
D0
D1
D2
D3
D4
D5
D6
D7
ALE
IRD
IWR
CINT
RST
ADR2
ADR3
SC1
SC2
N.C.
P20
P21
P22
P23
P24
P25
P26
P27
PROG
PSEN
P10
P11
P12
P13
P14
P15
P16
P17
T0
T1
RD
WR
SS
INT
EA
VSS
U11
PR
CLR
CLK
D
Q
TP1
TP2
R1
10K
EN NDAC
EN ATN INT
EN REN INT
EN IFC INT
SWITCH BUFFER
EXTERNAL CONTROL LATCH
U3
U4
U5D
U5C
R2
2.2K
DIS2
DIS1
CK
TALKER ACTIVE
CONTROLLER ACT


U8
U7
U5
U6
U4
U3
U10
R4
R3
R6
R2
R1
R5
C12
C11
C10
C9
C8
C7
C14
C6
C5
C4
C3
C2
C1
Y1
S1


82937-60001 HP-IB INTERFACE
+5V
+5V
C1 22μF
C3 .1μF
TR
+6V
DIS
C2 22μF
C4 .1μF
VDD
BØX
B1X
B2X
B3X
B4X
B5X
B6X
B7X
LMAX
RDX
WRX
Φ1
Φ2
RC
HALTX
IRLX
PRIH
PRIL
PWO
-5V
C5 .1μF
+12V
C6 .1μF
VGG
VSS
SCØ
LOGIC GROUND
SELECT CODE SWITCH
P/O S1
SI(0)
SWITCHES ARE SHOWN IN THE "1 POSITION (OPEN) THE CLOSED POSITION IS "Ø
P/O S1
SI(2)
SI(3)
SI(4)
SI(5)
SI(6)
SI(7)
Φ21 N.C.
Φ12 N.C.
OPEN N.C.
SPKR N.C.
OPEN N.C.
OPEN N.C.
-12V N.C.
OPEN N.C.
R5-4 3.3K
R5-5 3.3K
R5-6 3.3K
R5-7 3.3K
R5-8 3.3K
R5-9 3.3K
+5V

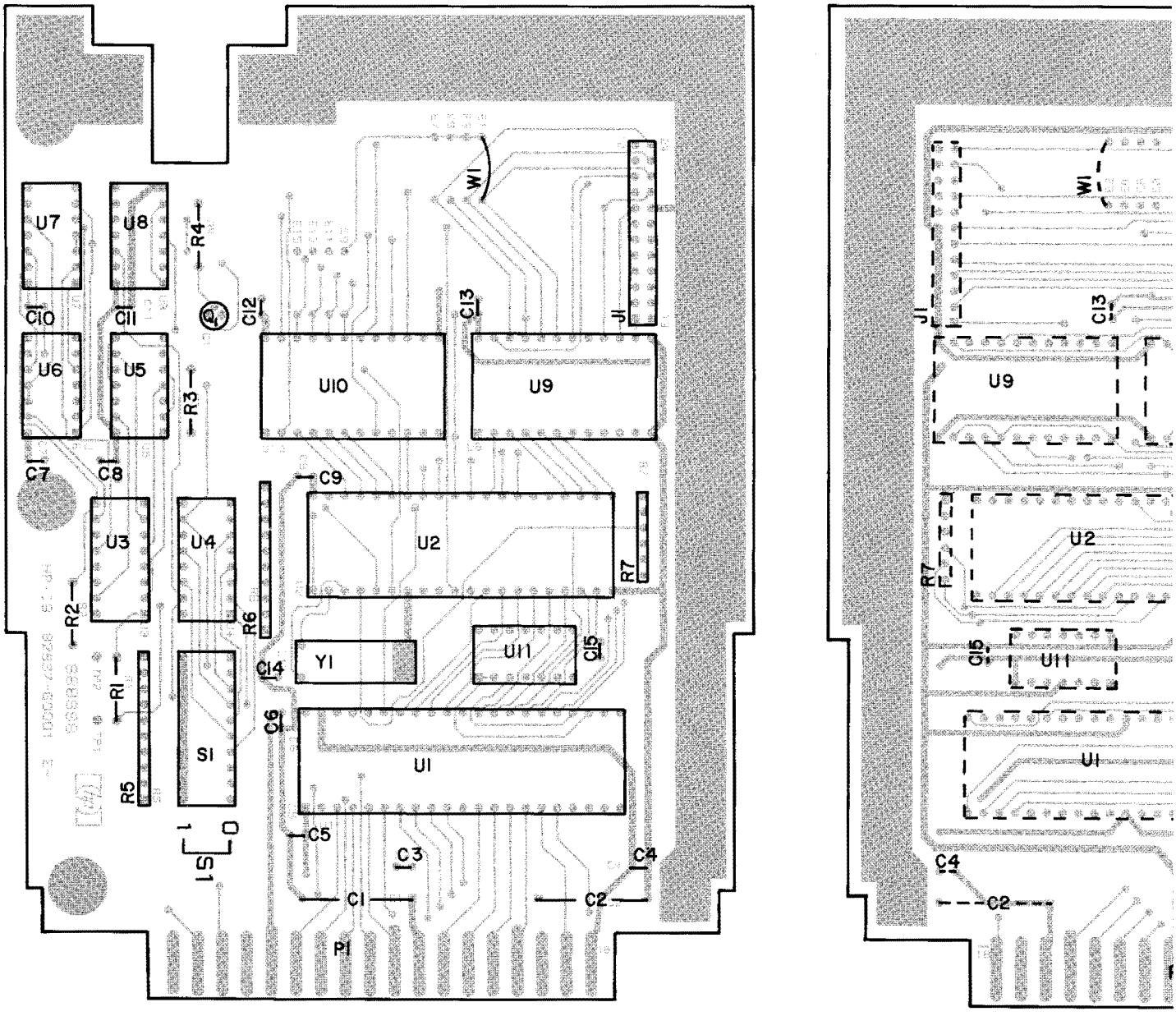


Figure 3-9. Schematic Diagram

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