

## HP85 Disk Project v1.0 by ©Mike Gore Feb 2015

### Schematics and Pin-out information for HP85 Disk Project

PIN	CPU Function	Role	CPU to component connection notes	GIPIB Name	GIPIB Pin
1	PB0	GIPIB	<b>120R to 5 GIPIB pin, GIPIB pin 10K to VCC</b> 2 HC32 Parallel Poll Circuit	EOI	5
2	PB1		<b>120R to 6 GIPIB pin, GIPIB pin 10K to VCC</b>	DAV	6
3	PB2	PP	12 RCLK HC595 Parallel Poll Circuit Latch		
4	PB3	/CS	/CS 1 Micro SD		
5	PB4(SS SPI)	NC			
6	PB5(MOSI SPI)	SPI	1K to 3 'MOSI Micro SD 4 ISP 14 SER HC595 Parallel Poll Circuit		
7	PB6(MISO SPI)	SPI	1K to 4 'MISO Micro SD 1 ISP		
8	PB7(SCK SPI))	SPI	1K to 2 'SCK Micro SD 11 SRCLK HC595 Parallel Poll Circuit 3 ISP		
9	/RESET		1K to VCC 5 ISP Reset button		
10	VCC	5V	4 VCC 5V FT232RL 5 VCC Micro SD 2 VCC ISP 5 VCC DS1307 RTC BOARD 16 VCC HC 595 Parallel Poll Circuit 14 VCC HC 32 Parallel Poll Circuit 14 VCC HC 05 Parallel Poll Circuit 0.1uf GND 22uf GND		
11	GND	GND	6 GND FT232RL 6 GND Micro SD 6 ISP 4 GND DS1307 RTC BOARD 8 GND HC 595 7 GND HC 32 7 GND HC 05 <b>12,18,19,20,21,22,23,24 GIPIB GND</b>	<b>GND</b>	<b>12 18 19 20 21 22 23 24</b>
12	XTAL2		20MHZ 22pf GND		
13	XTAL1		20MHZ 22pf GND		
14	PD0 (RXD0)	RS232	3 TXD FT232RL		
15	PD1 (TXD0)	RS232	2 RXD FT232RL		
16	PD2	GIPIB	<b>120R to 7 GIPIB pin, GIPIB pin 10K to VCC</b>	NRFD	7

<b>17</b>	PD3	GPIB	<b>120R to 8 GPIB pin, GPIB pin 10K to VCC</b>	<b>NDAC</b>	<b>8</b>
<b>18</b>	PD4	GPIB	<b>120R to 9 GPIB pin, GPIB pin 10K to VCC</b> 10 /SRCLR HC595 Parallel Poll Circuit	<b>IFC</b>	<b>9</b>
<b>19</b>	PD5	GPIB	<b>120R to 10 GPIB pin, GPIB pin 10K to VCC</b>	<b>SRQ</b>	<b>10</b>
<b>20</b>	PD6	GPIB	<b>120R to 11 GPIB pin, GPIB pin 10K to VCC</b> 3 HC32 Parallel Poll Circuit	<b>ATN</b>	<b>11</b>
<b>21</b>	PD7	GPIB	<b>120R to 17 GPIB pin, GPIB pin 10K to VCC</b>	<b>REN</b>	<b>17</b>
<b>22</b>	PC0(SCL)	<b>I2C</b>	1 SDA DS1307 RTC BOARD		
<b>23</b>	PC1(SDA)	<b>I2C</b>	2 SCL DS1307 RTC BOARD		
<b>24</b>	PC2(TCK JTAG)	NC			
<b>25</b>	PC3(TMS JTAG)	NC			
<b>26</b>	PC4(TD0 JTAG)	NC			
<b>27</b>	PC5(TDI JTAG)	NC			
<b>28</b>	PC6(TOSC1)	<b>NC</b>			
<b>29</b>	PC7(TOSC2)	<b>NC</b>			
<b>30</b>	AVCC		<b>VCC 10</b>		
<b>31</b>	GND		<b>GND 11</b>		
<b>32</b>	AREF	0.1uf	0.1uf to GND 11		
<b>33</b>	PA7	GPIB	<b>120R to 16 GPIB pin, GPIB pin 10K to VCC</b>	<b>D8</b>	<b>16</b>
<b>34</b>	PA6	GPIB	<b>120R to 15 GPIB pin, GPIB pin 10K to VCC</b>	<b>D7</b>	<b>15</b>
<b>35</b>	PA5	GPIB	<b>120R to 14 GPIB pin, GPIB pin 10K to VCC</b>	<b>D6</b>	<b>14</b>
<b>36</b>	PA4	GPIB	<b>120R to 13 GPIB pin, GPIB pin 10K to VCC</b>	<b>D5</b>	<b>13</b>
<b>37</b>	PA3	GPIB	<b>120R to 4 GPIB pin, GPIB pin 10K to VCC</b>	<b>D4</b>	<b>4</b>
<b>38</b>	PA2	GPIB	<b>120R to 3 GPIB pin, GPIB pin 10K to VCC</b>	<b>D3</b>	<b>3</b>
<b>39</b>	PA1	GPIB	<b>120R to 2 GPIB pin, GPIB pin 10K to VCC</b>	<b>D2</b>	<b>2</b>
<b>40</b>	PA0	GPIB	<b>120R to 1 GPIB pin, GPIB pin 10K to VCC</b>	<b>D1</b>	<b>1</b>

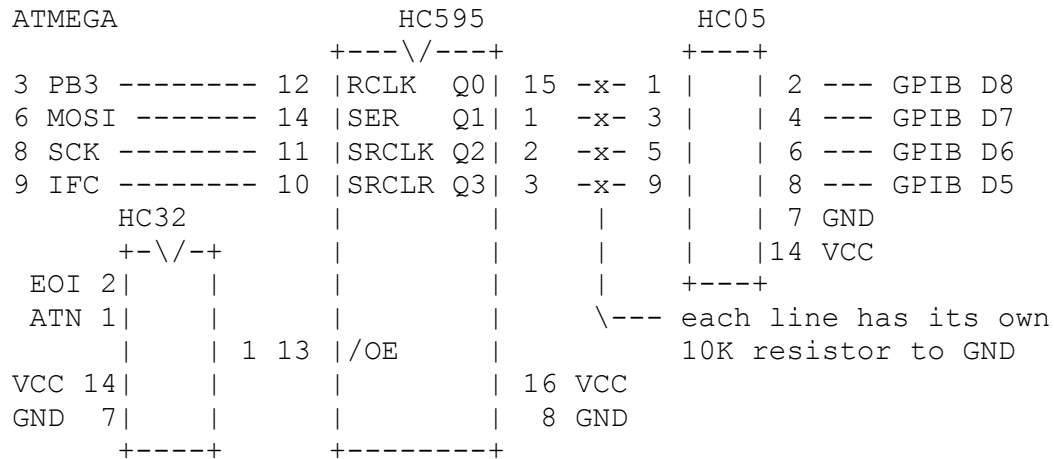
## AVR ATMEGA1284P pin assignments for HP85 Disk

- **GPIO:** Each GPIO pin (8 data and 8 control lines ) attach to CPU with a 120 ohm current limit resistor .
  - Each GPIO pin (8 data and 8 control lines ) have a 10K pull-up resistor to VCC.
- **ISP header:** MOSI,MISO,SCK,/Reset connects directly to ISP header
- **Micro SD Interface:** MOSI,MISO,SCK attach to CPU function via a 1k series resistor.
  - **Micro SD interface has level shifters and internal 5V to 3.3V regulator**
- **RS232 TTL:** connect to FTDI232 **USB** board which also provides **5V VCC** power to all circuits..
- **I2C:** SCL,SDA connect to optional DS1307 RTC board with each line having a 2k2 pull-up

ATMEGA1284P (and ATMEGA644P)									
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5	EOI	INT0	PB0	1		40	PA0	D1	1
6	DAV	INT1	PB1	2		39	PA1	D2	2
	PP	INT2	PB2	3		38	PA2	D3	3
SD	/CS	PWM	PB3	4		37	PA3	D4	4
	NC	PWM	PB4	5		36	PA4	D5	13
SD		MOSI	PB5	6		35	PA5	D6	14
SD		MISO	PB6	7		34	PA6	D7	15
SD		SCK	PB7	8		33	PA7	D8	16
10K	pullup		/RST	9		32	AREF	0.1uf	
	+5		VCC	10		31	GND	GND	
	GND		GND	11		30	AVCC	+5	
20MHZ			XTAL2	12		29	PC7	NC	
20MHZ			XTAL1	13		28	PC6	NC	
	RX	RX0	PD0	14		27	PC5	TDI	JTAG
	TX	TX0	PD1	15		26	PC4	TDO	JTAG
7	NRFD	RX1	PD2	16		25	PC3	TMS	JTAG
8	NDAC	TX1	PD3	17		24	PC2	TCK	JTAG
9	IFC	PWM	PD4	18		23	PC1	SDA	I2C
10	SRQ	PWM	PD5	19		22	PC0	SCL	I2C
11	ATN	PWM	PD6	20		21	PD7	PWM	REN 17
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## Parallel Poll Response circuit

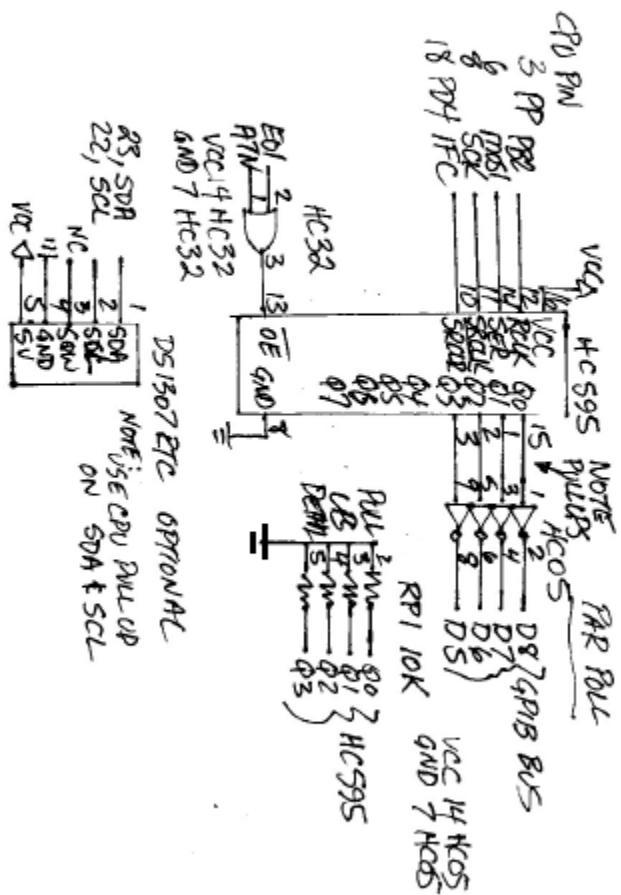
- Uses: Three chips 74HC05, 74HC32, 74HC595
- Parallel Poll Response must be less than 2 Microseconds therefore we use hardware to do it!



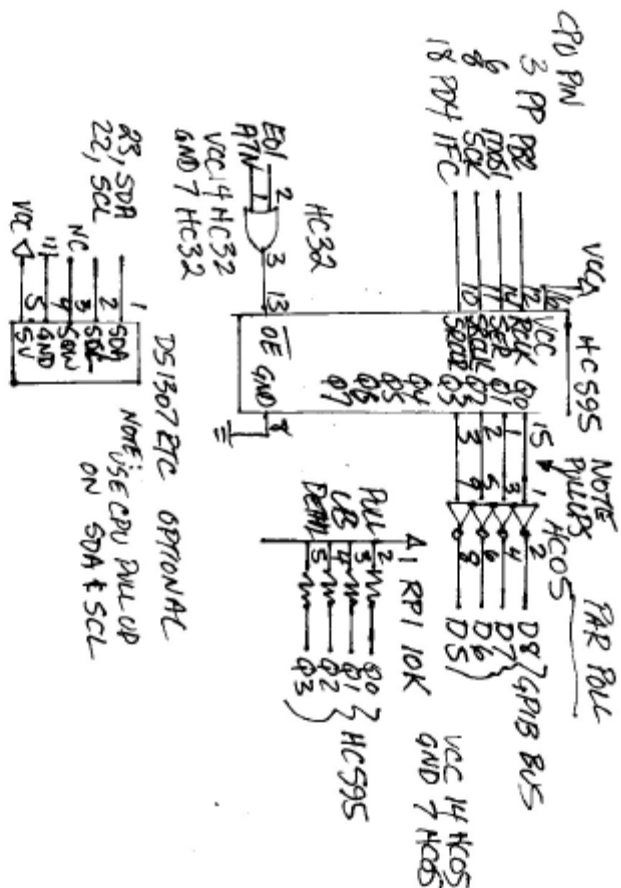
Notes: When both EOI and ATN are low the HC32 enables HC595 outputs

- If any HC595 output is high the GPIB bus bit will be pulled low
- IFC low resets the outputs low





v1.0 HP85 DISK MIKE GALE FEB2015



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