MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table Number	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION (SOLUTION)

TRIMESTER 2, 2022/2023

TSN1101 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

XX June 2023
9.00 am – 11.00 am
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 10 pages including a cover page with 4 Questions only.

2. Attempt **ALL** the **FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in this booklet.

QUESTION 1

a) Convert the Binary code 10110.0011111_2 into the following number systems: (Show the steps involved).

i) Octal
ii) Hexadecimal
iii) Decimal

[1 ×3 = 3 marks]

Binary code = 10 110 . 001 111 1_2

010	110 .	001	111	100

i) Octal = 2 6 . 17 4_8

0001	0110.	0011	1110

ii) Hexadecimal = 1 6 . $3E_{16}$

iii) $10110_2 = 16+4+2 = 22$,
$0.0011111_2 = 0.125 + 0.0625 + 0.03125 + 0.015625 + 0.0078125 =$
Decimal = 22.2421875_{10}

b) Given Multiplicand (M) = **- 4_{10}** and Multiplier (Q) = **3_{10}**

i) Convert the M and Q into two 4-bit two's complement binary numbers. [1 mark]
ii) Perform the multiplication of two 4-bit two's complement binary numbers from the answers obtained from i) by applying Booth's algorithm (refer flowchart from appendix). Show all the steps involved. [2 marks]
iii) convert the product obtained from ii) into decimal value. [1 mark]

4-bit two's complement binary numbers of Multiplicand (M) = **- 4_{10}** = 1100_2
4-bit two's complement binary numbers of Multiplier (Q) = 3_{10} = **0011_2**

[0.5 mark x 2 = 1 mark]

Continued …

A	Q	Q_{-1}	M		
0000	0011	0	1100	Initial	
0100	0011	0		A=A-M	
0010	0001	1		SHIFT RIGHT	1 st CYCLE
0001	0000	1		SHIFT RIGHT	2^{ND} CYCLE
1101	0000	1		A=A+M	
1110	1000	0		SHIFT RIGHT	3^{RD} CYCLE
1111	0100	0		SHIFT RIGHT	4^{TH} CYCLE

Each correct cycle = 0.5 mark, total = 0.5 x 4 = 2 marks

Product = $\boldsymbol{1111\ 0100_2}$ [1 mark]

= - 128+ 64+32+16+ 4 = -12_{10} [1 mark]

c) Change the function W from Product of Sums (POS) form to Sum of Products (SOP). (Show the steps involved).

$$W = (A + B + C)(\bar{A} + B + C)(A + \bar{B} + \bar{C})(\bar{A} + \bar{B})$$

[3 marks]

$$(\bar{A} + \bar{B}) = (\bar{A} + \bar{B} + \bar{C})(\bar{A} + \bar{B} + C)$$

A	B	C	W	POS	SOP
0	0	0	0	A+B+C	
0	0	1	1		A'B'C
0	1	0	1		A'BC'
0	1	1	0	A+B'+C'	
1	0	0	0	A'+B+C	
1	0	1	1		AB'C
1	1	0	0	A'+B'+C	
1	1	1	0	A'+B'+C'	

[truth table or other method to find the SOP, 2 marks]

$W = \bar{A}\,\bar{B}\,C + \bar{A}\,B\,\bar{C} + A\,\bar{B}\,C$ **[1 mark for SOP)**

Continued …

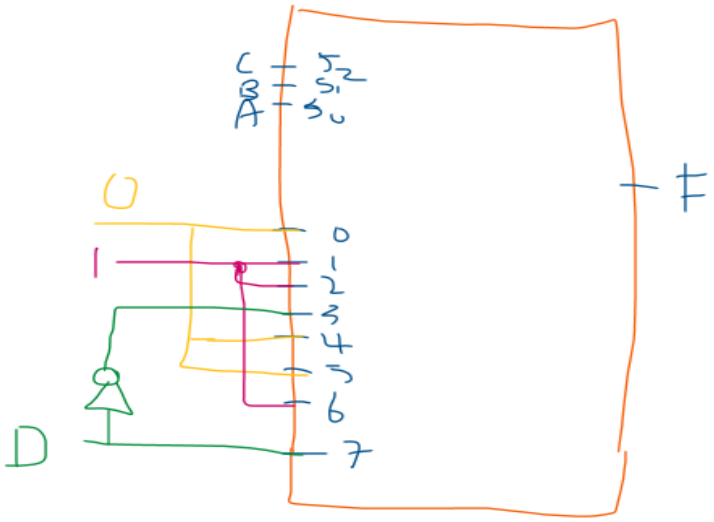
QUESTION 2

a) Given Boolean function F (A, B, C, D) = ∑ m (2, 3, 4, 5, 6, 12,13,15). You are required to design a circuit implementation of the function using 8x1 Multiplexer (MUX).

i) Provide the related truth table [2 marks]
ii) Implement the logic circuit by using an 8×1 MUX and the needed logic gates [3 marks]

	A	B	C	D	F	
0	0	0	0	0	0	F = 0
1	0	0	0	1	0	
2	0	0	1	0	1	F = 1
3	0	0	1	1	1	
4	0	1	0	0	1	F = 1
5	0	1	0	1	1	
6	0	1	1	0	1	F = D’
7	0	1	1	1	0	
8	1	0	0	0	0	F = 0
9	1	0	0	1	0	
10	1	0	1	0	0	F = 0
11	1	0	1	1	0	
12	1	1	0	0	1	F= 1
13	1	1	0	1	1	
14	1	1	1	0	0	F = D
15	1	1	1	1	1	

[0.125 X 16 = 2 marks]



[3 marks]

Continued …

b) Design a synchronous counter that has two negative-edged triggered **T flip-flops** with three inputs **X, Y and Z** (with order accordingly). Implement the counter based on the two conditions listed below:

- If X is 1, Y and Z will count up based on 00_2, 01_2, 10_2, 11_2 and repeat.
- If X is 0, Y and Z will count down based 11_2,10_2,01_2, 00_2 and repeat.

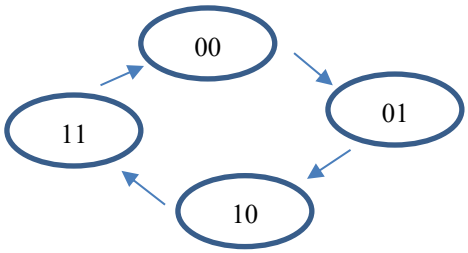
Your design should include:

(i) State Transition Diagram showing all possible states [1 mark]

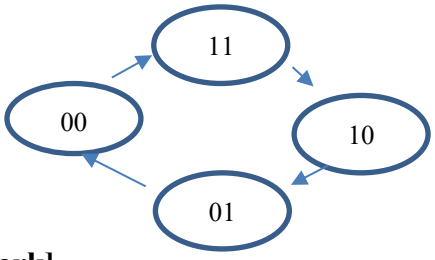
(ii) By referring to Excitation Table for T flip flop (provided in Appendix), construct the State Table. [2 marks]

(iii) Perform simplification for each T flip-flop input by using Karnaugh Map. [2 marks]

If X = 1,



If X= 0



[0.5 x2 = 1 mark]

State Table **[2 marks]**

Present			**Next**		**Inputs**	
X	**Y**	**Z**	**Y**	**Z**	**T_Y**	**Tz**
0	**0**	**0**	**1**	**1**	**1**	**1**
0	**0**	**1**	**0**	**0**	**0**	**1**
0	**1**	**0**	**0**	**1**	**1**	**1**
0	**1**	**1**	**1**	**0**	**0**	**1**
1	**0**	**0**	**0**	**1**	**0**	**1**
1	**0**	**1**	**1**	**0**	**1**	**1**
1	**1**	**0**	**1**	**1**	**0**	**1**
1	**1**	**1**	**0**	**0**	**1**	**1**

Continued …

X/YZ	00	01	11	10
0	1	0	0	1
1	0	1	1	0

T_Y == X'Z' + XZ
= X XNOR Z

[1 mark]

X/YZ	00	01	11	10
0	1	1	1	1
1	1	1	1	1

Tz= 1
[1 mark]

QUESTION 3

a) A processor often contains TWO types of registers. Name the TWO and provide one example for each type. [2 Marks]

User-Visible register
- General purpose/data/address/condition flags

Control and Status register
- IR/MAR/MBR

[1 X 2 = 2 marks]

b) Assume that a processor employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR). List the symbolic sequence of micro-operations of ARM instruction below according to the time sequence.

LDR R1, [R2]

[3 Marks]

t1 : MAR ← (IR(R2))
t2 : MBR <- Memory
t3 : R1 <- (MBR)

[1x3 = 3 Marks]

Continued …

c) A hypothetical computer system has a hierarchical memory architecture consisting of cache memory of size 8 KB with a block size of 8 bytes, and 16GB main memory. Identify the address structures for the following cache memory mapping functions. Show all the steps. [5 marks]

i) Direct Mapping (No. of bits required for Tag, Line and Word fields)
ii) Four-way Set Associative Mapping (No. of bits required for Tag, Set, and Word fields)
iii) Associative Mapping (No. of bits required for Tag, and Word fields)

Direct Mapping

Cache = 8KB
Block = 8B
Address length = 16 GB = 2^{34} (34 bits) [1 mark]

Total Line = 8K/8 = 2^{10}
Word = 8B = 2^4

Tag = 20 ; Line = 10 ; Word = 4 [0.5 * 3 = 1.5 marks]

Four-way Set Associative Mapping

Total Line = 8K/8 = 2^{10}
Set = Total Line / 4 = 1024/4 = 256 = 2^8
Word = 8B = 2^4
Tag = 22 ; Line = 8 ; Word = 4 [0.5 * 3 = 1.5 marks]

Associative Mapping

Tag = 30 ; Word = 4 [0.5 * 2 = 1 mark]

Continued …

QUESTION 4

a) Given the following instructions and a zero-address machine, write a program to compute.

$$Z = (A - B \times C) / (B + C).$$

Instructions: PUSH
POP
ADD
SUB
MUL
DIV

[4 marks]

```
PUSH A
PUSH B
PUSH C
MUL
SUB

PUSH B
PUSH C
ADD

DIV
POP Z
```

[4 marks]

b) There are various types of parallel processor organizations in the market. Explain the advantages of running processes in distributed memory particularly cluster.

[2 Marks]

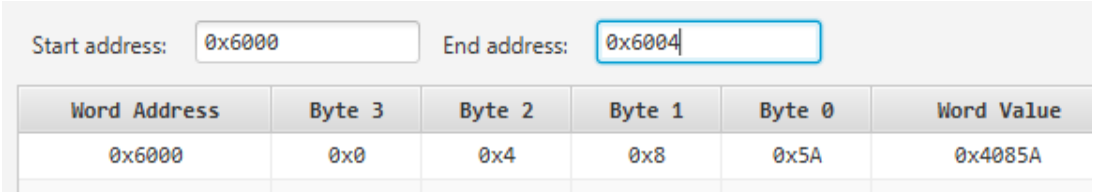
Over the long run, the advantages of the cluster approach are likely to result in clusters dominating the high-performance server market. Clusters are far superior in terms of incremental and absolute scalability. Clusters are also superior in terms of availability because all components of the system can readily be made highly redundant.

Continued …

c) Write ARM instructions to perform the below arithmetic. Store the result of each partial arithmetic accordingly into memory addresses of 0x6000, 0x6001, and 0x6002 respectively.

See below diagram for the expected output.

((54+36)-82) / 2

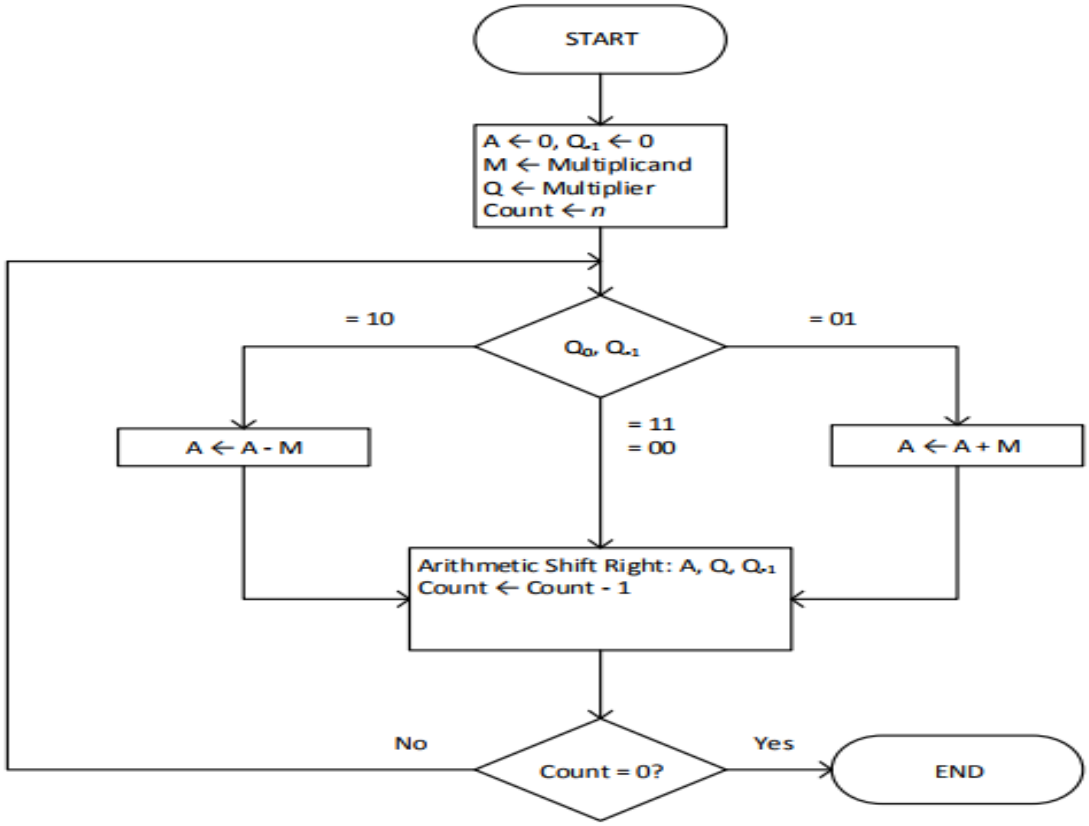


[4 marks]

```
MOV     R0, #0X6000
MOV     R1, #54
MOV     R2, #36

ADD     R3, R1,R2
STRB    R3, [R0], #1

MOV     R4, #82
SUB     R5, R3,R4
STRB    R5, [R0], #1

LSR     R6,R5,#1
STRB    R6, [R0], #1
```

Continued …

Appendix



JK Excitation table

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D Excitation table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

T Excitation table

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

End of paper