MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table Number	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER MARCH 2024 (TERM ID 2410)

CSN6114 –COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

XX JULY 2024
9.00 am – 11.00 am
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 14 pages including a cover page with 5 Questions only.

2. Attempt **ALL** the **FIVE** questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please print all your answers in this booklet.

QUESTION 1

a) Perform the following arithmetic, and write the necessary outputs [1x3= 3 marks]

i) 5A.04H – 3F. 2CH

ii) $35.42_7 + 6.26_7$

iii) $1000.001_2 - 111.11_2$

[1 ×3 = 3 marks]

Solution

i) 1A.D8

ii) 45.01

iii) 0.011

b) Design a combinational logic circuit in detecting odd numbers. The odd numbers detector is one that produces HIGH output when the decimal equivalent binary input is odd, else it produces LOW output. Do the following.

[2+1+1 marks]

i) Construct the truth table

ii) Simplify the Boolean expression into SOP using Karnaugh-Map

iii) Draw the 3-input odd number detector based on (ii) using only NAND.

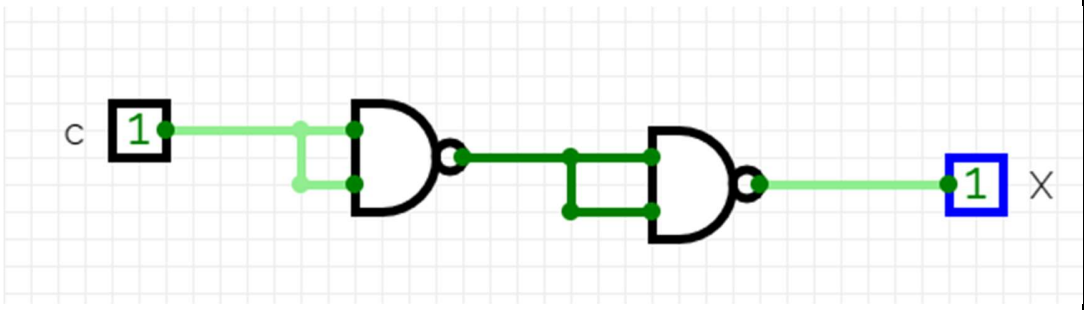
Continued …

Solution

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

	C’	C
A’B’	0	1
A’B	0	1
AB	0	1
AB’	0	1

X = C



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c) Change the function W from Product of Sums (POS) form to Sum of Products (SOP) following the steps below:

i) Construct a truth table

ii) Obtain the SOP from the truth table

$$W = (A + B + C)(\bar{A} + B + C)(A + \bar{B} + \bar{C})(\bar{A} + \bar{B})$$

[2+1+1 Marks]

i)

A	B	C	W
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

ii) W= A’B’C+A’BC’+AB’C

Continued …

QUESTION 2

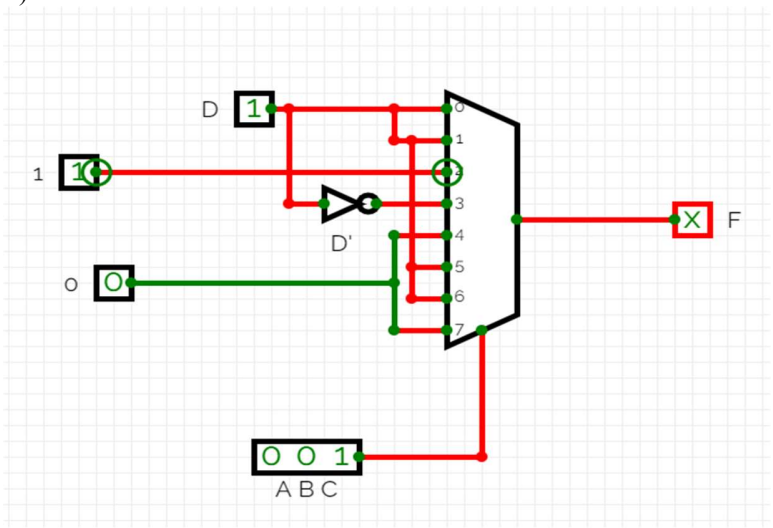
a) Given Boolean function F (A, B, C, D) = ∑ m (1, 3, 4, 5, 6, 11,13). You are required to design a circuit implementation of the function using 8x1 Multiplexer (MUX).

i) Construct the related truth table [2 Marks]
ii) Implement the logic circuit by using an 8×1 MUX and the needed logic gates [2 Marks]

i).

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1 F=D
0	0	1	0	0
0	0	1	1	1 F=D
0	1	0	0	1
0	1	0	1	1 F=1
0	1	1	0	1
0	1	1	1	0 F=D’
1	0	0	0	0
1	0	0	1	0 F=0
1	0	1	0	0
1	0	1	1	1 F=D
1	1	0	0	0
1	1	0	1	1 F=D
1	1	1	0	0
1	1	1	1	0 F=0

ii).



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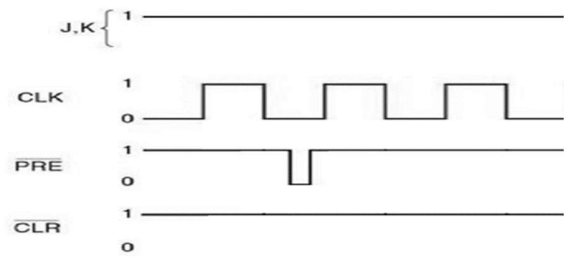
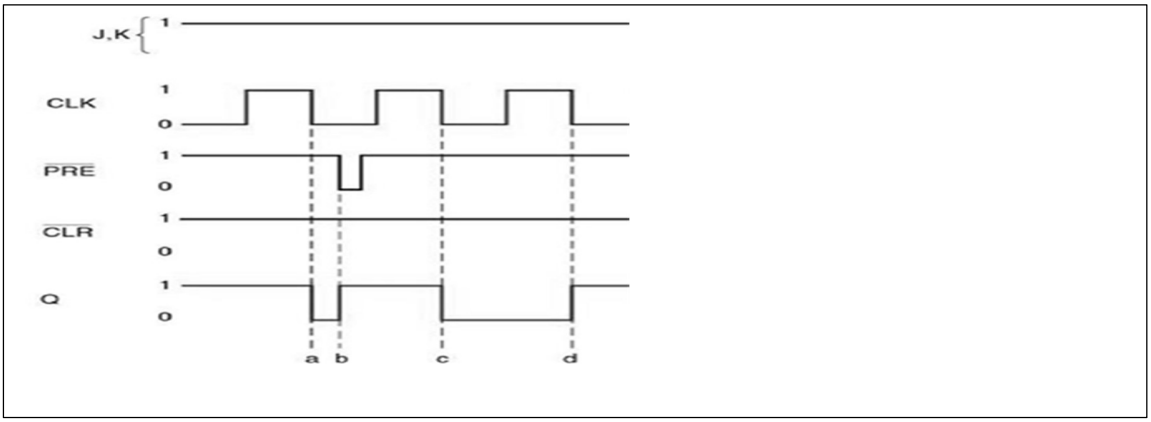
b) Draw the output (Q) of these Asynchronous inputs negative going transition JK Flip-Flop by complete the Q for the timing diagram below: [1 Mark]





c)Design a synchronous counter that has two negative-edged triggered **D flip-flops** with three inputs **X, Y and Z** (with order accordingly). Implement the counter based on the two conditions listed below:

- If X is 1, Y and Z will count up based on 00_2, 01_2, 10_2, 11_2 and repeat.
- If X is 0, Y and Z will count down based 11_2,10_2,01_2, 00_2 and repeat.

Your design should include:

(i) By referring to Excitation Table for D flip flop (provided in Appendix), construct the State Table. [2 marks]

(ii) Perform simplification for each D flip-flop input by using Karnaugh Map. [2 marks]

(iii) Construct the counter using D flip-flops. [1 mark]

Continued …

i.

X	Y	Z	Y	Z	Dy	Dz
0	0	0	1	1	1	1
0	0	1	0	0	0	0
0	1	0	0	1	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	1	1	1	1
1	1	1	0	0	0	0

ii.

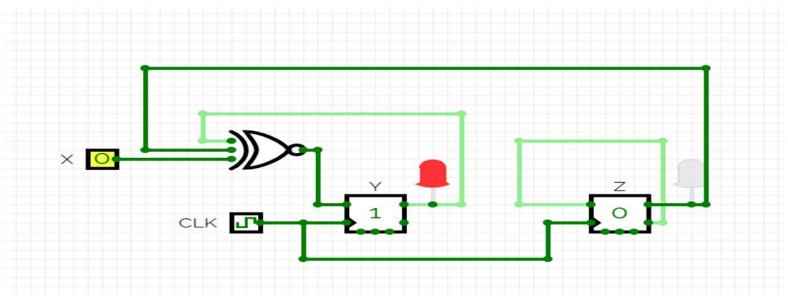
XY/Z	0	1
00	1	0
01	0	1
11	1	0
10	0	1

Dy= X'Y'Z'+ XYZ'+ X'YZ+ XY'Z
=X'(Y'Z'+YZ) + X(YZ'+Y'Z)
=X'(Y@X)' + X(Y@Z)
=(X @Y@Z)'

XY/Z	0	1
00	1	0
01	1	0
11	1	0
10	1	0

Dz= Z'

iii.



QUESTION 3

a) Assume the usage of 8-stage instruction pipelining with a program consisting of 10 instructions. The clock frequency is 40 KHz. Answer the following with showing the proper steps:

i. Identify the time needed to execute each stage of all instructions.
ii. Assume the usage of ideal pipelining without any hazards, what is the time needed to complete all the 10 instructions.
iii. If pipelining is not used, what is the time required to execute these 10 instructions.
iv. Identify the speed up factor, K for the instruction pipeline as compared to without pipeline.

[4 Marks]

i) Period = 1/Freq = $1/(40*10^3)$ = 0.000025 second or 25 microsecond

For 10 instructions.

ii) T = [8+ (10-1)]* 25 microsecond = 17*25 microsecond = 425 microsecond

iii) T = 10*8*25 microsecond = 2000 microsecond

iv) K = 2000 / 425 = 4.7059

b) Assume that a processor employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR). List the symbolic sequence of micro-operations of ARM instruction below according to the time sequence.

LDR R1, [R2]

[3 Marks]

Continued …

t1 : MAR ← (IR(R2))
t2 : MBR <- Memory
t3 : R1 <- (MBR)

c) Given the following registers and a two-address machine, write a program to compute T

$$\mathbf{T = (K \times M - R) / (S + L).}$$

Available instructions are given below:
a. Temporary Registers (in order): A, B, C, D and E
b. K, M, R, S and L are Data
c. Instructions: MOV R1; #DATA; MOV R1, R2; ADD R1, R2; SUB R1, R2; MUL R1,R2 and DIV R1,R2

Store the final result in Register T. (Hint: Instruction format = opcode destination, source) [3 marks]

```
MOV   A, #K
MOV   B, #M
MUL   A, B
MOV   C, #R
SUB   A,C
MOV D, #S
MOV E, #L
ADD   D, E
DIV   A, D
MOV T, A
```

Continued …

QUESTION 4

a) Given Multiplicand (M) = **- 4_{10}** and Multiplier (Q) = **3_{10}**

i) Convert the M and Q into two 4-bit two's complement binary numbers. [1 mark]
ii) Perform the multiplication of two 4-bit two's complement binary numbers from the answers obtained from i) by applying Booth's algorithm (refer flowchart from appendix). Show all the steps involved. [2 marks]
iii) convert the product obtained from ii) into decimal value. [1 mark]

4-bit two's complement binary numbers of Multiplicand (M) = **- 4_{10}** = 1100_2
4-bit two's complement binary numbers of Multiplier (Q) = 3_{10} = **0011_2**

[0.5 mark x 2 = 1 mark]

A	Q	Q_{-1}	M		
0000	0011	0	1100	Initial	
0100	0011	0		A=A-M	
0010	0001	1		SHIFT RIGHT	1 st CYCLE
0001	0000	1		SHIFT RIGHT	2^{ND} CYCLE
1101	0000	1		A=A+M	
1110	1000	0		SHIFT RIGHT	3^{RD} CYCLE
1111	0100	0		SHIFT RIGHT	4^{TH} CYCLE

Each correct cycle = 0.5 mark, total = 0.5 x 4 = 2 marks

Product = ***$1111\ 0100_2$*** [1 mark]

= - 128+ 64+32+16+ 4 = -12_{10} [1 mark]

Continued …

b) Given the following register and memory values, what values do the following ARM instructions load into the destination register? Assume instructions are in sequence.

Address 1000 contains 0x6E
Address 1020 contains 0x42
Address 2030 contains 0x5B
R0 contains 0x0020
R1 contains 0x0030
R2 contains 0x1000
R3 contains 0x0090

i) MOV R0, #0x2A
ii) ADD R0, R1, R3
iii) LDR R0, [R2, #0x20]!
iv) LDR R0, [R2]

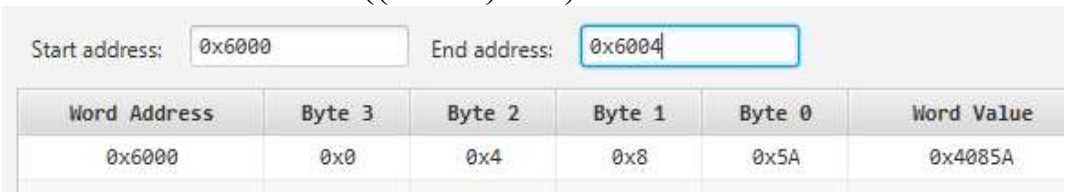
[2 Marks]

i) 0x2A
ii) 0x00C0
iii) 0x42
iv) 0x42
[0.5 x 4 = 2 Marks]

c) Write ARM instructions to perform the below arithmetic. Store the result of each partial arithmetic accordingly into memory addresses of 0x6000, 0x6001, and 0x6002 respectively.

See below diagram for the expected output.

((54-36)+82) / 2



[4 Marks]

Continued …

```
MOV         R0, #0X6000
MOV         R1, #54
MOV         R2, #36

ADD         R3, R1,R2
STRB        R3, [R0], #1

MOV         R4, #82
SUB         R5, R3,R4
STRB        R5, [R0], #1

LSR         R6,R5,#1
STRB        R6, [R0], #1
```

ADD to be SUB ; line 4
SUB to be ADD ;line 7

QUESTION 5

a) State any ONE type of addressing mode of instructions that involve memory access with TWO examples from ARM instructions.

[2 Marks]

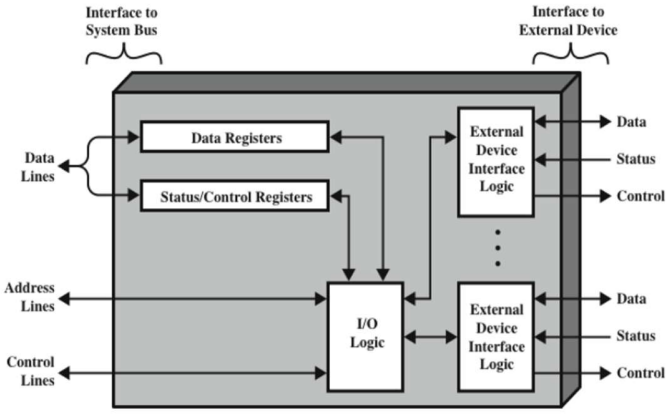
-Register indirect addressing mode. STR R0, [R1] LDR R1,[R2]

b) I/O modules vary considerably in complexity and the number of external devices that they control. Draw a general block diagram of an I/O module that consists of data registers, status registers, bus, address and control lines. Illustrate how the I/O module performs its functions in it.

[4 Marks]

- The module connects to the rest of the computer through a set of signal lines (e.g., system bus lines). (0.5 M)
-Data transferred to and from the module are buffered in one or more data registers. (0.5 M)
- There may also be one or more status registers that provide current status information. A status register may also function as a control register, to accept detailed control information from the processor. (0.5 M)
-The logic within the module interacts with the processor via a set of control lines. The processor uses the control lines to issue commands to the I/O module. Some of the control lines may be used by the I/O module (e.g., for arbitration and status signals). (0.5 M)

-The module must also be able to recognize and generate addresses associated with the devices it controls. Each I/O module has a unique address or, if it controls more than one external device, a unique set of addresses. (0.5 M)
- Finally, the I/O module contains logic specific to the interface with each device that it controls. (0.5 M). Diagram (1 M)



Block Diagram of an I/O Module

c) In computer science, floating-point numbers are represented by IEEE 754-32 bit single-precision format (as given below).

Sign	Biased exponent	Mantissa / Significand
1 bit	8 bits	23 bits

For the given positive 58_{10} in decimal number
i) Convert the decimal code to 8 bits unsigned binary number.
ii) Identify the normalized form of the 8 bits unsigned binary number.
iii) Identify the 8-bit biased exponent.
iv) Provide 58_{10} in IEEE 754-32 bit single-precision format

[1x 4 = 4 marks]

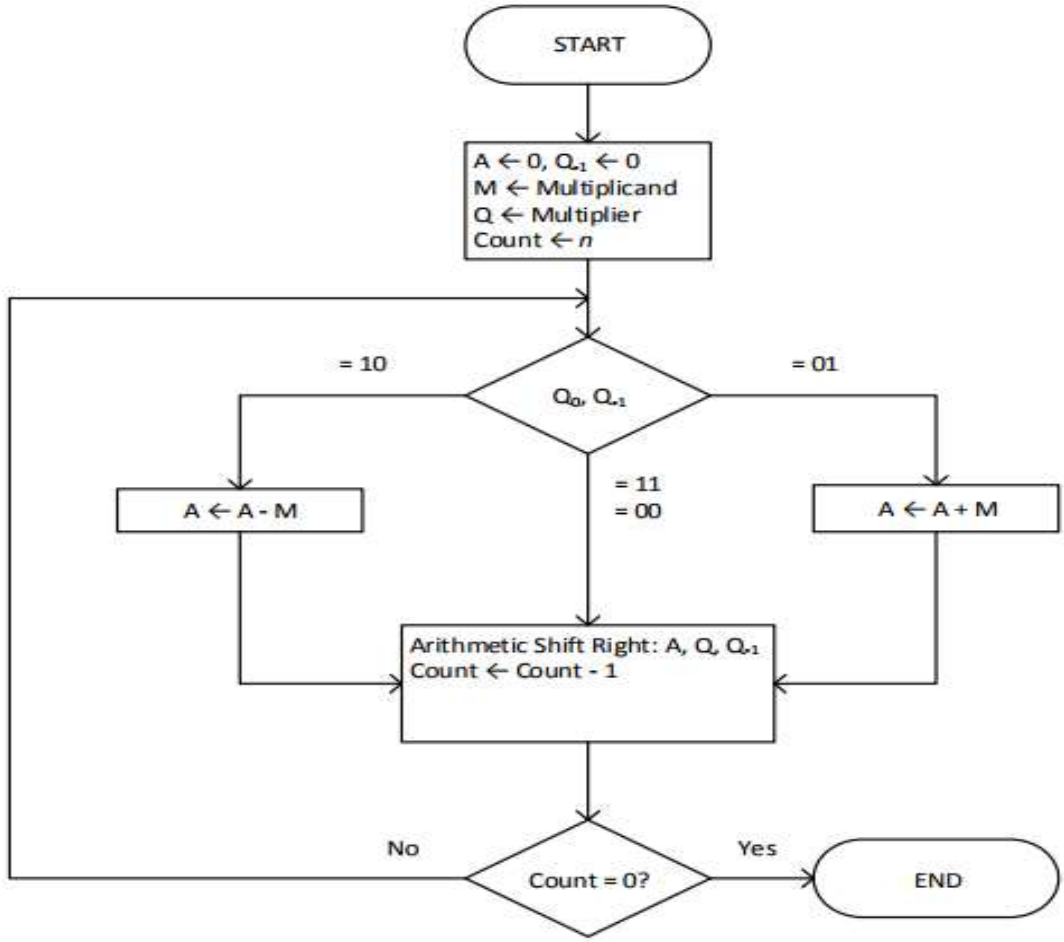
i) $0011\ 1010_2$ [1 mark]
ii) Represent the given binary in floating point format ($M*b^E$)
$0011\ 1010 * 2^0$
Normalized form of the given binary number 1.bbbbbbbb * 2n
$1.11010 * 2^5$ [1 mark]
iii) add the bias 127 to the exponent and convert it into binary in order to store for 8-bit biased exponent. $127 + 5 = 132\ (10000100_2)$ [1 mark]
iv)

0	1000 0100	1101 0000 0000 0000 0000 000

[1 mark]

Continued …

Appendix



JK Excitation table

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

D Excitation table

Q	Q^+	D
0	0	0
0	1	1
1	0	0
1	1	1

T Excitation table

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

End of paper