MULTIMEDIA UNIVERSITY

STUDENT ID NO

TABLE NO:

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION SOLUTIONS

TRIMESTER 1, 2022/2023

TSN1101 – COMPUTER ARCHITECTURE AND ORGANIZATION

(All Sections /Groups)

28 FEBRUARY 2023
9.00 a.m. - 11.00 a.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of **14 pages (excluding this page)** with **FIVE QUESTIONS.**

2. Attempt a total of **ALL** questions. Each question carries **12 marks** and the distribution of the marks for each subdivision is given. Maximum allotted marks are **60 marks**.

2. Please **write all your answers in the Question Paper itself** in the space provided.

QUESTION 1:

a. Convert the Binary number 101101_2 into the following number systems:
   i. Decimal
   ii. Octal
   iii. Hexadecimal
   iv. Gray Code

(4 ×1=4 marks)

(i) $45_{(10)}$

(ii) $55_{(8)}$

(iii) $2D_{(16)}$

(iv) $111011_{(gray)}$

b. i. What is an 'Overflow condition' during addition of signed numbers?
   ii. When does an 'Overflow condition' occur?

(2 marks)

i. When two numbers are added in binary and the number of bits required to represent the sum exceeds the number bits in the two numbers an overflow results.

ii. (1 Mark)

When carry into sign bit is different from carry out from the sign bit.

If the sum of two positive numbers yields a negative result, the sum has overflowed.
If the sum of two negative numbers yields a positive result, the sum has overflowed.

(1Mark)

c. Perform the binary addition using 8 bit **2's complement** form for the following decimal numbers:
   i. 33 and 15
   ii. - 46 and 25

(2x 2=4 marks)

Continued...

i. Code for 33 = 00100001 (0.5 mark)

Code for 15 = 00001111 (0.5 mark)

SUM = 00110000 (1 Mark)

ii. Code for 46 = 00101110 (0.5 mark)

1's complement =11 010001

2's complement = 11010010 = -45 (0.5 mark)

Code for 25 = 00011001 (0.5 mark)

SUM = 11101011 (1 mark)

d. Simplify the following expression using Boolean algebra:
$A\bar{B} + A\bar{B}C + A\bar{B}CD + A\bar{B}CDE$

(2 marks)

$A\bar{B} + A\bar{B}C + A\bar{B}CD + A\bar{B}CDE$

$A\bar{B}(1 + C) + A\bar{B}CD(1 + E)$

$A\bar{B}(1 + CD)$

$A\bar{B}$

QUESTION 2:

a. For the Boolean function $F = A + \bar{C}D + AC\bar{D} + \bar{A}BC\bar{D}$:

i. Obtain the truth table for function F .

(2 marks)

ii. Use Karnaugh Map (K map) to simplify F in SOP. **(1.5 marks)**

iii. Draw the logic diagram for the simplified function F in (ii) above.

(1.5 marks)

Continued...

i.

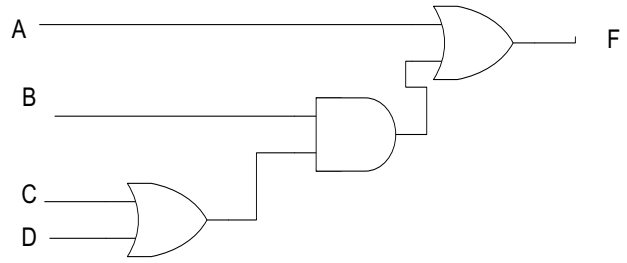
A	B	C	D	A'	C'	D'	C'D	ACD'	A'BCD'	F
0	0	0	0	1	1	1	0	0	0	0
0	0	0	1	1	1	0	1	0	0	1
0	0	1	0	1	0	1	0	0	0	0
0	0	1	1	1	0	0	0	0	0	0
0	1	0	0	1	1	1	0	0	0	0
0	1	0	1	1	1	0	1	0	0	1
0	1	1	0	1	0	1	0	0	1	1
0	1	1	1	1	0	0	0	0	0	0
1	0	0	0	0	1	1	0	0	0	1
1	0	0	1	0	1	0	1	0	0	1
1	0	1	0	0	0	1	0	1	0	1
1	0	1	1	0	0	0	0	0	0	1
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	0	1	0	1	0	0	1
1	1	1	0	0	0	1	0	1	0	1
1	1	1	1	0	0	0	0	0	0	1

ii.

	C'D'	C'D	CD	CD'
A'B'	0	1	0	0
A'B	0	1	0	1
AB	1	1	1	1
AB'	1	1	1	1

F = A + C'D+BCD'

iii.



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b. For the input combinations 010, 100, 001, 011, a HIGH output will be presented in decoding. For other input combinations, the outputs are LOW. Implement the circuit for the above with a suitable decoder and necessary logic gates.

i. Write down the truth table **(1 marks)**
ii. Expression for the output function **(1 mark)**
iii. Draw the logic diagram of the implemented decoder **(1 marks)**

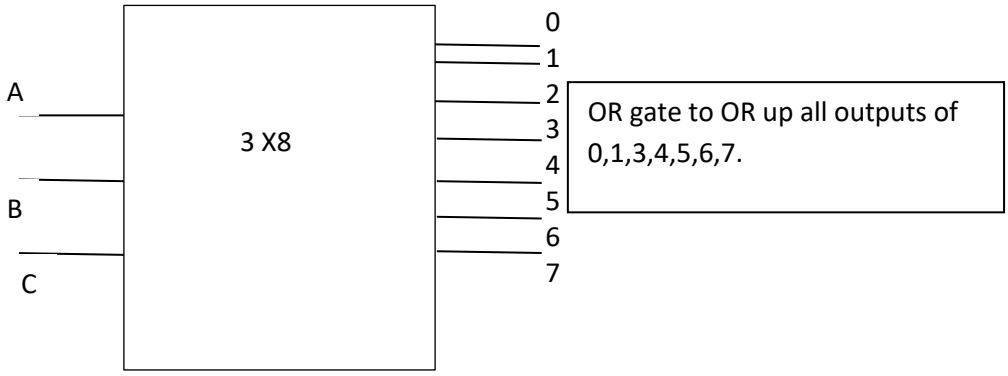
i.

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

ii)

$$X = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}\bar{C}$$

iii.



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c. Implement the following Boolean function with a suitable 8-1 multiplexer:

$F(A,B,C,D)=\Sigma\, m\,(1,3,4,11,12,13,14,15)$

i. Write down the truth table with the output function F. **(2 marks)**

ii. Draw the multiplexer implementation **(2 mark)**

i.

A	B	C	D	F	
0	0	0	0	0	**F =D**
0	0	0	1	1	
0	0	1	0	0	**F=D**
0	0	1	1	1	
0	1	0	0	1	**F=D'**
0	1	0	1	0	
0	1	1	0	0	**F=0**
0	1	1	1	0	
1	0	0	0	0	**F=0**
1	0	0	1	0	
1	0	1	0	0	**F=D**
1	0	1	1	1	
1	1	0	0	1	**F=1**
1	1	0	1	1	
1	1	1	0	1	**F=1**
1	1	1	1	1	

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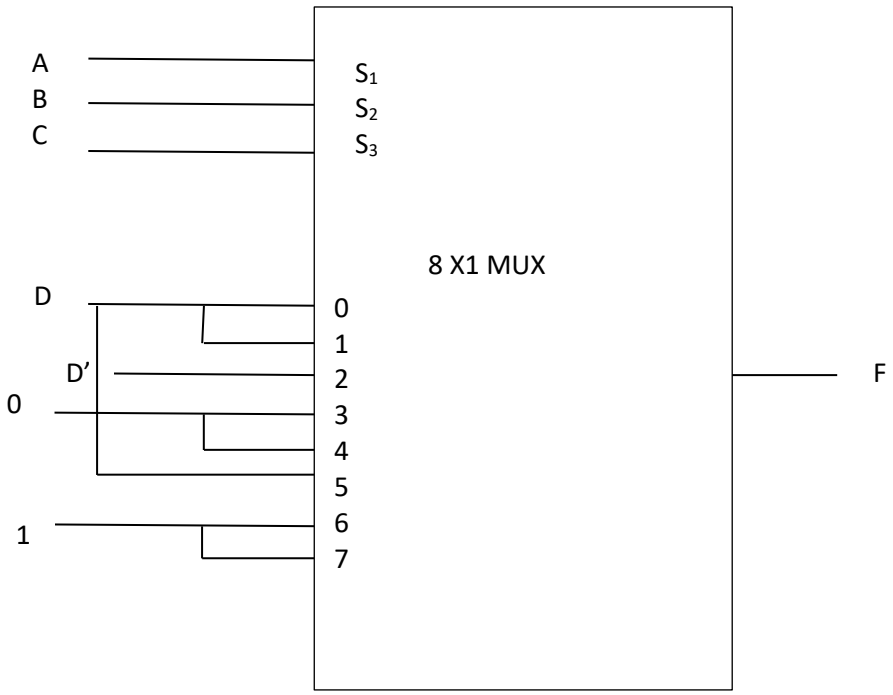
ii.



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QUESTION 3:

a. A synchronous counter has two postive-edged triggered D flip-flops and three inputs X, Y and Z. Design the counter based on the two conditions listed below:
   - If Z is 0, X and Y will count up based on the present state of X and Y.
   - If Z is 1, X and Y will count down based on the present state of X and Y.

   i..Complete the excitation table.

   (4 marks)

   ii .Simplify D_X and D_Y using K-maps in SOP.

   (2 marks)

   iii .Draw the synchronous counter.

   (3 marks)

i) 0.5 marks for each row

Present			Next		Inputs	
X	Y	Z	X	Y	D_X	D_Y
0	0	0	0	1	0	1
0	0	1	1	1	1	1
0	1	0	1	0	1	0
0	1	1	0	0	0	0
1	0	0	1	1	1	1
1	0	1	0	1	0	1
1	1	0	0	0	0	0
1	1	1	1	0	1	0

ii)

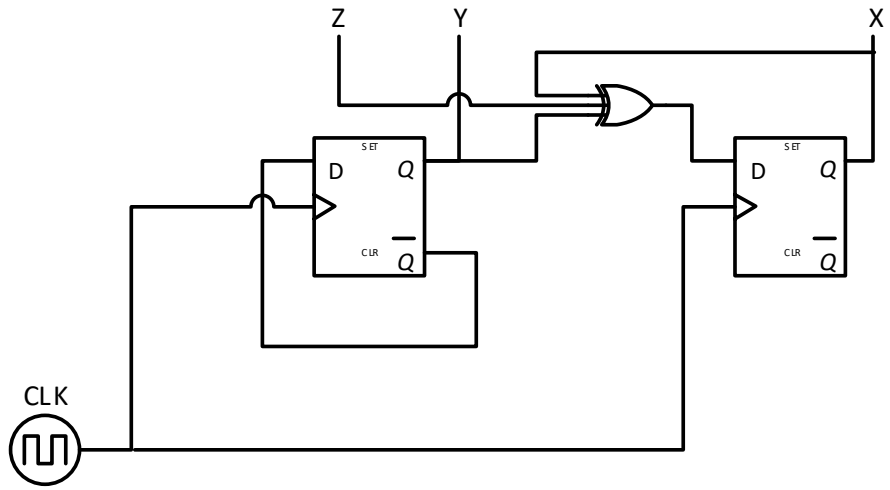
XY \ Z	0	1
00	0	1
01	1	0
11	0	1
10	1	0

$$D_X = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + XYZ + X\bar{Y}\bar{Z}$$
$$= X \oplus Y \oplus Z$$

XY \ Z	0	1
00	1	1
01	0	0
11	0	0
10	1	1

$$D_Y = \bar{Y}$$

iii)



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b. The system bus is a communication pathway connecting major computer components such as processor, memory and I/O. The three common buses are the data lines, address lines and control lines. How are these buses used in a computer system?

(3 marks)

- The data lines provide a path for moving data among system modules. The number of lines determines how many bits can be transferred at a time. [1]
- The address lines are used to designate the source or destination of the data on the data bus. They are also used to address the I/O ports. [1]
- The control lines are used to control the access to and the use of the data and address lines. Control signals transmit both command and timing information among system modules. [1]

QUESTION 4

a. Many processor designs include a register or set of registers, often known as the program status word (PSW), that contain status information. The PSW typically contains condition codes plus other status information. List six common fields or flags of the PSW.

(3 marks)

Any four [0.5x6]

Sign
Zero
Carry
Equal
Overflow
Interrupt Enable/Disable
Supervisor

Continued...

b. Assume a three-stage pipeline (fetch, decode & execute). Draw a timing diagram to show how many units are needed for four instructions.

(3 marks)

Time →

	1	2	3	4	5	6
Instruction 1	Fetch	Decode	Execute			
Instruction 2		Fetch	Decode	Execute		
Instruction 3			Fetch	Decode	Execute	
Instruction 4				Fetch	Decode	Execute

c. Assume that a processor employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR), supporting only one-address instructions. List the symbolic sequence of micro-operations for an indirect cycle.

(3 marks)

t1: MAR ← $(IR_{address})$
t2: MBR ← Memory
t3: $IR_{address}$ ← $(MBR_{address})$

Continued...

d. Assume that Word 11 contains 22, Word 22 contains 33, Word 33 contains 44, and Word 44 contains 55. Given the memory values above and a one-address machine with an Accumulator (Register A), what values do the following instructions load into the Accumulator?

i.	LOAD IMMEDIATE 22	ii.	LOAD DIRECT 22
iii.	LOAD INDIRECT 22	iv.	LOAD IMMEDIATE 33
v.	LOAD DIRECT 33	vi.	LOAD INDIRECT 33

(3 marks)

[0.5 mark each]

i) 22
ii) 33
iii) 44
iv) 33
v) 44
vi) 55

QUESTION 5

a. One of the distinctions among memory types is the method of accessing units of data such as **sequential access, direct access** and **random access**. Explain each of them by giving example.

(3 marks)

Each explanation (0.5 M) and example (0.5 M) for each method:

• **Sequential access**: Memory is organized into units of data, called records. Access must be made in a specific linear sequence. Stored addressing information is used to separate records and assist in the retrieval process. A shared read–write mechanism is used, and this must be moved from its current location to the desired location, passing and rejecting each intermediate record. Thus, the time to access an arbitrary record is highly variable. **Tape units,** discussed

Direct access: As with sequential access, direct access involves a shared read–write mechanism. However, individual blocks or records have a unique address based on physical location. Access is accomplished by direct access to reach a general vicinity plus sequential searching, counting, or waiting to reach the final location. Again, access time is variable. **Disk units**,

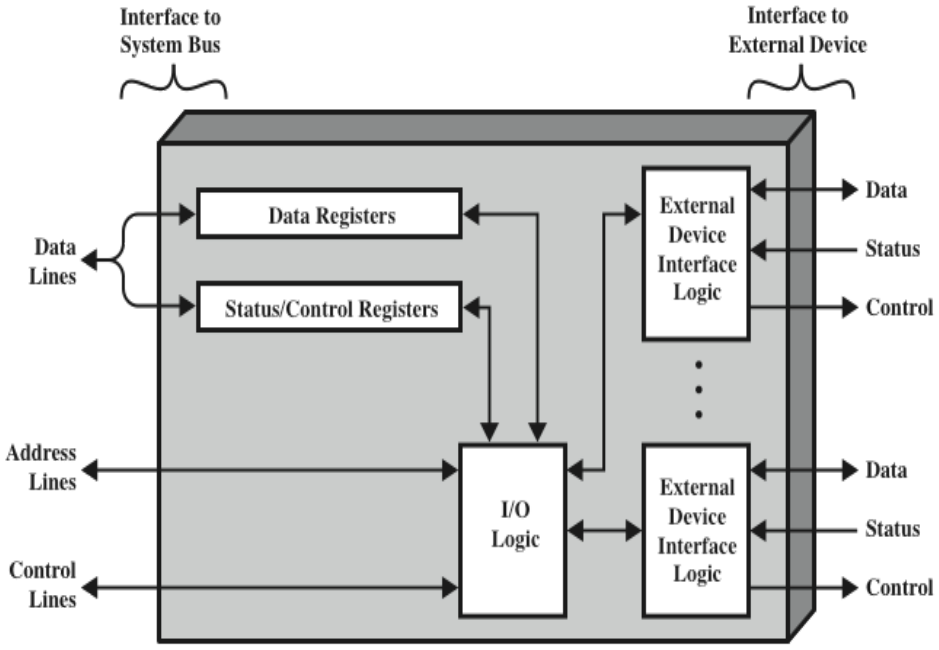
• **Random access:** Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access a given location is independent of the sequence of prior accesses and is constant. Thus, any location can be selected at random and directly addressed and accessed. **Main memory**

and some **cache system**s are random access.

b. I/O modules vary considerably in complexity and the number of external devices that they control. Draw a general block diagram of an I/O module that consists of data registers, status registers, bus, address and control lines. Illustrate how the I/O module performs its functions in it.

(4 marks)

- The module connects to the rest of the computer through a set of signal lines (e.g., system bus lines). (0.5 M)
-Data transferred to and from the module are buffered in one or more data registers. (0.5 M)
- There may also be one or more status registers that provide current status information. A status register may also function as a control register, to accept detailed control information from the processor. (0.5 M)
-The logic within the module interacts with the processor via a set of control lines. The processor uses the control lines to issue commands to the I/O module. Some of the control lines may be used by the I/O module (e.g., for arbitration and status signals). (0.5 M)
-The module must also be able to recognize and generate addresses associated with the devices it controls. Each I/O module has a unique address or, if it controls more than one external device, a unique set of addresses. (0.5 M)
- Finally, the I/O module contains logic specific to the interface with each device that it controls. (0.5 M).
Diagram (1 M)



Block Diagram of an I/O Module

c. **Snoopy protocols** distribute the responsibility for maintaining **cache coherence** among all of the cache controllers in a multiprocessor. One of the basic approaches to the snoopy protocol is '**write invalidate**'. Explain how '**write invalidate**' is able to maintain cache coherence.

(2 marks)

-With a write-invalidate protocol, there can be multiple readers but only one writer at a time. (0.5 M)
-Initially, a line may be shared among several caches for reading purposes. (0.5 M)
-When one of the caches wants to per- form a write to the line, it first issues a notice that invalidates that line in the other caches, making the line exclusive to the writing cache. (0.5 M)
-Once the line is exclusive, the owning processor can make cheap local writes until some other processor requires the same line. (0.5 M)

Continued...

d. State any **ONE** type of addressing mode of instructions that involve memory access with **TWO** examples from ARM instructions.

[3 marks]

-Register indirect addressing mode. STR R0, [R1]
LDR R1,[R2]

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