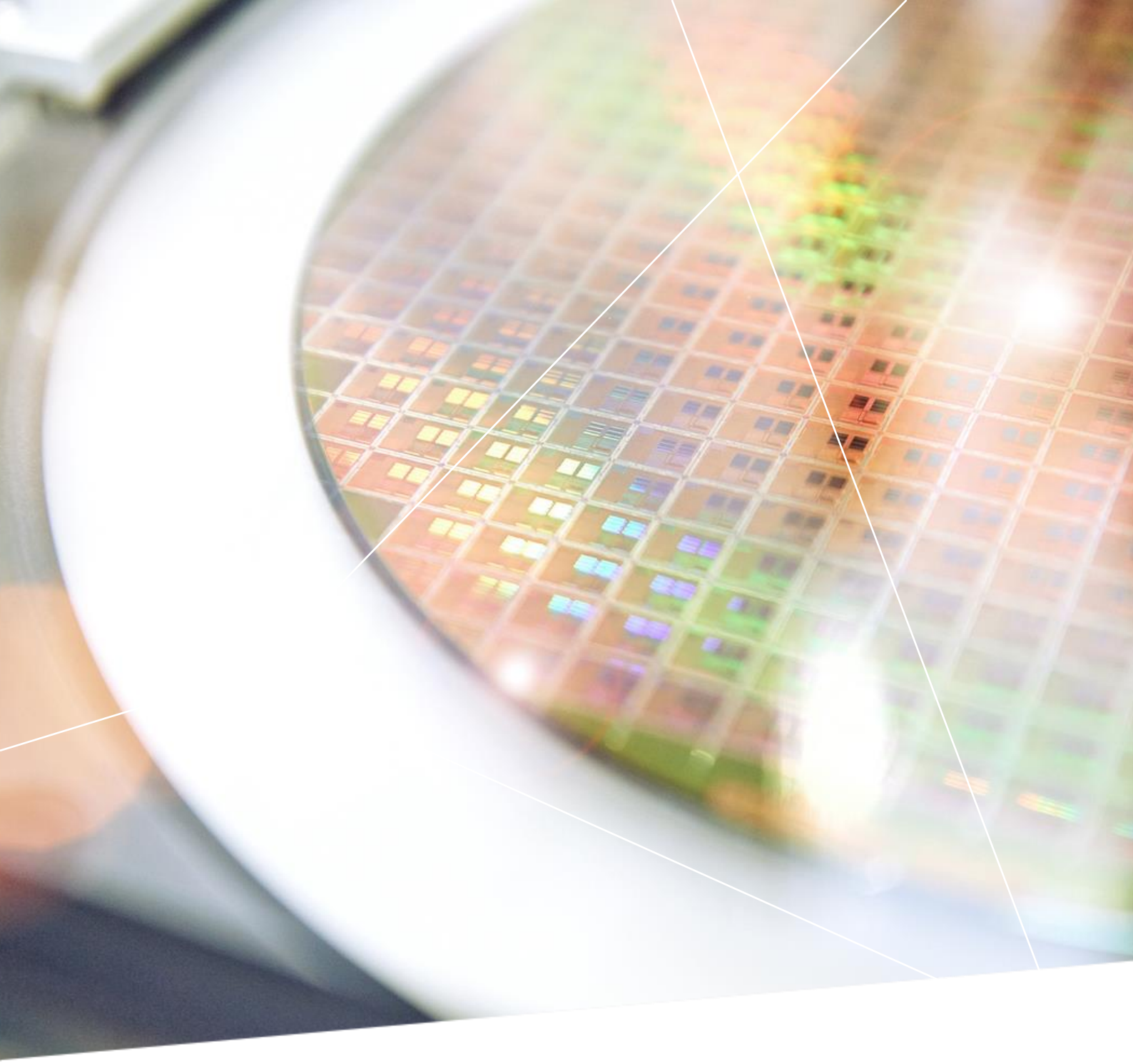

TRAVEO™ T2G Sample Driver Library Release Notes

v8.3.0, October 10, 2024

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Release Notes

TRAVEO™ T2G Sample Driver Library

Release Date: October 10, 2024

Thank you for your interest in Infineon TRAVEO™ T2G Sample Driver Library (SDL) version 8.3.0. This document lists the content of release package.

1 Contents

Infineon provides the Sample Driver Library (SDL) to simplify software development for the TRAVEO™ T2G family of devices.

The release provides the following features:

- Drivers for the extensive set of peripherals supported on TRAVEO™ T2G devices
- The Arm® Cortex Microcontroller Software Interface Standard (CMSIS®) core access header files from the CMSIS v5.9.0 release.
- CMSIS® complaint device header files, startup code (platform initialization) and device configuration header files
- Application Programming Interface Reference Manual specific to every device
- FreeRTOS support for the main application cores
- Examples to evaluate various peripherals
- Multiple build systems via command line using CMake

If you have technical questions, visit Infineon Technical Support for help or contact information.

2 Releases Details

SDL Release	Description - Supported Devices
1.0.0	**PSVP**: TVIIBE1M/a
2.0.0	**PSVP**: TVIIBE1M/a **Silicon**: TVIIBE1M/a
2.0.1	**PSVP**: TVIIBE1M/a **Silicon**: TVIIBE1M/a, Update and Fixes
3.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a
4.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a
5.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a **Silicon**: TVIIBH8M/a 176-TEQFP
6.0.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a **Silicon**: TVIIBH8M/a 320-BGA, TVIIBE2M/a
6.1.0	**PSVP**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a, TVIIC2D6M/a, **Silicon**: TVIIBE1M/b, TVIIBE2M/a, TVIIBH8M/a 176-TEQFP/320-BGA
6.2.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, **Silicon**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b 176-TEQFP/320-BGA, TVIIC2D6M/a 500-BGA Addition of untested TVIIBH4M/a
6.3.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8Ma/b, TVIIC2D6M/a, **Silicon**: TVIIBE1M/b/c, TVIIBE2Ma/b/c, TVIIBH8M/a/b/c 176-TEQFP/320-BGA, TVIIC2D6M/a 500-BGA, TVIIBH4M/a 176-TEQFP/272-BGA Addition of untested TVIIC2D4M/a, TVIIBE1M/d
6.4.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c 176-TEQFP/320-BGA, TVIIC2D6M/a 327-/500-BGA, TVIIBH4M/a 176-TEQFP/272-BGA Untested: TVIIBH8M/d, TVIIBE4M/a (new device)
6.5.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b Untested: TVIIBE512K/d, TVIIBE4M/a (new devices)
6.6.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a, TVIIC2D4M/a **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b, TVIIBE512K/a, TVIIBE4M/a, TVIIC2D4M/a
7.0.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.1.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.2.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a
7.3.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b, TVIICE4M/a
7.4.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a
7.5.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/a/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a
7.6.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a
7.7.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a
7.8.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a
7.9.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a
8.0.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a
8.1.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/a (Partially tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a
8.2.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/b (Not tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a
8.3.0	**PSVP**: TVIIBE1M/b/c, TVIIBE2M/a/b, TVIIBH8M/a/b, TVIIC2D6M/a/b, TVIIC2D4M/a, TVIIC2D6MDDR/b (Not tested), TVIICE4M/a (Partially tested), TVIIBH16M/a (Partially tested) **Silicon**: TVIIBE1M/b/c/d, TVIIBE2M/a/b/c, TVIIBH8M/b/c/d, TVIIC2D6M/b/c, TVIIBH4M/a/b, TVIIBE512K/d, TVIIBE4M/a, TVIIC2D4M/a/b/c, TVIICE4M/a, TVIIC2D6MDDR/a, TVIIBH16M/a

3 Device Support

The SDL includes:

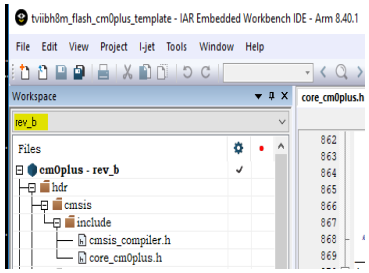
- Device-specific header files that provide a complete definition of all peripheral registers and bits in the device.
- CMSIS-compliant startup code to initialize the system after device reset, and transfer the code execution to “main ()”.
- Linker files for each supported device and toolchain (IAR/GHS, DIAB for TVIIBE1M)
- SVD files with a detailed description of peripherals, registers, fields, and bit values.
- GRD files to support register level debugging in GHS
- FreeRTOS support for all devices (Tested only on TVIIBE2M and TVIIC2D4M devices)

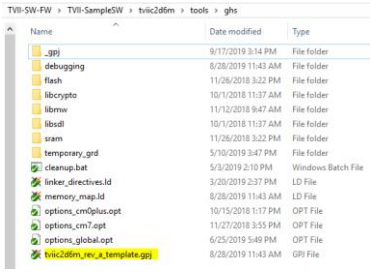
Table 1: Device RTL and MPN Revision Mapping

Device	Device RTL Revision	Datasheet MPN/SDL Revision
TVIIBE1M	B0	B
	B1	C
	B2	D
TVIIBE2M	A0	A
	A1	B
	A2	C
TVIIBH8M	B0	B
	B1	C
	B2	D
TVIIC2D6M	B0	B
	B1	C
TVIIBH4M	A0	A
	A1	B
TVIIC2D4M	A0	A
	A1	B
	A2	C
TVIIBE4M	A0	A
TVIIBE512K	B2	D
TVIIC2D6MDDR	A0	A
	B0	B
TVIICE4M	A0	A
TVIIBH16M	A0	A

4 Project configuration

1. Choose proper build and then perform the compilation in IAR. In case of GHS, device revision is part of the main project file.





2. **TVIIBE1M: Rev_B, Rev_C, Rev_D**
   a. PSVP 176-LQFP: CY_USE_PSVP=1 and either CYT2B78XAX (176-LQFP package fixed for PSVP and no other package supported)
   b. Silicon 176-LQFP: CY_USE_PSVP=0 and either CYT2B78XAX
   c. Supports both REV *A and REV *C CPU boards through the selection of CPU_BOARD_REVA or CPU_BOARD_REVC respectively
   d. Rev_D has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
3. **TVIIBE2M: Rev_A, Rev_B, Rev_C**
   a. PSVP: CY_USE_PSVP=1 and either CYT2B98XAX (176-LQFP package fixed for PSVP and no other package supported)
   b. Silicon 176-LQFP: CY_USE_PSVP=0 and either CYT2B98XAX
   c. Supports both REV *A and REV *C CPU boards through the selection of CPU_BOARD_REVA or CPU_BOARD_REVC respectively
   d. Rev_C has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
4. **TVIIBH8M: Rev_B, Rev_C, Rev_D**
   a. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection
   b. PSVP 320-BGA: CY_USE_PSVP=1 and either CYT4BFCCXX (320-BGA package fixed for PSVP and no other package supported)
   c. Silicon 320-BGA: CY_USE_PSVP=0 and either CYT4BFCCXX
      (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   d. Silicon 176-TEQFP: CY_USE_PSVP=0 and either CYT4BF8CXX / CYT4A0100S
      (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   e. Rev_C onwards has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
   f. Rev_A support is removed
5. **TVIIC2D6M: Rev_B, Rev_C**
   a. PSVP: CY_USE_PSVP=1 and tviic2d6m, CYT4DNDBHS
      (Rev_B only in PSVP, SMIF/ETH/LIN modules have not been tested due to limitations in the bitfile)
   b. Silicon 327-BGA: CY_USE_PSVP=0 and tviic2d6m, CYT4DNJBHS
      (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)
   c. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection
   d. Rev_B onwards has initial 2KB of SRAM reserved for internal purposes, and for other revisions last 6KB is reserved
   e. Rev_B, 500-BGA support removed. Only 327-BGA devices are supported.
   f. Rev_A, support removed.
6. **TVIIBH4M: Rev_A, Rev_B**
   a. Defines CY_CORE_CM7_0 or CY_CORE_CM7_1 for either core CM7_0 or CM7_1 selection

b. Silicon 272-BGA: CY_USE_PSVP=0 and either CYT4BBBCEX

(IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Silicon 176-TEQFP: CY_USE_PSVP=0 and either CYT4BB8CEX

(IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

d. Initial 2KB of SRAM reserved for internal purposes

e. CYT3BB support added

7. **TVIIC2D4M: Rev_A, Rev_B, Rev_C**

a. PSVP: CY_USE_PSVP=1 and tviic2d4m, CYT3DLBBHS.

b. Silicon 216-TEQFP: CY_USE_PSVP=0 and CYT3DLABAS / CYT3DLABBS / CYT3DLABCS / CYT3DLABDS / CYT3DLABES / CYT3DLABFS / CYT3DLABGS / CYT3DLABHS

(IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0)

c. Initial 2KB of SRAM reserved for internal purposes

8. **TVIIBE4M: Rev_A**

a. Silicon: 176-LQFP: CY_USE_PSVP=0 and either CYT2BL8XAX / CYT2BL7XAX / CYT2BL5XAX / CYT2BL4XAX / CYT2BL3XAX

b. Rev_A has initial 2KB of SRAM reserved for internal purposes

9. **TVIIBE512K: Rev_D**

a. Silicon: 100-LQFP: CY_USE_PSVP=0 and either CYT2B65BAS / CYT2B65BAE / CYT2B65CAS / CYT2B65CAE

b. Rev_D has initial 2KB of SRAM reserved for internal purposes

10. **TVIIC2D6MDDR: Rev_A**

a. PSVP: CY_USE_PSVP=1, Device CYT4ENDBAS, MCU revision as CY_MCU_rev_a

b. Silicon 500-BGA: CY_USE_PSVP=0, Device as CYT4ENDBAS or CYT4ENDBCS or CYT4ENDBES or CYT4ENDBGS or CYT4ENDBJS or CYT4ENDBLS or CYT4ENDBNS or CYT4ENDBQS, MCU revision CY_MCU_rev_a, EVK revision CY_500BGA_EVK_rev_a

(IAR linker “use_psvp = 0” in its ICF file, GHS uses global definition CY_USE_PSVP=0)

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

11. **TVIICE4M: Rev_A**

a. PSVP: CY_USE_PSVP=1, Device CYT2CL8BAS, MCU revision as CY_MCU_rev_a

b. Silicon 176-LQFP: CY_USE_PSVP=0 and CYT2CL8BAS (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0), MCU revision CY_MCU_rev_a, EVK revision CY_176LQFP_EVK_REV_A

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

12. **TVIIBH16M: Rev_A**

a. PSVP: CY_USE_PSVP=1, Device CYT6BJCCJS, MCU revision as CY_MCU_rev_a, Only IAR supports all core download and debug. GHS supports only CM0+/CM7_0/CM7_1.

b. Silicon 320-BGA: CY_USE_PSVP=0 and CYT6BJCDHE (IAR linker “use_psvp = 0” in its ICF file, GHS relies on global definition CY_USE_PSVP=0), MCU revision CY_MCU_rev_a, EVK revision CY_320BGA_EVK_rev_a

c. Rev_A has initial 2KB of SRAM reserved for internal purposes

Note:

- ‘X’ in the device MPN above signifies different package variants or temperatures supported. Please check the device specific datasheet for more details.
- In all devices, last 6kB of SRAM cannot be used for retention.
- SRAM reserved for internal purposes is NOT available for the user.

Table 2: Device Memory Map

Device	Type	Brief Device Description
TVIIBE1M	PSVP	Dual core CM0+/CM4, Flash 1088-KB, SRAM 128-KB, Work flash 96-KB
	176-LQFP	Dual core CM0+/CM4, Flash 1088-KB, SRAM 128-KB, Work flash 96-KB
TVIIBE2M	PSVP	Dual core CM0+/CM4, Flash 2112-KB, SRAM 256-KB, Work flash 128-KB
	176-LQFP	Dual core CM0+/CM4, Flash 2112-KB, SRAM 256-KB, Work flash 128-KB
TVIIBH8M	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 2048-KB, SRAM 1024-KB, Work flash 256-KB
	320-BGA 176-TEQFP	Triple core CM0+/CM7_0/CM7_1, Flash 8384-KB, SRAM 1024-KB, Work flash 256-KB
TVIIC2D6M	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 1024-KB, SRAM 1024-KB, Work flash 128-KB
	327-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 6336-KB, SRAM 640-KB, Work flash 128-KB
TVIIBH4M	176-TEQFP 272-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 4160-KB, SRAM 768-KB, Work flash 256-KB
TVIIC2D4M	216-TEQFP	Dual core CM0+/CM7_0, Flash 4160-KB, SRAM 384-KB, Work flash 128-KB
TVIIBE4M	176-LQFP	Dual core CM0+/CM4, Flash 4160-KB, SRAM 512-KB, Work flash 128-KB
TVIIBE512K	100-LQFP	Dual core CM0+/CM4, Flash 576-KB, SRAM 64-KB, Work flash 64-KB
TVIIC2D6MDDR	PSVP	Triple core CM0+/CM7_0/CM7_1, Flash 1024-KB, SRAM 1024-KB, Work flash 128-KB
	500-BGA	Triple core CM0+/CM7_0/CM7_1, Flash 6336-KB, SRAM 640-KB, Work flash 128-KB
TVIICE4M	PSVP	Dual core CM0+/CM4, Flash 1024-KB (Split), SRAM 512-KB, Work flash 128-KB
	176-LQFP	Dual core CM0+/CM4, Flash 4160-KB, SRAM 512-KB, Work flash 128-KB
TVIIBH16M	PSVP	Five cores CM0+/CM7_0/CM7_1/CM7_2/CM7_3, Flash 2560-KB, SRAM 2048-KB, Work flash 256-KB
	320-BGA	Five cores CM0+/CM7_0/CM7_1/CM7_2/CM7_3, Flash 16768-KB, SRAM 2048-KB, Work flash 512-KB

5 Supported Toolchains

- Green Hills MULTI: 7.1.4, Compiler: 2017.1.4, Probe Version: 5.6.5
    - *DEVELOPMENT AUTOBUILD 5.6 634260/AB as of patch #12996, or higher*
    - *Flash loaders are not available as part of SDL, will be provided on case by case basis through Cypress Customer Support (Patches are of size in GBs)*
- IAR Embedded Workbench for ARM 8.22.1 (EWARM-CD-8221-xxxxx.exe), IAR I-Jet Debugger
    - *Supported only for tviic2d4m, tviic2d6m, and tviic2d6mddr devices for flash projects*
    - *Flash loaders are available at the location*
        - *"\misc\tools\iar\IAR_EWARM_8222_FlashLoader_Patch_TraveoII"*
- IAR Embedded Workbench for ARM 9.30.1 (EWARM-9301-50054.exe), IAR I-Jet Debugger
    - *This EWARM revision is NOT functional safety complaint*
    - *Flash loaders are available at the location*
        - *"\misc\tools\iar\IAR_EWARM_9301_FlashLoader_Patch_TraveoII.7z"*
    - *Go through "\misc\tools\iar\Readme_Patch.txt" to update the TRAVEO™ T2G patch for IAR.*
- Windriver DIAB revision diab-5.9.8.1 (Right now only for TVIIBE1M, later will be extended to all devices. Only via command line-based system via CMake)
- Arm® GNU GCC revision 11.3, rel1 (via CMake)

6 Peripheral Drivers

The SDL provides a high-level API to configure, initialize, and use a peripheral driver. The drivers are designed for peripheral IP blocks, therefore work on all TRAVEO™ T2G products that instantiate that IP block.

Following driver (src/driver) modules have been tested and the respective examples are available in the src/examples folder. Some of these drivers/mw are available in the common/src/drivers or common/src/mw which are common across dies, and some are specific to a particular die is available in the die specific drivers/mw say, tviibh8m/src/drivers or tviibh8m/src/mw.

Table 3: Drivers

Driver	Description	API Functionality
ADC	Analog to Digital Converter	Manage ADC operations
Audioss	Sound Subsystem for I^2S, DAC, Mixer, PWM, SG, TDM (TVIIC devices only)	Manages I2S, Audio DAC, Mixer, PCM-PWM, Sound Generator, TDM as part of sound subsystem
AXIDMA	M-DMA on AXI bus	Memory to memory transfer over AXI bus
CAN FD	Controller Area Network Flexible Data-Rate	Manages Classic and FD operations
CPU	CPU driver	Enables core of CPU specific features
CRYPTO	Cryptographic Operations	Perform cryptographic operations on user-designated data. Available as libraries.
CXPI	Clock eXtension Peripheral Interface	Manages communication over CXPI interface
DAC	Audio DAC	Provides global DAC defines and API function definitions
DMA	Direct Access Memory (AHB bus)	Perform memory-to-memory (M-DMA) and peripheral-to-memory (P-DMA) (and vice versa) operations
EVTGEN	Event Generator	Performs event generation for interrupts and triggers in active power mode
FLASH	Flash Memory	Manage code/work flash memory operations
FLEXRAY	FlexRay Interface	Manages FlexRay communication
FPDLINK	FDP-Link or LVDS	Analog LVDS video driver
GPIO	General Purpose I/O Ports	Configure and access device input/output pins
I^2S	Inter-IC Sound (TVIIBH4M/8M all revisions)	Manage Inter-IC Sound. I2S is used to send digital audio streaming data to external I2S devices, such as audio codecs or simple DACs. It can also receive digital audio streaming data.
IPC	Inter Process Communication	Manage data transfer between CPUs or processes in a device
LIN	Local Interconnect Network	Provides master and slave data transfer capabilities
LVD	Low Voltage Detection	Provides LVD capabilities
LPDDR4	Low-Power DDR SDRAM	Provides basic capabilities to access DDR memories
MCWDT	Multi-counter Watchdog timer	Provides control and status capabilities
MIPI-CSI2	Video Input	Manage and control analog video inputs
Mixer	Audio Mixer for I2S, PWM etc.	Provides global Mixer defines and API function definitions
MPU	Memory Protection Unit	Manages the configuration of MPU
PROT	Memory and Peripheral Protection	Manage the MPU, Shared MPU (SMPU), and Peripheral Protection Unit (PPU)
PWM	Audio Pulse Width Modulation	PWM interface drives PWM output lines and their complementary output lines.
SCB	Serial Communication Block	Manage serial communication as EZI2C, I2C, SPI, or UART
SEGLCD	Segment LCD	Manage Segment LCD interfaces
SD_HOST	Secure Digital Host Controller	Manages SD and eMMC devices
SG	Audio Sound Generator	Helps produce PWM tone (frequency) and amplitude (volume) signals
SMART IO	Smart I/O	Configure and access the Smart I/O hardware present between the GPIOs (pins) and HSIOMs (pin multiplexers) on select device ports. It can be used to perform simple logic operations on peripheral and GPIO signals at the GPIO port
SMIF	Serial Memory Interface	SPI-based communication interface for interfacing external memory devices to T2G. The SMIF supports Octal-SPI, Dual Quad-SPI, Quad-SPI, DSPI, and SPI. This interface also supports xSPI interfaces like HyperRAM and HyperFlash devices.
SROM	Internal SROM driver	APIs to support some basic access to SROM System calls
SYSCLK	System Clock	Provides APIs to control and read status of various clocking capabilities of the device
SYSFLT	System Fault	Controls CPUs fault processing Subsystem
SYSINT	System Interrupt	Manage interrupts and exceptions, in conjunction with the CMSIS core NVIC API
SYSLIB	System Library	Utility functions to handle delays, register read/write, asserts, silicon unique ID, and more
SYSPM	System Power Modes	Controls device power modes
SYSREGHC/ SYSPMIC	REGHC/PMIC Control and Status	Controls High Current Regulator or the PMIC module

SYSRESET	System Reset	Provides APIs for reading reset reason and clearing them
SYSRTC	System Real Time Clock	Provides capabilities to handle RTC, Alarms etc.
SYSTICK	System Tick Timer	Manage a 24-bit down-counter timer
SYSWDT	Free running Watchdog timer	Provides control and status capabilities
TDM	Audio Time-division multiplexing	TDM transmitter and a TDM receiver, I2S support also included in latest revisions.
TCPWM	Timer Counter PWM	Manage a 16- or 32-bit periodic Counter, PWM, Quadrature decoder, Shift register
TRIGMUX	Trigger Multiplexer	Manage the multiplexing of trigger outputs to specific trigger inputs across multiple peripherals

Table 4: Device Specific Middleware

Middleware	Description	API Functionality
GFX_ENV	Graphics Environment Setup	Supported only for TVIIC2D6M/TVIIC2D4M (Graphics environment setup support)
MIPI_SENSOR	MIPI CSI2 controller	Support top level MIPI CSI2 APIs for camera access map to capture interface of VIDEOSS IP
POWER	REGHC or PMIC based power control	REGHC or PMIC controller middleware (REGHC/TVIIBH4M/TVIIBH8M, PMIC/TVIIC2D6M/TVIIC2D4M)
SMIF_MEM	SMIF SPI/Hyper Access Control	SPI or xSPI specific device support
LVDS_HDMI	LVDS to HDMI transceiver	Supported only for TVIIC2D6M (Graphics environment setup is must)

Table 5: Common Middleware

Middleware	Description	API Functionality
Button	Button middle layer	APIs to support buttons
Semihosting	SCB/UART middle layer	Support top level UART APIs for debugging
SW_Timer	Software Timer	Enables multiple software timers
Flash	Code and work flash	User level APIs for ease of use
AIC261	Audio Codec	Provides APIs for audio codec (ADC/DAC) TI AIC 261

Hardware-specific middleware such as CS42488, DP83867, AIC26, TJA110, etc.

7 Release Contents

The SDL is organized into several folders. The following table shows the SDL folder structure.

Table 6: SDL Folder Structure

Path/Folder	Description
cmake	CMake device, toolchain specific configurations, debug template files, usage documentation, etc.
common/hdr/cmsis	CMSIS core access headers
common/src/drivers	Drivers common across all the devices
common/src/mw	Middleware common across all the devices
common/src/rtos	FreeRTOS support for application cores
common/src/startup	Tool specific startup code for all the devices
docs	API Documentation
misc/tools	GHS/IAR specific flash loaders, SVD files
TRAVEO™ T2G Body, and Cluster Entry Devices (tviibe1m/2m/4m/512k, tviice4m)	
hdr/rev_x	Device specific header files, BSP for T2G CPU/Base Board, GPIO assignments
hdr/rev_x/ip	Device IP specific headers, register representation
hdr/rev_x/mcureg	IP Specific Register Addresses
src/drivers	Driver source and respective headers specific to the device
src/examples	Code examples in accordance to the device
src/system	Device's system specific code and system header for clock configurations
src/main_cm0plus.c	Sample main source file for CM0+ core
src/interrupts/cy_interrupt_map_cm0plus.h	User interrupt mapping file
src/main_cm4.c	Sample main source file for CM4 core
src/interrupts/cy_interrupt_map_cm4.h	User interrupt mapping file
tools/ghs	GHS MULTI workspaces for SRAM/Flash for CM0+/CM4 core, linker specific files, and GRD files
tools/iar	IAR workspaces for SRAM/Flash for CM0+/CM4 cores, linker specific files
TRAVEO™ T2G Body High, and Cluster 2D Devices (tviibh4m/8m/16m, tviic2d4m/6m/6mddr)	
hdr/rev_x/	Device specific header files, BSP for T2G CPU/Base Board, GPIO assignments
hdr/rev_x/ip	Device IP specific headers, register representation
hdr/rev_x/mcureg	IP Specific Register Addresses
src/drivers	Driver source and respective headers specific to the device
src/mw/	Middleware support
src/examples	Code examples in accordance device specific
src/system	Device system specific code and system header for clock configurations
src/main_cm0plus.c	Sample main source file for CM0+ core
src/interrupts/cy_interrupt_map_cm0plus.h	User interrupt mapping file
src/main_cm7_0.c	Sample main source file for CM7_0 core
src/interrupts/cy_interrupt_map_cm7_0.h	User interrupt mapping file
src/main_cm7_1.c	Sample main source file for CM7_1 core
src/interrupts/cy_interrupt_map_cm7_1.h	User interrupt mapping file
src/main_cm7_2.c	Sample main source file for CM7_2 core (tviibh16m only)
src/interrupts/cy_interrupt_map_cm7_2.h	User interrupt mapping file (tviibh16m only)
src/main_cm7_3.c	Sample main source file for CM7_3 core (tviibh16m only)
src/interrupts/cy_interrupt_map_cm7_3.h	User interrupt mapping file (tviibh16m only)
tools/ghs	GHS MULTI workspaces for SRAM/Flash for CM0+/CM7_0/CM7_1/CM7_2/CM7_3 cores, linker specific files, and GRD files
tools/iar	IAR workspaces for SRAM/Flash for CM0+/CM7_0/CM7_1/ CM7_2/CM7_3 cores, linker specific files

8 Documentation

API Reference Manual are located in the \docs subdirectory of the SDL installation directory.

9 General Notes

a. Application address mapping,

a. *TVIIBE1M/TVIIBE2M/TVIIBE4M/TVIIBE512K/TVIICE4M: In the header "system_cyt2b7.h" / "system_cyt2b9.h" / "system_cyt2bl.h" / "system_cyt2b6.h"/ "system_cyt2cl.h" macro "CY_CORTEX_M4_APPL_ADDR" needs to be updated to CM4 start address as per the linker config file, it is picked by the respective tool chain automatically*

b. *TVIIBH4M/TVIIBH8M/TVIIC2D4M/TVIIC2D6M: In the header "system_cyt4bf.h" /" system_cyt4bb.h" /" system_tviic2d6m.h" macro "CY_CORTEX_M7_0_APPL_ADDR" and "CY_CORTEX_M7_1_APPL_ADDR" needs to be updated to CM7_0/CM7_1 start address as per the linker config file, it is picked by the respective tool chain automatically*

c. *TVIIC2D4M: In the header "system_cyt3dl.h" macro "CY_CORTEX_M7_0_APPL_ADDR" needs to be updated to CM7_0 start address as per the linker config file, it is picked by the respective tool chain automatically*

b. Clock Configuration

Table 7: PSVP Clock Configuration

Sl. No.	Device (PSVP)	Clock	Clock Frequency
2	TVIIBE1M, TVIIBE2M	CM0+/CM4	24 MHz
3	TVIIBH8M, TVIIC2D6M, TVIIC2D4M	CM0+/CM7_x	24 MHz
4	TVIIC2D6M, TVIIC2D4M, TVIIC2D6MDDR, TVIIBH16M	IMO	8 MHz
5	TVIIBE1M, TVIIBE2M	ILO	32.9 kHz
6	TVIIBH8M, TVIIC2D6M, TVIIC2D4M, TVIIC2D6MDDR	ILO	12.8 kHz
7	TVIIC2D6MDDR	CM0+/CM7_x	26.6 MHz
8		LPDDR	80 MHz
9	TVIICE4M	CM0+/CM4	24 MHz
		IMO/ILO	8MHz/12.8kHz
10	TVIIBH16M	CM0+/CM7_x	20 MHz (PLL_OUT)
		ILO	14.178 kHz

Table 8: Silicon Clock Configuration

Sl. No.	Device (Silicon)	Clock	Clock Frequency
1	TVIIBH8M/b/c/d 320-BGA, 176-TEQFP TVIIBH4M/a/b 176-TEQFP, 272-BGA	CM0+	80 MHz
		CM7_0, CM7_1	250/350 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
2	TVIIBE2M/a/b/c 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
3	TVIIBE1M/b/c/d 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
4	TVIIC2D6M/b/c 327-BGA	CM0+	80 MHz
		CM7_0, CM7_1	320 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
		SMIF	166 MHz
5	TVIIC2D4M/a/b/c 216-TEQFP	CM0+	80 MHz
		CM7_0	240 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
6	TVIIBE512K/d 100-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
7	TVIICE4M/a 176-LQFP	CM0+	80 MHz
		CM4	160 MHz
		Bus	80 MHz
		IMO	8 MHz
		ILO	~32 kHz
8	TVIIC2D6MDDR/a 500-BGA	CM0+	80 MHz

		CM7_0, CM7_1	320 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz
		LPDDR4	752 MHz
		VIDEOSS	266 MHz
9	TVIIBH16M/a 320-BGA	CM0+	80 MHz
		CM7_0, CM7_1, CM7_2, CM7_3	250/350 MHz
		Bus	160 MHz
		IMO	8 MHz
		ILO	~32 kHz

c. CM0+ samples shall not use IRQs 0/1 (CPUIntIdx0_IRQn/CPUIntIdx1_IRQn), as they are internally used by the SROM based System calls. This can be seen as part of the examples for reference. It would cause hard fault, if used.

d. Interrupt usage:

All the examples are modified to use the IRQ table in SRAM and thereby relives from maintaining core specific interrupt map headers (example: cy_interrupt_map_cm7_0.h)

For IRQs part of SRAM

a. No need to update core specific interrupt map headers for any IP specific ISRs, instead update respective example as below (default interrupt map headers at src level will be used as is without any modifications)

b. Cy_SysInt_SetSystemIrqVector(irq_cfg.sysIntSrc, ButtonIntHandler); // typical use case example

For IRQs part of flash region

a. Users will still need to update the core specific interrupt map header against the IP which is being tested and remove the below define from the respective header,
#define CY_LINK_SYSTEM_IRQ_TABLE_TO_RAM

Table 9: Device to SMIF revision mapping

Device	Device Revision	SMIF Revision
TVIIBH4M/TVIIBH8M/TVIIBH16M	All	v2
TVIIC2D4M	Rev_A/Rev_B/Rev_C	v3.1
TVIIC2D6M	Rev_B/Rev_C	v4.0
TVIIC2D6MDDR	Rev_A	v4.0
TVIICE4M	Rev_A	v3.1

10 Change Log from v8.2.0 to v8.3.0

Sl. No.	Change	Files	Action
1	Updates the SMIF memory middleware S26H default configuration for CFR2V register.	TVII-SampleSW/tviibh8m/src/mw/smif_mem/cy_smif_hb_flash.h	Updated
2	Updates the missing return value from the LPDDR block API : Cy_Lpddr_ControllerDeInit().	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Updated
3	Fixes an issue causing a GSM error after WR Shmoo (command sequence error SRE was send in PHOPE)	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Updated
4	Adapted LPDDR4 driver as per the rev_b silicon updates (currently not supported by SDL).	TVII-SampleSW/ tviic2d6mddr/src/examples/lpddr4/	Added
5	Added different configuration files based on LPDDR4 memory capacity.	TVII-SampleSW/ tviic2d6mddr/src/examples/lpddr4/Sol_Designer_Sample/	Added
6	Updates the Cy_Flash_Checksum() api to provide the correct checksum values based on the rowAddress.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/ flash/cy_flash.h TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/ flash/cy_flash.c	Updated
7	Updated middleware for the LVDS to HDMI converter ITE6263 to take video parameter from example.	TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_base_hdmi.c TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_base_hdmi.h TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_lvds_hdmi.c TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_lvds_hdmi.h	Updated

11 Change Log from v8.1.0 to v8.2.0

Sl. No.	Change	Files	Action
1	Add "used" attribute to stub functions that will prevent link errors with -flto in certain situations.	TVII-SampleSW/common/src/drivers/syslib/gcc/cy_syslib_newlib_systemcalls.c	Added
2	Added a fix for API in clock system (did not add "1" to integer divider) - Cy_SysClk_PeriphGetFrequency()	TVII-SampleSW/tviibe1m/src/drivers/sysclk/cy_sysclk.c TVII-SampleSW/tviibh8m/src/drivers/sysclk/cy_sysclk.c	Updated
3	Removes the possibility to set 64Bytes Training pattern and set 128Byte Pattern by default. - #define BUFFER_SIZE SIZE_128_BYTE	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Updated
4	Added two new commands to the cy_en_lpddr4_uci_cmd_op_t - CY_LPDDR4_UCI_CMD_OP_USER_CMD_PHYOPE = 0xE - CY_LPDDR4_UCI_CMD_OP_USER_CMD_PHYOPX = 0xF	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Added
5	Added two new functions: - Cy_Lpddr_DisablePHYOperation() - Cy_Lpddr_PrepareForPHYOperation()	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Added
6	Added new state in cy_en_lpddr4_cntrl_gsm_state_t - CY_LPDDR4_CNTRL_GSM_STATE_PHY_OPERATION	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Added
7	Added new middleware for the LVDS to HDMI converter ITE6263.	TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_base_hdmi.c TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_base_hdmi.h TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_lvds_hdmi.c TVII-SampleSW/tviic2d6m/src/mw/lvds_hdmi/cy_lvds_hdmi.h	Added

Delta Change Log from v8.2.0 to v8.2.1

Sl. No.	Change	Files	Action
1	Updates the SVN revision number (330491) for the LPDDR4 driver file (cy_lpddr4.h) in driver revision xls	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/LPDDR4 Driver Release Version.xls	Updated

12 Change Log from v8.0.0 to v8.1.0

Sl. No.	Change	Files	Action
1	Added dummy configuration to avoid build errors: “RELEASE_BUILD_DUMMY_CONFIG”	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dramconfsel.h	Modified
2	Updated “Cy_Lpddr_ReadDQSOscValue()” in the LPDDR4 driver configuration file for: - corrected check for DQS Osc max values to 0xFFFF - corrected abort condition - changed the condition to detect the read for a channel completed.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
3	Updated the LPDDR4 driver to 3.0: - added JESD209_4B_NS_TDQS2DQ_MIN and JESD209_4B_NS_TDQS2DQ_MAX - added new datatype for reading the DRAM vendor - added new datatype for reading the channel density - added a data type for easy register access for lpddr4 - added function for DLL Re-Initialization Cy_LPDDR4_DLLResMCStoSta()	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Updated
4	Updated the LPDDR4 driver: - added software aided training. - added DLL re-initialization - added the support for to replace the DQS2DQ HW re-training by SW	TVII-SampleSW/tviibh8m/src/drivers/ lpddr4/cy_lpddr4.h	Updated
5	Updated the LPDDR4 driver: - added SW aided training feature for read and write	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Updated
6	Updated the eMMC driver: - Added CLK_IN and CLK_OUT delay APIs - Added the DDR mode support for eMMC	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c	Updated
7	Minor warning fixes on the FPD_LINK driver	TVII-SampleSW/tviibh8m/src/drivers/fpdlink/cy_fpdlink.h	Modified

13 Change Log from v7.9.0 to v8.0.0

Sl. No.	Change	Files	Action
1	Adds the fix for the SD Host driver to include new line at the end of the file.	TVII-SampleSW/tviibh8m/src/drivers/sd_host/cy_sd_host.c	Modified
2	Adds Ethernet driver files with proper licencing and terms.	TVII-SampleSW/tviibh8m/src/drivers/ethernet/cdn_errno.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cdn_stdint.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cedi.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cps_v2.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/cy_ethif.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd_int.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd_rx.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/edd_tx.c TVII-SampleSW/tviibh8m/src/drivers/ethernet/emac_regs.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/emac_regs_macro.h TVII-SampleSW/tviibh8m/src/drivers/ethernet/log.h	Modified
3	Moved the LPDDR4 power sequencing function out of the system initialization.	TVII-SampleSW/tviic2d6mddr/src/system/rev_a/system_tviic2d6mddr_cm7.c	Modified
4	Adds new JEDEC timing parameter ODTLON which is calculated based on FSP[1] and the used WL Set refer JEDED209-4C.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
5	Adds some JEDEC timing parameters related to JESD209_4B_NS	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
6	Adds support to configure LPDDR4 Inline ECC Addresses via linker file using the macro: ECC_USE_LINKER_ADDRESSES	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dram_config.h	Modified
7	Corrected PLL SSCG setting in PLL manual configuration function.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
8	Changed the attribute volatile to driver context variable.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Modified
9	Adds re-training detection, direction with new driver context fields based on tDQS2DQ value	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.c	Added
10	Adds the feature for the retraining detection, adds additional functions for the AXI performance counter usage.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_lpddr4.h	Added
11	Updates LPDDR4 default config from the Solution Designer.	TVII-SampleSW/tviic2d6mddr/src/drivers/lpddr4/cy_dramconfsel.h	Modified
12	Fixes the opcode bug in API's Cy_Flash_ConfigureFMIntr() and Cy_Flash_ConfigureFMIntr1() from flash driver.	TVII-SampleSW/common/src/drivers/flash/cy_flash.c	Modified

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