# PROT: SMPU_PC: cm4

- **Description**:
  - This example uses SMPUs to verify the functionality of the PC (Protection context).
  - The CM4 tries to access the prohibited memory area, and the CM0+ catches the details of violation by fault reporting system.
    - Setting MSx_CTL (in SMPU) to allow the PC bits of the PROT_MPU register to be changed to "6"
    - Setting the PC bits of the PROT_MPU register of the CM4 to "6"
    - Setting SMPU STRUCTURE2 so that only masters who have "6" as PC value can access the area (1).
    - Setting SMPU STRUCTURE3 so that only masters who have "5" as PC value can access the area (2).
    - Accessing the area (1) to confirm the CM4 can access the area.
    - Accessing the area (2) to confirm the CM4 can’t access the area and causes HardFault.
    - The CM0+ was notified of the violation details by the fault reporting system.

- **Target Device**:
  - Traveo-II CYT2Bx devices

- **CPU Board**:
  - CYTVII-B-E-1M-176-CPU Rev. C Board

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- **Dependency:**

- **Expectation**:
  - CM4 core gets into a hard fault handler.
  - CM0+ blinks an LED continuously in its fault report handler.

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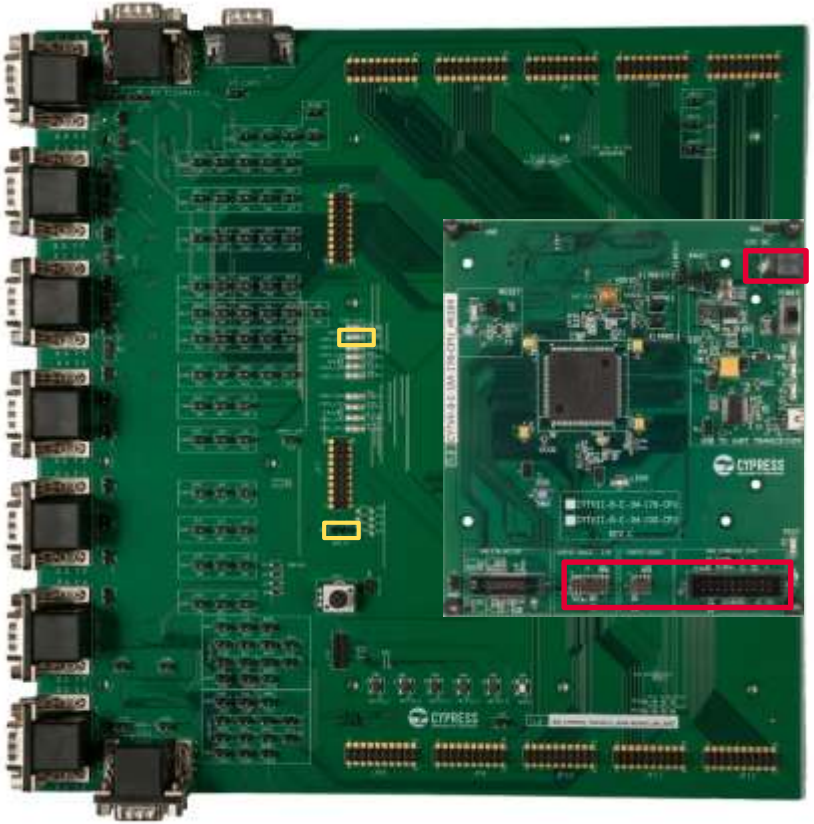

- **Legend**:
  - Red block for power, debug (Mandatory)
  - Yellow block for the example specific connections