

## TRAVEO™ T2G Sample Driver Library (SDL) FOSS Report

### Arm® CMSIS v5.9.0:

Open source link: [https://github.com/ARM-software/CMSIS\\_5/releases/tag/5.9.0](https://github.com/ARM-software/CMSIS_5/releases/tag/5.9.0)  
[https://github.com/ARM-software/CMSIS\\_5/tree/5.9.0](https://github.com/ARM-software/CMSIS_5/tree/5.9.0)

These contain Apache 2.0 license text as part of the files.

CMSIS Core: [https://github.com/ARM-software/CMSIS\\_5/tree/5.9.0/CMSIS/Core/Include](https://github.com/ARM-software/CMSIS_5/tree/5.9.0/CMSIS/Core/Include)

### Comparison between CMSIS files used in SDL and Arm® CMSIS files:

Name	Size	Modified		Name	Size	Modified
■ cache1_armv7.h	12,070	23-08-2022 09:44:41	✗	■ cache1_armv7.h	12,087	02-05-2022 16:26:44
■ cmsis_armcc.h	27,911	23-08-2022 09:44:41	✗	■ cmsis_armcc.h	27,999	02-05-2022 16:26:44
■ cmsis_armclang.h	47,770	23-08-2022 09:44:41	✗	■ cmsis_armclang.h	48,417	02-05-2022 16:26:44
■ cmsis_armclang_ltm.h	55,364	23-08-2022 09:44:41	✗	■ cmsis_armclang_ltm.h	56,021	02-05-2022 16:26:44
■ cmsis_compiler.h	4,675	23-08-2022 09:44:41	✗	■ cmsis_compiler.h	9,481	02-05-2022 16:26:44
■ cmsis_diab.h	3,449	31-03-2022 19:33:59	✗			
■ cmsis_gcc.h	62,712	23-08-2022 09:44:41	✗	■ cmsis_gcc.h	63,374	02-05-2022 16:26:44
■ cmsis_ghs.h	3,249	09-03-2022 11:59:50	✗			
■ cmsis_iccarm.h	28,334	23-08-2022 09:44:41	✗	■ cmsis_iccarm.h	29,069	02-05-2022 16:26:44
■ cmsis_version.h	1,676	23-08-2022 09:44:41	✗	■ cmsis_version.h	1,680	02-05-2022 16:26:44
				■ core_armv8mbl.h	115,004	02-05-2022 16:26:44
				■ core_armv8mml.h	183,191	02-05-2022 16:26:44
				■ core_armv8tmmh.h	276,640	02-05-2022 16:26:44
				■ core_cm0.h	41,643	02-05-2022 16:26:44
■ core_cm0plus.h	51,126	23-08-2022 09:44:41	✗	■ core_cm0plus.h	49,877	02-05-2022 16:26:44
				■ core_cm1.h	42,626	02-05-2022 16:26:44
■ core_cm4.h	123,466	23-08-2022 09:44:41	✗	■ core_cm3.h	109,529	02-05-2022 16:26:44
■ core_cm7.h	138,927	23-08-2022 09:44:41	✗	■ core_cm4.h	120,975	02-05-2022 16:26:44
				■ core_cm7.h	138,948	02-05-2022 16:26:44
				■ core_cm23.h	121,556	02-05-2022 16:26:44
				■ core_cm33.h	189,524	02-05-2022 16:26:44
				■ core_cm35p.h	189,539	02-05-2022 16:26:44
				■ core_cm55.h	317,450	02-05-2022 16:26:44
				■ core_cm85.h	308,328	02-05-2022 16:26:44
				■ core_sc000.h	46,562	02-05-2022 16:26:44
				■ core_sc300.h	108,524	02-05-2022 16:26:44
				■ core_starmc1.h	193,055	02-05-2022 16:26:44
■ mpu_armv7.h	11,727	23-08-2022 09:44:41	✗	■ mpu_armv7.h	11,731	02-05-2022 16:26:44
				■ mpu_armv8.h	11,370	02-05-2022 16:26:44
				■ pac_armv8l.h	6,062	02-05-2022 16:26:44
				■ pmu_armv8.h	22,786	02-05-2022 16:26:44
				■ tz_context.h	2,687	02-05-2022 16:26:44

Left side is the list of files used in SDL, RED marker shows the files which are modified.

### cmsis\_compiler.h:

- GHS and Windriver DIAB support added

<pre> 1  /** 2  * @file   cmsis_compiler.h 3  * @brief  CMSIS compiler generic header file 4  * @version V5.1.0 5  * @date   09. October 2018 6  */ 7  /** 8  * IAR Compiler 9  */ 10 #elif defined ( __ICCARM__ ) 11 #include &lt;cmsis_iccarm.h&gt; 12 13 /** 14 * GHS Compiler 15 */ 16 #elif defined ( __ghs__ ) 17 #include &lt;cmsis_ghs.h&gt; 18 19 /** 20 * Wind River DIAB Compiler 21 */ 22 #elif defined ( __DCC__ ) 23 #include &lt;cmsis_diab.h&gt; </pre>	<pre> 1  /** 2  * @file   cmsis_compiler.h 3  * @brief  CMSIS compiler generic header file 4  * @version V5.1.0 5  * @date   09. October 2018 6  */ 7  /** 8  * IAR Compiler 9  */ 10 #elif defined ( __ICCARM__ ) 11 #include &lt;cmsis_iccarm.h&gt; 12 13 /** 14 * TI Arm Compiler 15 */ 16 #elif defined ( __TI_ARM__ ) 17 #include &lt;cmsis_ccs.h&gt; </pre>
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## core\_cm0plus.h:

- GHS support added

<pre> 1  /***** 2  * @file    core_cm0plus.h 3  * @brief   CMSIS Cortex-M0+ Core Peripheral Access Layer Header File 4  * @version V5.0.9 5  * @date    21. August 2019 6  *****/ 7 8  #ifndef __CORE_CM0PLUS_H__ 9  #define __CORE_CM0PLUS_H__ 10 11 #if defined (__ICCARM__) 12 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 13 #endif 14 15 #if defined (__ghs__) 16 #if defined (__VFP__) 17 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 18 #endif 19 20 #if defined (__TI_ARM__) 21 #if defined (__TI_VFP_SUPPORT__) 22 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 23 #endif 24 #endif 25 26 #endif </pre>	<pre> 1  /***** 2  * @file    core_cm0plus.h 3  * @brief   CMSIS Cortex-M0+ Core Peripheral Access Layer Header File 4  * @version V5.0.9 5  * @date    21. August 2019 6  *****/ 7 8  #ifndef __CORE_CM0PLUS_H__ 9  #define __CORE_CM0PLUS_H__ 10 11 #if defined (__ICCARM__) 12 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 13 #endif 14 15 #if defined (__ghs__) 16 #if defined (__VFP__) 17 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 18 #endif 19 20 #if defined (__TI_ARM__) 21 #if defined (__TI_VFP_SUPPORT__) 22 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 23 #endif 24 #endif 25 26 #endif </pre>
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## core\_cm4.h:

- GHS support added

<pre> 1  /***** 2  * @file    core_cm4.h 3  * @brief   CMSIS Cortex-M4 Core Peripheral Access Layer Header File 4  * @version V5.1.1 5  * @date    27. March 2020 6  *****/ 7 8  /* Copyright (c) 2009-2020 Arm Limited. All rights reserved. 9 10 #ifndef __CORE_CM4_H__ 11 #define __CORE_CM4_H__ 12 13 #if defined (__ghs__) 14 #if defined (__VFP__) 15 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 16 #define __FPU_USED 1U 17 #else 18 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 19 #define __FPU_USED 0U 20 #endif 21 #else 22 #define __FPU_USED 0U 23 #endif 24 #endif 25 26 #if defined (__TI_ARM__) 27 #if defined (__TI_VFP_SUPPORT__) 28 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 29 #define FPU_USED 1U 30 #endif 31 #endif 32 #endif 33 34 #endif </pre>	<pre> 1  /***** 2  * @file    core_cm4.h 3  * @brief   CMSIS Cortex-M4 Core Peripheral Access Layer Header File 4  * @version V5.1.2 5  * @date    04. June 2021 6  *****/ 7 8  /* Copyright (c) 2009-2020 Arm Limited. All rights reserved. 9 10 #ifndef __CORE_CM4_H__ 11 #define __CORE_CM4_H__ 12 13 #if defined (__ghs__) 14 #if defined (__VFP__) 15 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 16 #define __FPU_USED 1U 17 #else 18 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 19 #define __FPU_USED 0U 20 #endif 21 #else 22 #define __FPU_USED 0U 23 #endif 24 #endif 25 26 #if defined (__TI_ARM__) 27 #if defined (__TI_VFP_SUPPORT__) 28 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 29 #define FPU_USED 1U 30 #endif 31 #endif 32 #endif 33 34 #endif </pre>
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## core\_cm7.h:

- GHS support added

<pre> 1  /***** 2  * @file    core_cm7.h 3  * @brief   CMSIS Cortex-M7 Core Peripheral Access Layer Header File 4  * @version V5.1.2 5  * @date    27. March 2020 6  *****/ 7 8  /* Copyright (c) 2009-2020 Arm Limited. All rights reserved. 9 10 #ifndef __CORE_CM7_H__ 11 #define __CORE_CM7_H__ 12 13 #if defined (__ghs__) 14 #if defined (__VFP__) 15 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 16 #define __FPU_USED 1U 17 #else 18 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 19 #define __FPU_USED 0U 20 #endif 21 #else 22 #define __FPU_USED 0U 23 #endif 24 #endif 25 26 #if defined (__TI_ARM__) 27 #if defined (__TI_VFP_SUPPORT__) 28 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 29 #define FPU_USED 1U 30 #endif 31 #endif 32 #endif 33 34 #endif </pre>	<pre> 1  /***** 2  * @file    core_cm7.h 3  * @brief   CMSIS Cortex-M7 Core Peripheral Access Layer Header File 4  * @version V5.1.6 5  * @date    04. June 2021 6  *****/ 7 8  /* Copyright (c) 2009-2021 Arm Limited. All rights reserved. 9 10 #ifndef __CORE_CM7_H__ 11 #define __CORE_CM7_H__ 12 13 #if defined (__ghs__) 14 #if defined (__VFP__) 15 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 16 #define __FPU_USED 1U 17 #else 18 #error "Compiler generates FPU instructions for a device without an FPU (check __FPU_PRESENT)" 19 #define __FPU_USED 0U 20 #endif 21 #else 22 #define __FPU_USED 0U 23 #endif 24 #endif 25 26 #if defined (__TI_ARM__) 27 #if defined (__TI_VFP_SUPPORT__) 28 #if defined (__FPU_PRESENT) &amp;&amp; (__FPU_PRESENT == 1U) 29 #define FPU_USED 1U 30 #endif 31 #endif 32 #endif 33 34 #endif </pre>
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