Lab #1 Xilinx Tool Flow,Pins Assignment, Pins Assignment , UART on Zybo PL

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1 Objectives

Lab1 includes two parts,the total tasks have been showed below:

(1) Implement the UART circuit from Xilinx on the PL fabric of Zybo only.

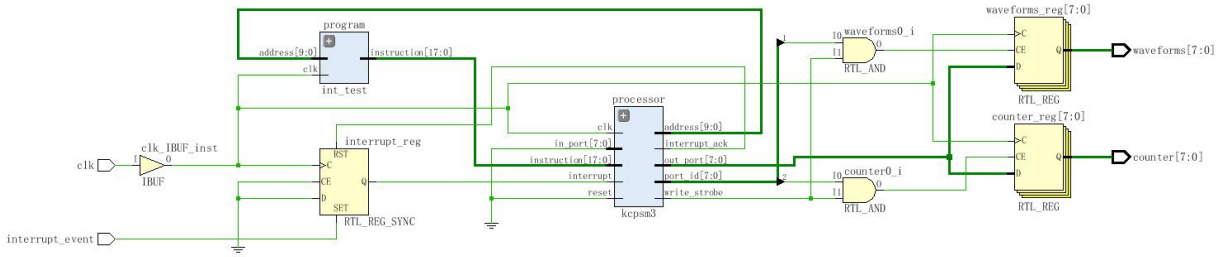
(2) Connect a SparkFun 3.3V FTDI Basic Breakout to SelectIO pins on a Pmod

(3) Demonstrate your UART transmit and receive on a Terminal of laptop

2 Part 1 : Xilinx Tool Flow

Create,Simulate and Implement kcpsm3_int_test.v Circuit

Select file kcpsm3_int_test.v as the top-level circuit. Choose "Open Elaborated Design" to see the top-level circuit schematic of this file as follows.



Simulate the Circuit

Click on Untitle1 in the following case to see the resulting simulation waveforms.

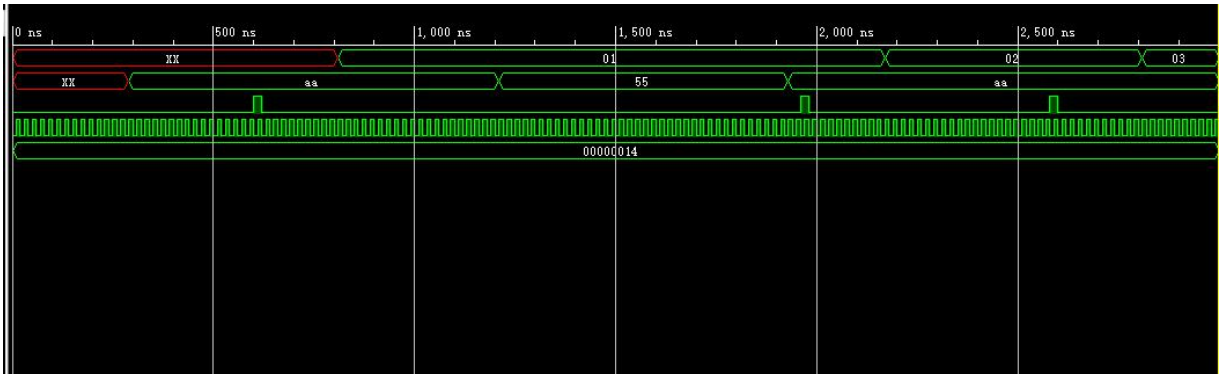


Figure 11. Behaviour Simulation Results [1] runtime=3000ns from Lab #1 of Xilinx

Analyze the Internal Signals of a Circuit over Scope

Monitor internal signals by adding them to the design,add interrupt, interrupt_ack, and instruction signals to the waveform display.Change radix of address and instructions to hexadecimal and Re-Simulate.

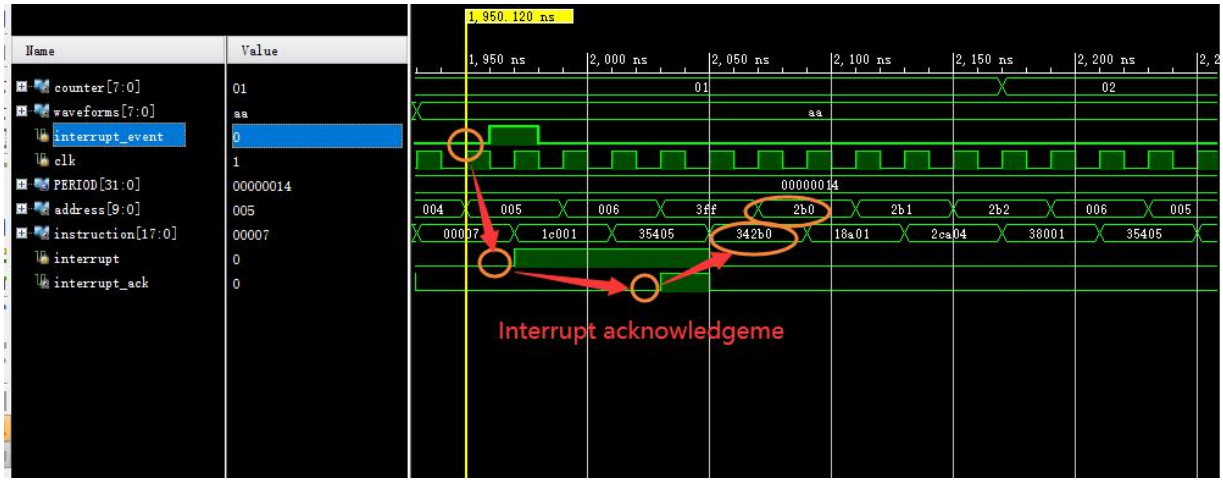


Figure 13. Interrupt Service Routime from Lab #1 of Xilinx

Change simulation run time to 25000ns, add write_strobe signal and re-simulate the design. Analyze the output waveform process (Figure 14).

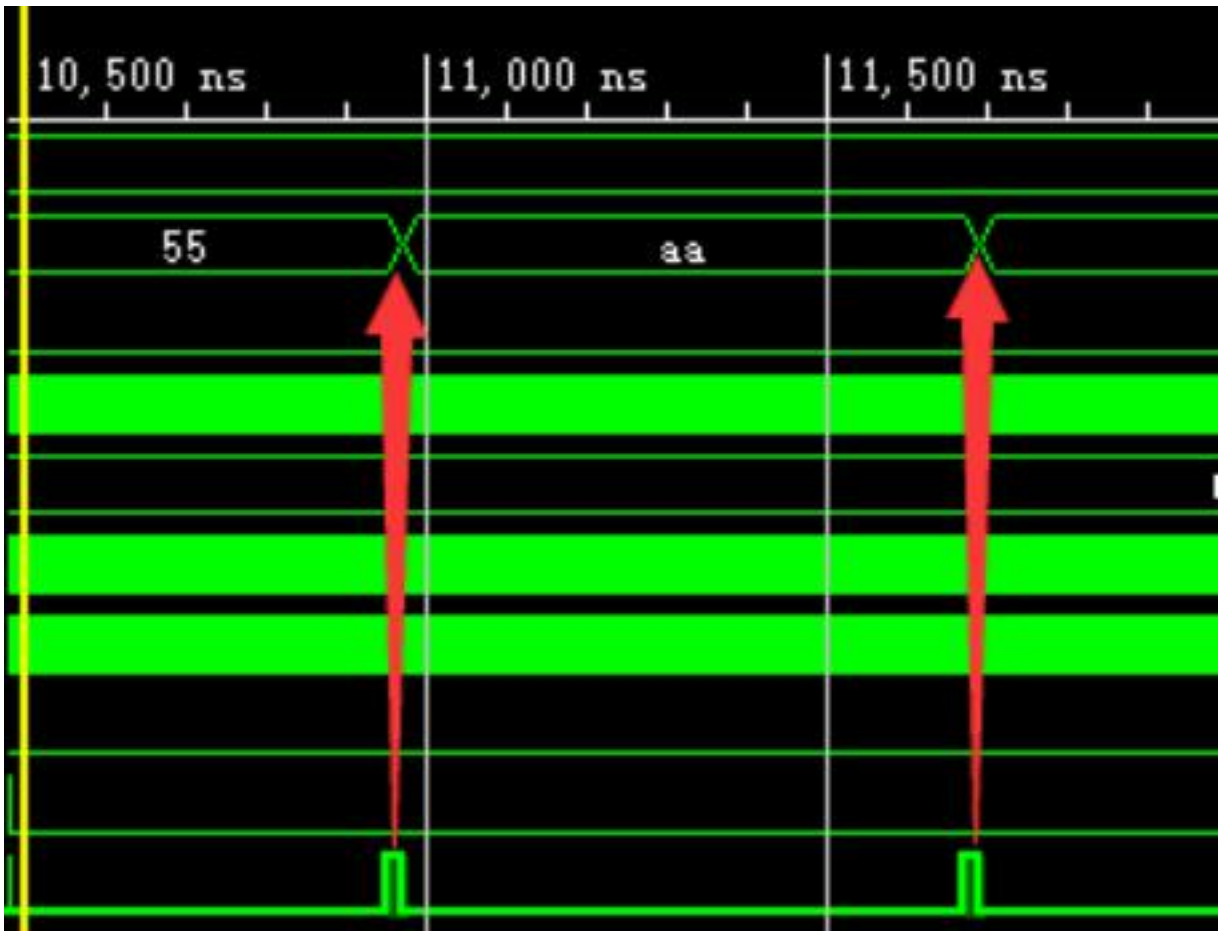
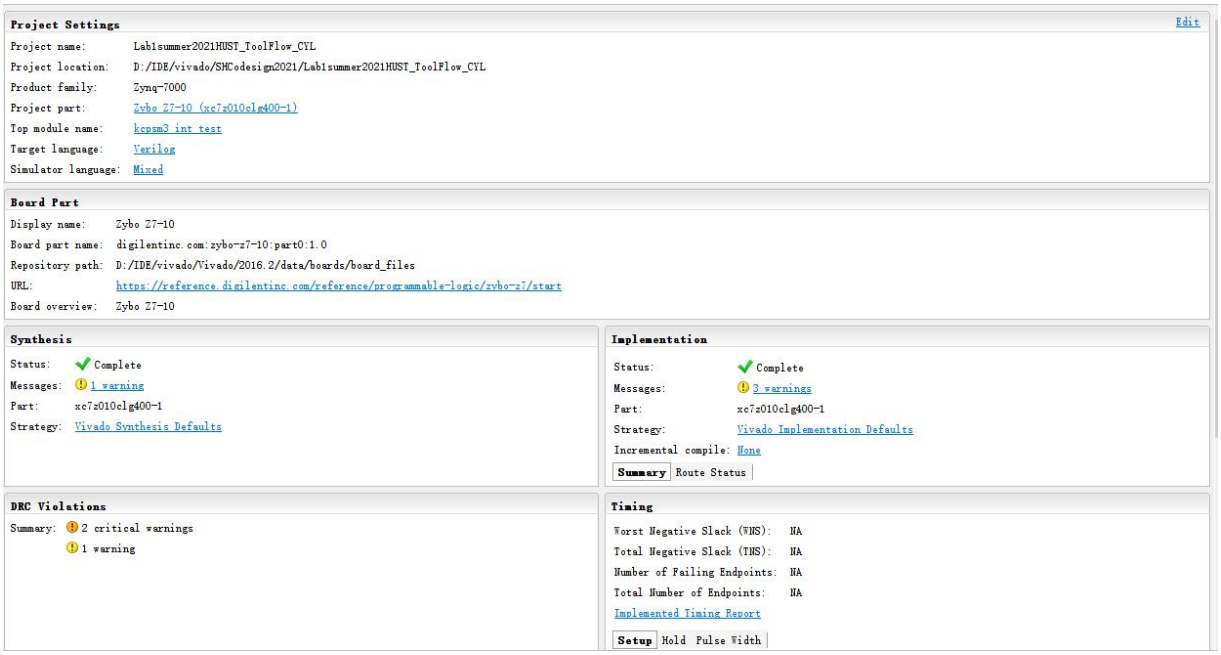


Figure 14. Output Waveforms from Lab #1 of Xilinx

Click on Project Manager at the upper left corner to see Project Summary.Project Summary Overview is copied below.



Project Settings (Edit)

Project name:	Lab1summer2021HUST_ToolFlow_CYL
Project location:	D:/IDE/vivado/SMCodesign2021/Lab1summer2021HUST_ToolFlow_CYL
Product family:	Zynq-7000
Project part:	Zybo Z7-10 (xc7z010clg400-1)
Top module name:	kcpsm3_int_test
Target language:	Verilog
Simulator language:	Mixed

Board Part

Display name:	Zybo Z7-10
Board part name:	digilentinc.com:zybo-z7-10:part0:1.0
Repository path:	D:/IDE/vivado/Vivado/2016.2/data/boards/board_files
URL:	https://reference.digilentinc.com/reference/programmable-logic/zybo-z7/start
Board overview:	Zybo Z7-10

Synthesis

Status:	Complete
Messages:	1 warning
Part:	xc7z010clg400-1
Strategy:	Vivado Synthesis Defaults

Implementation

Status:	Complete
Messages:	3 warnings
Part:	xc7z010clg400-1
Strategy:	Vivado Implementation Defaults
Incremental compile:	None

Summary | Route Status

DRC Violations

Summary: 2 critical warnings
1 warning

Timing

Worst Negative Slack (WNS):	NA
Total Negative Slack (TNS):	NA
Number of Failing Endpoints:	NA
Total Number of Endpoints:	NA

Implemented Timing Report

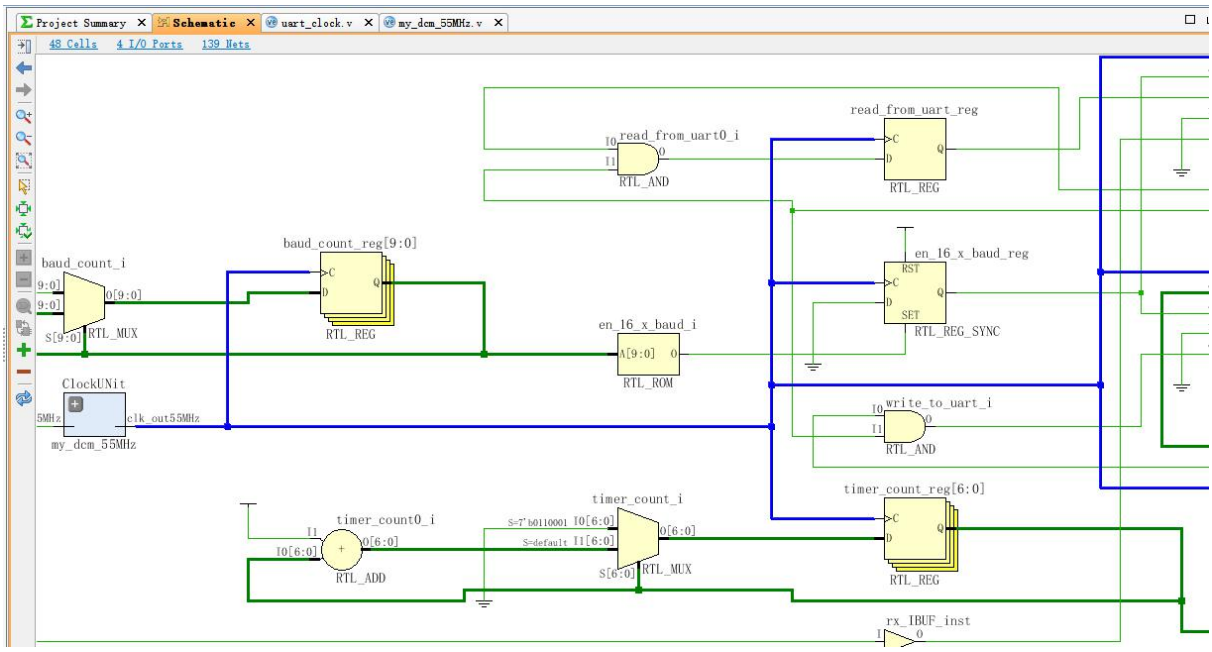
Setup | Hold | Pulse Width

Table 17. Design Summary from Lab #1 of Xilinx.

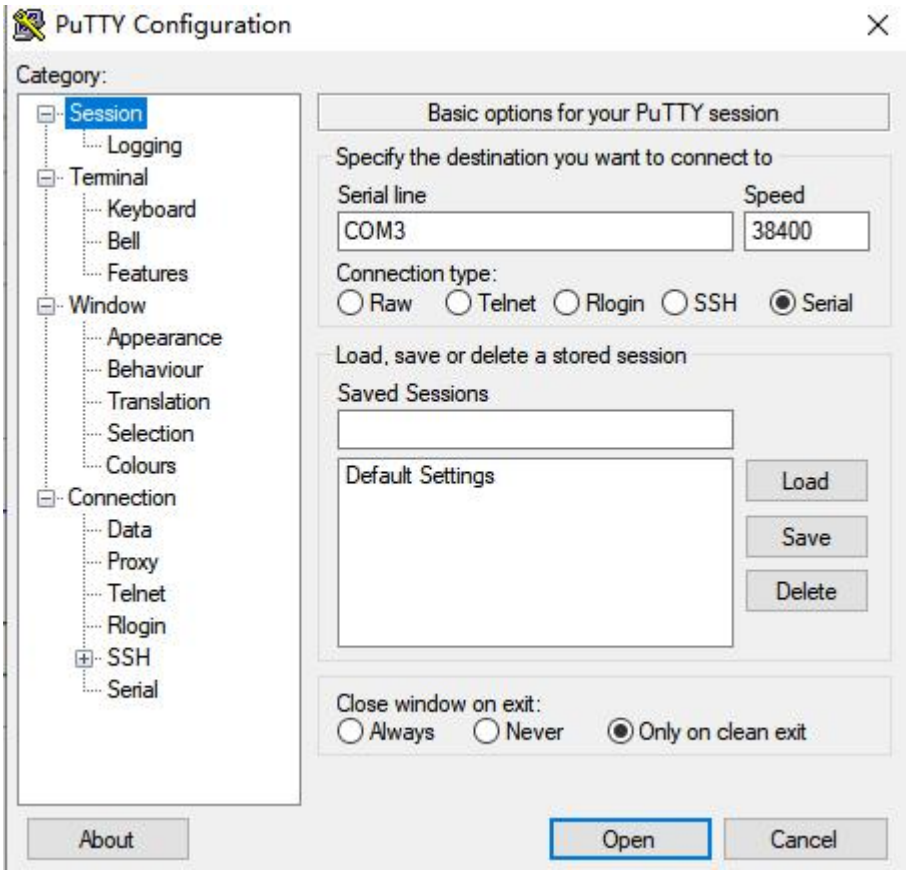
3 Part 2 : Architecture Wizard and Pins Assignment from Lab #2 of Xilinx

This part is to create a UART real-time clock and add it to Zybo so that UART can work normally while send and receive data.To realize the function, creating a clock IP to generate 55MHz clock from 125MHz Crystal Oscillator is the first thing to do.Then , I create a module named by my_dcm_55MHz.v. Finally, add one signal lock to uart_clock.v.

Open top-level schematic to see the clock module is connected to circuit as shown below

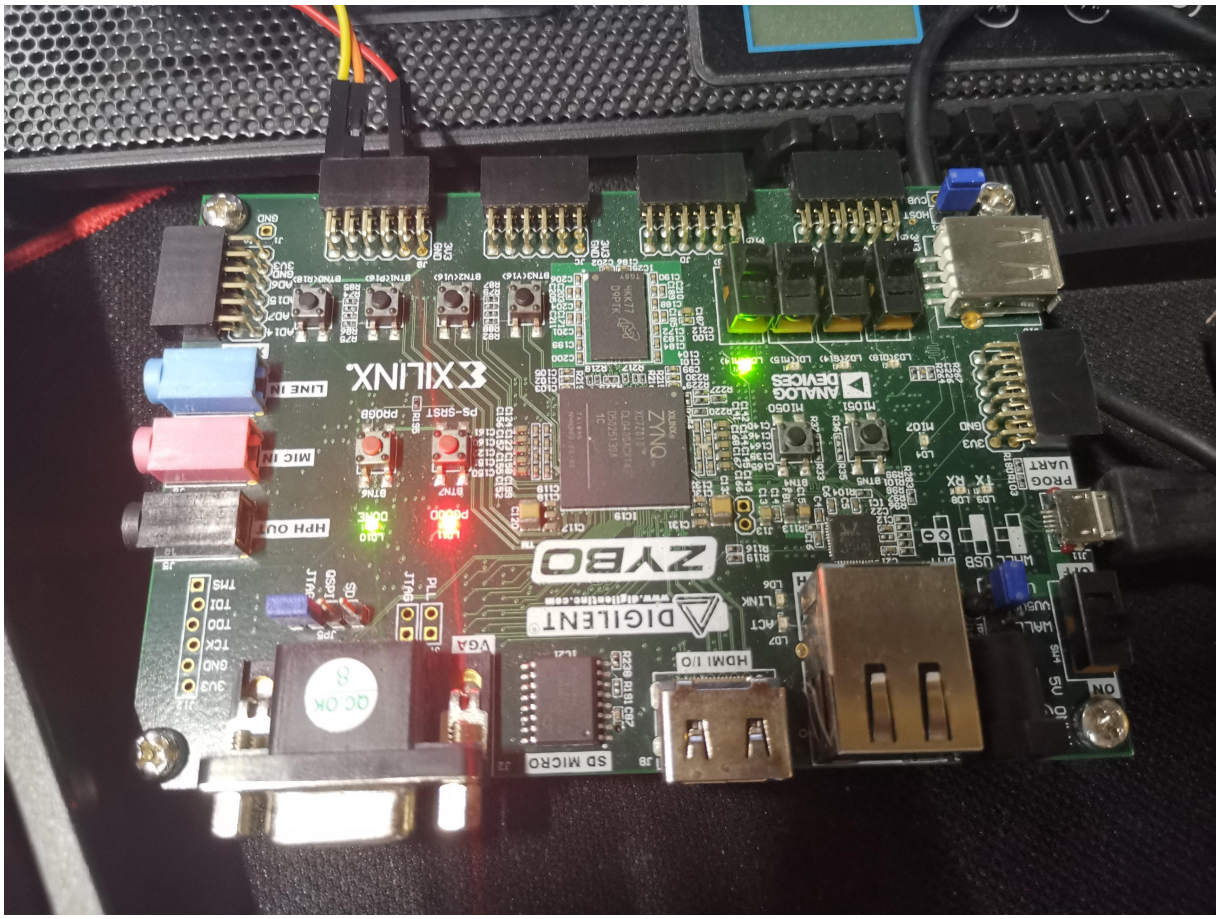


Test uart_clock circuit with a serial terminal

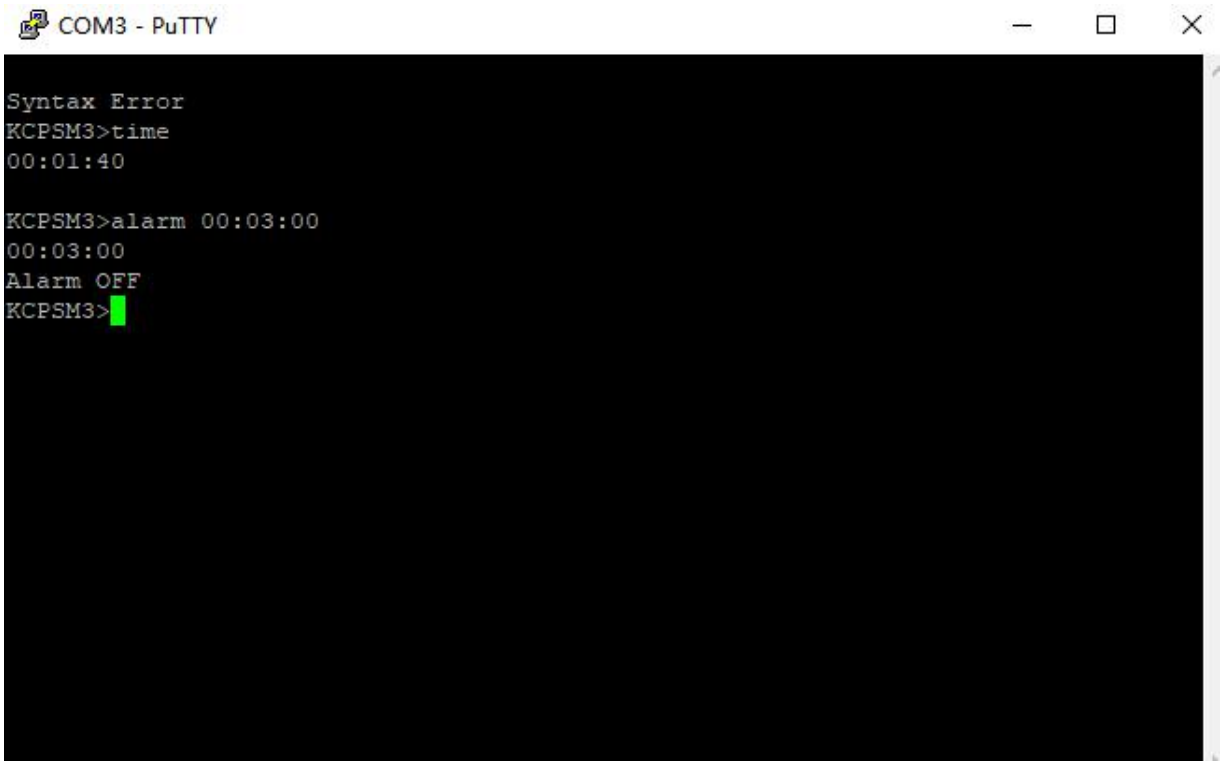


Show the real time

When the ZYBO is connected to PC ,we can see the LD0,LD10 and LD11 are on

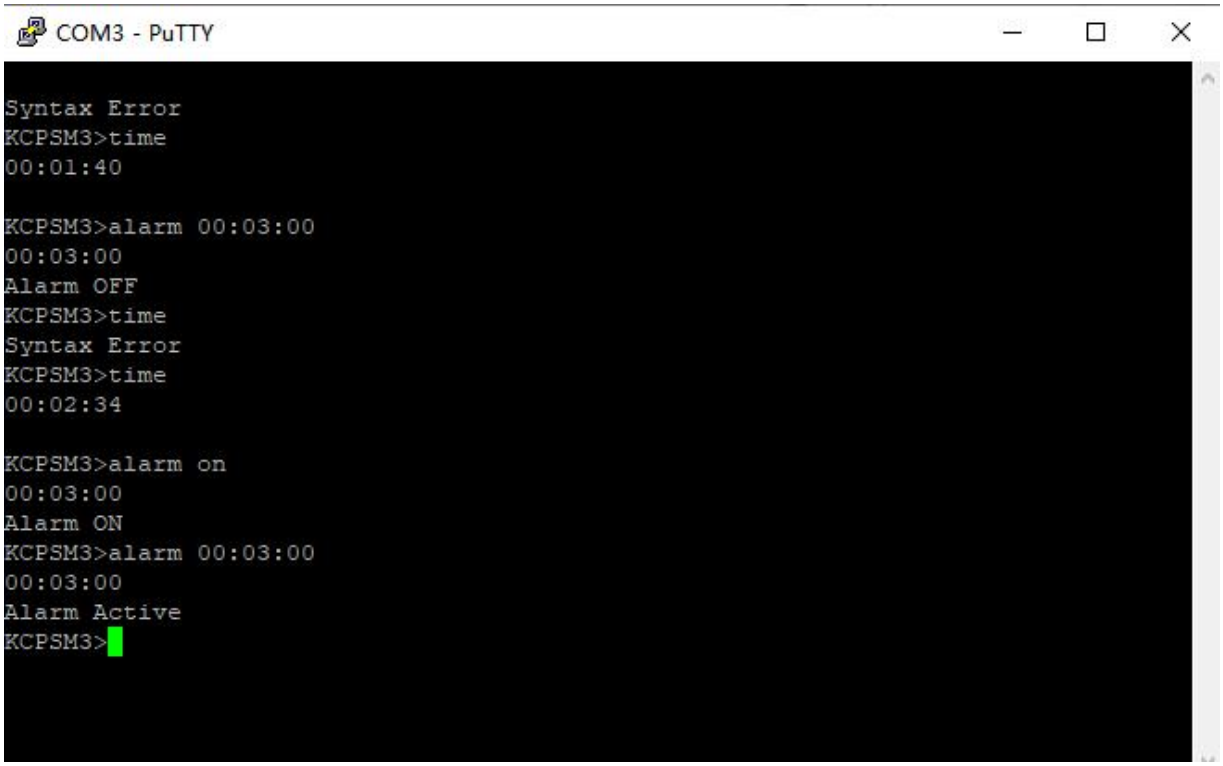


Set the LD3 will light on when the time reachs 00:03:00 the first time,we can see the alarm is off now

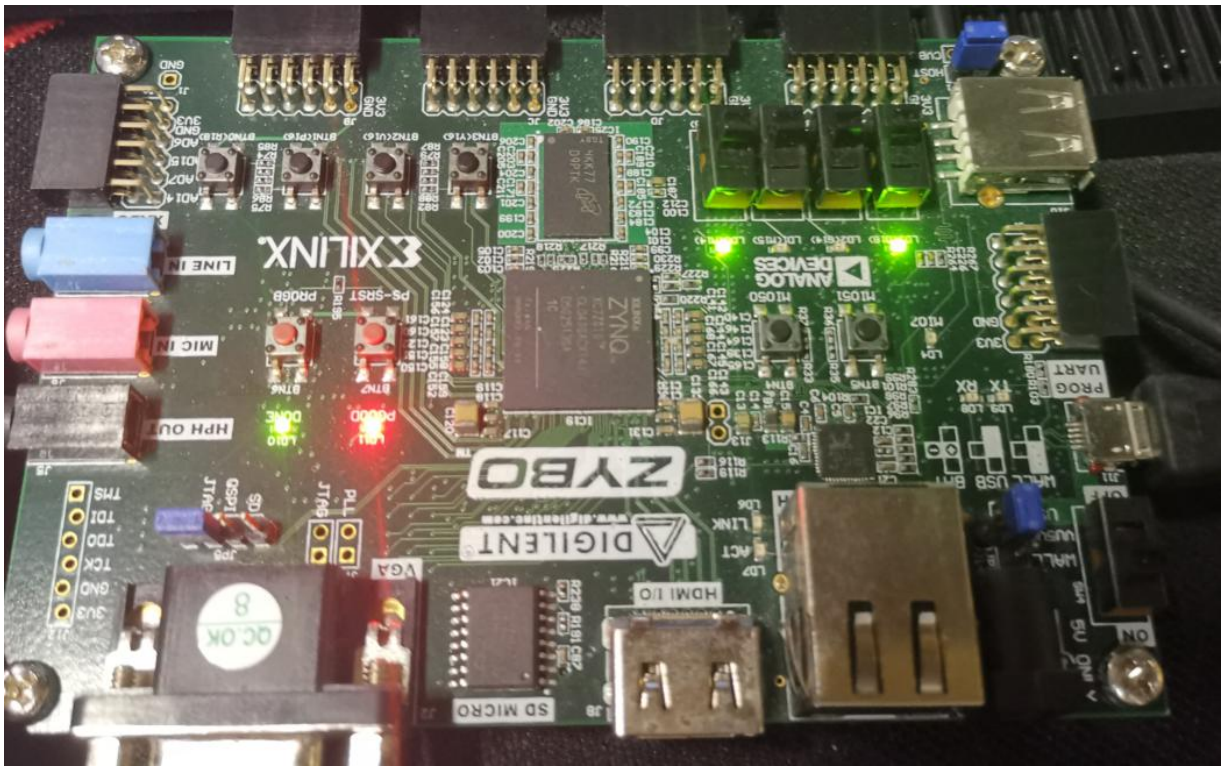


Enter "alarm on" to set up the alarm

Set the LD3 will light on when the time reachs 00:03:00 the second time,we can see when the time reachs 00:03:00,the alarm is active and LD3 is on.



LD3 is on when the time reachs 00:03:00



4 Summary

Through this experiment, I learned how to implement UART circuit on Zybo's PL structurethe ,realized clock with timing function on Xilinx and serial communication.