Name _________________ ID __________ Due date: Friday, August 20, 2021

S&H Co-Design Homework #2 Handout Summer 2021

(Zynq-7010, xil_printf(), Zybo Board Interface Files)

Refer to the Zynq Book, Zybo Reference Manual (ZYBO_RM_B_V6.pdf), and Zynq-7000 Technical Reference Manual (ug585) and the other related Xilinx user guide (ugxxx) and data sheet (ds187) documents to answer the following questions.

1 Define the following terms as used in Zynq-7000 (Most definitions are copied from the Zynq Book.)

1.1 Processing System (PS)

1.2 Programmable Logic (PL)

1.3 Multiplexed IO (MIO)

1.4 Extended Multiplexed IO (EMIO)

1.5 AXI 3.0

1.6 SelectIO

1.7 GPIO

2 *The Zybo's Zynq-7010 chip bears the following marking: "XC7Z010-1CLG400C". It uses the "Ball Grid Array" (BGA) pinout for maximum packaging density. Answer the following questions about the chip. Include sources and evidences to support your answers such as document names and page numbers etc.*

2.1 What is the maximum number of physical pin connections available with this particular BGA layout? (Hint: see ug865)

2.2 What is the vertical and horizontal spacing (pitch) between adjacent ball grid pins?

2.3 What are the overall physical dimensions of the Zybo's Zynq chip?

2.4 How many processing system (PS) I/O pins are available?

2.5 How many programmable logic (PL) ("Select I/O") single-ended I/O pins are available?

2.6 How many programmable logic (PL) ("Select I/O") differential I/O pairs pin pairs are available?

3 Find out if I/O pins on the Zybo board are mapped to either MIO or Select I/O pins from ZYBO FPGA Board Reference Manual 2016 available from https://reference.digilentinc.com/_media/zybo:zybo_rm.pdf.

3.1 Circle the components on Zybo below that are connected to MIO pins.

○ LED4

○ HDMI

○ SPI

○ LEDs LD3-0

○ UART 1

○ USB 0

○ SDIO 0

○ LED4

○ BTN4

○ Push Buttons BTN3-0

○ BTN5

○ Pmod JA

3.2 Find where MicroSD interface pins are connected, Select I/O or MIO, and their pin numbers? You can include screen shots as your answer.

3.3 Find where HDMI interface pins are connected, Select I/O or MIO, and their pin numbers? Include screen shots to support your answer.

4 *Describe major differences between printf() and xil_printf() and why and when xil_printf() is better than printf(). (Hint: read the header of xil_printf().c source code.) Include screen shots to support your conclusion.*

5 *Read the source code for xil_printf(), describe what it does and how it is implemented to accomplish its function. Include screen shot or reference pages to support your conclusion.*

5.1 *Where is the base address of the STDOUT and STDIN. Describe the call structure and how the driver knows the base address of UART 1.*

5.2 *Describe the call structure and how*

5.3 *5.3 How does xil_printf() know where or which com port, to send its formatted character string?*

5.4 *How are data received and transmitted?*

5.5 *Are the sending and transmitting subroutines interrupt-driven or blocking calls?*

5.6 *Indicate how Level 1 driver of xil_printf() relates to Level 0 driver of uart device. Hint: xil_printf() uses outbyte() from uartps_3_0 library, which sends data to UART 1. Include screen captures to support your answer.*

6 Zybo Board Interface Files. Use XML Notepad from Microsoft to describe how Pmod Connector JC is defined in Board Support File A.0 for zybo-z7-10. Include screen captures to support your description. (zybo-z7-10 board files can be downloaded from https://github.com/Digilent/vivado-boards/archive/master.zip. XML Notepad is available from http://www.lovettsoftware.com/downloads/xmlnotepad/readme.htm.)

6.1 How is the component defined?

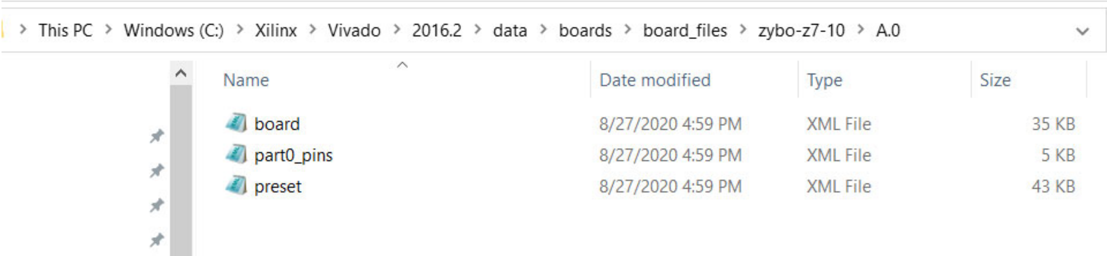
6.2 How is connection defined?

6.3 Where in the board file and how is the interface defined?

6.4 How are the pins described and mapped between logical and physical pins?

The board interface file is under directory: C:\Xilinx\Vivado\2016.2\data\boards\board_files\zybo-z7-10.

The xml files can be reviewed and edited with the free Microsoft XML Notepad available from Microsoft Download Center. Or at this website: http://www.lovettsoftware.com/downloads/xmlnotepad/XmlNotepad.application.



› This PC › Windows (C:) › Xilinx › Vivado › 2016.2 › data › boards › board_files › zybo-z7-10 › A.0

Name	Date modified	Type	Size
board	8/27/2020 4:59 PM	XML File	35 KB
part0_pins	8/27/2020 4:59 PM	XML File	5 KB
preset	8/27/2020 4:59 PM	XML File	43 KB

6.1 The component is named jc

6.2 The connection is defined as part0_jc. The two components are part0 and jc.

6.3 How are interfaces defined? All interfaces are defined under the first component of part0, the chip definition.

6.4 The pins are described and mapped in part0_pins.xml file between logical and physical pins. However, pins 55 to 62 are not included in zybo-z7-10 A.0 part0_pins.xml file. They are given in zybo-z7-20 A.0 part0_pins.xml file as follows. JC1 to JC10 are connected to pins 55 to 62.each one is connected to a physical pin such as JC1 on V15, JC2 on W15, etc.