

Name: _____ CM: _____

Start Date: Monday, August 9, 2021
Due Date: Tuesday, August 10, 2021

Lab #0: Installation of Vivado Design Suite Version 2016.2, Zybo Files and Implementation of Gate3 on Zybo

1. Objectives and Deliverable

This prelab installation exercise has two objectives: to install Vivado Webpack Version 2016.2 and Zybo Files on your laptop and to implement and demonstrate your gate3.v circuit on your Zybo board.

Demonstrate your gate3 circuit on your Zybo to obtain credit for this lab.

2. Create a Xilinx Account

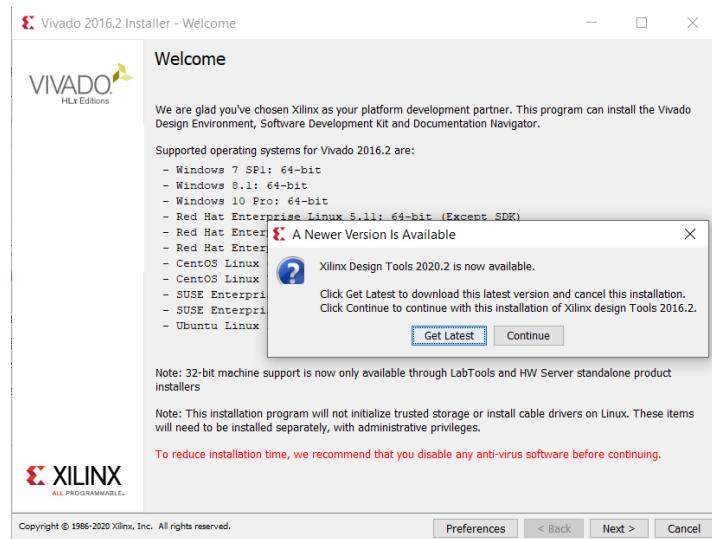
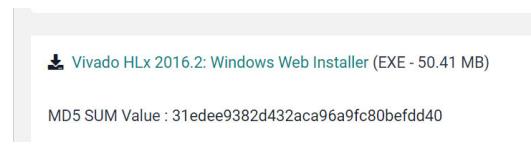
You will need a Xilinx account to install software. If you do not have a Xilinx account, go to www.xilinx.com and click on the body icon on the upper right corner to register and create a Xilinx account.

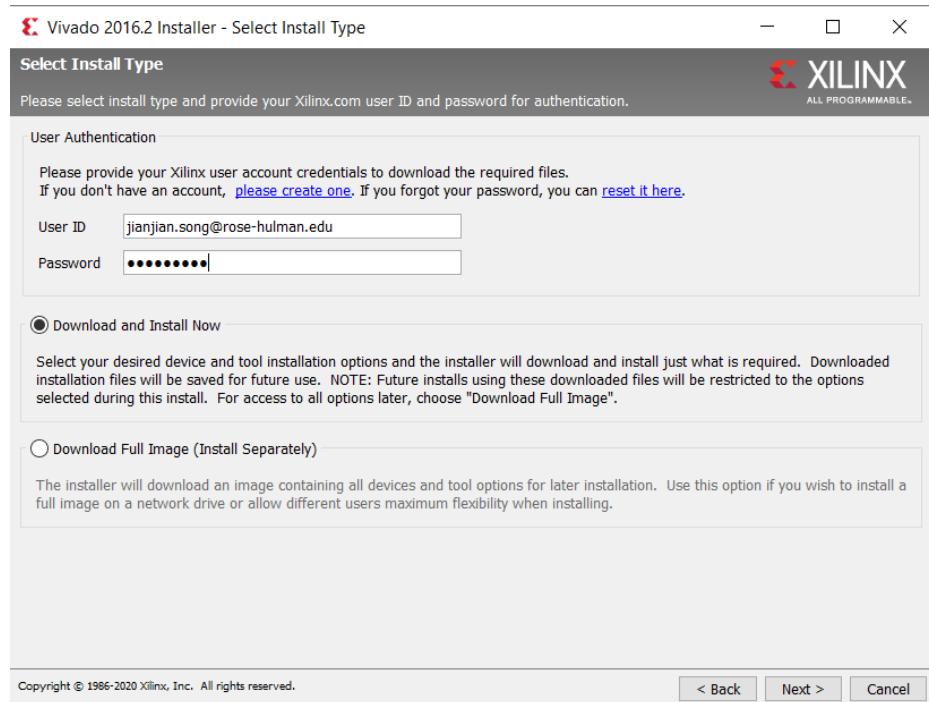
3. Install Xilinx Vivado Design Suite Software Version 2016.2 from Web Installer

Xilinx Vivado Design Suite Software is available from www.xilinx.com under Support->Services->/Downloads & Licensing. The latest version of Vivado is Version Vivado HLx 2020.2. We will not use this version as this installation requires up to 75 GB of disk space to install Vivado for hardware and Vitis for software development. If you installed other higher versions, you could uninstall them or keep them.

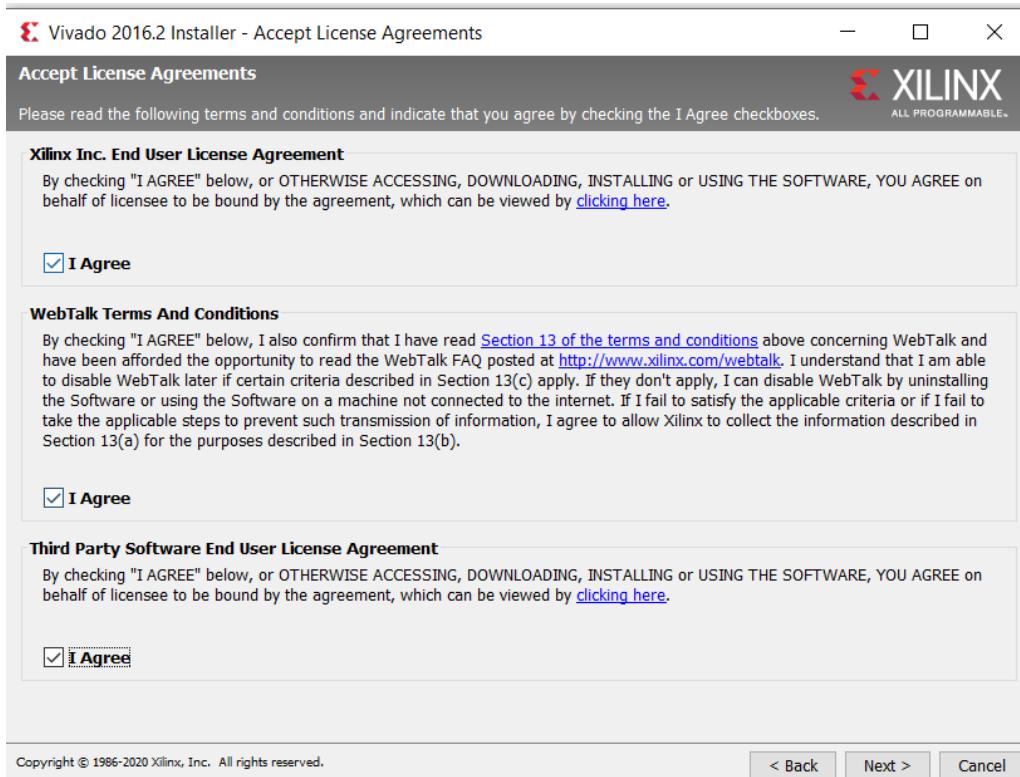
Vivado HLx 2016.2 will be used for this course since it will take about 4.7 GBs of disk space and the Xilinx workshop Version 2015 was only tested with Version HLx 2016.2.

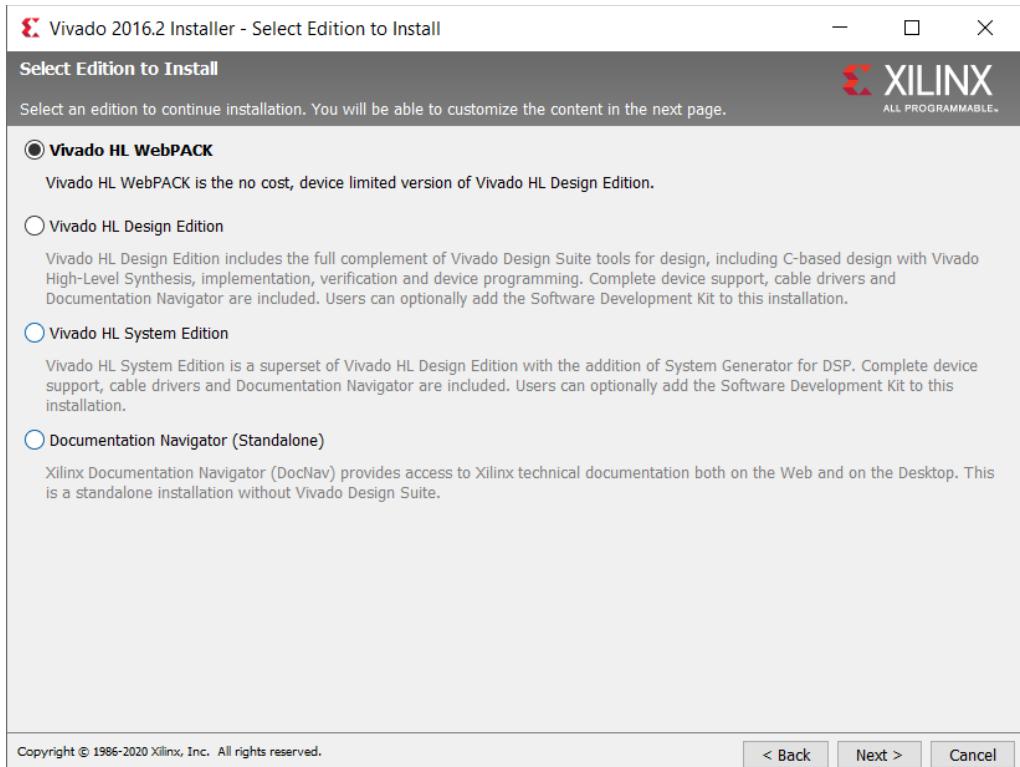
Vivado HLx 2016.2 can be found under Vivado Archive and click on Vivado HLx 2016.2: Windows Web Installer (EXE – 50.41 MB) to download the installer file: Xilinx_Vivado_SDK_2016.2_0605_1_Win64.exe. Execute this file to install 2016.2 version of Vivado HLx. Click Continue to install 2016.2 version when prompted to get latest version. Make sure to choose to install SDK as well, which is Software Development Kit.



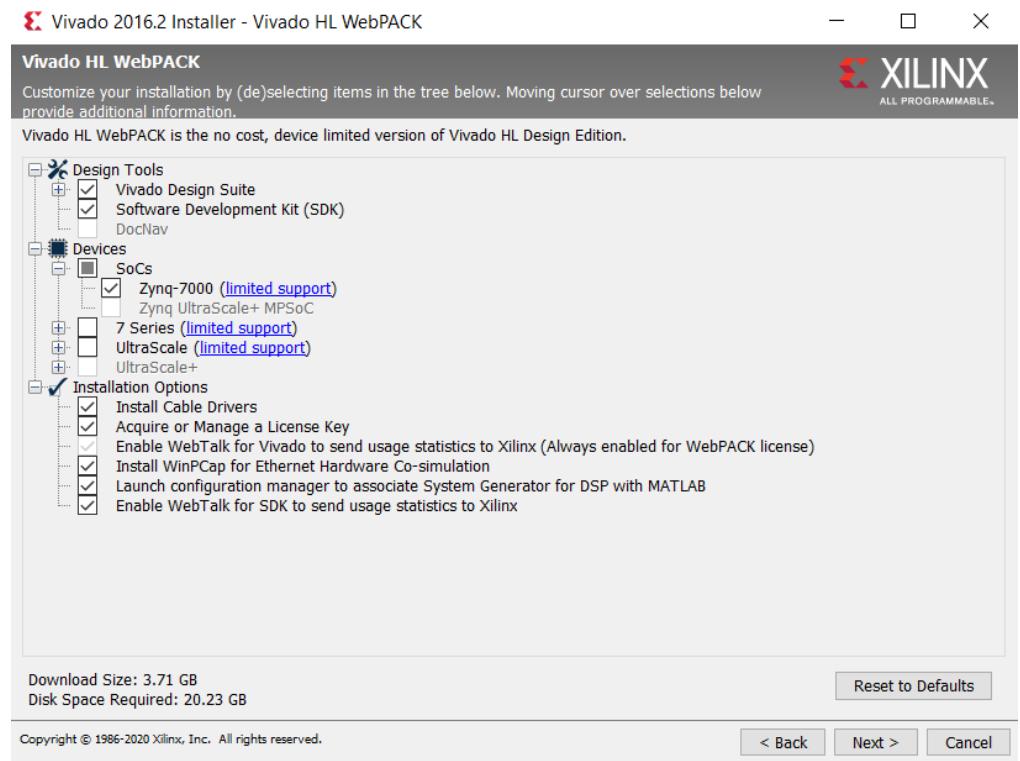


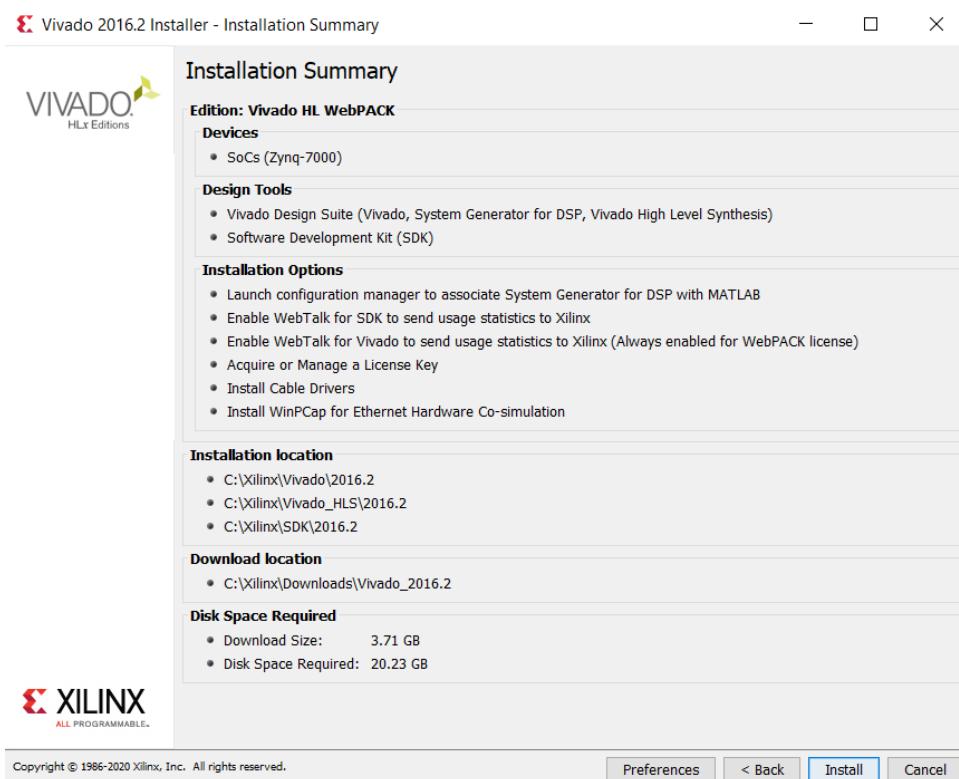
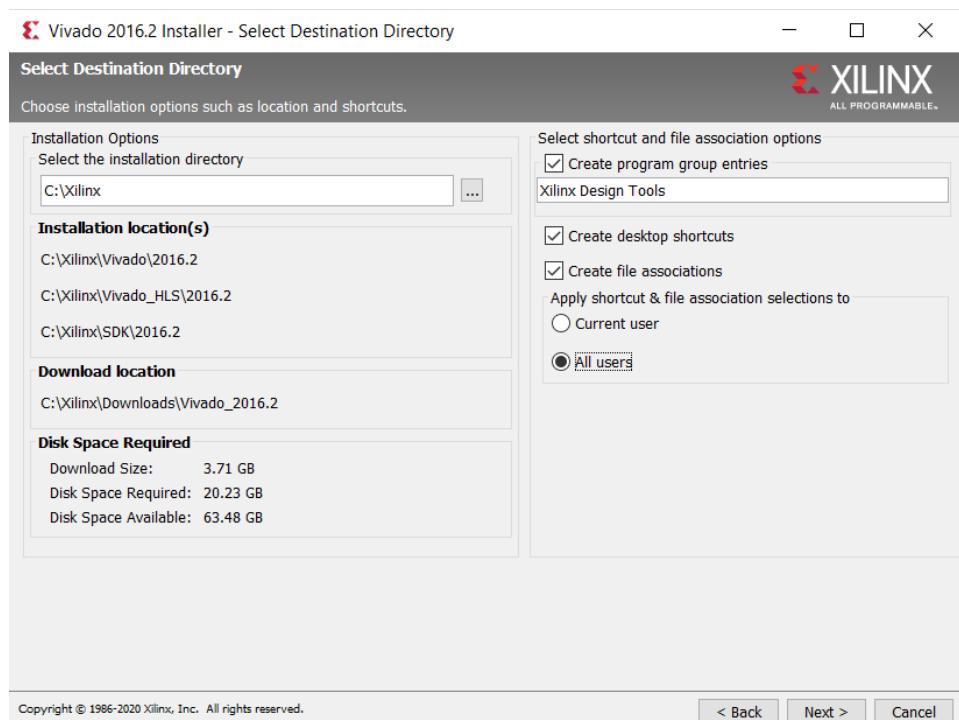
If you get an error that your account cannot be validated, you should try a few more times. Xilinx server will respond eventually.



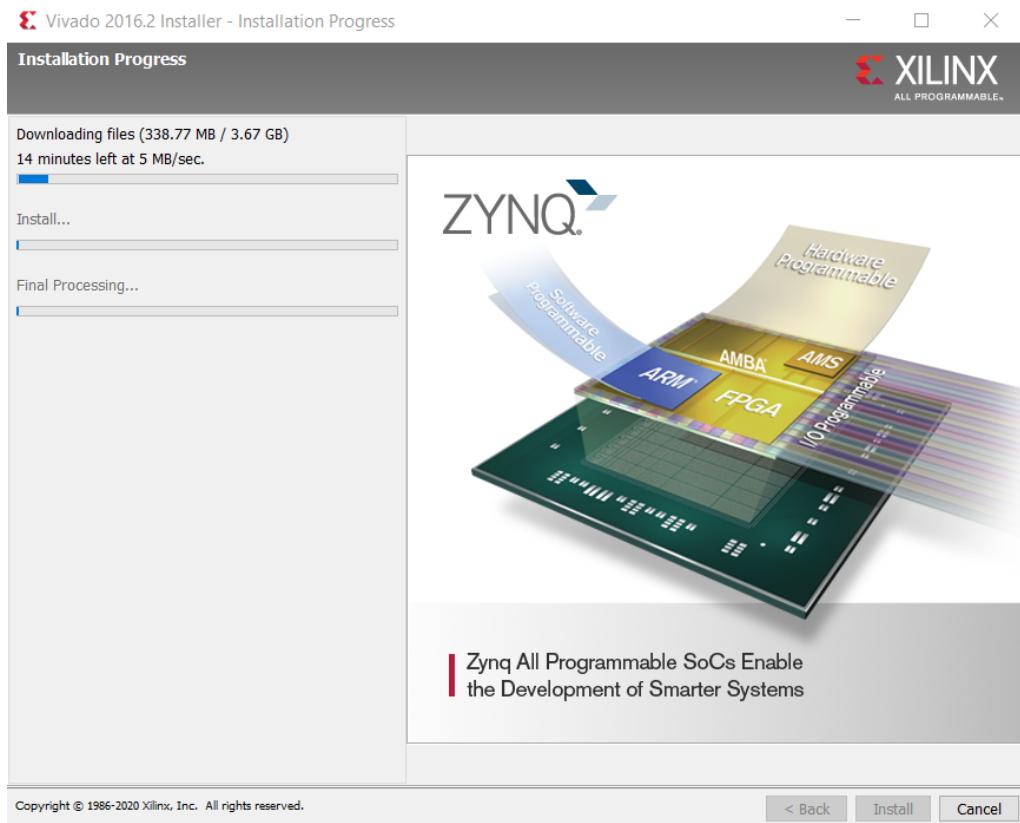


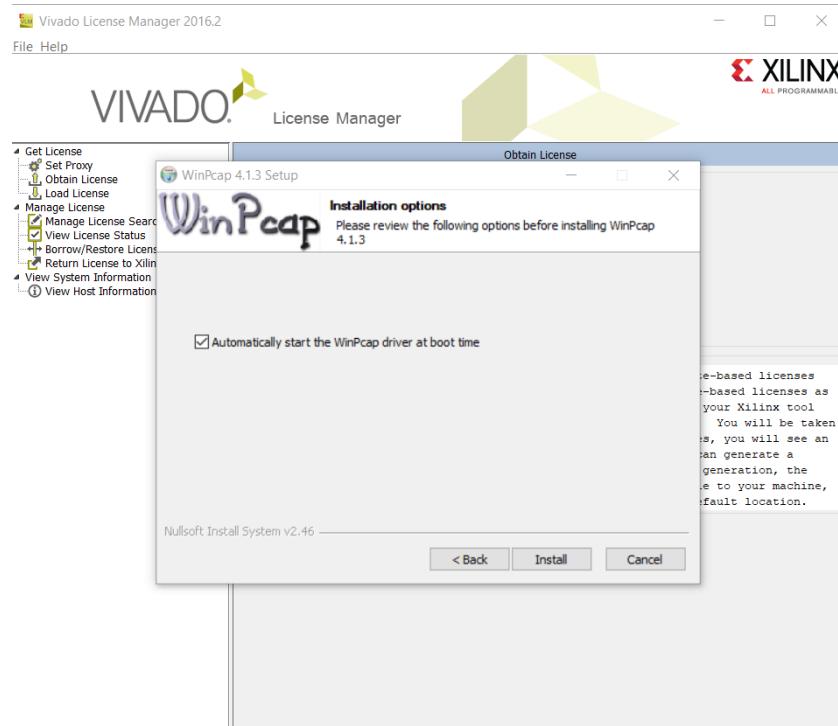
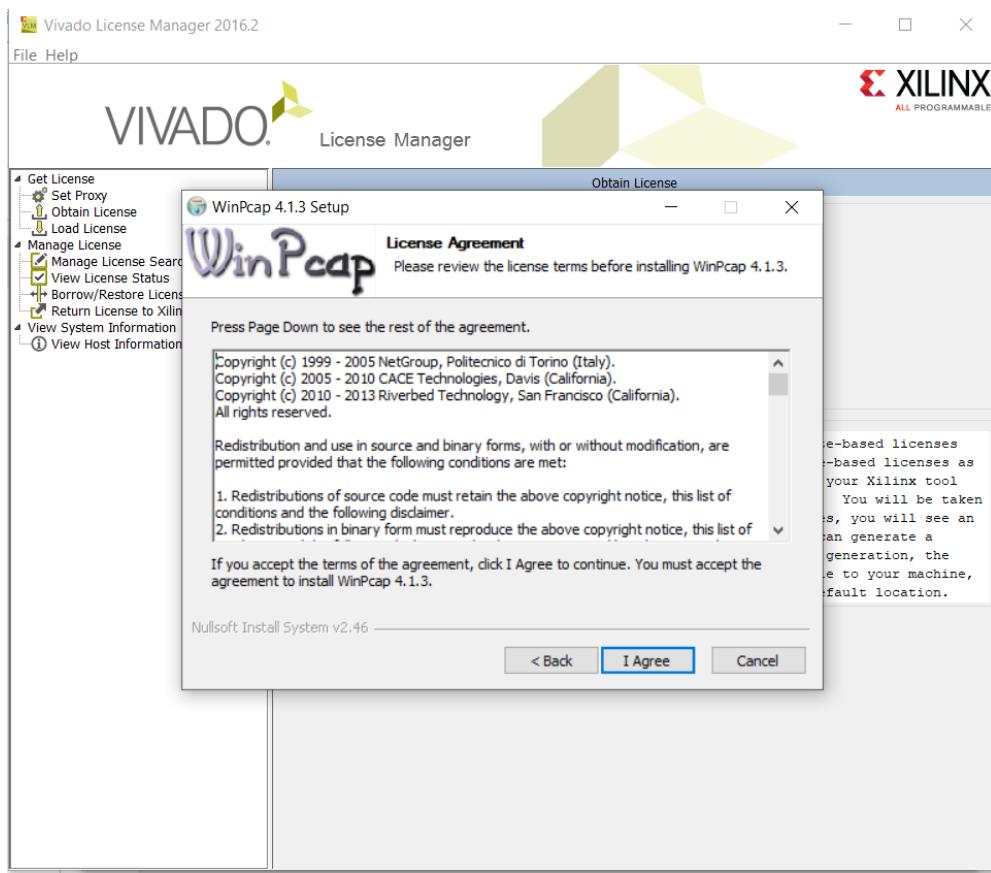
Make sure to check Vivado Design Suite for hardware design and Software Development Kit (SDK) for software design. We only need Zynq-7000 chips which is what Zybo uses.

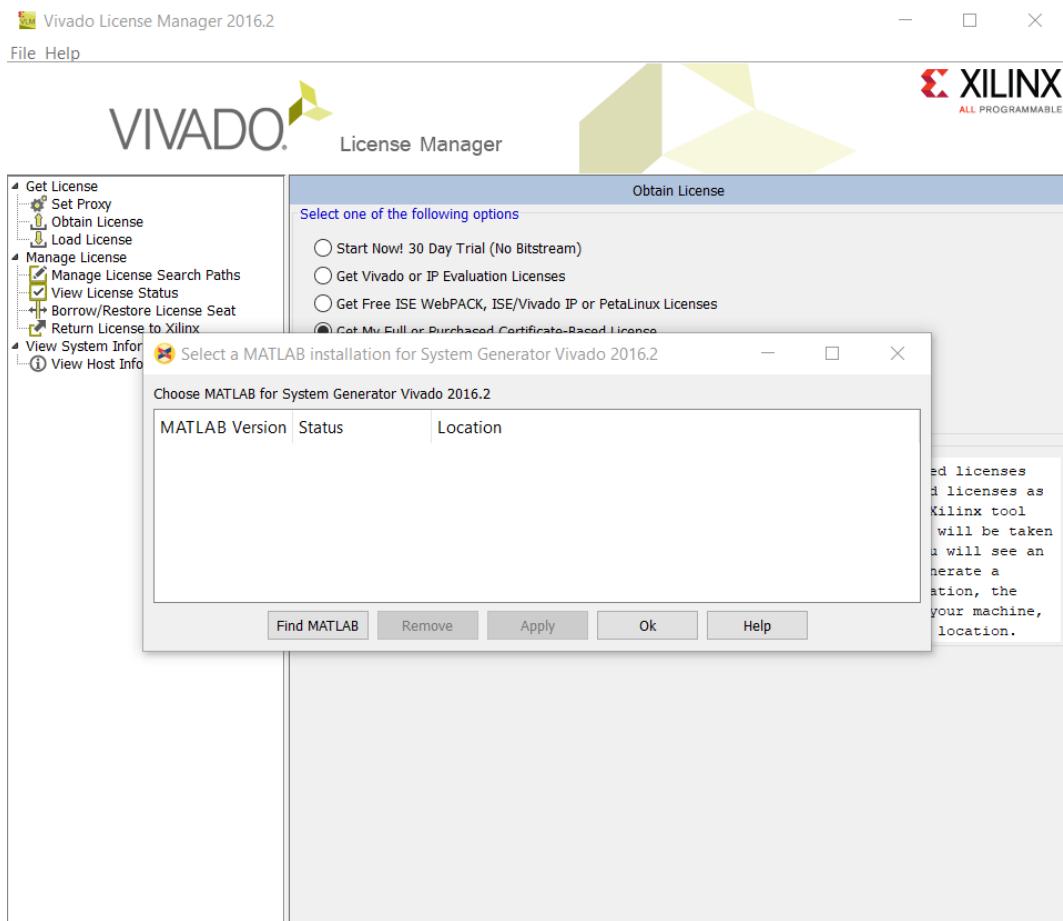




It took about 10 minutes to download and install it. Skip the matlab installation part as we would need to use dsp system generator.







Click “Connect Now” to get Free ISE WebPACK, IS/Vivado IP or PetaLinux License.



Log onto your Xilinx account and choose “Vivado Design Suite: HL WebPACK 2015 AND Earlier License” under Certificate Based License. Click “Generate Node-Locked License”.

Certificate Based Licenses

Product	Type	License	Available Seats	Status	Subscription End Date
SDSoC Environment, 60 Day Evaluation License	Certificate - Evaluation	Node / Floating	1/1	Current	60 days
SDAccel OpenCL Development Environment: 30 Day Node Locked Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days
SDAccel OpenCL Development Environment: 30 Day Floating Evaluation License	Certificate - Evaluation	Floating	1/1	Current	30 days
<input checked="" type="checkbox"/> Vivado Design Suite: HL WebPACK 2015 and Earlier License	Certificate - No Charge	Node	1/1	Current	None
OEM Zynq-7000 SoC XC7Z10 Vivado Design Edition Voucher	Certificate - Full	Node	1/1	Expired	03 Mar 2017
ISE WebPACK License	Certificate - No Charge	Node	1/1	Current	None
Xilinx MicroBlaze/All Programmable SoC Software Development Kit – Standalone	Certificate - No Charge	Node	1/1	Current	None
Petalinux Tools License	Certificate - Evaluation	Node	1/1	Current	365 days
Petalinux Tools License, Floating License	Certificate - Evaluation	Floating	1/1	Current	365 days
Vivado HLS Evaluation License	Certificate - Evaluation	Node	1/1	Current	30 days

[Generate Floating License](#)

[Generate Node-Locked License](#)

What is the difference between a floating and a node license? [?](#)

Click Next to generate node-locked license on any host ID. Click Next. Click Next under REVIEW LICENSE REQUEST

Generate Node License

4 REVIEW LICENSE REQUEST

Product Selections				
Product	Subscription End Date	Available Seats	Requested Seats	
Vivado Design Suite: HL WebPACK 2015 and Earlier ...	1/1	1	1	

System Information

License	Node
Host ID	ANY

Note: WebTalk is always enabled for WebPACK users. WebTalk ignores user and install preference when a bitstream is generated using the WebPACK license. If a design is using a device contained in WebPACK and a WebPACK license is available, the WebPACK license will always be used. To get additional information on WebTalk, go to www.xilinx.com/webtalk.

[Previous](#) [Next](#) [Cancel](#)

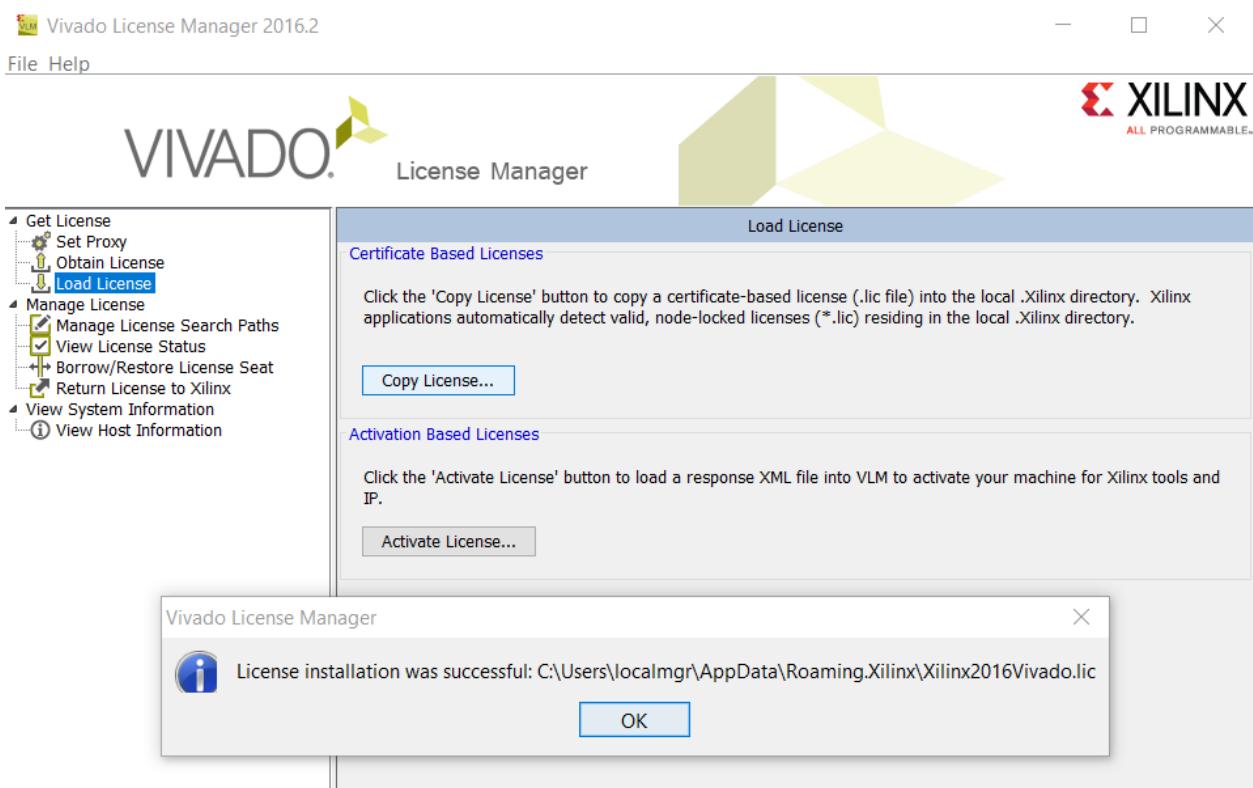
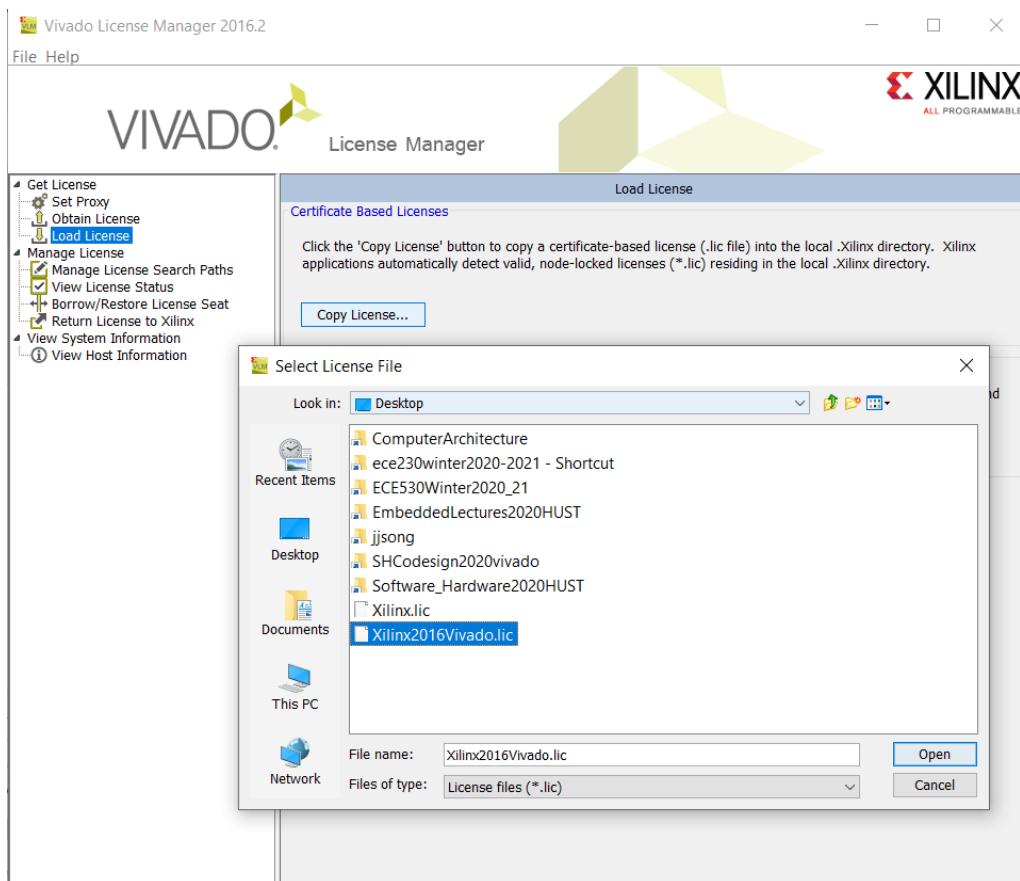
The following message will appear if the license is generated correctly.



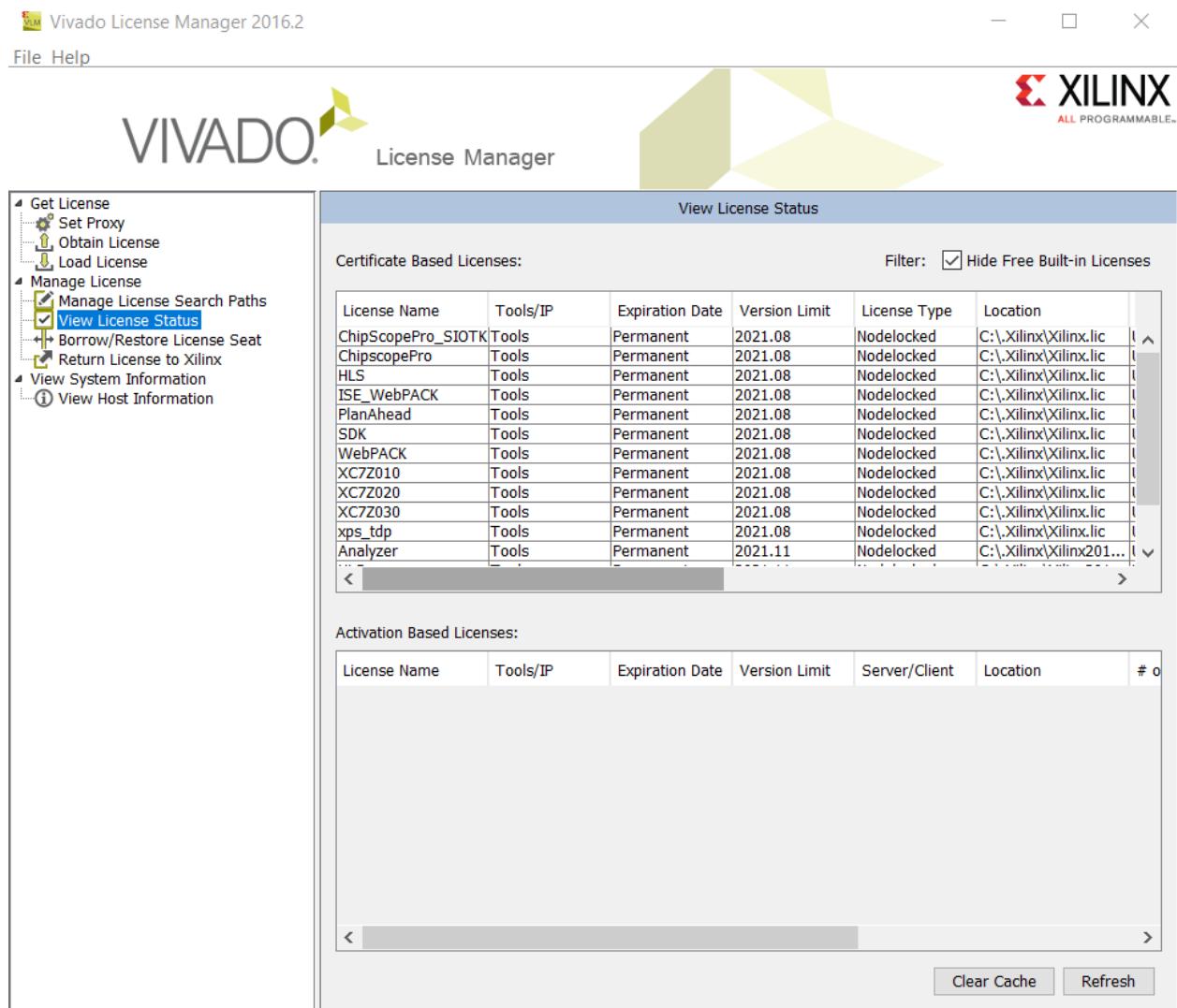
You will receive a license file, entitled Xilinx.lic from your email. Save this file as Xilinx2016Vivado.lic file to indicate it is for 2016 Version of Vivado.

If your Vivado License Manager 2016.2 is still open, Select “Load License” and Click “Copy License”. Close Vivado License Manager after seeing “License Installation was Successful” as seen below. You can then View License Status by unchecking “Hide Free Built-in Licenses”.

You can open Manage Xilinx Licenses from Xilinx Design Tools under Program List-> VLM Manage Xilinx Licenses.

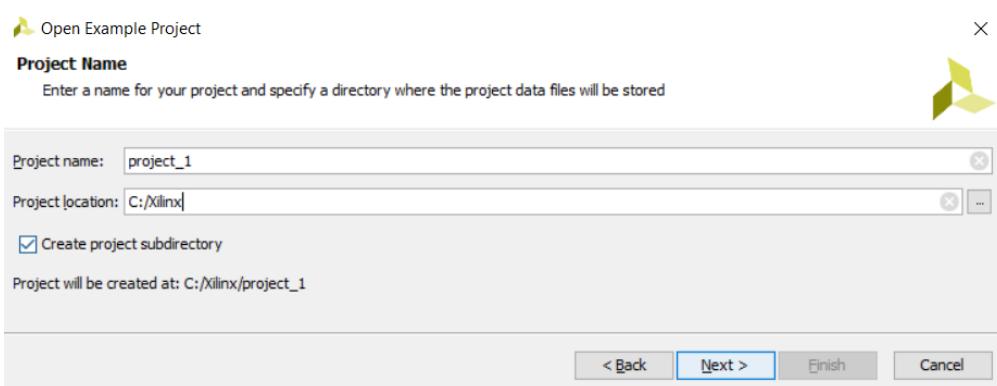
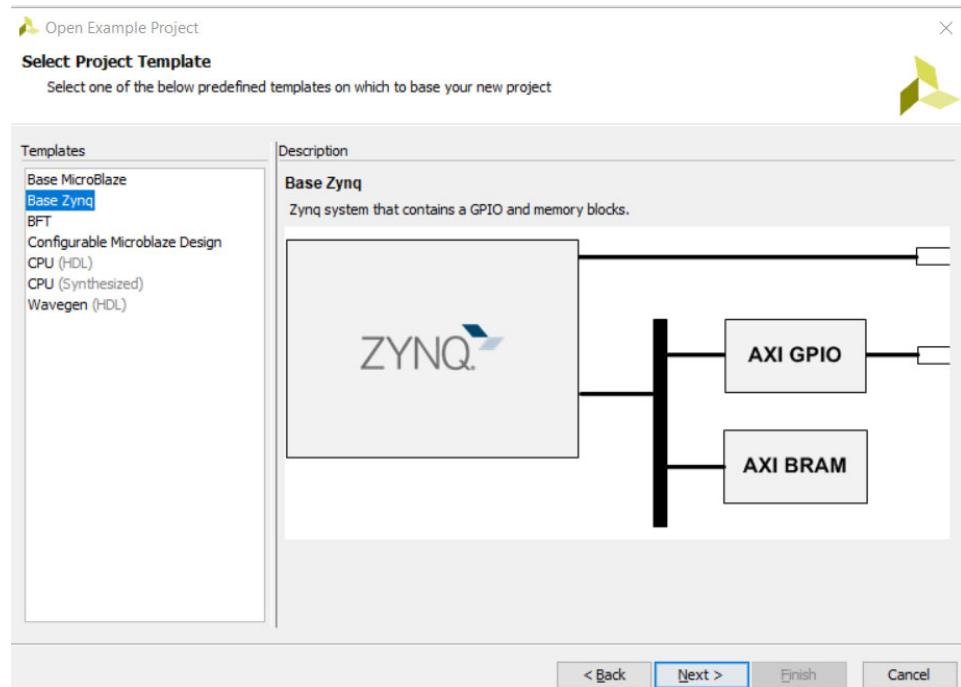


Choose View License Status to see the following licenses. If you do not see the licenses, you may need to close the license manager and reopen it to make the licenses visible.

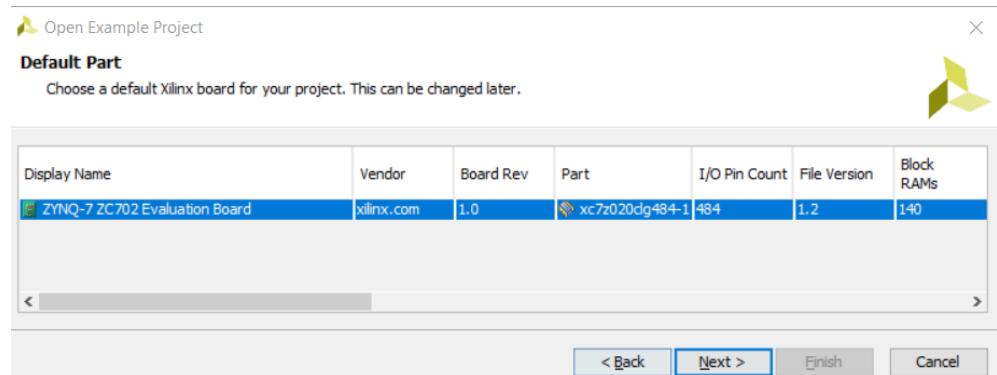


4. Run an Example Project to Test your Vivado Design Suite WebPACK

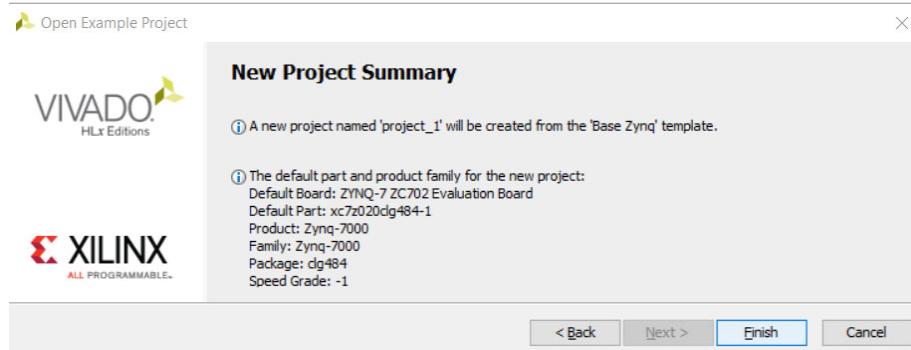
As a test of your Vivado installation, you should now be able to compile an example embedded design for a base Zynq system, that may be found by starting Vivado, clicking on **Open Example Project**. Click Next and choose **Base Zynq**, click Next. Keep project name to be project_1 and set Project location to be C:/Xilinx, click Next.



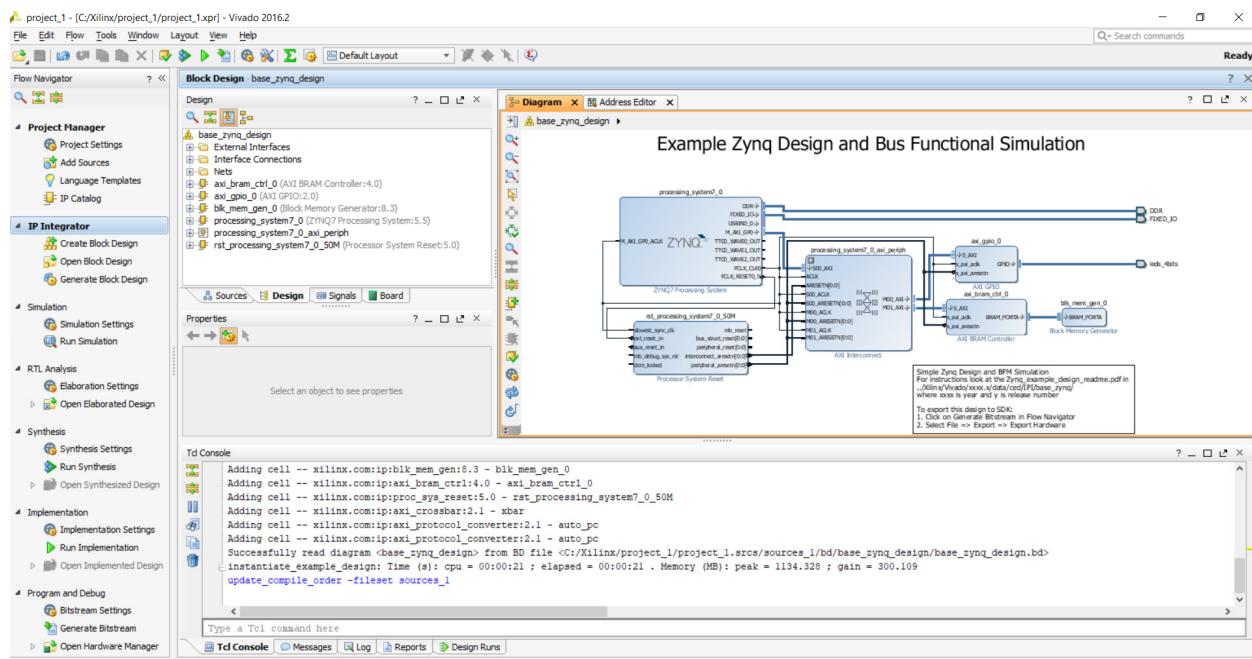
Choose **ZYNQ-7 ZC702 Evaluation Board**, Click Next to see New Project Summary.



Click "Finish" on New Project Summary Menu.

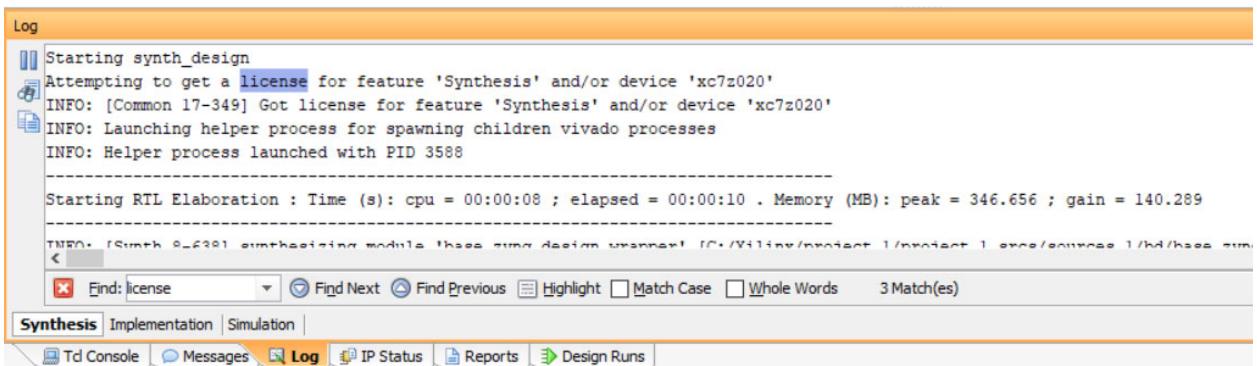


A Vivado Block Design project will be opened as follow.



Choose Flow->Run Synthesis F11 in Flow Navigator panel located on the left of the project window. The top right corner of the project window will display “Running synth_design” bargraph.

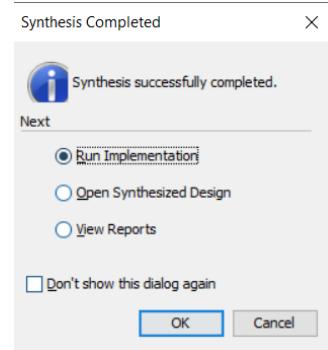
Click “Log” window at the bottom the progress of the synthesis. During the course of the synthesis, there will be a number of warnings that can be ignored and messages that start with “Attempting to get license for...”, if the next message says, “Got license....”, then things are looking good! The license server has been correctly pointed to, and your Vivado installation is successful!



The entire synthesis process should terminate after a few minutes, with a “**Synthesis Completed**” window bearing the happy message “**Synthesis successfully completed**”!

Do not run Implementation. You cannot download this design onto your Zybo board since the Zybo uses the Zynq 7010 chip, not the Zynq 7020 that is used on the ZedBoard.

Click “Cancel” on Synthesis successfully completed menu.



5. Set up hardware to connect your ZYBO board

Set the power supply jumper to “USB”, so the board can be powered up and laboratory assignments can be carried out using single micro-usb cable (without needing to use the included dc power supply module.)

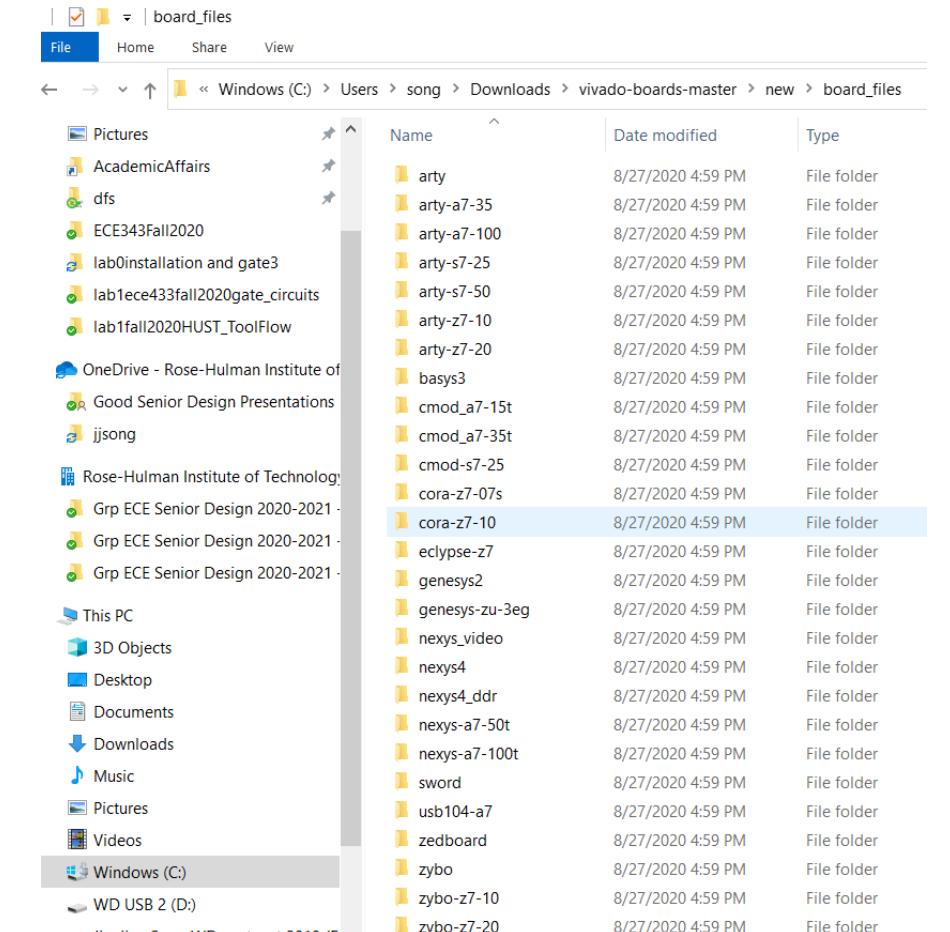
Connect the micro USB cable between the “PROG UART” port of ZYBO and PC.

6. Install Digilent Zybo Board File

This section is copied from this webpage: <https://reference.digilentinc.com/vivado/installing-vivado/start>.

Digilent provides board files for each FPGA development board. These files make it easy to select the correct part when creating a new project and allow for automated configuration of several complicated components used in many designs.

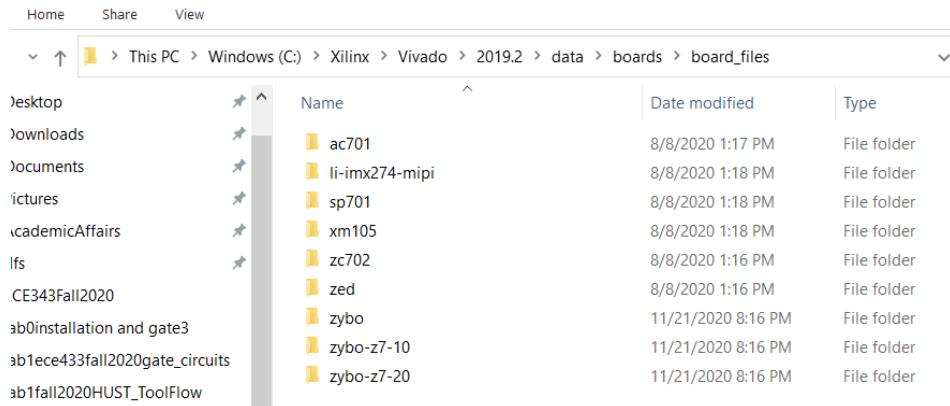
Download the archive of the Vivado-boards GitHub repository at <https://github.com/Digilent/vivado-boards/archive/master.zip>. The file name is Vivado-boards-master. Extract the folder as seen below. Open the folder extracted from the archive and navigate to its 'new/board_files' directory. Select all three Zybo folders within this directory and copy them. Open the folder that Vivado was installed into - 'C:/Xilinx/Vivado' or '/opt/Xilinx/Vivado' by default. Under this folder, navigate to its '<version>/data/boards/board_files' directory, then paste the Zybo board files into this directory.



File Home Share View

Windows (C:) > Users > song > Downloads > vivado-boards-master > new > board_files

	Name	Date modified	Type
	arty	8/27/2020 4:59 PM	File folder
	arty-a7-35	8/27/2020 4:59 PM	File folder
	arty-a7-100	8/27/2020 4:59 PM	File folder
	arty-s7-25	8/27/2020 4:59 PM	File folder
	arty-s7-50	8/27/2020 4:59 PM	File folder
	arty-z7-10	8/27/2020 4:59 PM	File folder
	arty-z7-20	8/27/2020 4:59 PM	File folder
	basy3	8/27/2020 4:59 PM	File folder
	cmod_a7-15t	8/27/2020 4:59 PM	File folder
	cmod_a7-35t	8/27/2020 4:59 PM	File folder
	cmod-s7-25	8/27/2020 4:59 PM	File folder
	cora-z7-07s	8/27/2020 4:59 PM	File folder
	cora-z7-10	8/27/2020 4:59 PM	File folder
	eclypse-z7	8/27/2020 4:59 PM	File folder
	genesys2	8/27/2020 4:59 PM	File folder
	genesys-zu-3eg	8/27/2020 4:59 PM	File folder
	nexys_video	8/27/2020 4:59 PM	File folder
	nexys4	8/27/2020 4:59 PM	File folder
	nexys4_ddr	8/27/2020 4:59 PM	File folder
	nexys-a7-50t	8/27/2020 4:59 PM	File folder
	nexys-a7-100t	8/27/2020 4:59 PM	File folder
	sword	8/27/2020 4:59 PM	File folder
	usb104-a7	8/27/2020 4:59 PM	File folder
	zedboard	8/27/2020 4:59 PM	File folder
	zybo	8/27/2020 4:59 PM	File folder
	zybo-z7-10	8/27/2020 4:59 PM	File folder
	zybo-z7-20	8/27/2020 4:59 PM	File folder



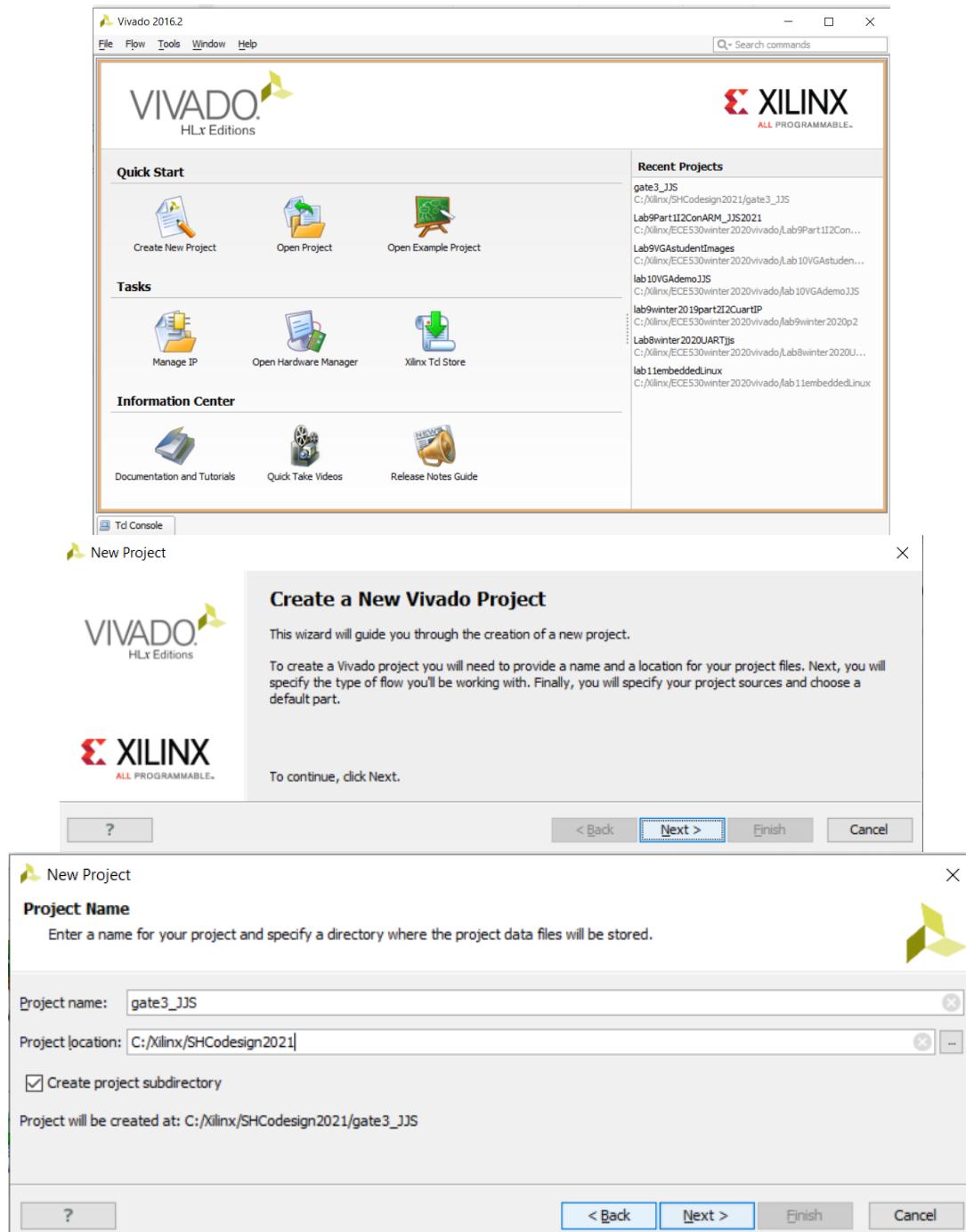
Home Share View

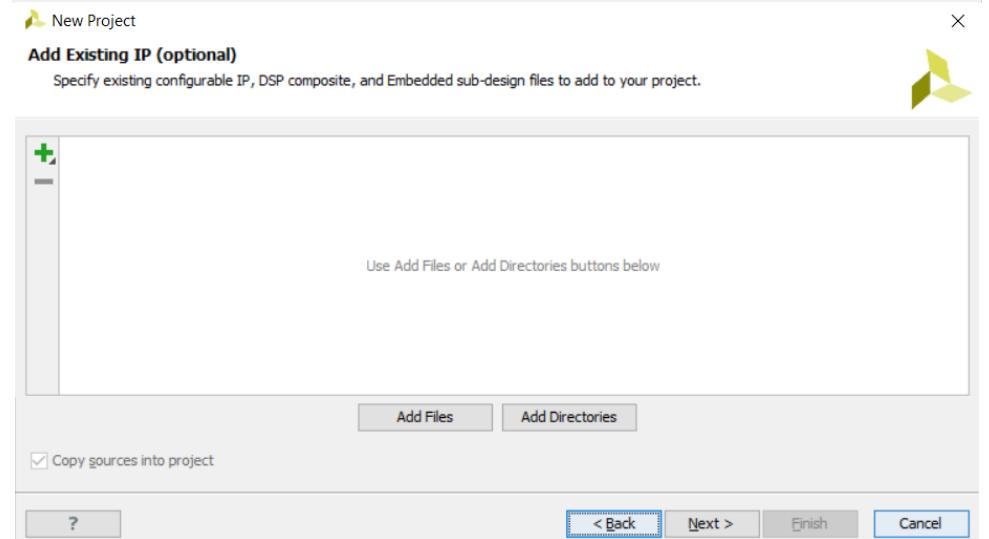
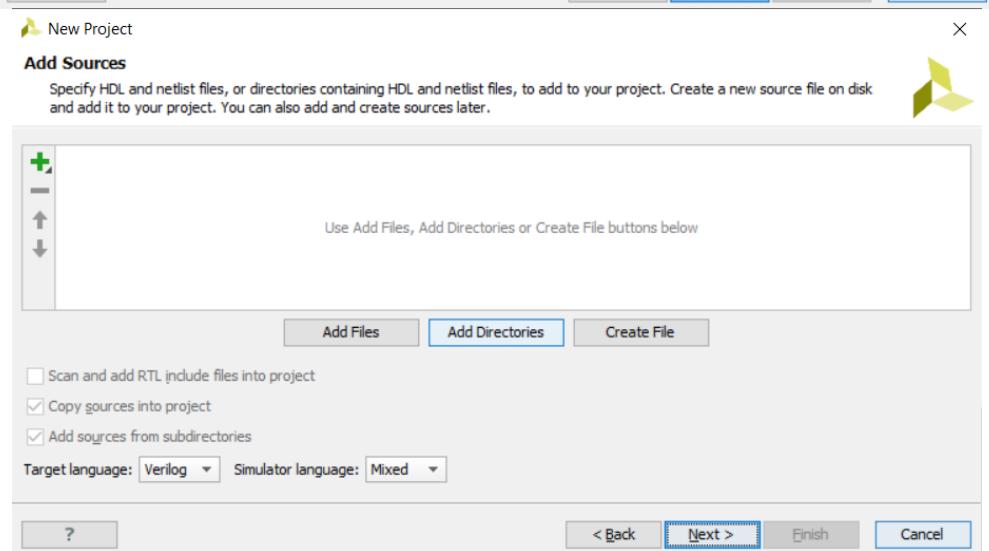
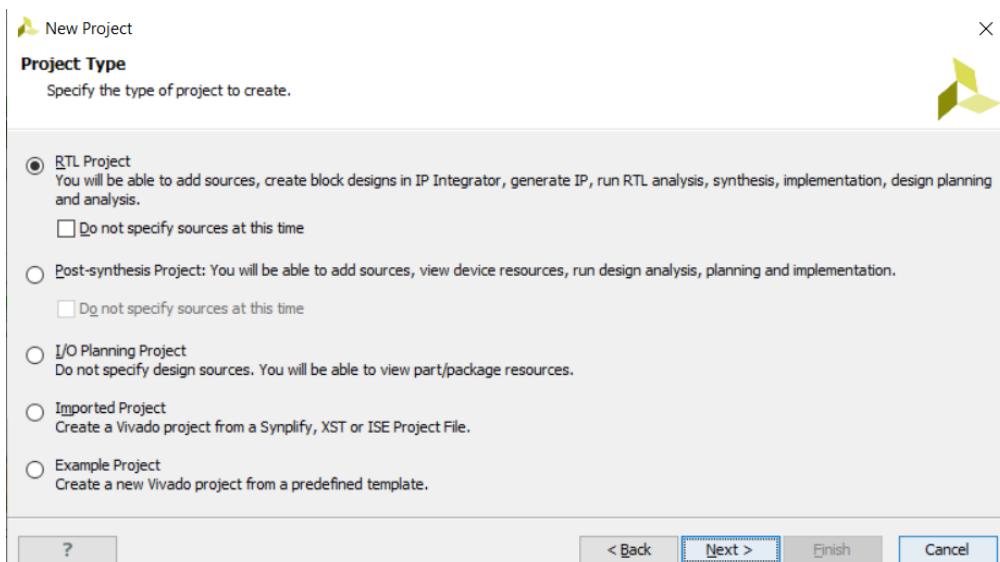
This PC > Windows (C:) > Xilinx > Vivado > 2019.2 > data > boards > board_files

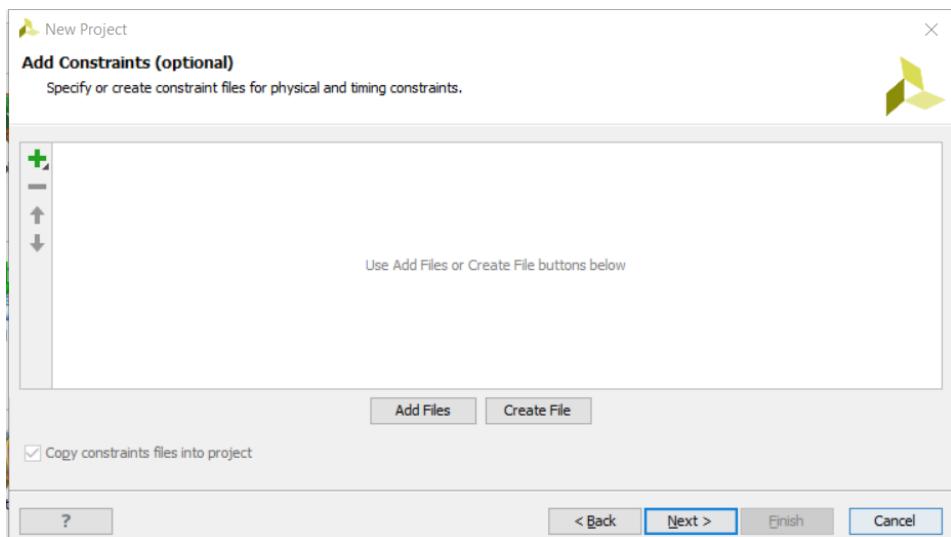
	Name	Date modified	Type
	ac701	8/8/2020 1:17 PM	File folder
	li-imx274-mipi	8/8/2020 1:18 PM	File folder
	sp701	8/8/2020 1:18 PM	File folder
	xm105	8/8/2020 1:18 PM	File folder
	zc702	8/8/2020 1:16 PM	File folder
	zed	8/8/2020 1:16 PM	File folder
	zybo	11/21/2020 8:16 PM	File folder
	zybo-z7-10	11/21/2020 8:16 PM	File folder
	zybo-z7-20	11/21/2020 8:16 PM	File folder

7. Implement Gate3.v on your Zybo Board

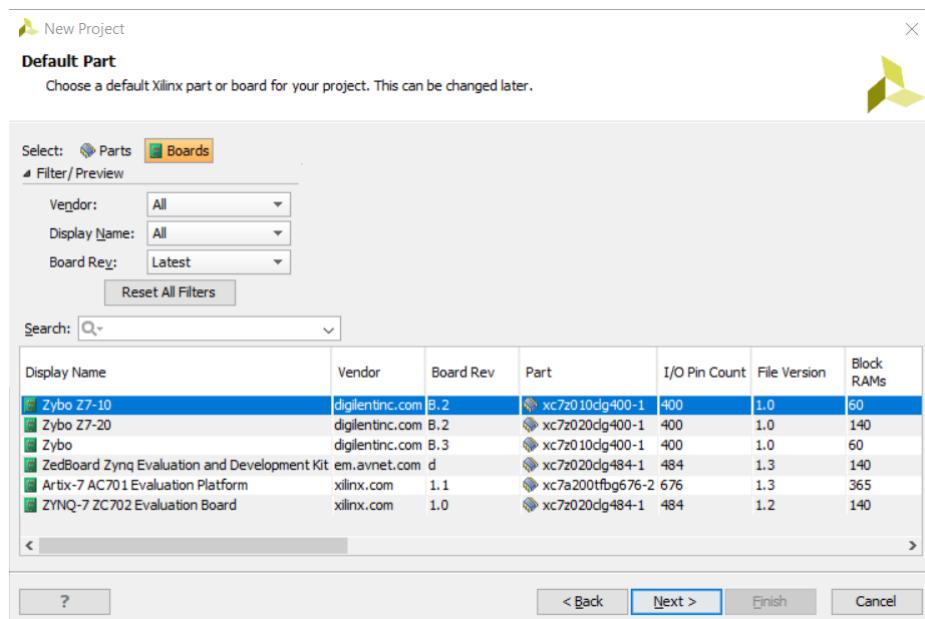
Create class project directory C:/Xilinx/ SHCodesign2021 under C:/Xilinx folder. C:/Xilinx folder should be created when you installed Vivado. Start Vivado and create a new project and named it gate3_JJS, where JJS is your name initials. Choose project location to be C:/Xilinx/ SHCodesign2021. This is the folder where you keep all your lab folders. Click Next and choose RTL Project and Next. Skip Add Sources, Add Existing IP (optional) and skip Add Constraints (optional).

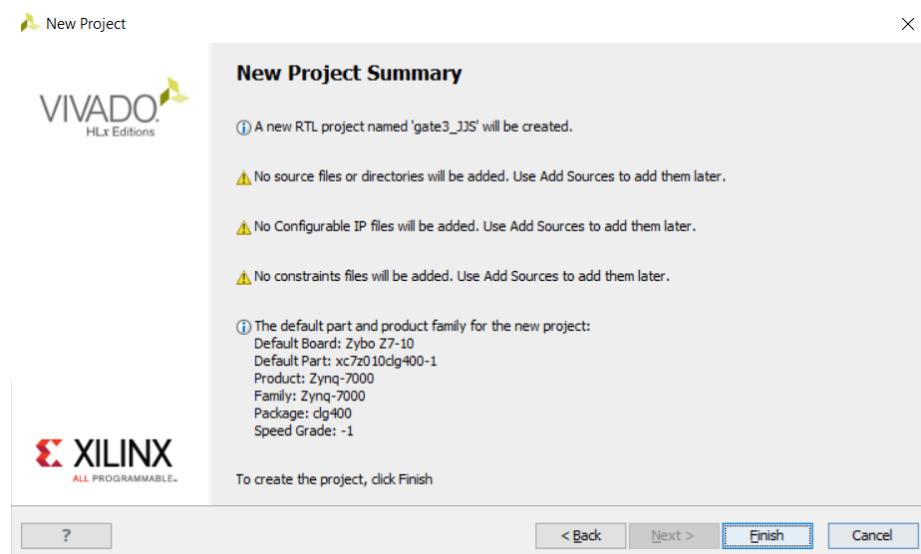






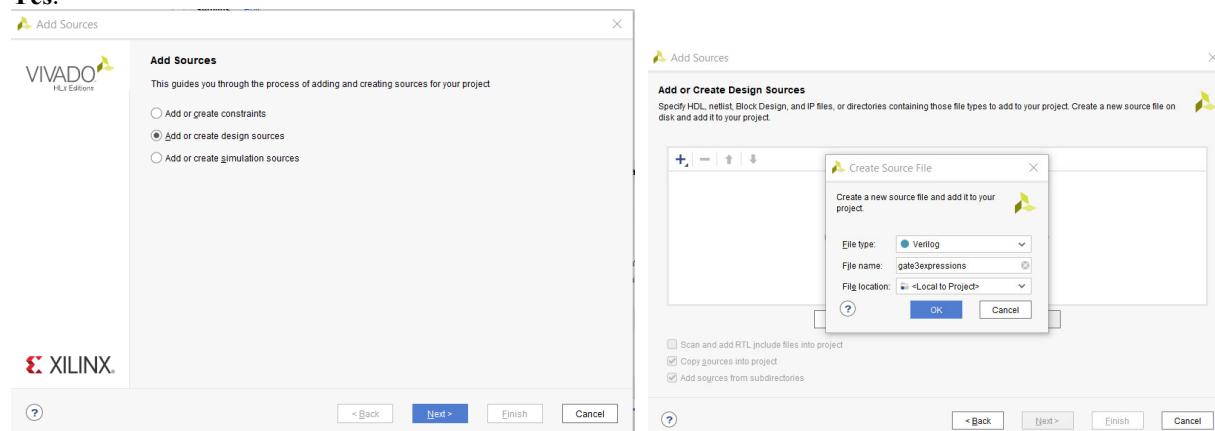
Choose Zybo Z7-10 board. Click Next and Finish.





7.1 Create a Verilog circuit module gate3Expression.v

Under PROJECT MANAGER on Vivado, click Add Sources. Choose **Add or create design sources** and next. Choose Create File and name your file `gate3expressions`. Click **OK** and **Finish**. Cancel Define Module and click **Yes**.



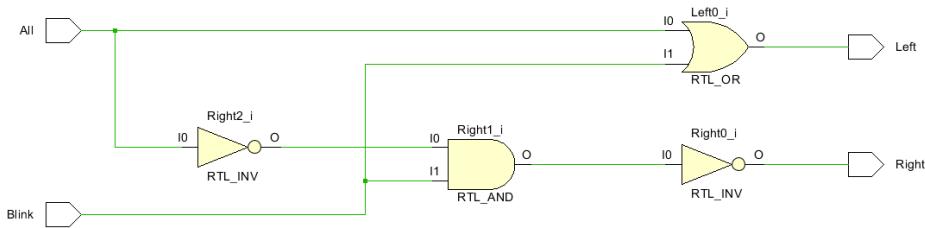
Open your `gate3expressions` file under Design Sources/. Copy and paste the following Verilog circuit to your `gate3expressions.v` file. Change the Author name to your name. Notice the back slash before timescale must be correctly copied. Save this file. You should not see any syntax error.

```
'timescale 1ns / 1ps          //simulation time unit is 1ns and resolution is 1ps
//Author: Jianjian Song
//Date: August 6, 2021
//Purpose: example circuit

module gate3expressions (All, Blink, Right, Left);
input All, Blink;
output reg Right, Left;

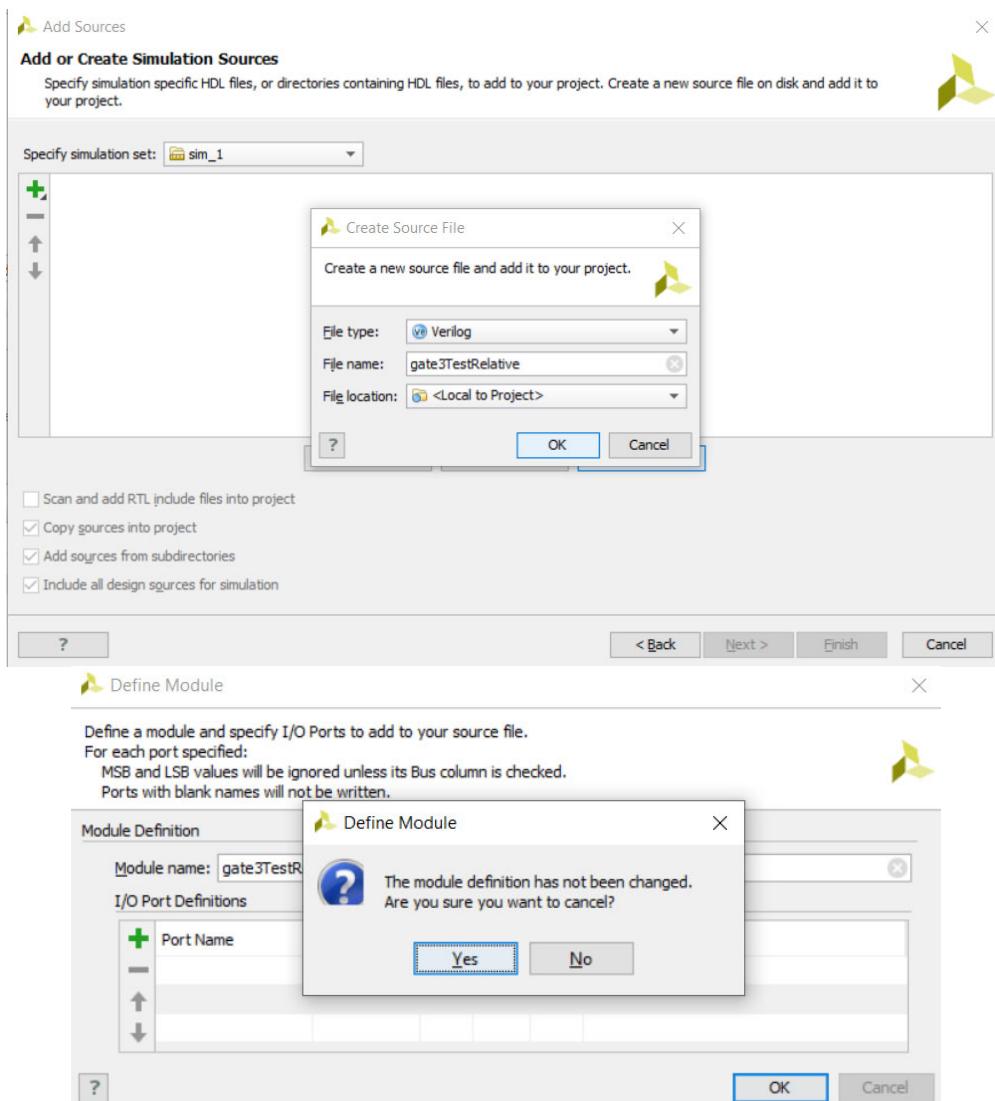
always @ (All, Blink)
    Right <= !(All&Blink);
    Left <= All | Blink;
end
endmodule
```

Click on Open Elaborated Design under TTL ANALYSIS. You should see the following schematic.



7.2 Create a test bench file for gate3 circuit and simulate gate3 circuit

Click Add Sources again and choose Add or create simulation sources. Choose Create File. Name it gate3TestRelative. Click OK and Finish. Cancel “Define Module” and click Yes.



Find and open gate3TestReleitive.v under Simulation Sources->sim_1 folder. Copy and paste the following text to this file. Save this file. You should not have any syntax error.

```

`timescale 1ns / 1ps

//Jianjian Song
//August 6, 2021

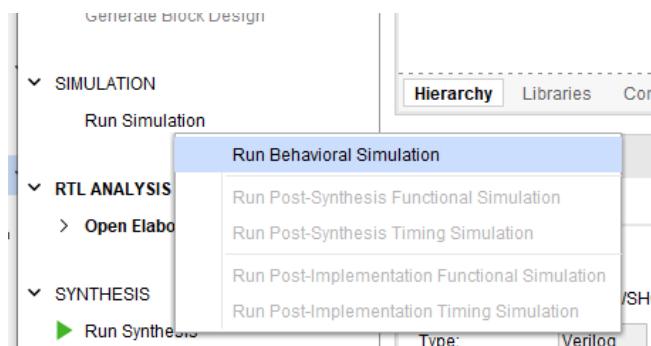
module gate3TestRelative;
reg all1, blink1;      // Inputs
wire RightBehavior, LeftBehavior;

initial begin
// Initialize Inputs
    all1 = 0; blink1 = 0; #3;
    all1 = 1; blink1 = 0; #4;
    all1 = 0; blink1 = 0; #5;
    all1 = 0; blink1 = 1; #5;
    all1 = 0; blink1 = 0; #3;
    all1 = 0; blink1 = 1; #4;
    all1 = 0; blink1 = 0; #3;
    $stop;
end

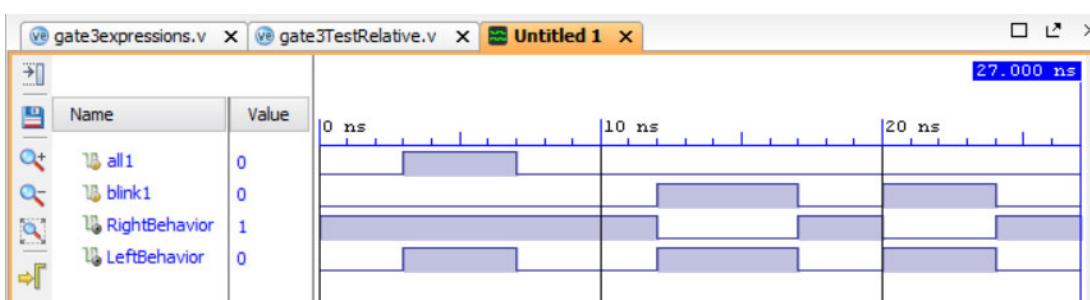
gate3expressions Gate3ExpressionUnit (all1, blink1, RightBehavior, LeftBehavior);
endmodule

```

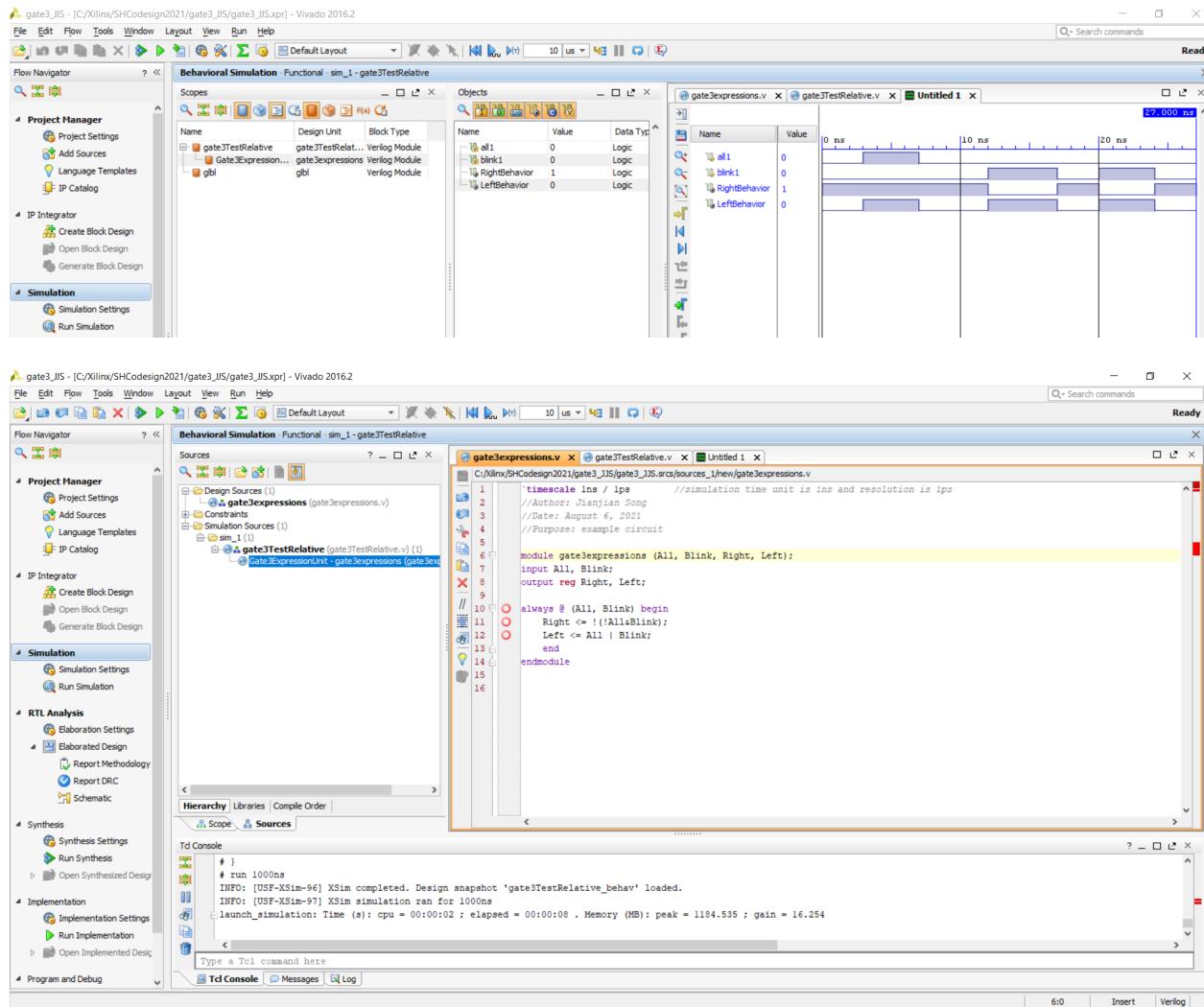
choose gate3TestRelative.v file under **Simulation Sources** and choose **Run Simulation** under **Simulation** to execute the test bench gate3TestRelative.v with gate3expressions.v circuit. Choose **Run Behavioral Simulation**.



A file called Untitled 1 is generated and it stores simulation waveforms. Select this file and click Zoon Fit symbol to make the complete waveforms show on the window.

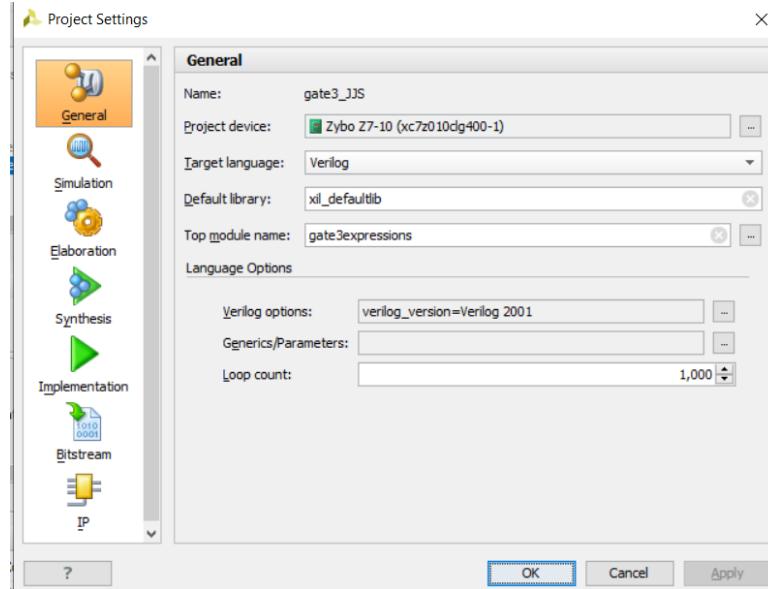


your Vivado project should look as follows.

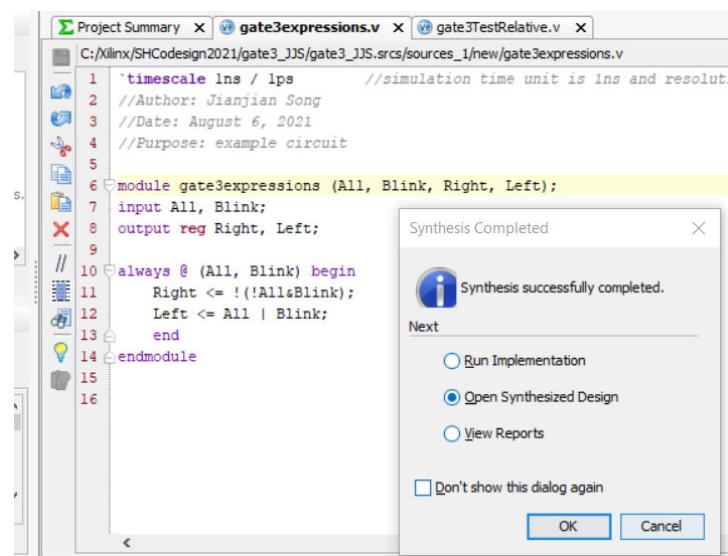


7.3 Synthesize gate3 circuit, Assign physical pins and Generate its bit stream file

Check to make sure you have chosen Zybo z7-10 board by clicking on Settings under PROJECT MANAGER. You can click on the choice button \cdots to change the device to Zybo Z7-10.



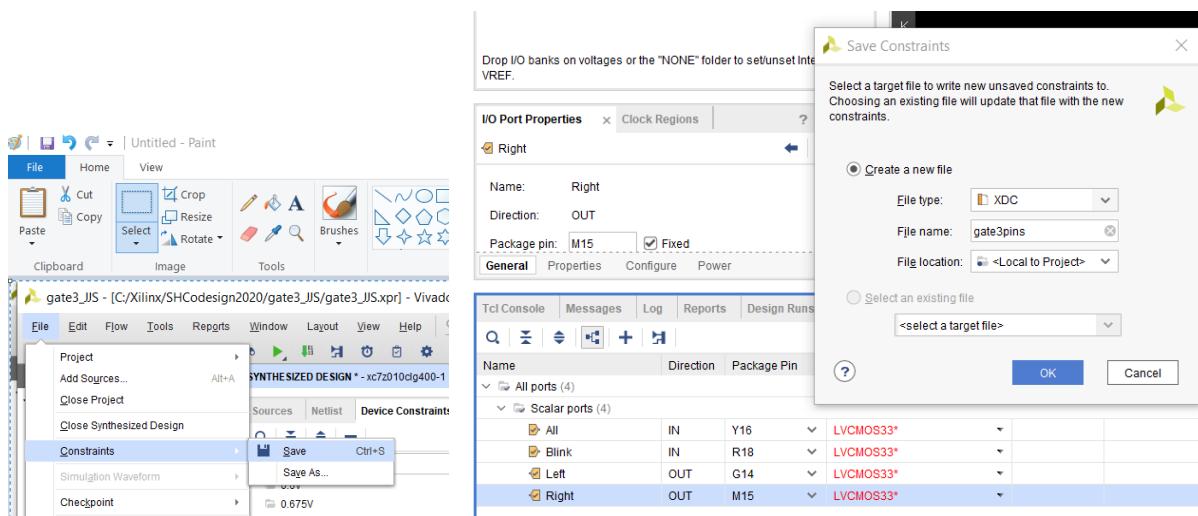
Now, choose to Run Synthesis under **Synthesis**. Choose **Open Synthesis Design** when it is complete and click OK.



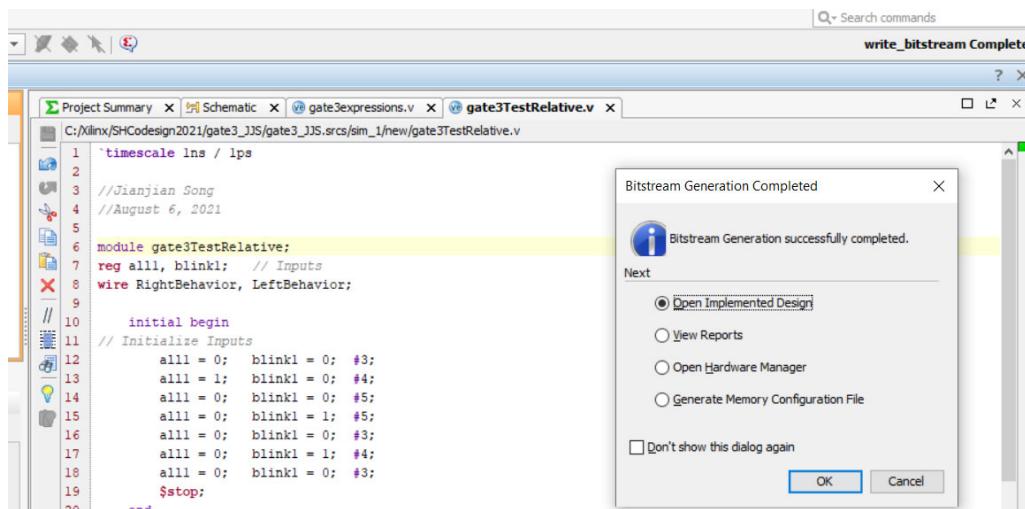
You should see I/O package ball grid array picture opened. You should see I/O Ports display at the bottom of your window. If you do not see I/O Ports, click on Window->I/O Ports. You may need to open wider the first column of the I/O Ports table to see the pin names. Change I/O standard to 3.3V LVCMOS33 for all pins. Under Package Pin, add the following pin numbers. You can press, hold and move a column to be closer to signal names.

I/O Ports				
Name	Direction	Package Pin	I/O Std	
All ports (4)				
Scalar ports (4)				
All	IN	Y16	LVC MOS33*	
Blink	IN	R18	LVC MOS33*	
Left	OUT	G14	LVC MOS33*	
Right	OUT	M15	LVC MOS33*	

To save this pin assignment to a Xilinx Design Constraint (XDC) file, click File->Save Constraints-Save. Name this XDC file gate3pins. Click OK to save file gate3pins.

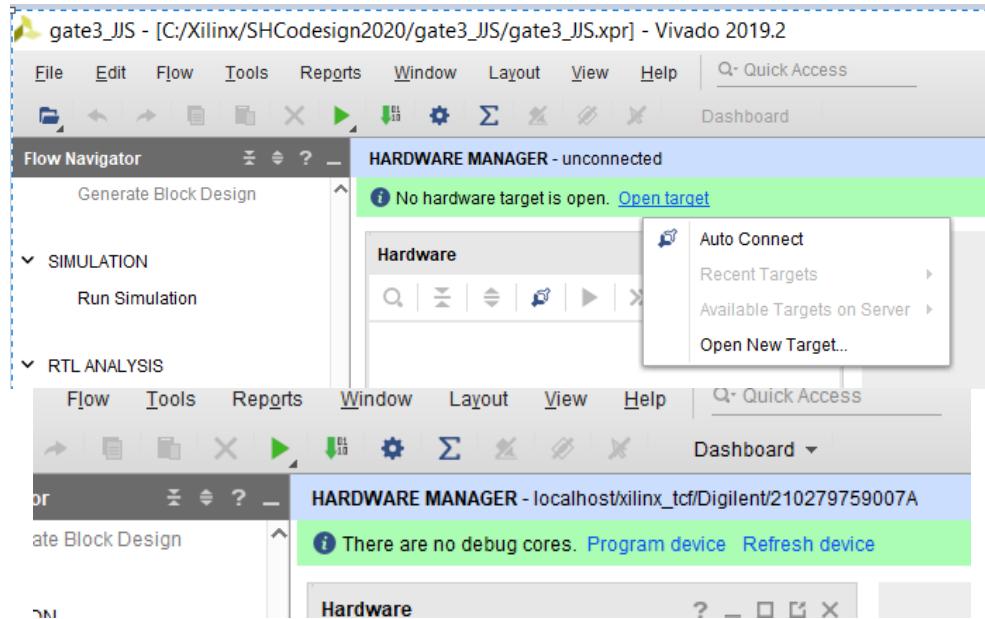


Now click **Generate Bitstream** under **Program and Debug** at the bottom of the Flow Navigator in the left column to generate a bit stream file for gate3 circuit. You can ignore the elaboration warning. If you are successful, you will see “write_bitstream Complete” on the top right of your window. Choose **Open Implemented Design** and click **OK**.

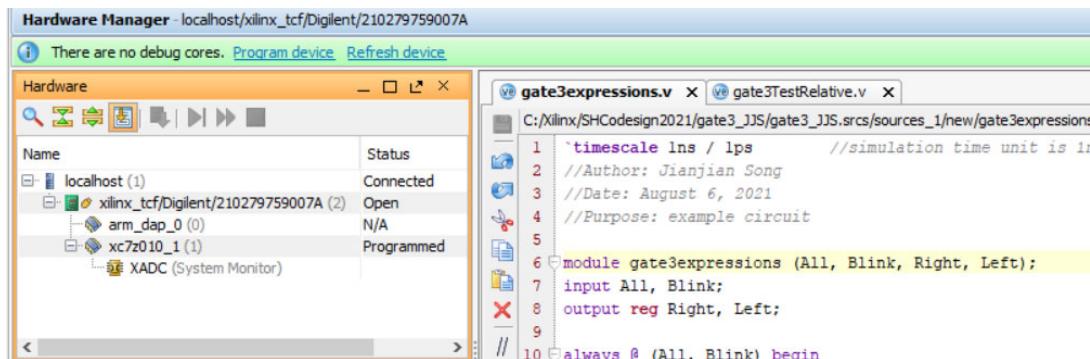


7.4 Download the bitstream file to your Zybo board and test gate3 circuit

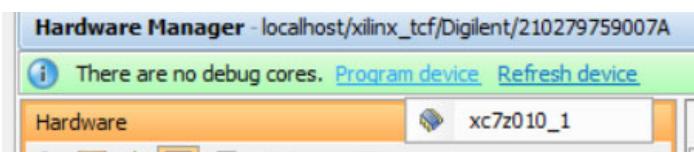
Now connect your Zybo board to your laptop. Click **Open Hardware Manager** under PROGRAM AND DEGUG menu at the bottom of the left column. Click **Open Target -> Auto Connect** at the bottom or top of the window.



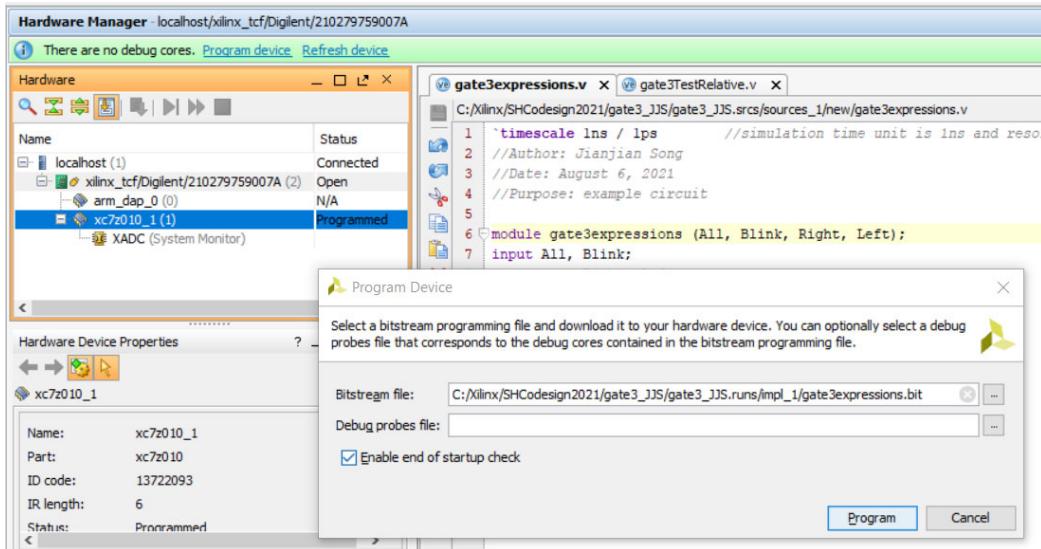
If your Zybo is connected correctly, your will see localhost connected as follows.



Click **Program device** and choose xc7z010_1 chip.



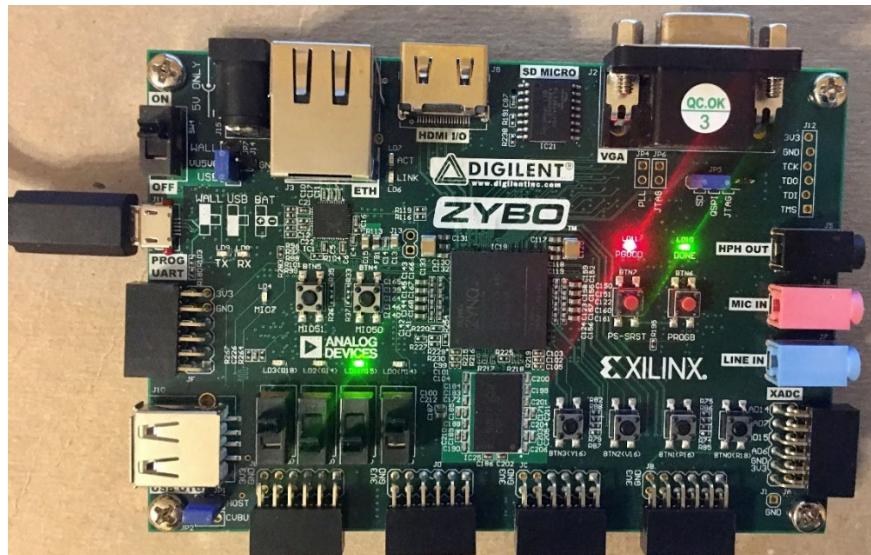
Notice gate3expressions.bit should appear under Program Device menu. Clock Program to send the bit stream file to your Zybo Board.



7.5 Test your gate3 circuit on your Zybo board

Gate3 circuit has two input switches BTN0 and BTN3. Press Button 0 and Button 3 on your Zybo board to test your circuit.

All BTN3	Blink BTN0	Right LD1	Left LD2
0	0	1	0
0	1	0	1
1	0	1	1
1	1	1	1



8. Demonstrate your gate3 circuit on your Zybo board

To obtain credit for this lab, demonstrate your Zybo board to your instructor or teaching assistant.