Name: _____ CM: _____ Start Date: Friday, August 13, 2021

Name: _____ CM: _____ Due Date: Saturday, August 14, 2021

Software and Hardware Co-Design with Zybo, Summer 2021 HUST
Lab #3 Block Design and IPs Creation on Zybo

This is an individual lab. Each student must perform it and demonstrate parts 1 and 2 of this lab to obtain credit for it. Late lab submission will be accepted with a grade reduction of 10% for each day that it is late.

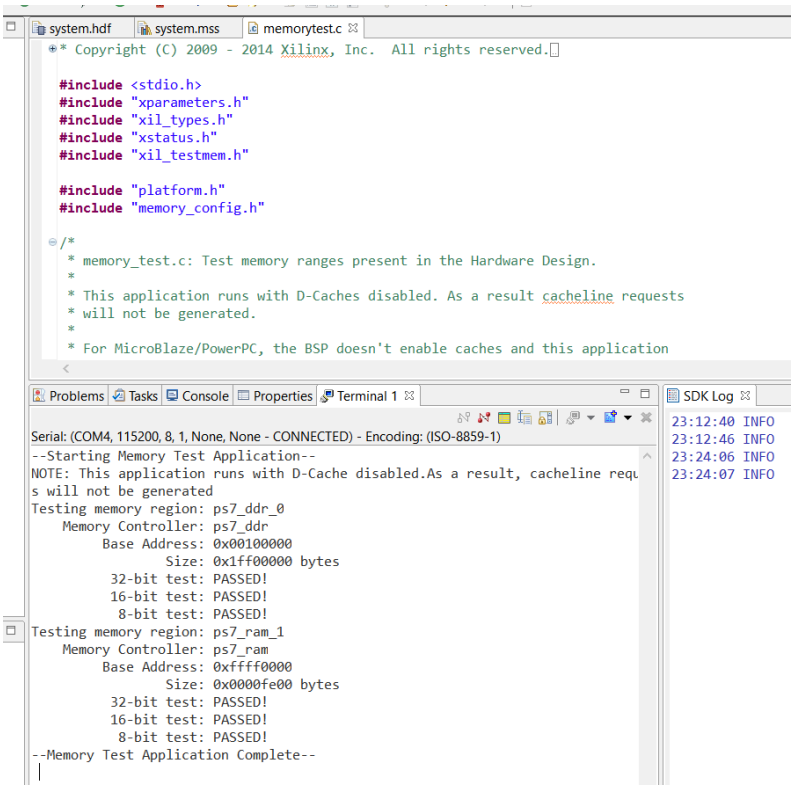
You will need to download the first five labs are under "Embedded System Design Flow on Zynq using Vivado" from the Xilinx University Program (XUP) Website. Go to www.xilinx.com. Choose **Support/University Program** and then **Resource/Workshops.** See the appendix of this lab for more details.

1. Objectives

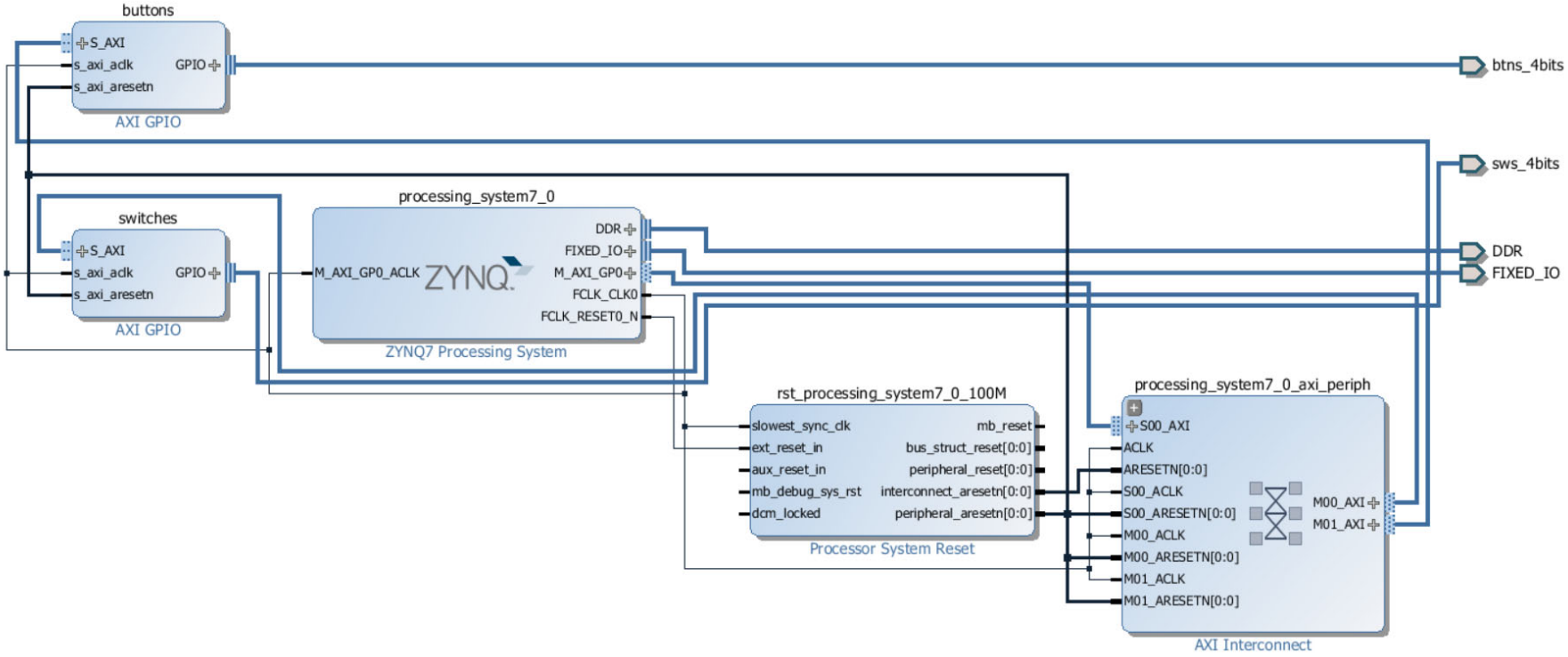
- *Follow the first two labs from Xilinx University Program on Advanced Embedded System Design on Zynq using Vivado.*
  a. ***Lab #3 Part 1: ZYNQ Lab 1*** *Use Vivado to Build Embedded Systems, pages ZYNQ1-1 to ZYNQ1-16.*
  b. ***Lab #3 Part 2: ZYNQ Lab 2*** *Adding IP Cores in PL, pages ZYNQ2-1 to ZYNQ2-16.*

2. Deliverables

2.1 Demonstrate Lab #3 Part 1 on memory test display on an SDK terminal.



2.1 Demonstrate Lab #3 Part 2 circuit to display status of push buttons and slide switches.



```
XGpio_Initialize(&push, XPAR_BUTTONS_DEVICE_ID);
XGpio_SetDataDirection(&push, 1, 0xffffffff);

while (1)
{
  psb_check = XGpio_DiscreteRead(&push, 1);
  xil_printf("Push Buttons Status %x\r\n", psb_check);
```

Problems | Tasks | Console | Properties | Terminal 1

Serial: (COM4, 115200, 8, 1, None, None - CONNECTED) - Encoding: (ISO-8859-1)

```
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
```

3. Appendix Download the first five labs from Xilinx U Program

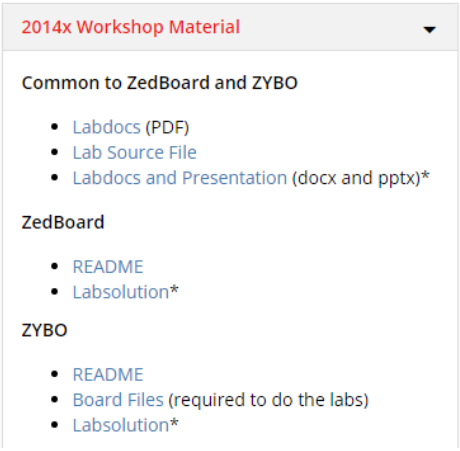
3.1 Install files needed for the first five labs of Embedded Design Workshop

The first five labs are under "Embedded System Design Flow on Zynq using Vivado" from the Xilinx University Program (XUP) Website.

Go to www.xilinx.com. Choose **Support/University Program** and then **Resource/Workshops**.

Open **Embedded System Design Flow on Zynq**.

Find the relevant files under **2015x Workshop Material** as shown on the right.



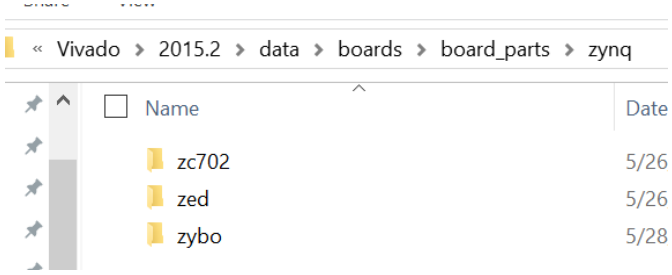
Download the following three zipped files:

(1) labdocs.zip which contains 2015_2_zynq_labdocs_pdf folder.
(2) Lab Source File.zip, which contains 2015_2_zynq_sources folder.
(3) Zybo Board Files, which contains Zybo folder.

Your download folder should have the following zipped files.

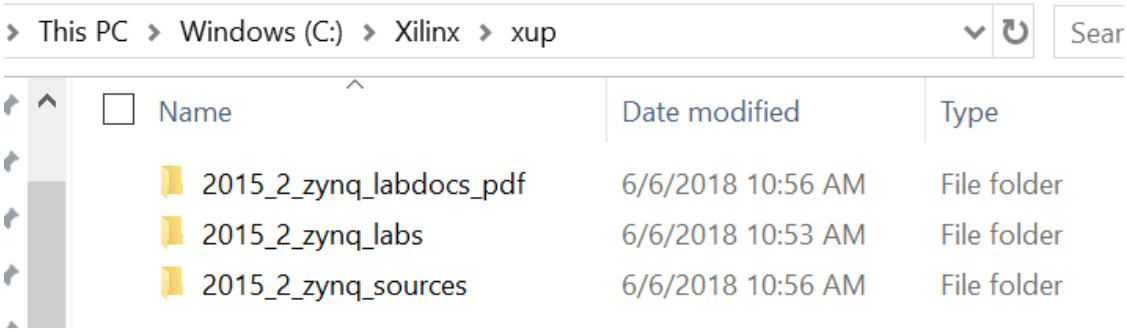
(a) Create a folder "c:\xup\embedded\" on your laptop PC's hard drive. Upzip both 2015_2_zynq_labdocs_pdf.zip and 2015_2_zynq_sources.zip into this "c:\xup\embedded\" folder.
(b) Finally, unzip zybo.zip file to the following folder C:\Xilinx\Vivado\2015.2\data\boards\board_parts\zynq. This directory contains the board files for

various boards, which has other default board files. Placing this "Zybo" file in the specified directory will allow you to select the Zybo board during the design. Vivado is not aware of the Zybo board without performing this step.



3.2 Create a directory for folders and files of these labs

Create a directory "c:\xup\embedded\2015_2_zynq_labs" as a folder to contain all five labs of "Embedded System Design Flow on Zynq using Vivado".



4. An error when SDK Launch is executed

Click "Repair". It does not work.