

# Zynq-7000 All Programmable SoC: Embedded Design Tutorial

***A Hands-On Guide to Effective  
Embedded System Design***

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# Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/23/2015	v2015.1	Initial Xilinx release.

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# Introduction

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## About This Guide

This document provides an introduction to using the Xilinx® Vivado® Design Suite flow for using the Zynq®-7000 All Programmable SoC. The examples are targeted for the Xilinx ZC702 Rev 1.1 evaluation board and the tool version used is Vivado and the Xilinx Software Development Kit (SDK) 2015.1.

**Note:** To install SDK as part of the Vivado Design Suite, you must elect to include SDK in the installer. See [Software Development Kit, page 8](#).

The examples in this document were created using the Windows 7, 64-bit operating system. Other versions of Windows might provide varied results. These examples focus on introducing you to the following aspects of embedded design:

**Note:** The sequence mentioned for booting Linux on the hardware in the test drives for [Chapter 5](#), [Chapter 6](#), and [Chapter 9](#) is specific to the PetaLinux tool chain released for **2014.4**, which must be installed on the Linux host machine for exercising the Linux portions of this document.

- [Chapter 1, Introduction](#) provides a general overview.
- [Chapter 2, Using the Zynq SoC Processing System](#) describes creation of a system with the Zynq SoC Processing System (PS) and running a simple "Hello World" application. This chapter is an introduction into the hardware and software tools using a simple design as the example.
- [Chapter 3, Using the GP Port in Zynq Devices](#) describes how to create a system using the Zynq SoC PS and the Programmable Logic (PL, or "fabric") and how to use a simple application to exercise both the PS and PL.
- [Chapter 4, Debugging with SDK](#) provides an introduction into debugging software using the debug features of the Software Development Kit (SDK). This chapter uses the previous design and runs the software bare metal (without an OS) to show how to debug.
- [Chapter 5, Using the HP Slave Port with AXI CDMA IP](#) provides information about booting the Linux OS on the Zynq SoC board and application debugging with PetaLinux tools. This chapter also introduces the different devices Zynq SoC can boot from and how to program these devices.

- [Chapter 6, Linux Booting and Debug in SDK](#) describes the steps to boot the Linux OS on the Zynq SoC board with *PetaLinux Tools*. This chapter provides information about instantiating the AXI CDMA IP in Fabric and integration with the High Performance (HP) 64 bit slave port.
- [Chapter 7, Software Profiling Using SDK](#) describes the profiling feature for the Standalone BSP and the Application related to AXI CDMA, which is created in [Chapter 6](#). This highlights how to look at software and see if there are any bottlenecks.
- [Chapter 8, Accelerator Coherency Port](#) provides information about accelerator coherency port (ACP) coherent and non-coherent read and write requests.
- [Chapter 9, Creating Custom IP and Device Driver for Linux](#) guides you through creating Intellectual Property (IP) using the Create and Package New IP wizard. It describes Linux-based device driver development and kernel compilation. You will also design a system using your created IP for the Zynq device.
- [Appendix A, Additional Resources and Legal Notices](#) provides links to additional resources related to this guide.

## Example Project

The best way to learn a tool is to use it. So, this guide provides opportunities for you to work with the tools under discussion. Specifications for sample projects are given in the example sections, along with an explanation of what is happening behind the scenes. Each chapter and examples are meant to showcase different aspects of embedded design. The example takes you through the entire flow to complete the learning and then move on to another topic.

## Additional Documentation

Additional documentation is listed in [Appendix A, Additional Resources and Legal Notices](#).

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## How Zynq Devices Simplify Embedded Processor Design

Embedded systems are complex. Hardware and software portions of an embedded design are projects in themselves. Merging the two design components so that they function as one system creates additional challenges. Add an FPGA design project to the mix, and your design has the potential to become very complicated.

The Zynq SoC solution reduces this complexity by offering an ARM Cortex-A9 dual core, along with programmable logic, all within a single SoC.

To simplify the design process, Xilinx offers the Vivado Design Suite and the Xilinx Software Development Kit (SDK). This set of tools provides you with everything you need to simplify embedded system design for a device that merges an SoC with an FPGA. This combination of tools offers hardware and software application design, debugging capability, code execution, and transfer of the design onto actual boards for verification and validation.

**Note:** To install SDK as part of the Vivado Design Suite, you must elect to include SDK in the installer. See [Software Development Kit, page 8](#).

## The Vivado Design Suite, System Edition

Xilinx offers a broad range of development system tools, collectively called the Vivado Design Suite. Various Vivado Design Suite Editions can be used for embedded system development. In this guide we will utilize the System Edition. The Vivado Design Suite Editions are shown in [Figure 1-1](#).

Pillars of Productivity	Features	WebPACK (Device Limited)	Design Edition	System Edition	Free 30-day Evaluation
IP Integration and Implementation	Integrated Design Environment	✓	✓	✓	✓
	Software Development Kit (SDK)	✓	✓	✓	✓
	Partial Reconfiguration *	✓	✓	✓	
Verification and Debug	Vivado Simulator	✓	✓	✓	✓
	Vivado Logic Analyzer		✓	✓	✓
	Vivado Serial I/O Analyzer		✓	✓	✓
Design Exploration and IP Generation	Vivado High-Level Synthesis			✓	✓
	System Generator for DSP			✓	✓

\* Can be purchased as an option.

*Figure 1-1: Vivado Design Suite Editions*

## Other Vivado Components

Other Vivado components include:

- Embedded/Soft IP for the Xilinx embedded processors
- Documentation
- Sample projects

## Software Development Kit

The Software Development Kit (SDK) is an integrated development environment, complementary to Vivado, that is used for C/C++ embedded software application creation and verification. SDK is built on the Eclipse open-source framework and might appear familiar to you or members of your design team.

SDK is available as a stand-alone product, which you install using the Vivado installer. On the Select Edition to Install page of the installer, select **Documentation Navigator (Standalone)**.

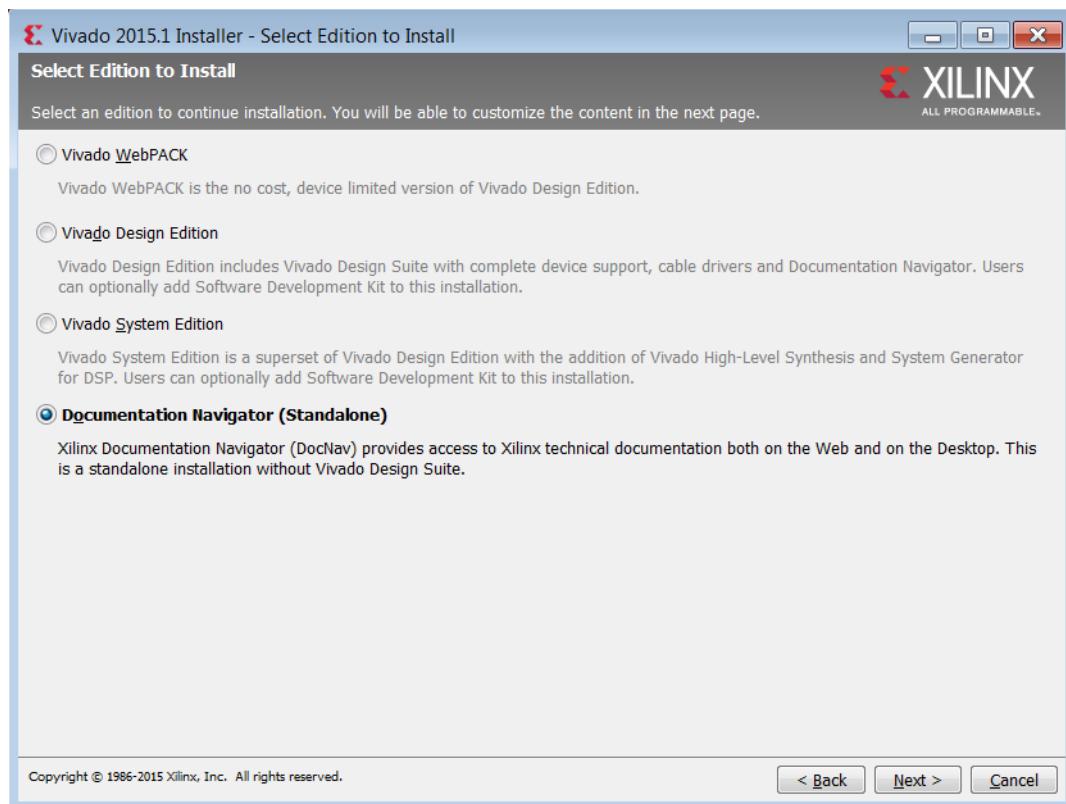
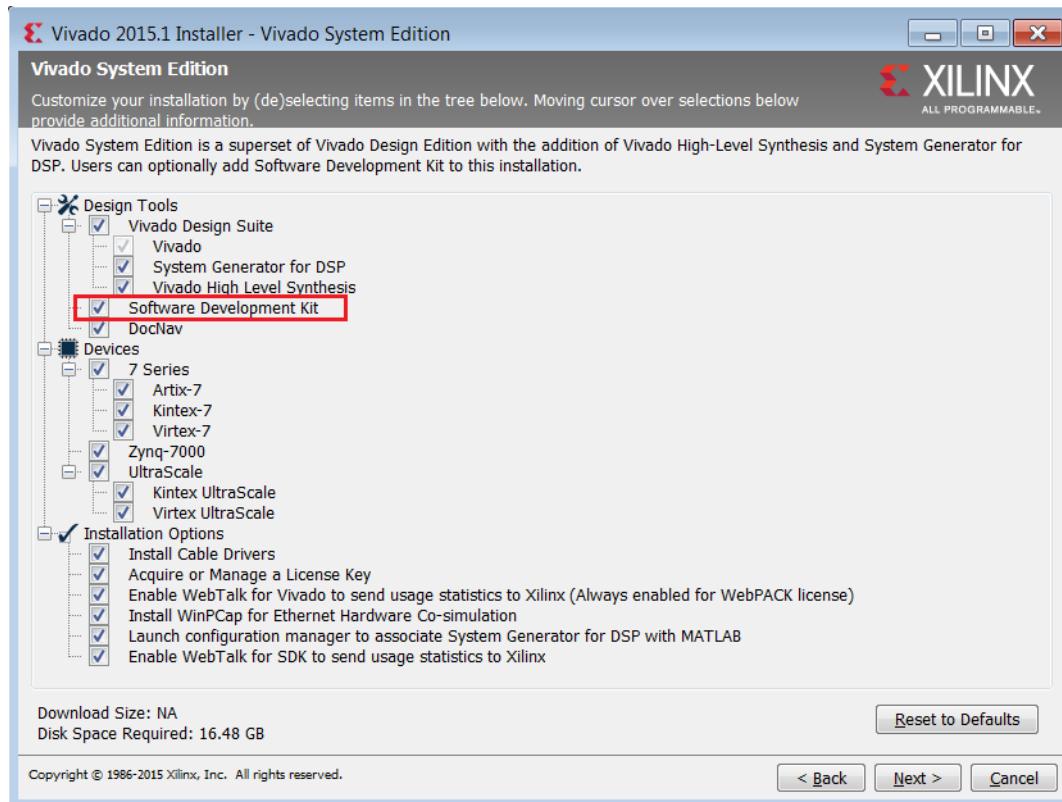


Figure 1-2: Installing Documentation Navigator Standalone Version

When you install the Vivado Design Suite, SDK is available as an optional software tool that you must elect to include in your installation by selecting the **Software Development Kit** check box, as shown in [Figure 1-3](#).



*Figure 1-3: Vivado Installer - Select Software Development Kit*

For more information about the Eclipse development environment, refer to <http://www.eclipse.org>.

Other SDK components include:

- Drivers and libraries for embedded software development
- GNU compiler and debugger for C/C++ software development targeting the ARM Cortex-A9MP processors in the Zynq SoC Processing System

## PetaLinux Tools

PetaLinux Tools is an Embedded Linux System Development Kit. It offers a full Linux distribution which includes the Linux OS as well as a complete configuration, build, and deploy environment for Xilinx silicon.

For more information, refer to the Xilinx PetaLinux webpage [\[Ref 8\]](#).

The PetaLinux Tools design hub provides information and links to documentation specific to PetaLinux Tools. For more information, refer to [Related Design Hubs, page 108](#).

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## How the Vivado Tools Expedite the Design Process

Vivado is used to add design sources to your hardware. Using IP integrator makes it simple to add desired IPs to your existing design source and create connections for ports (such as clock and reset).

- Vivado and IP integrator are used for all hardware system development. Specification of the microprocessor, peripherals, and the interconnection of these components, along with their respective detailed configuration, takes place in Vivado.
- SDK is used for software development and is available either as part of the Vivado Design Suite, or it can be installed and used without any other Xilinx tools installed on the machine on which it is loaded. SDK can also be used to debug software applications.

The Zynq SoC Processing System (PS) can be booted and made to run without programming the FPGA programmable logic (PL). However, in order to use any soft IP in the fabric, or to bond out PS peripherals using EMIO, programming of the PL is required. You can program the PL in SDK.

For more information on the embedded design process, refer to the *Vivado Design Suite Tutorial: Embedded Processor Hardware Design* (UG940) [\[Ref 1\]](#).

# What You Need to Set Up Before Starting

Before discussing the tools in depth, you should make sure they are installed properly and that your environments match those required for the "Example Project" sections of this guide.

## Hardware Requirements for this Guide

This tutorial targets the Zynq ZC702 Rev 1.1 evaluation board, and can also be used for Rev 1.0 boards. To use this guide, you need the following hardware items, which are included with the evaluation board:

- The ZC702 evaluation board
- AC power adapter (12 VDC)
- USB Type-A to USB Mini-B cable (for UART communications)
- Digilent cable for programming and debugging via JTAG
- SD-MMC flash card for Linux booting

Ethernet cable to connect target board with host machine

## Installation Requirements

### *Vivado Design Suite and SDK*

Make sure that you have installed the 2015.1 software. Visit <http://www.xilinx.com/support/download.html> to confirm that you have the latest software version.

Ensure that you have both the Vivado Design Suite and SDK Tools installed. You can install these two tools together or you can install them separately. When installing them together, make sure you check the **Software Development Kit** check box when running the installer, as shown in [Figure 1-3, page 9](#). For more information on installing the Vivado Design Suite and SDK, refer to the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973) [\[Ref 2\]](#).

## PetaLinux Tools

You will also need to install the PetaLinux Tools to run through the Linux portion of this tutorial. PetaLinux tools run under the Linux host system running one of the following:

- RHEL 5 (32-bit or 64-bit)
- RHEL 6 (32-bit or 64-bit)
- SUSE Enterprise 11 (32-bit or 64-bit)

This can use either a dedicated Linux host system or a virtual machine running one of these Linux operating systems on your Windows development platform. When you install PetaLinux Tools on your system of choice, you must do the following:

- Download PetaLinux **2014.4** SDK software from the Xilinx Website
- Install the PetaLinux **2014.4** release package.
- Add common system packages and libraries to the workstation or virtual machine
- Ensure you have a valid PetaLinux license

### Prerequisites

- 2GB RAM (recommended minimum for Xilinx tools)
- Pentium 4 2GHz CPU clock or equivalent
- 5 GB free HDD space

### Extract the PetaLinux Package

By default, the installer will install the package as a subdirectory within the current directory. Alternatively, you can specify an installation path. Run the downloaded PetaLinux installer.

**Note:** Ensure that the PetaLinux installation path is kept short. The PetaLinux build will fail if the path exceeds 255 characters.

```
bash> ./petalinux-v2014.4-final-installer.run
```

PetaLinux will be installed in the petalinux-v2014.4-final directory, directly underneath the working directory of this command. If the installer is placed in the home directory /home/user, PetaLinux is installed in /home/user/petalinux-v2014.4-final.

Refer to [Chapter 6](#) for additional information about the PetaLinux environment setup, project creation, and project usage examples. A detailed guide on PetaLinux Installation and usage can be found in the *PetaLinux Tools Documentation Reference Guide* (UG1044) [\[Ref 3\]](#).

## Software Licensing

Xilinx software uses FLEXnet licensing. When the software is first run, it performs a license verification process. If license verification does not find a valid license, the license wizard guides you through the process of obtaining a license and ensuring that the license can be used with the tools installed. If the full version of software is not needed, an evaluation license can be used.

For installation instructions and information, see the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973) [Ref 2].

## Tutorial Design Files

See [Design Files for This Tutorial, page 109](#) for information about downloading the design files for this tutorial.

# Using the Zynq SoC Processing System

Now that you've been introduced to the Xilinx® Vivado® Design Suite, you'll begin looking at how to use it to develop an embedded system using the Zynq®-7000 AP SoC Processing System (PS).

The Zynq SoC consists of ARM Cortex-A9 hard intellectual property (IP) and programmable logic (PL). This offering can be used in two ways:

- The Zynq SoC PS can be used in a standalone mode, without attaching any additional fabric IP.
  - IP cores can be instantiated in fabric and attached to the Zynq PS as a PS + PL combination.
- 

## Embedded System Construction

Creation of a Zynq device system design involves configuring the PS to select appropriate boot devices and peripherals. As long as the PS peripherals and available MIO connections meet the design requirements, no bitstream is required. This chapter guides you through creating a design that does not require a bitstream.

### Example Project: Creating a New Embedded Project with Zynq SoC

For this example, you will launch the Vivado Design Suite and create a project with an embedded processor system as the top level.

#### ***Starting Your Design***

1. Start the Vivado Design Suite.
2. In the Vivado Quick Start page, click **Create New Project** to open the New Project wizard.

3. Use the information in the table below to make selections in each of the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Project Name	Project name	edt_tutorial
	Project Location	C:/designs
	Create Project Subdirectory	Leave this checked
Project Type	Specify the type of sources for your design. You can start with RTL or a synthesized EDIF.	<b>RTL Project</b>
	Do not specify sources at this time	Leave this unchecked
Add Sources	Do not make any changes to this screen	
Add Existing IP	Do not make any changes to this screen	
Add Constraints	Do not make any changes to this screen	
Default Part	Select	<b>Boards</b>
	Board	<b>ZYNQ-7 ZC702 Evaluation Board</b>
New Project Summary	Project Summary	Review the project summary before clicking <b>Finish</b> to create the project.

When you click **Finish**, the New Project wizard closes and the project you just created opens in the Vivado design tool.

### ***Creating an Embedded Processor Project***

You will now use the Add Sources wizard to create an embedded processor project.

1. In the Flow Navigator, under **IP Integrator**, click **Create Block Design**.



*Figure 2-1: Create Block Design Button*

The Create Block Design wizard opens.

2. Use the information in the table below to make selections in the Create Block Design wizard.

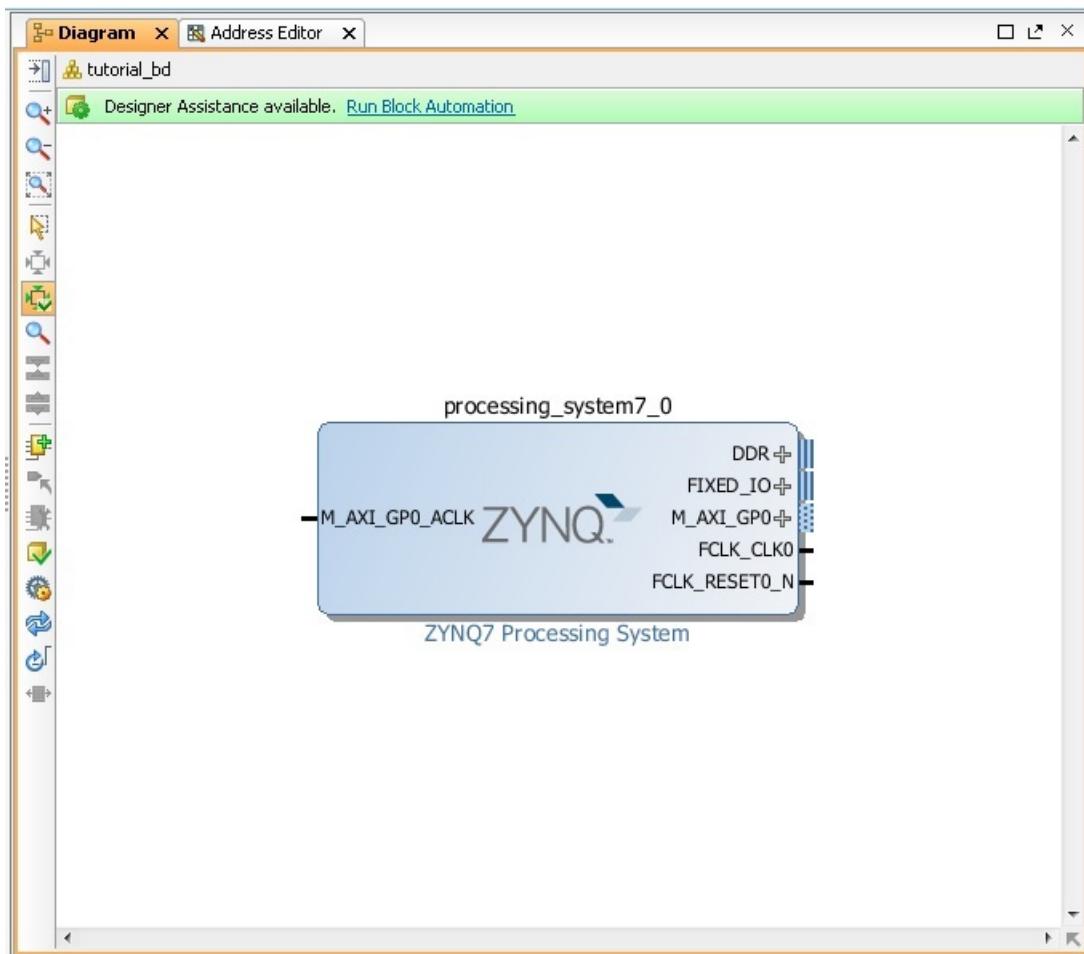
Wizard Screen	System Property	Setting or Command to Use
Create Block Design	Design Name	tutorial_bd
	Directory	<Local to Project>
	Specify Source Set	<b>Design Sources</b>

3. Click **OK**.

The Diagram window view should automatically appear with a message that states that this design is empty. To get started, add some IP from the catalog.

4. Click the **Add IP** button .

5. In the search box, type "zynq" to find the Zynq device IP options, and double-click the **ZYNQ7 Processing System** IP to add it to the Block Design. The Zynq SoC processing system IP block appears in the Diagram view ([Figure 2-2](#)).



*Figure 2-2: Zynq SoC Processing System IP Block*

## Managing the Zynq7 Processing System in Vivado

Now that you've added the processor system to the design, you can begin by managing the various options available for the Zynq7 Processing System.

1. Double-click the **ZYNQ7 Processing System** block in the Block Diagram window. The Re-customize IP dialog box opens. Notice that by default, the processor system does not have any peripherals connected. Connections are symbolized with check marks, as shown in [Figure 2-4, page 18](#).

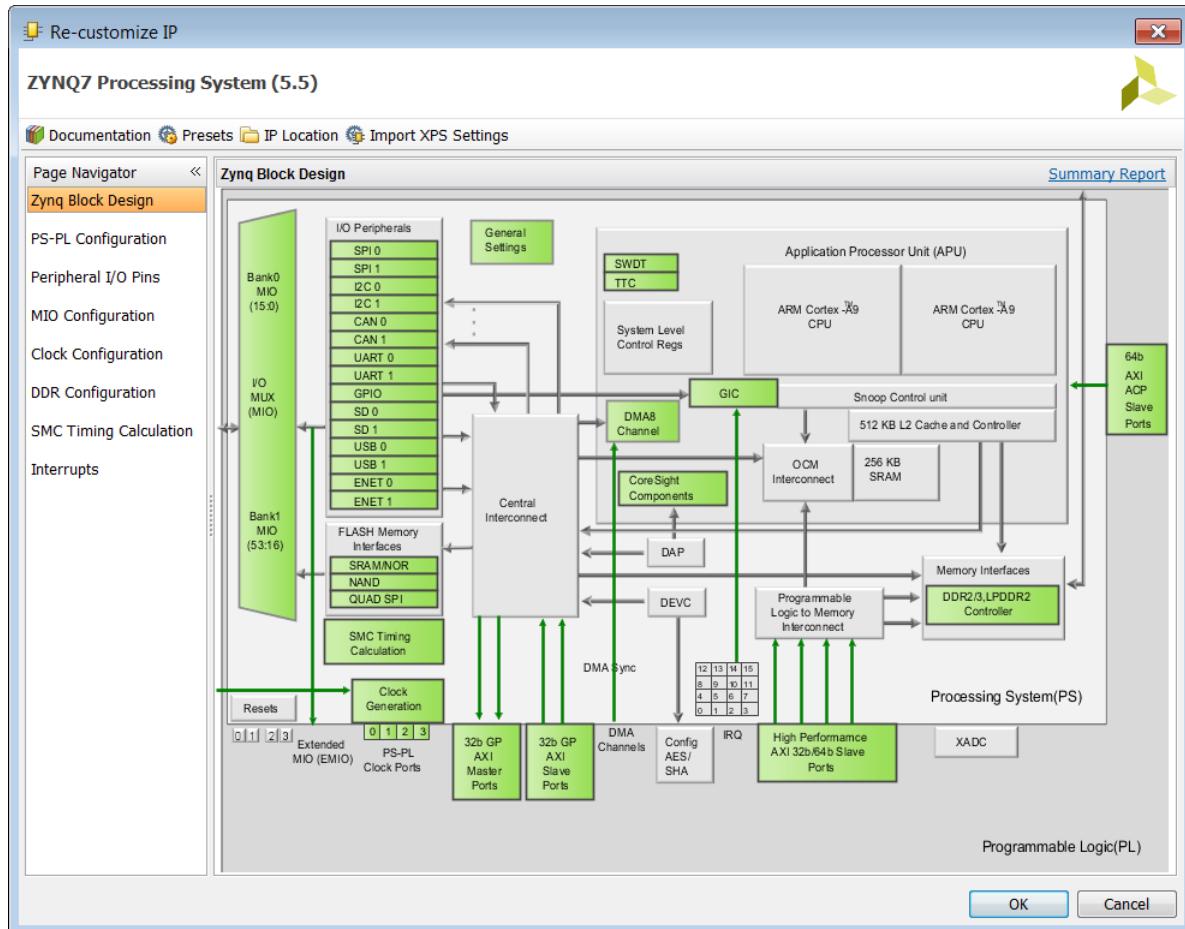


Figure 2-3: Re-customize IP Dialog Box

2. You will use a preset template created for the ZC702 board. In the Re-customize IP window, click the **Presets** button and select **ZC702**.

This configuration wizard enables many peripherals in the Processing System with some MIO pins assigned to them as per the board layout of the ZC702 board. For example, UART1 is enabled and UART0 is disabled. This is because UART1 is connected to the USB-UART connector through UART to the USB converter chip on the ZC702 board.

Note the check marks that appear next to each peripheral name in the Zynq device block diagram that signify the **I/O Peripherals** that are active.

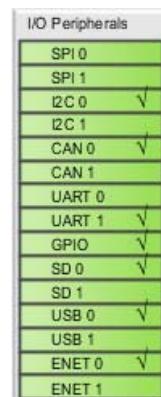


Figure 2-4: I/O Peripherals with Active Peripherals Identified

3. In the block diagram, click one of the green I/O Peripherals (as shown in Figure 2-4). The MIO Configuration window opens for the selected peripheral.

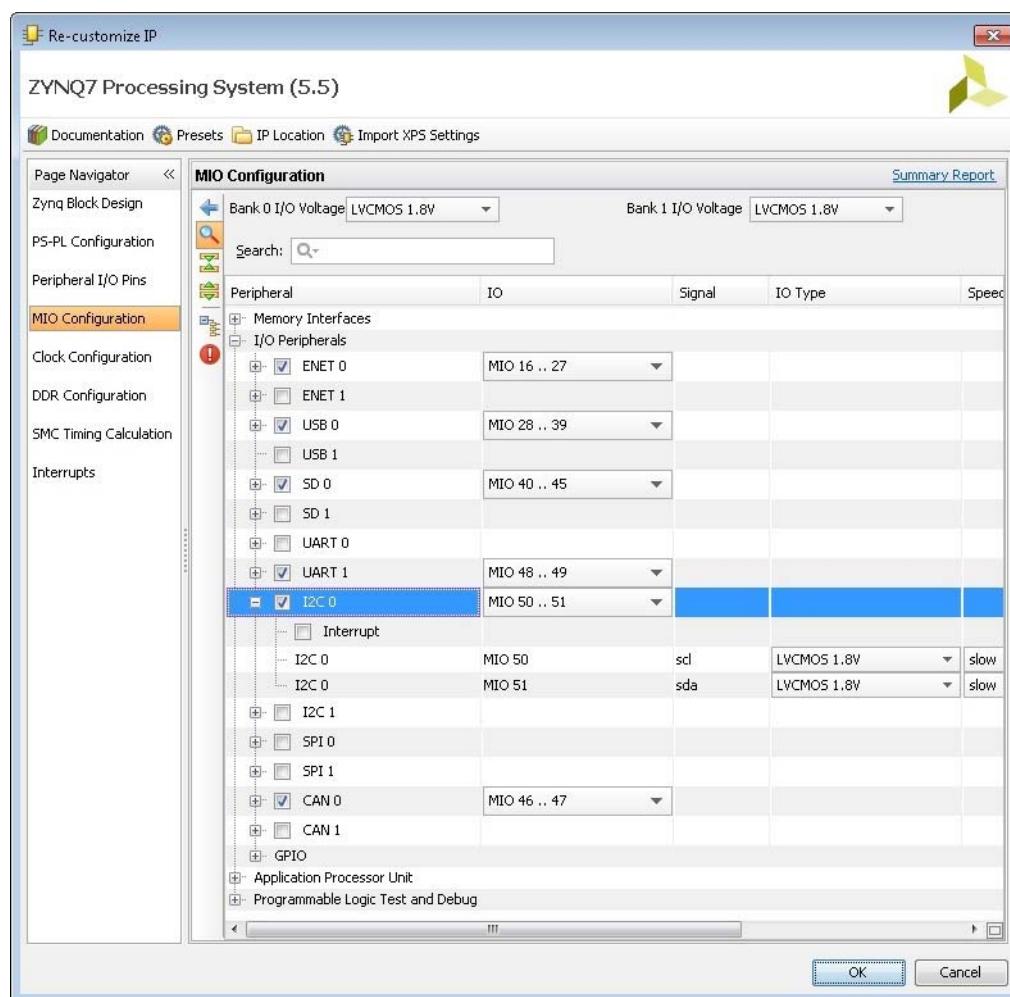


Figure 2-5: MIO Configuration Window

4. Click **OK** to close the Re-customize IP wizard. Vivado implements the changes that you made to apply the ZC702 board presets.

In the Block Diagram window, notice the message stating that Designer assistance is available ([Figure 2-6](#)).

5. Click the **Run Block Automation** link.



*Figure 2-6: Run Block Automation Link*

The Run Block Automation dialog box opens.

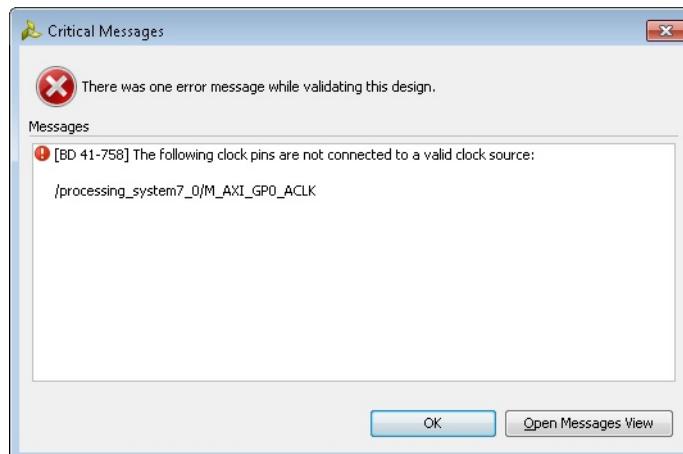
Note that Cross Trigger In and Cross Trigger Out are disabled. For a detailed tutorial with information about cross trigger set-up, refer to *Vivado Design Suite Tutorial: Embedded Processor Hardware Design (UG940)* [[Ref 1](#)].

6. Click **OK** to accept the default processor system options and make default pin connections.

### ***Validating the Design and Connecting Ports***

Now, validate the design.

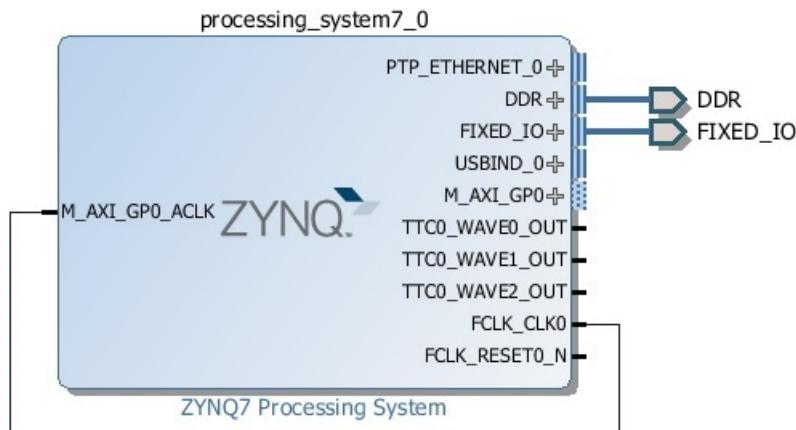
1. Right-click in the white space of the Block Diagram view and select **Validate Design**. Alternatively, you can press the **F6** key.
2. A critical error message appears, indicating that the M\_AXI\_GPO\_ACLK must be connected.



*Figure 2-7: Critical Message Dialog Box*

3. Click **OK** to clear the message.

4. In the Block Diagram view of the ZYNQ7 Processing System, locate the M\_AXI\_GP0\_ACLK port. Hover your mouse over the connector port until the pencil icon appears. Click the **M\_AXI\_GP0\_ACLK** port and drag to the **FCLK\_CLK0** input port to make a connection between the two ports.



*Figure 2-8: ZYNQ7 Processing System with Connection*

5. Validate the design again to ensure there are no other errors. To do this, right-click in the white space of the Block Diagram view and select **Validate Design**.

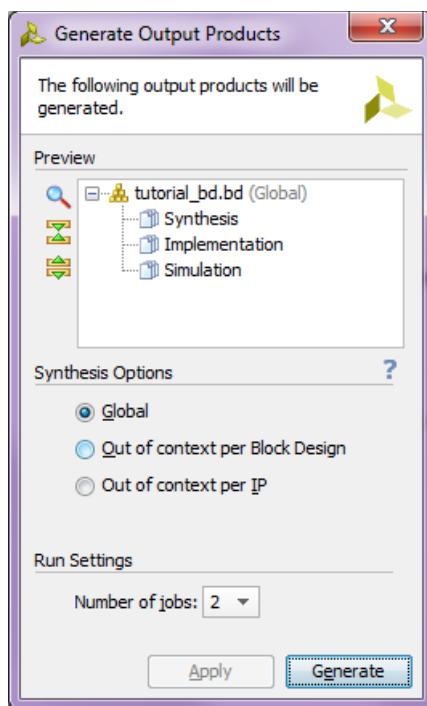
A message dialog box opens and states "Validation successful. There are no errors or critical warnings in this design."

6. Click **OK** to close the message.
7. In the Block Design view, click the **Sources** tab.
8. Click **Hierarchy**.
9. Under **Design Sources**, right-click **tutorial\_bd** and select **Create HDL Wrapper**.

The Create HDL Wrapper dialog box opens. You will use this dialog box to create a HDL wrapper file for the processor subsystem.

10. Select **Let Vivado manage wrapper and auto-update** and click **OK**.
11. In the Block Diagram view Sources window, navigate to **Design Sources > tutorial\_bd\_wrapper**. Right-click the top level block diagram titled **tutorial\_bd\_i - tutorial\_bd (tutorial\_bd.bd)** and select **Generate Output Products**.

The Generate Output Products dialog box opens ([Figure 2-9](#)).



*Figure 2-9: Generate Output Products Dialog Box*

**12. Click **Generate**.**

This step builds all required output products for the selected source. For example, constraints do not need to be manually created for the IP processor system. Vivado automatically generates the .XDC file for the processor sub-system when **Generate Output Products** is selected.

**13. When the Generate Output Products process completes, click **OK**.**

14. In the Block Diagram view Sources window, navigate to **IP Sources**. In this directory you will find the output products that you just generated.

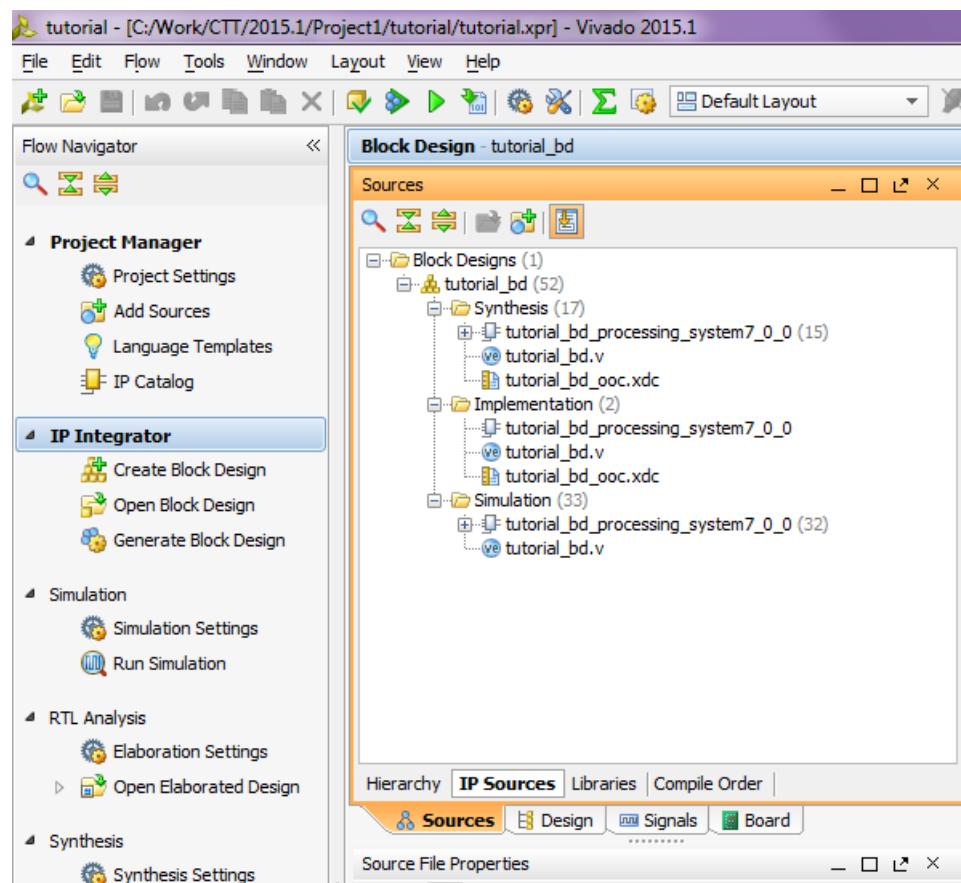


Figure 2-10: Outputs Generated Under IP Sources

### **Synthesizing the Design, Running Implementation, and Generating the Bitstream**

1. You can now synthesize the design. In the Flow Navigator pane, under **Synthesis**, click **Run Synthesis**.

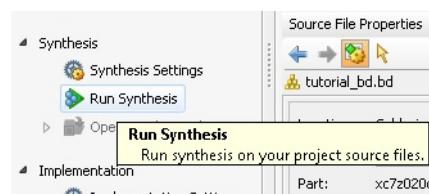
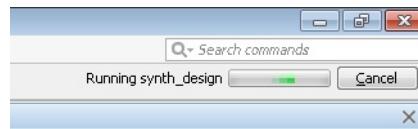


Figure 2-11: Run Synthesis Button

2. If Vivado prompts you to save your project before launching synthesis, click **Save**.

While synthesis is running, a status bar displays in the upper right-hand window. This task bar will spool for various reasons throughout the design process. The status bar signifies that a process is working in the background



*Figure 2-12: Status Bar*

When synthesis completes, the Synthesis Completed dialog box opens.

3. Click **Run Implementation** and click **OK**.

Again, notice that the status bar describes the process running in the background. When implementation completes, the Implementation Completed dialog box opens.

4. Click **Generate Bitstream** and click **OK**.

When Bitstream Generation completes, the Bitstream Generation Completed dialog box opens.

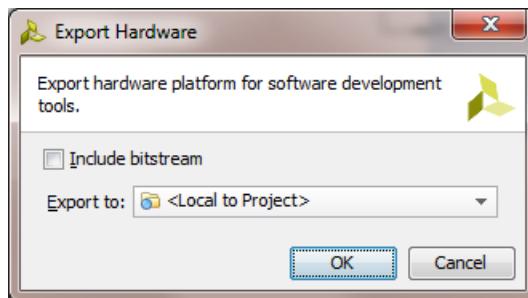
5. Click **Cancel** to close the window.
6. After the Bitstream generation completes, export the hardware and launch the Software Development Kit (SDK) as described in the next section.

### ***Exporting to SDK***

In this example, you will launch SDK from Vivado.

1. From the Vivado toolbar, select **File > Export > Export Hardware**.

The Export Hardware dialog box opens. Make sure that the **Include bitstream** check box is checked (Only when design has PL design and bitstream generated), and that the Export to field is set to the default option of **<Local to Project>**.



*Figure 2-13: Export Hardware to SDK*

2. Click **OK**.

3. Select **File > Launch SDK** to launch SDK.

The Launch SDK dialog box opens.

4. Accept the default selections for **Exported location** and **Workspace**.

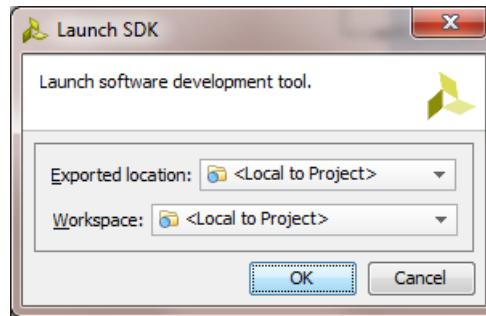


Figure 2-14: Launch SDK Dialog Box

5. Click **OK**.

SDK opens. Notice that when SDK launches, the hardware description file is automatically loaded. The `system.hdf` tab shows the address map for the entire Processing System.

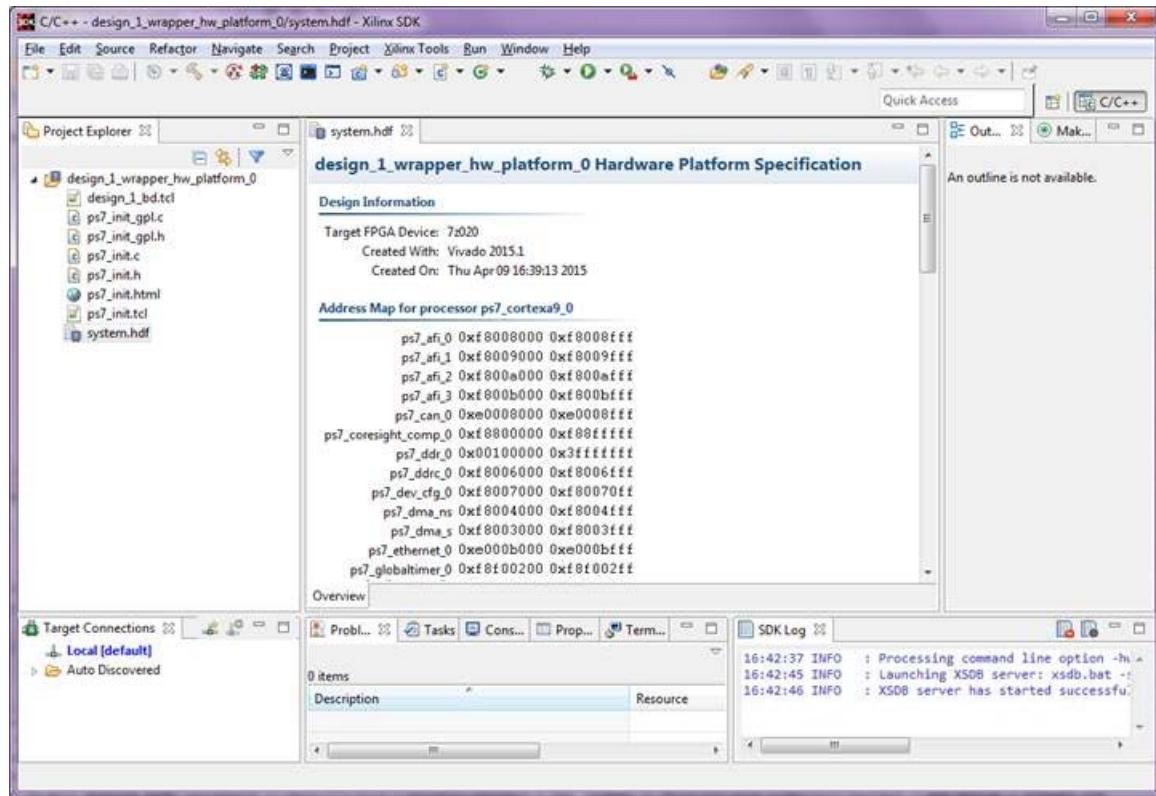


Figure 2-15: Address Map in SDK system.hdf Tab

6. Close SDK.

## What Just Happened?

Vivado exported the hardware specifications to the selected workspace where software development will take place. If <**Local to Project**> was selected, then Vivado created a new workspace in the Vivado project folder. The name of the workspace is <project\_name>.sdk. In this example, the workspace created is C:/designs/edt\_tutorial/edt\_tutorial.sdk.

The Vivado design tool exported the Hardware Platform Specification for your design (system.hdf in this example) to SDK. In addition to system.hdf, the following additional files are exported to SDK:

- design\_1\_bd.tcl
- ps7\_init.c
- ps7\_init.h
- ps7\_init.html
- ps7\_init.tcl
- ps7\_init\_gpl.c
- ps7\_init\_gpl.h
- system.hdf

The system.hdf file opens by default when SDK launches. The address map of your system read from this file is shown by default in the SDK window.

The ps7\_init.c, ps7\_init.h, ps7\_init\_gpl.c, and ps7\_init\_gpl.h files contain the initialization code for the Zynq SoC Processing System and initialization settings for DDR, clocks, phase-locked loops (PLLs), and MIOs. SDK uses these settings when initializing the processing system so that applications can be run on top of the processing system. Some settings in the processing system are fixed for the ZC702 evaluation board.

## What's Next?

Now you can start developing the software for your project using SDK. The next sections help you create a software application for your hardware platform.

## Example Project: Running the "Hello World" Application

1. In this example, you will learn how to manage the board settings, make cable connections, connect to the board through your PC, and run a simple hello world software application in SDK. Connect the power cable to the board.
2. Connect a Digilent cable between the Windows Host machine and the Target board with the following SW10 switch settings:

Bit-1 is 0

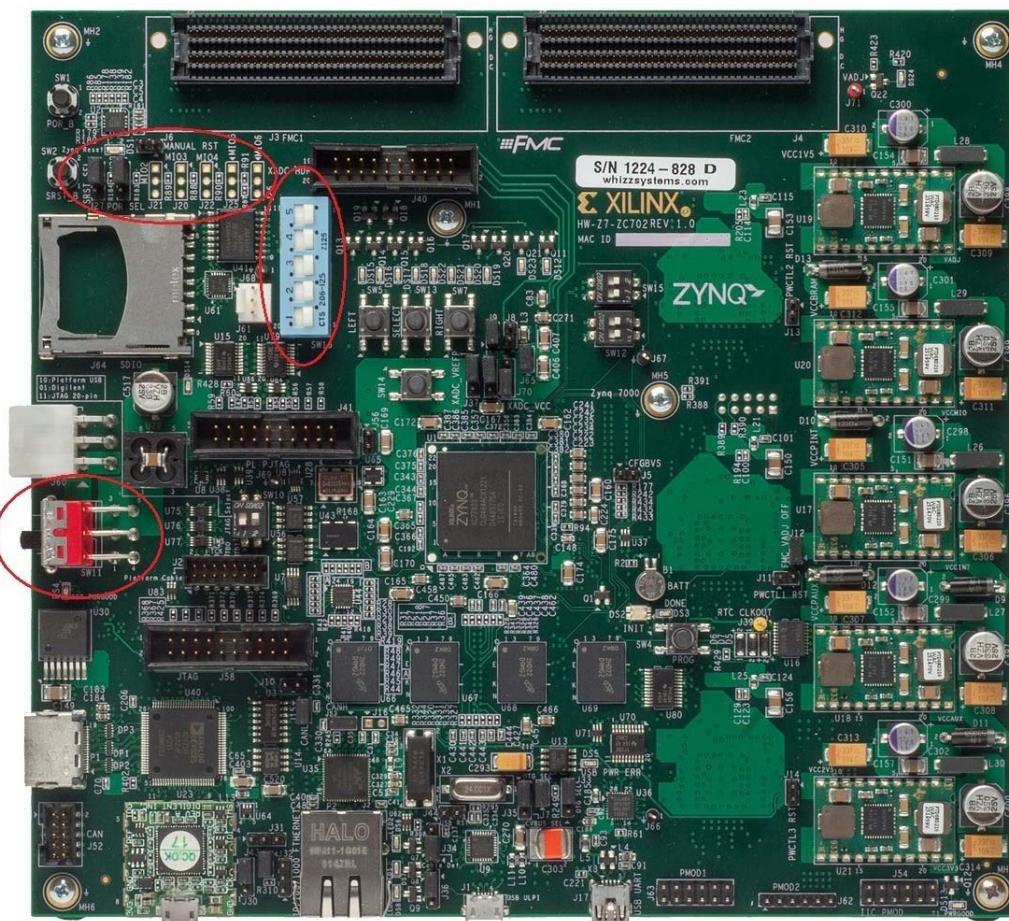
Bit-2 is 1

**Note:** 0 = switch is open. 1 = switch is closed.

3. Connect a USB cable to connector **J17** on the target board with the Windows Host machine. This is used for USB to serial transfer.
4. Power on the ZC702 board using the switch indicated in the figure below.



**IMPORTANT:** Ensure that jumpers J27 and J28 are placed on the side farther from the SD card slot and change the SW16 switch setting as shown in *Figure 2-16*.

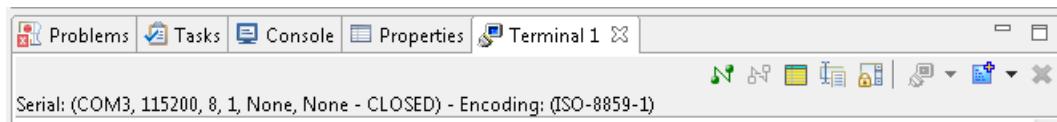


*Figure 2-16: ZC702 Board Power Switch*

5. Open SDK and set the workspace path to your project file, which in this example is C:/designs/edt\_tutorial/edt\_tutorial.sdk.

Alternately, you can open SDK with a default workspace and later switch it to the correct workspace by selecting **File > Switch Workspace** and then selecting the workspace.

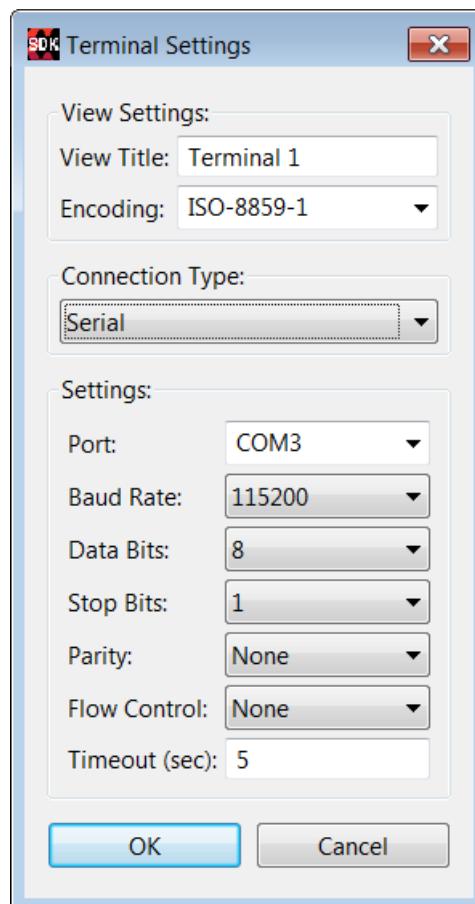
6. Open a serial communication utility for the COM port assigned on your system. SDK provides a serial terminal utility, which will be used throughout the tutorial; select **Window > Show View > Terminal** to open it.



*Figure 2-17: Terminal Window Header Bar*

7. Click the **Connect** button  to set the serial configuration and connect it.  
 8. Click the **Settings** button  to open the Terminal Settings dialog box.

*Figure 2-18* shows the standard configuration for the Zynq SoC Processing System.



*Figure 2-18: Terminal Settings Dialog Box*

9. Select **File > New > Application Project**.

The New Project wizard opens.

10. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Properties	Setting or Command to Use
Application Project	Project Name	hello_world
	Use Default Location	Select this option
	Hardware Platform	<b>tutorial_bd_wrapper_hw_platform_0</b>
	Processor	PS7_cortexa9_0
	OS Platform	<b>standalone</b>
	Language	<b>C</b>
	Board Support Package	Select <b>Create New</b> and provide the name of hello_world_bsp
Templates	Available Templates	<b>Hello World</b>

SDK creates the `hello_world` application project and `hello_world_bsp` board support package (BSP) project under the project explorer. It automatically compiles both and creates the ELF file.

11. Right-click **hello\_world** and select **Run as > Run Configurations**.

12. Right-click **Xilinx C/C++ application (GDB)** and click **New**.

SDK creates the new run configuration, named `hello_world Debug`.

The configurations associated with the application are pre-populated in the Main tab of the launch configurations.

13. Click the **Target Setup** tab in the launch configurations and review the settings.

Notice that there is a configuration path to the initialization TCL file. The path of `ps7_init.tcl` is mentioned here. This file was exported when you exported your design to SDK; it contains the initialization information for the processing system.

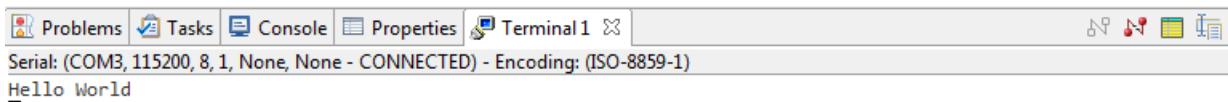
14. The STDIO Connection tab is available in the launch configurations settings. You can use this to have your STDIO connected to the console. You will not use this now because you have already launched a serial communication utility. There are more options in launch configurations, but you will focus on them later.

15. Click **Run**.

A message appears asking if you want to launch the application even though configuration of the FPGA is not done.

## 16. Click **OK**.

"Hello World" appears on the serial communication utility in Terminal 1.



*Figure 2-19: Output on Serial Terminal*

**Note:** There was no bitstream download required for the above software application to be executed on the Zynq SoC evaluation board. The ARM Cortex A9 dual core is already present on the board. Basic initialization of this system to run a simple application is done by the Device initialization TCL script.

## What Just Happened?

The application software sent the "Hello World" string to the UART1 peripheral of the PS section.

From UART1, the "Hello world" string goes byte-by-byte to the serial terminal application running on the host machine, which displays it as a string.

## Additional Information

### ***Board Support Package***

The board support package (BSP) is the support code for a given hardware platform or board that helps in basic initialization at power up and helps software applications to be run on top of it. It can be specific to some operating systems with bootloader and device drivers.

### ***Standalone OS***

Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts, and exceptions, as well as the basic processor features of a hosted environment. These basic features include standard input/output, profiling, abort, and exit. It is a single threaded semi-hosted environment.

The application you ran in this chapter was created on top of the Standalone OS. The BSP that your software application targets is selected during the New Application Project creation process. If you would like to change the target BSP after project creation, you can manage the target BSP by right-clicking the software application and selecting **Change Referenced BSP**.

# Using the GP Port in Zynq Devices

One of the unique features of using the Xilinx® Zynq®-7000 AP SoC as an embedded design platform is in using the Zynq SoC Processing System (PS) for its ARM Cortex-A9 dual core processing system as well as the Programmable Logic (PL) available on it.

In this chapter, you will create a design with:

- AXI GPIO and AXI Timer with interrupt from fabric to PS section
- Zynq SoC PS GPIO pin connected to the PL side pin via the EMIO interface

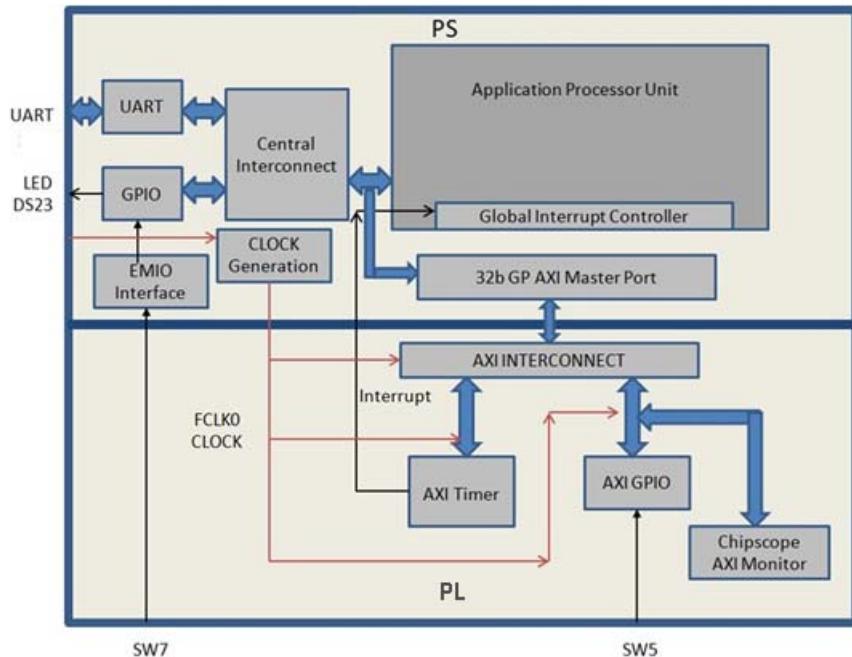
The flow of this chapter is similar to that in [Chapter 2](#) and uses the Zynq device as a base hardware design. It is assumed that you understand the concepts discussed in [Chapter 2](#) regarding adding the Zynq device into a Vivado® IP integrator block diagram design. If you skipped that chapter, you might want to look at it because we will continually refer to the material in [Chapter 2](#) throughout this chapter.

---

## Adding IPs in Fabric to the Zynq SoC Processing System

There is no restriction on the complexity of an intellectual property (IP) that can be added in fabric to be tightly coupled with the Zynq SoC PS. This section covers a simple example with the AXI GPIO, AXI Timer with interrupt, and the PS section GPIO pin connected to PL side pin via the EMIO interface.

In this section, you will create a design to check the functionality of the AXI GPIO, AXI Timer with interrupt instantiated in fabric, and PS section GPIO with EMIO interface. The block diagram for the system is as shown in [Figure 3-1, page 31](#).



*Figure 3-1: Block Diagram*

You can use the system created in [Chapter 2](#) and continue after [Example Project: Creating a New Embedded Project with Zynq SoC, page 14](#).

In the examples in this chapter, we will expand on the design in [Chapter 2](#). You will make the following design changes:

- The fabric-side AXI GPIO is assigned a 1-bit channel width and is connected to the SW5 push-button switch on the ZC702 board.
- The PS GPIO ports are modified to include a 1-bit interface that routes a fabric pin (via the EMIO interface) to the SW7 push-button switch on the board.
- In the PS section, another 1-bit GPIO is connected to the DS23 LED on the board, which is on the MIO port.
- The AXI timer interrupt is connected from fabric to the PS section interrupt controller. The timer starts when you press any of the selected push buttons on the board. After the timer expires, the timer interrupt is triggered.
- Along with making the above hardware changes, you will write the application software code. The code will function as follows:
  - A message appears in the serial terminal and asks you to select the push button switch to use on the board (either SW7 or SW5).
  - When the appropriate button is pressed, the timer automatically starts, switches OFF LED DS23, and waits for the timer interrupt to happen.
  - After the Timer Interrupt, LED DS23 switches ON and execution starts again and waits for you to again select the push button switch in the serial terminal.

## Example Project: Validate Instantiated Fabric IP Functionality

In this example, you will add the AXI GPIO, AXI Timer, the interrupt instantiated in fabric, and the EMIO interface. You will then validate the fabric additions.

1. Open the Vivado® Design Suite.
2. Under the Recent Projects column, click the **edt\_tutorial** design that you created in [Chapter 2](#).
3. Under **IP Integrator**, click **Open Block Design**.
4. In the Diagram window, right-click in the blank space and select **Add IP**.
5. In the search box, type **AXI GPIO** and double-click the **AXI GPIO** IP to add it to the Block Design.

The AXI GPIO IP block appears in the Diagram view.

6. In the Diagram window, right-click in the blank space and select **Add IP**.
7. In the search box, type **AXI Timer** and double-click the **AXI Timer** IP to add it to the Block Design. The AXI Timer IP block appears in the Diagram view.
8. You also need to edit the EMIO configuration of the ZYNQ7 SoC Processing system and enable interrupts. Right-click the **ZYNQ7 Processing System** IP block and select **Customize Block**.

**Note:** You can also double-click the IP block to make customizations.

The Customize Block dialog box opens ([Figure 3-2, page 33](#)).

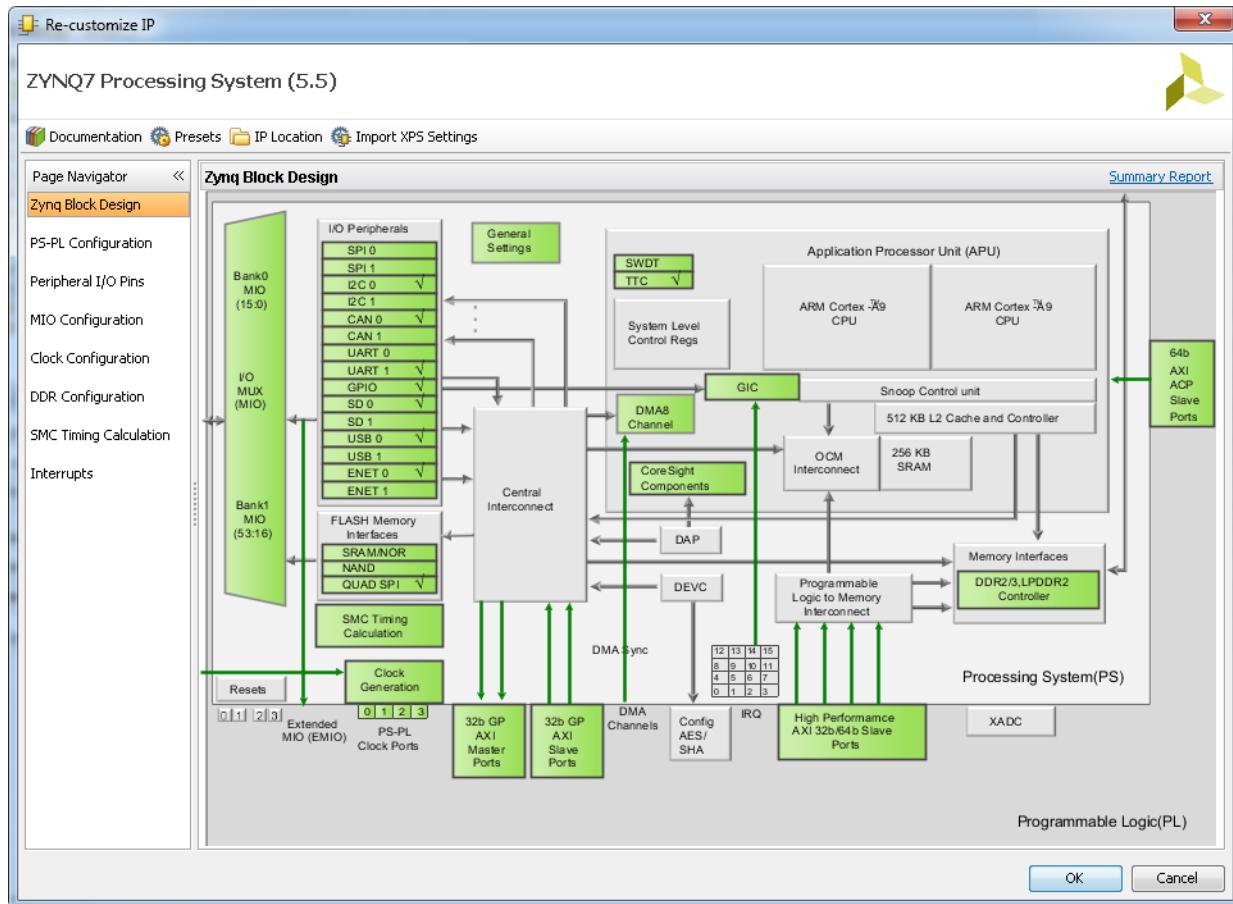


Figure 3-2: Customize Block Dialog Box

9. Click **MIO Configuration**.
10. Expand **I/O Peripherals > GPIO** and select the **EMIO GPIO (Width)** check box.
11. Change the EMIO GPIO (Width) to **1**.
12. With the ZYNQ7 Processing System configuration options still open, navigate to **Interrupts > Fabric Interrupts > PL-PS Interrupt Ports**.
13. Check the **Fabric Interrupts** box and also check **IRQ\_F2P[15:0]** to enable PL-PS interrupts in the IP Core.
14. Click **OK** to accept the changes to the ZYNQ7 Processing System IP. The Diagram looks like Figure 3-3, page 34.

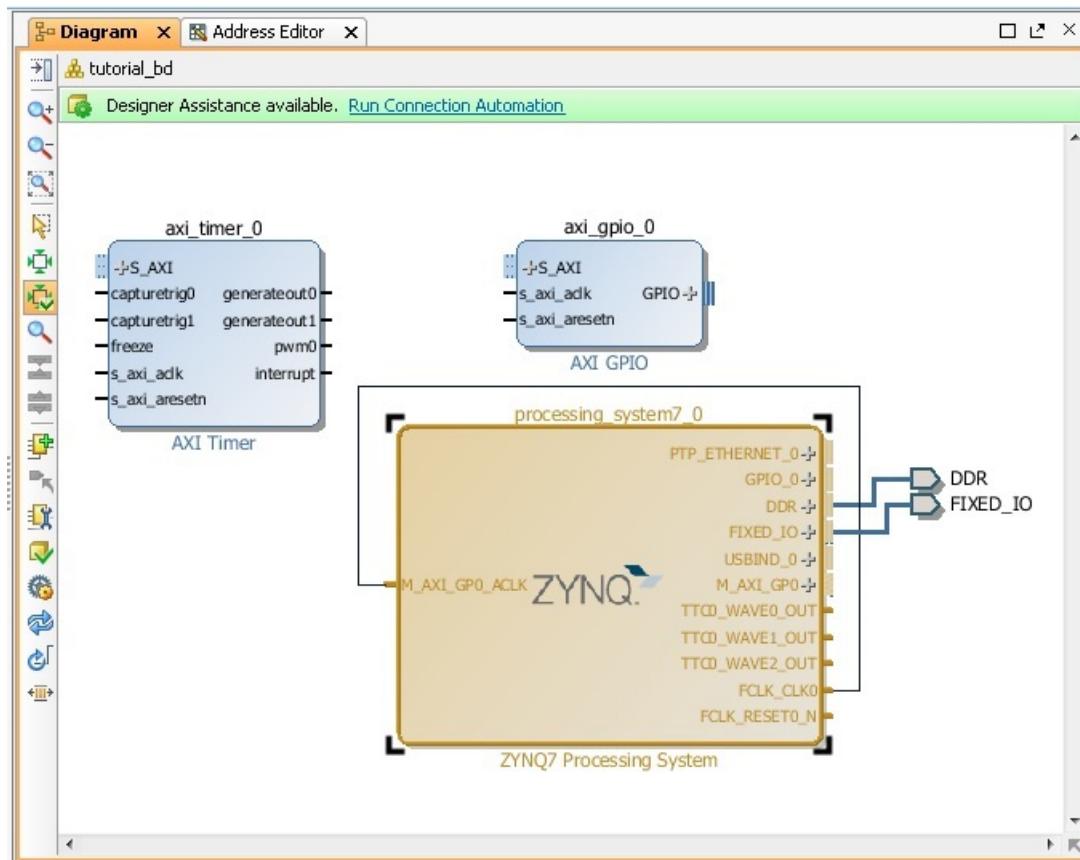


Figure 3-3: ZYNQ7 Processing System IP

15. Click the **Run Connection Automation** link at the top of the page to automate the connection process for the newly added IP blocks.
16. In the Run Connection Automation wizard, select the check box next to **All Automation** (Figure 3-4).
17. Click **OK**.

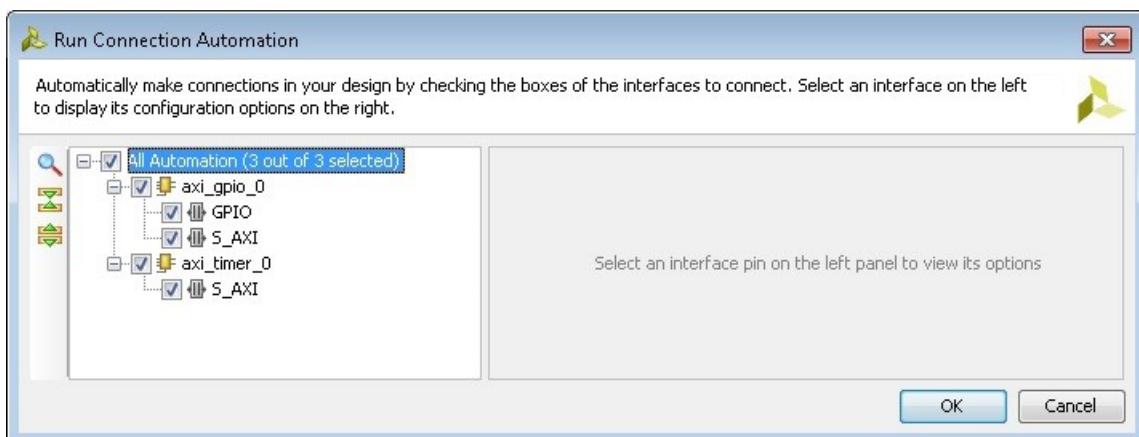
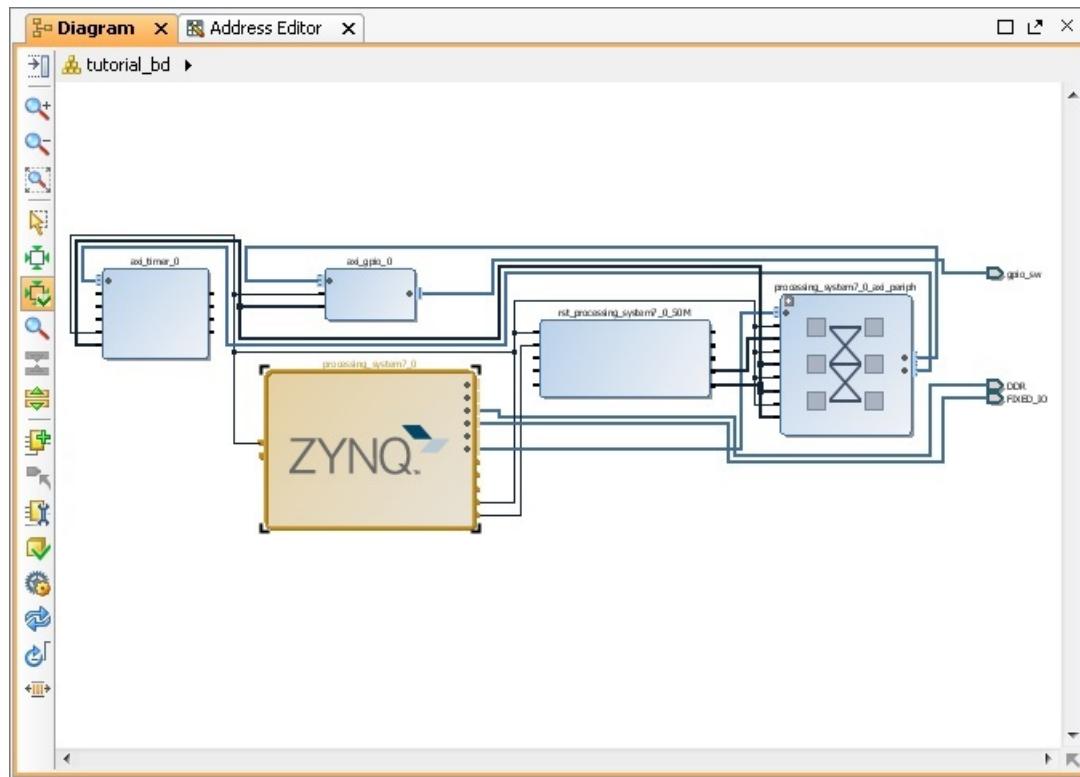


Figure 3-4: Run Connection Automation Wizard

Upon completion, the updated diagram looks like [Figure 3-5](#).



*Figure 3-5: Updated Block Diagram with Connections*

18. Right-click the **AXI GPIO** IP block and select **Customize Block**.

**Note:** You can also double-click the IP block to make customizations.

19. Under the **Board** tab, make sure that **GPIO** is set to **Custom**.

20. Select the **IP Configuration** tab. In the GPIO section, change the **GPIO Width** to **1** because you only need one GPIO port. Also ensure that **All Inputs** and **All Outputs** are both unchecked.

21. Click **OK** to accept the changes.

22. Notice that the Interrupt port is not automatically connected to the AXI Timer IP Core. In the Block Diagram view, locate the **IRQ\_F2P[0:0]** port on the ZYNQ7 Processing System.

23. Scroll your mouse over the connector port until the pencil icon appears, then click the **IRQ\_F2P[0:0]** port and drag to the **interrupt** output port on the AXI Timer IP core to make a connection between the two ports.

24. Notice that the ZYNQ7 Processing System GPIO\_0 port is not connected. Right-click the **GPIO\_0** output port on the **ZYNQ7 Processing System** and select **Make External**.

The pins are external but do not have the needed constraints for our board. In order to constrain your hardware pins to specific device locations, follow the steps below. These steps can be used for any manual pin placements.

25. Click **Open Elaborated Design** under RTL Analysis in the Flow Navigator view.

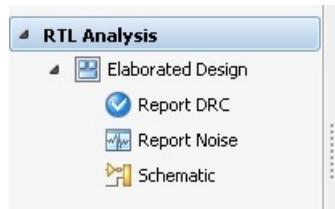


Figure 3-6: Open Elaborated Design

26. When the Elaborate Design message box opens, as shown in Figure 3-7, click **OK**.

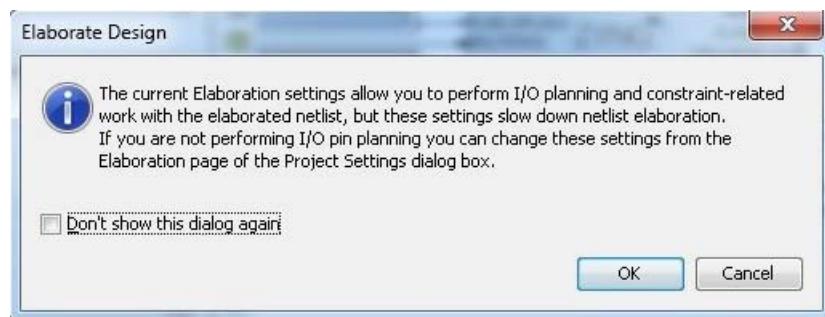


Figure 3-7: Elaborate Design Message Box



**TIP:** The design might take a few minutes to elaborate. If you want to do something else in Vivado while the design elaborates, you can click the Background button to have Vivado continue running the process in the background.

27. Under the I/O Ports tab view at the bottom of the Vivado window (Figure 3-8), expand the **GPIO\_0\_1522** and **GPIO\_23220** ports to check the site (pin) map.

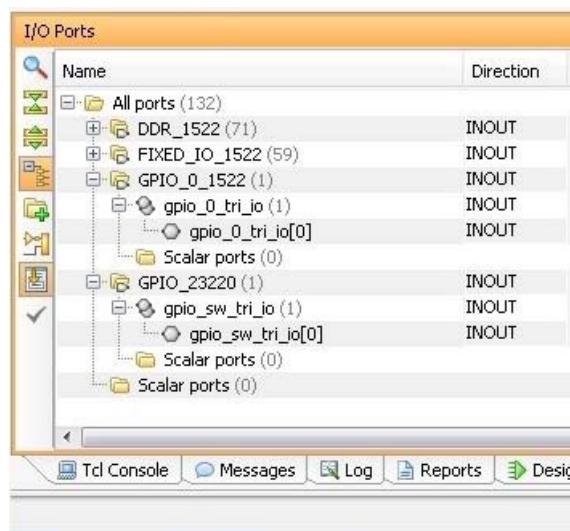


Figure 3-8: I/O Ports Site Map

28. Find **gpio\_0\_tri\_io[0]** and set the following properties, shown in Figure 3-9:

- **Site = F19**
- **I/O Std = LVCMOS25**

29. Find **gpio\_sw\_tri\_io[0]** and set the following properties, shown in Figure 3-9:

- **Site = G19**
- **I/O Std = LVCMOS25**

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Site	Fixed	Bank	I/O Std
All ports (132)								(Multiple)*
DDR_1522 (71)	INOUT					✓		(Multiple)*
FIXED_IO_1522 (59)	INOUT					✓		(Multiple)*
GPIO_0_1522 (1)	INOUT					✓		35 LVCMOS25*
gpio_0_tri_io (1)	INOUT				F19	✓		35 LVCMOS25*
gpio_0_tri_io[0]	INOUT					✓		35 LVCMOS25*
Scalar ports (0)								
GPIO_23220 (1)	INOUT					✓		35 LVCMOS25*
gpio_sw_tri_io (1)	INOUT					✓		35 LVCMOS25*
gpio_sw_tri_io[0]	INOUT				G19	✓		35 LVCMOS25*
Scalar ports (0)								
Scalar ports (0)								

Figure 3-9: I/O Port Properties

**Note:** For additional information about creating other design constraints, refer to the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 4].

30. In the Flow Navigator, under **Program and Debug**, select **Generate Bitstream**.

The Save Project dialog box opens. Make sure the **Elaborated Design - constrs\_1** check box is selected.

31. Click **Save**.

The Synthesis is Out-of-date dialog box opens.

32. Click **Yes**.

33. After the Bitstream generation completes, export the hardware and launch the Xilinx Software Development Kit (SDK) as described in [Exporting to SDK, page 23](#).

## Working with SDK

1. SDK launches with the "Hello World" project you created with the Standalone PS in [Chapter 2](#).
2. Select **Project > Clean** to clean and build the project again.
3. Open the `helloworld.c` file and modify the application software code as described in Standalone Application Software for the Design, in [Chapter 2](#).
4. Open the serial communication utility with baud rate set to **115200**.

**Note:** This is the baud rate that the UART is programmed to on Zynq devices.

5. Connect to the board.

Because you have a bitstream for the PL Fabric, you must download the bitstream.

6. Select **Xilinx Tools > Program FPGA**. The Program FPGA dialog box, shown in [Figure 3-10, page 39](#), opens. It displays the bitstream exported from Vivado.

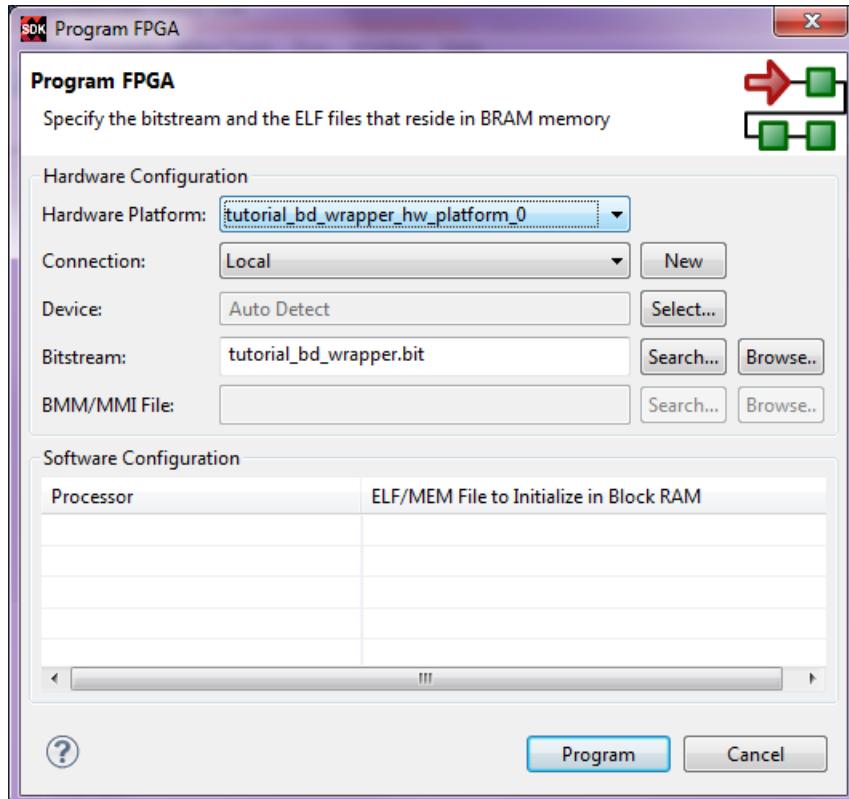


Figure 3-10: Program FPGA Dialog Box with Bitstream File

7. Click **Program** to download the bitstream and program the PL Fabric.
8. Run the project similar to the steps in [Example Project: Running the "Hello World" Application, page 26](#).
9. In the system, the AXI GPIO pin is connected to push button **SW5** on the board, and the PS section GPIO pin is connected to push button **SW7** on the board via an EMIO interface.
10. Follow the instructions printed on the serial terminal to run the application.

## Standalone Application Software for the Design

The system you designed in this chapter requires application software for the execution on the board. This section describes the details about the application software.

The `main()` function in the application software is the entry point for the execution. This function includes initialization and the required settings for all peripherals connected in the system. It also has a selection procedure for the execution of the different use cases, such as AXI GPIO and PS GPIO using EMIO interface. You can select different use cases by following the instruction on the serial terminal.

## Application Software Steps

Application Software is composed of the following steps:

1. Initialize the AXI GPIO module.
2. Set a direction control for the AXI GPIO pin as an input pin, which is connected with the **SW5** push button on the board. The location is fixed via LOC constraint in the user constraint file (UCF) during system creation.
3. Initialize the AXI TIMER module with device ID 0.
4. Associate a timer callback function with AXI timer ISR.

This function is called every time the timer interrupt happens. This callback switches on the LED **DS23** on the board and sets the interrupt flag.

The `main()` function uses the interrupt flag to halt execution, waits for timer interrupt to happen, and then restarts the execution.

5. Set the reset value of the timer, which is loaded to the timer during reset and timer starts.
6. Set timer options such as Interrupt mode and Auto Reload mode.
7. Initialize the PS section GPIO.
8. Set the PS section GPIO, channel 0, pin number 10 to the output pin, which is mapped to the MIO pin and physically connected to the LED **DS23** on the board.
9. Set PS Section GPIO channel number 2, pin number 0, to an input pin, which is mapped to PL side pin via the EMIO interface and physically connected to the **SW7** push button switch.
10. Initialize Snoop control unit Global Interrupt controller. Also, register Timer interrupt routine to interrupt ID '91', register the exceptional handler, and enable the interrupt.
11. Execute a sequence in the loop to select between AXI GPIO or PS GPIO use case via serial terminal.

The software accepts your selection from the serial terminal and executes the procedure accordingly.

After the selection of the use case via the serial terminal, you must press a push button on the board as per the instruction on terminal. This action switches off the LED **DS23**, starts the timer, and tells the function to wait infinitely for the Timer interrupt to happen. After the Timer interrupt happens, LED **DS23** switches ON and restarts execution.

For more details about API related to device drivers, refer to the *Zynq-7000 Software Developers Guide* (UG821) [\[Ref 5\]](#).

## Application Software Code

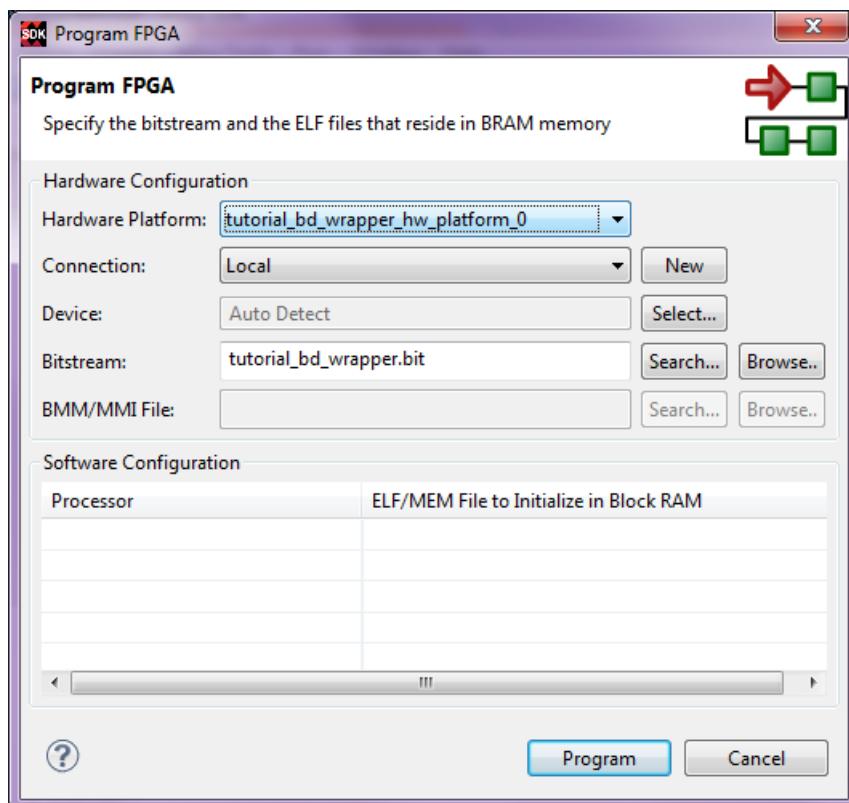
The Application software for the system is included in `helloworld.c`, which is available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

## Run the New Software Application in SDK

Next, you will run the new software application in SDK.

1. Select **Xilinx Tools > Program FPGA**.

The Program FPGA dialog box, shown in [Figure 3-11](#), opens. It displays the bitstream exported from Vivado.



*Figure 3-11: Program FPGA Dialog Box with Bitstream file*

2. Follow the steps in [Example Project: Running the "Hello World" Application, page 26](#), to run the new application.

# Debugging with SDK

This chapter describes debug possibilities with the design flow you have already been working with. The first option is debugging with software using the Xilinx® Software Development Kit (SDK).

SDK debugger provides the following debug capabilities:

- Supports debugging of programs on MicroBlaze™ and ARM Cortex-A9 processor architectures
- Supports debugging of programs on hardware boards
- Supports debugging on heterogeneous multi-processor hardware systems
- Supports debugging on remote hardware systems
- Provides a feature-rich IDE to debug programs
- Provides a Tool Command Language (Tcl) interface for running test scripts and automation

The SDK debugger enables you to see what is happening to a program while it executes. You can set breakpoints or watchpoints to stop the processor, step through program execution, view the program variables and stack, and view the contents of the memory in the system.

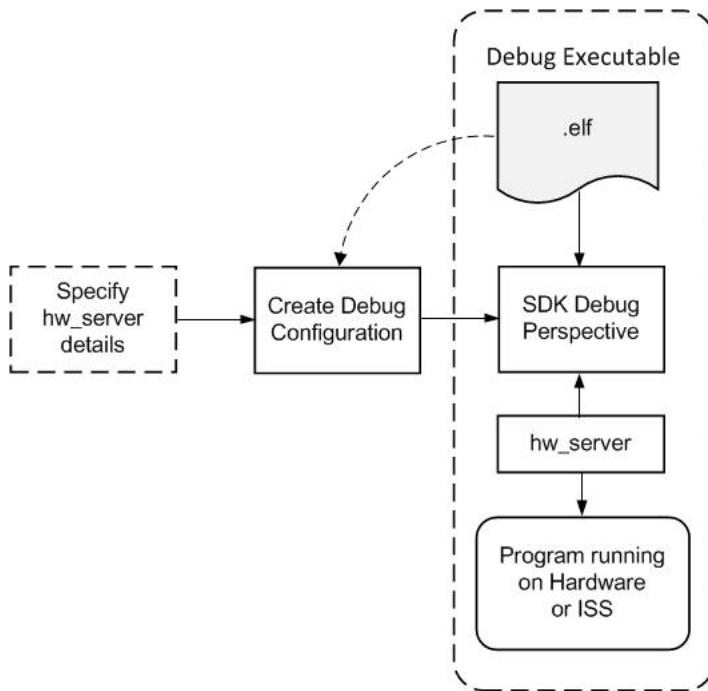
The SDK debugger supports debugging through Xilinx System Debugger and GNU Debugger (GDB).

**Note:** The GDB flow is deprecated and will not be available for future devices.

## Xilinx System Debugger

The Xilinx® System Debugger uses the Xilinx hw\_server as the underlying debug engine. SDK translates each user interface action into a sequence of TCF commands. It then processes the output from System Debugger to display the current state of the program being debugged. It communicates to the processor on the hardware using Xilinx hw\_server.

The debug workflow is described in [Figure 4-1, page 43](#).



*Figure 4-1: System Debugger Flow*

The workflow is made up of the following components:

- **Executable ELF File:** To debug your application, you must use an Executable and Linkable Format (ELF) file compiled for debugging. The debug ELF file contains additional debug information for the debugger to make direct associations between the source code and the binaries generated from that original source. To manage the build configurations, right-click the software application and select **Build Configurations > Manage**.
- **Debug Configuration:** In order to launch the debug session, you must create a debug configuration in SDK. This configuration captures options required to start a debug session, including the executable name, processor target to debug, and other information. To create a debug configuration, right click your software application and select **Debug As > Debug Configurations**.
- **SDK Debug Perspective:** Using the Debug perspective, you can manage the debugging or running of a program in the Workbench. You can control the execution of your program by setting breakpoints, suspending launched programs, stepping through your code, and examining the contents of variables. To view the Debug Perspective, select **Window > Open Perspective > Debug**.

You can repeat the cycle of modifying the code, building the executable, and debugging the program in SDK.

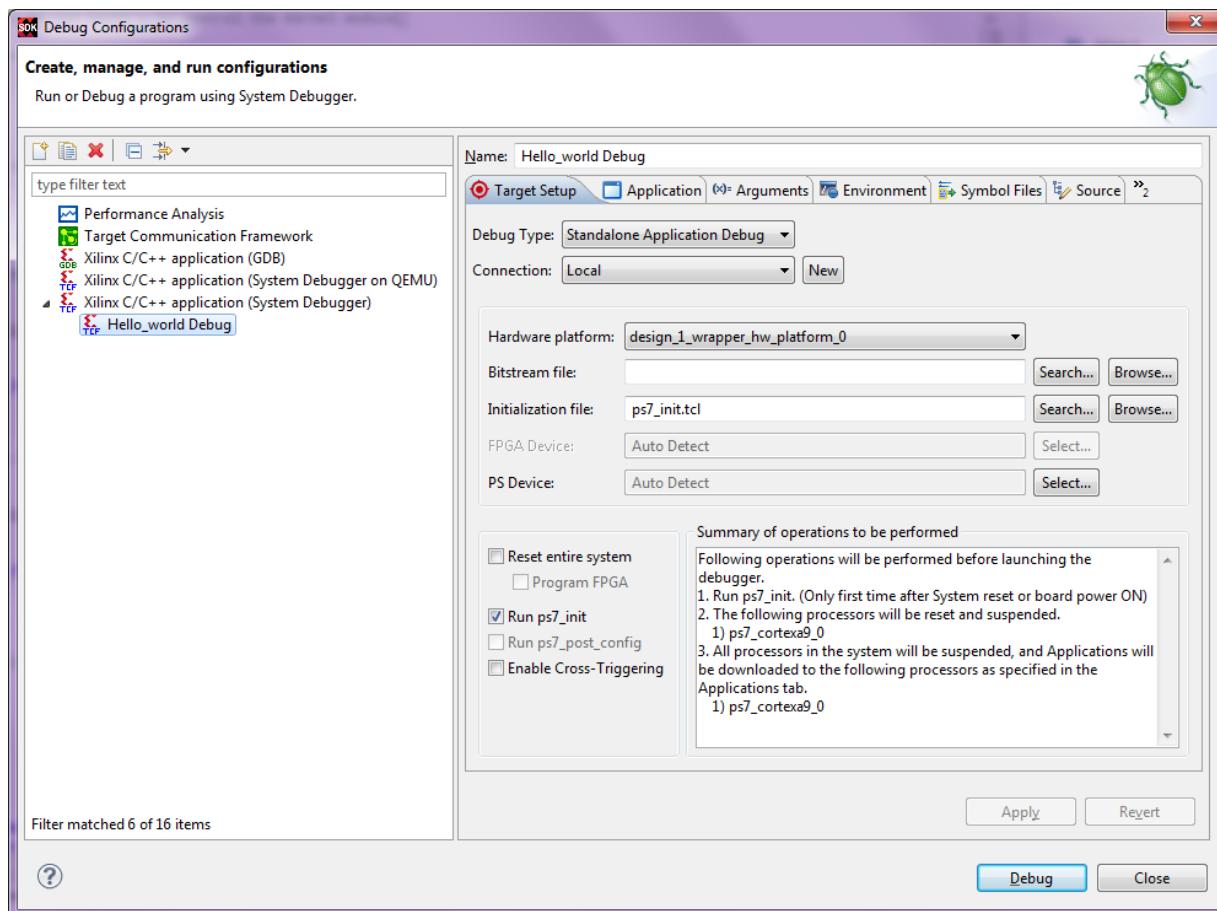
**Note:** If you edit the source after compiling, the line numbering will be out of step because the debug information is tied directly to the source. Similarly, debugging optimized binaries can also cause unexpected jumps in the execution trace.

## Debugging with Software Using SDK

In this example, you will walk through debugging a hello world application. If you modified the hello world application in the prior chapter, you will need to create a new hello world application prior to debugging. Follow the steps in [Example Project: Running the "Hello World" Application, page 26](#), to create a new hello world application.

After you create the Hello World Application, you will work through the below example to debug the software using SDK.

1. In the C/C++ Perspective, right-click on the `Hello_world` Project and select **Debug As > Launch on Hardware (System Debugger)**. The Debug Perspective opens.



*Figure 4-2: Debug Configurations*

**Note:** If the Debug Perspective window does not automatically open, select **Window > Open > Perspective > Other**, then select **Debug** in the Open Perspective wizard.

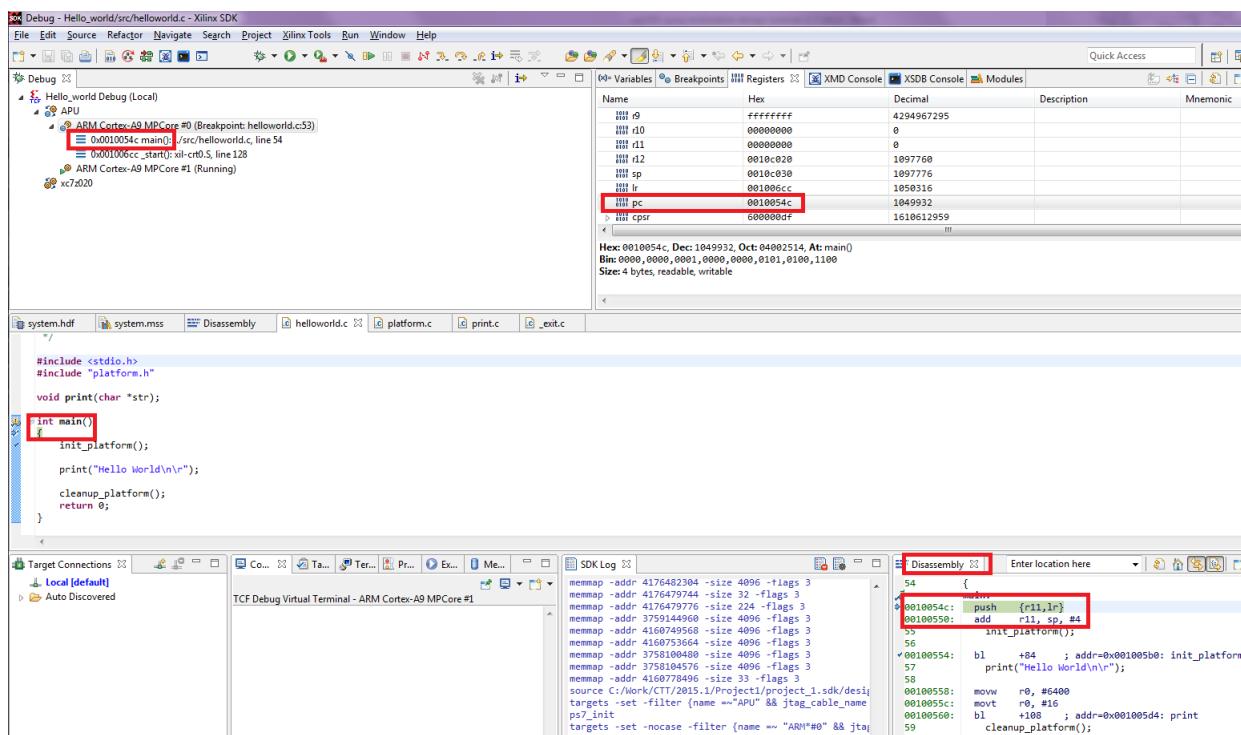


Figure 4-3: Debugging Application Debug Perspective

**Note:** The addresses shown on this page might slightly differ from the addresses shown on your system.

The processor is currently sitting at the beginning of `main()` with program execution suspended at line 0x0010054C. You can confirm this information in the Disassembly view, which shows the assembly-level program execution also suspended at 0x0010054C.

**Note:** If the Disassembly view is not visible, select **Window > Show view > Disassembly**.

2. The `helloworld.c` window also shows execution suspended at the first executable line of C code. Select the Registers view to confirm that the program counter, pc register, contains **0x0010054C**.

**Note:** If the Registers view is not visible, select **Window > Show View > Registers**.

3. Double-click in the margin of the `helloworld.c` window next to the line of code that reads `init_platform ()`. This sets a breakpoint at `init_platform ()`. To confirm the breakpoint, review the Breakpoints window.

**Note:** If the Breakpoints window is not visible, select **Window > Show View > Breakpoints**.

4. Select **Run > Resume** resuming running the program to the breakpoint.

Program execution stops at the line of code that includes `init_platform ()`. The Disassembly and Debug windows both show program execution stopped at `0x00100554`.

**Note:** The execution address in your debugging window might differ if you modified the hello world source code in any way.

5. Select **Run > Step Into** to step into the `init_platform ()` routine.

Program execution suspends at location `0x001005c4`. The call stack is now two levels deep.

6. Select **Run > Resume** running the program to conclusion.

When the program completes, the Debug window shows that the program is suspended in a routine called `exit`. This happens when you are running under control of the debugger.

7. Re-run your code several times. Experiment with single-stepping, examining memory, breakpoints, modifying code, and adding print statements. Try adding and moving views.
8. Close SDK.

# Using the HP Slave Port with AXI CDMA IP

In this chapter, you will instantiate AXI CDMA IP in fabric and integrate it with the processing system high performance (HP) 64-bit slave port. In this system, AXI CDMA acts as master device to copy an array of the data from the source buffer location to the destination buffer location in DDR system memory. The AXI CDMA uses the processing system HP slave port to get read/write access of DDR system memory.

You will write Standalone application software and Linux OS based application software using `mmap()` for the data transfer using AXI CDMA block. You will also execute both standalone and Linux-based application software separately on the ZC702 board.

---

## Integrating AXI CDMA with the Zynq SoC PS HP Slave Port

Xilinx® Zynq®-7000 AP SoC devices internally provide four high performance (HP) AXI slave interface ports that connect the programmable logic (PL) to asynchronous FIFO interface (AFI) blocks in the processing system (PS). The HP Ports enable a high throughput data path between AXI masters in programmable logic and the processing system's memory system (DDR and on-chip memory). HP slave ports are configurable to 64 bit or 32 bit interfaces.

In this section, you'll create a design using AXI CDMA intellectual property (IP) as master in fabric and integrate it with the PS HP 64 bit slave port. The block diagram for the system is as shown in [Figure 5-1, page 48](#).

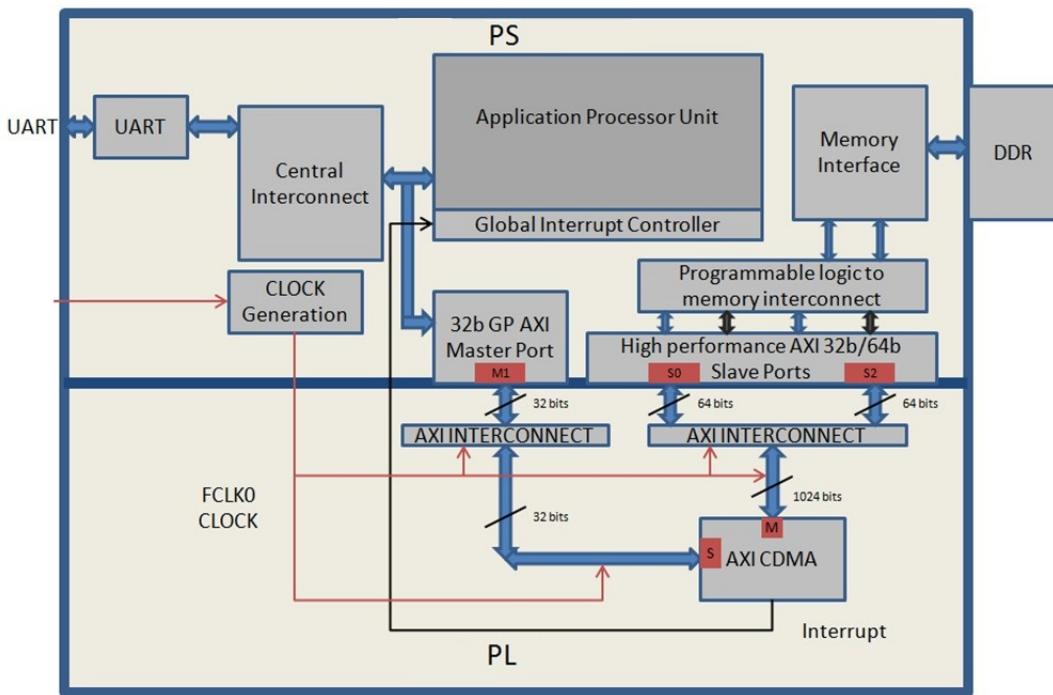


Figure 5-1: Block Diagram

This system covers the following connections:

- AXI CDMA Slave Port is connected to the PS General Purpose master port 1 (`M_AXI_GP1`). It is used by the PS CPU to configure the AXI CDMA register set for the data transfer and also to check the status.
- AXI CDMA Master Port is connected to the PS High performance Slave Port 0 (`S_AXI_HP0`). It is used by the AXI CDMA to read from the DDR system memory. It acts as the source buffer location for the CDMA during data transfer.
- AXI CDMA Master Port is connected to the PS High performance Slave Port 2 (`S_AXI_HP2`). It is used by the AXI CDMA to write the data to the DDR system memory. It acts as a destination buffer location for the CDMA during the Data transfer.
- AXI CDMA interrupt is connected from fabric to the PS section interrupt controller. After Data Transfer or Error during Data transaction, the AXI CDMA interrupt is triggered.

In this system, you will configure the HP slave port 0 to access a DDR memory location range from `0x20000000` to `0x2FFFFFFF`. This DDR system memory location acts as the source buffer location to CDMA for reading the data.

You will also configure HP slave Port 2 to access a DDR memory Location range from `0x30000000` to `0x3FFFFFFF`. This DDR system memory location acts as a destination location to CDMA for writing the data.

You will also configure the AXI CDMA IP data width of the Data Transfer channel to 1024 bits with Maximum Burst length set to 32. With this setting, CDMA Maximum transfer size is set to 1024x32 bits in one transaction.

You will write the application software code for the above system. When you execute the code, it first initializes the source buffer memory with the specified data pattern and also clears the destination buffer memory by writing all zeroes to the memory location. Then, it starts configuring the CDMA register for the DMA transfer. It writes the source buffer location, destination buffer location, and number of bytes to be transferred to the CDMA registers and waits for the CDMA interrupt. When the interrupt occurs, it checks the status of the DMA transfers.

If the data transfer status is successful, it compares the source buffer data with the destination buffer data and displays the comparison result on the serial terminal.

If the data transfer status is an error, it displays the error status on the serial terminal and stops execution.

## Example Project: Integrating AXI CDMA with the PS HP Slave Port

1. Start with one of the following:
  - Use the system you created in Checking the Functionality of the IPs Instantiated in the Fabric.
  - Create a new project as described in [Example Project: Creating a New Embedded Project with Zynq SoC, page 14](#).
2. Open the Vivado design from [Chapter 3](#) called **edt\_tutorial** and from the IP integrator view click **Open Block Design**.
3. In the Diagram window, right-click in the blank space and select **Add IP**.
4. In the search box, type "CDMA" and double-click the **AXI Central Direct Memory Access** IP to add it to the Block Design. The AXI Central Direct Memory Access IP block appears in the Diagram view.
5. In the Diagram window, right-click in the blank space and select **Add IP**.
6. In the search box type **concat** and double-click the **Concat** IP to add it to the Block Design. The Concat IP block appears in the Diagram view. This block will be used to concatenate the two interrupt signals if you are using the prior design with the AXI Timer.
7. Right-click the **interrupt > IRQ\_F2P[0:0]** net and select delete.
8. Click the **IRQ\_F2P[0:0]** port and drag to the **dout[1:0]** output port on the Concat IP core to make a connection between the two ports.

9. Click the **interrupt** port on the AXI Timer IP core and drag to the **In0[0:0]** input port on the Concat IP core to make a connection between the two ports.
10. Click the **cdma\_intout** port on the AXI CDMA IP core and drag to the **In1[0:0]** input port on the Concat IP core to make a connection between the two ports.
11. Right-click the **ZYNQ7 Processing System** core and select **Customize Block**.
12. Select **PS-PL Configuration** and expand the **HP Slave AXI Interface**.
13. Select the check box for **S AXI HP0 interface** and for **S AXI HP2 interface**.
14. Click **OK** to accept the changes.
15. Right-click the **AXI CDMA IP** core and select **Customize Block**.
16. Set the block settings in the Re-customize IP wizard screen as follows:

System Property	Setting or Command to Use
Enable Scatter Gather	Unchecked
Disable 4K Boundary Checks	Unchecked
Allow Unaligned Transfers	Unchecked
Write/Read Data Width	1024
Write/Read Burst Size	32
Enable Asynchronous Mode (Auto)	Unchecked
Address Width	32

17. Click **OK** to accept the changes.
18. Click the **Run Connection Automation** link in the Diagram view to automate the remaining connections.
19. In the Run Connection Automation wizard view make sure the All Automation box is checked, then, click **OK** to accept the default connections. The finished diagram should look like [Figure 5-2, page 51](#).

**Note:** You might receive a Critical Message regarding forcibly mapping a net into a conflicting address. You will address the error by manually updating the memory mapped address in the next steps. Click **OK** if you see the error message.

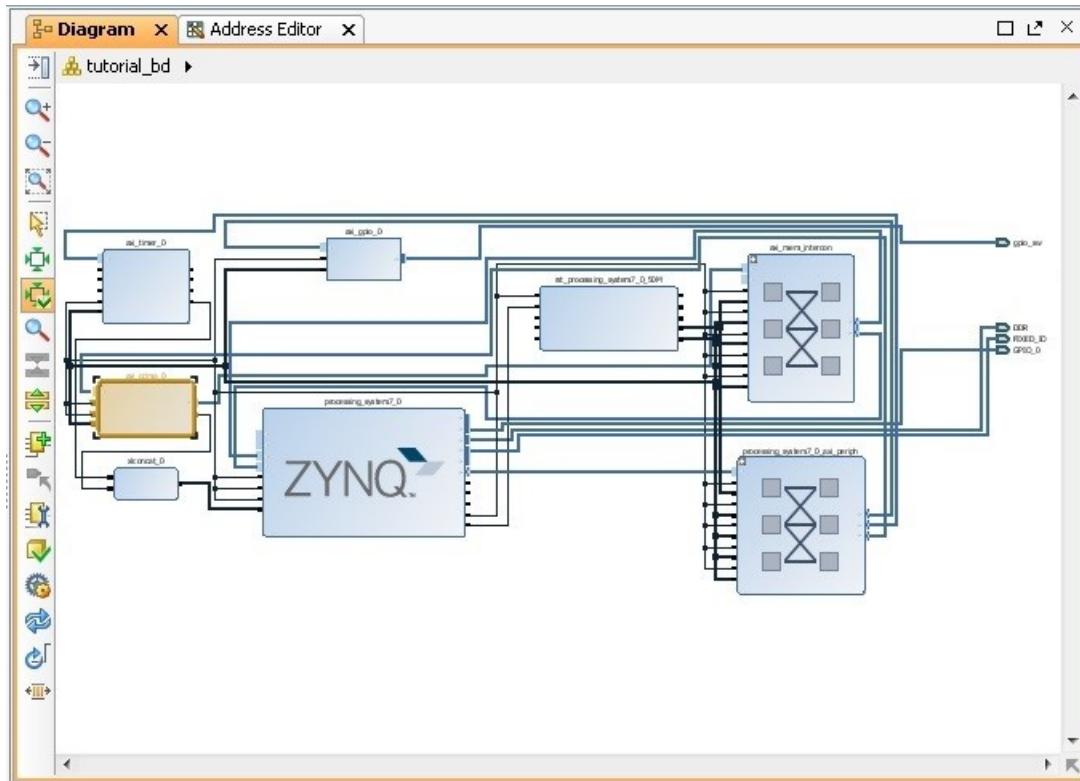


Figure 5-2: Updated Block Diagram

20. Select the **Address Editor** tab.

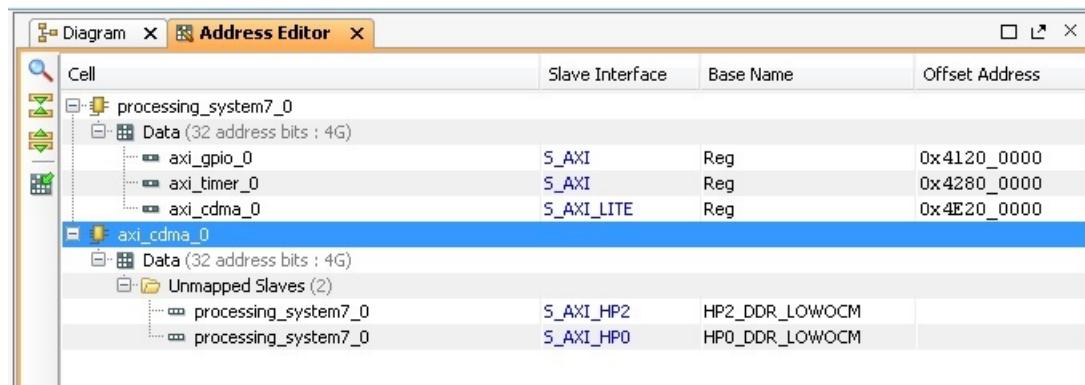


Figure 5-3: Address Editor Tab

21. In the Address Editor view, expand **axi\_cdma\_0 > Data > Unmapped Slaves**.

22. Right-click **HP0\_DDR\_LOWOCM** and select **Assign Address**.

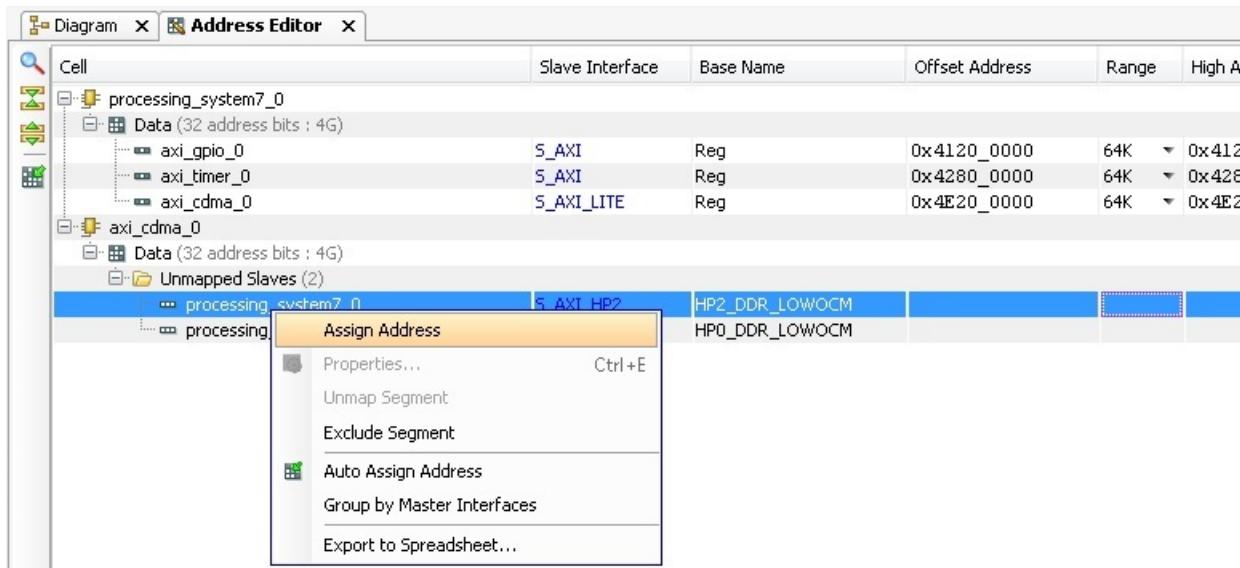


Figure 5-4: Assigning Addresses in the Address Editor

23. In the Range column for **S\_AXI\_HP0**, select **256M**.
24. Under Offset Address for **S\_AXI\_HP0**, set a value of **0x2000\_0000**.
25. In the Address Editor view, expand **axi\_cdma\_0 > Data > Unmapped Slaves**.
26. Right-click **HP2\_DDR\_LOWOCM** and select **Assign Address**.
27. In the Range column for **S\_AXI\_HP2**, select **256M**.
28. Under Offset Address for **S\_AXI\_HP2**, set a value of **0x3000\_0000**.

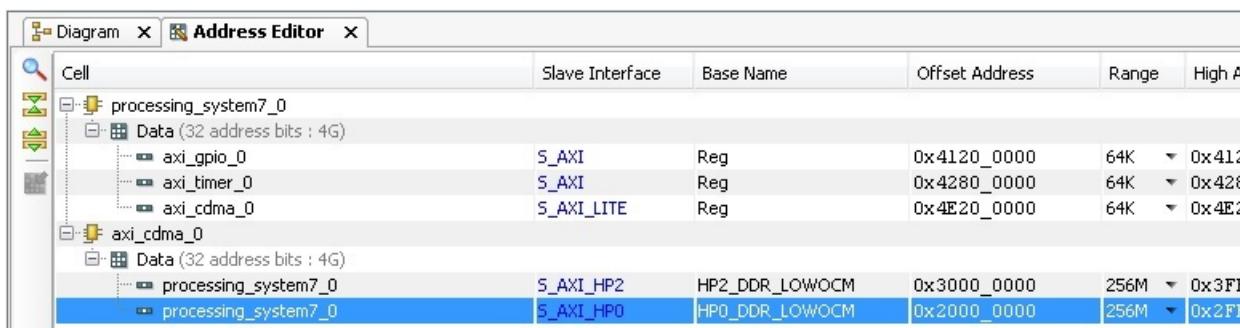


Figure 5-5: Address Changes to processing\_system7\_0

29. Select **Generate Bitstream** in the Program and Debug view.

The Save Project dialog box opens.

30. Ensure that the **Block Design - tutorial\_bd** check box is selected, then click **Save**.
31. A message might appear that states Synthesis is out of date. If it does, click **Yes**.
32. After the Bitstream generation completes, export the hardware and launch the Xilinx Software Development Kit (SDK) as described in [Exporting to SDK, page 23](#).

# Standalone Application Software for the Design

The CDMA-based system that you designed in this chapter requires application software to execute on the board. This section describes the details about the CDMA-based Standalone application software.

The `main()` function in the application software is the entry point for the execution. It initializes the source memory buffer with the specified test pattern and clears the destination memory buffer by writing all zeroes.

The application software then configures the CDMA registers sets by providing information such as source buffer and destination buffer starting locations. To initiate DMA transfer, it writes the number of bytes to be transferred in the CDMA register and waits for the CDMA interrupt to happen. After the interrupt, it checks the status of the DMA transfer and compares the source buffer with the destination buffer. Finally, it prints the comparison result in the serial terminal and stops running.

## Application Software Flow

The application software does the following:

1. Initializes the source buffer with the specified test pattern. The source buffer location ranges from 0x20000000 to 0x2FFFFFFF.

Clears the destination buffer by writing all zeroes into the destination address range. The destination buffer location ranges from 0x30000000 to 0x3FFFFFFF.

2. Initializes AXI CDMA IP and does the following:

- a. Associates a CDMA callback function with AXI CDMA ISR and Enable the Interrupt.

This Callback function executes during the CDMA interrupt. It sets the interrupt Done and/or Error flags depending on the DMA transfer status.

Application software waits for the Callback function to populate these flags and executes the software according to the status flag.

- b. Configures the CDMA in Simple mode.
- c. Checks the Status register of the CDMA IP to verify the CDMA idle status.
- d. Sets the source buffer starting location, 0x20000000, to the CDMA register.
- e. Sets the destination buffer starting location, 0x30000000, to the CDMA register.
- f. Sets the number of bytes to transfer to the CDMA register. The application software starts the DMA transfer.

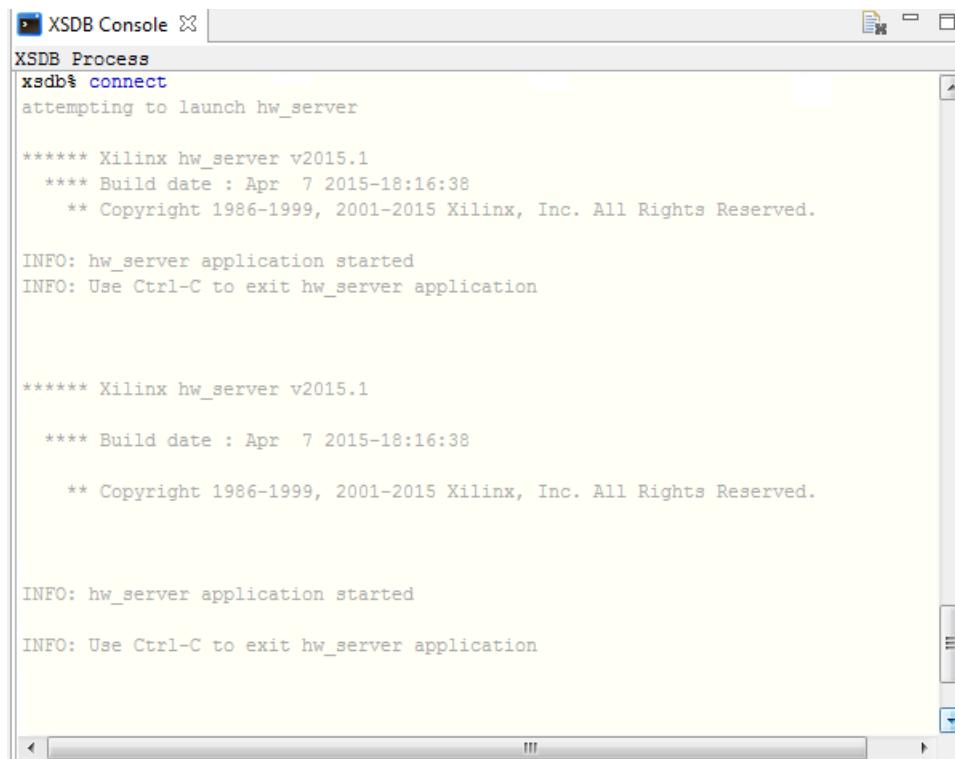
3. After the CDMA interrupt is triggered, checks the DMA transfer status.

If the transfer status is successful, the application software compares the source buffer location with the destination buffer location and displays the comparison result on the serial terminal, and then exits from the execution.

If the transfer status displays an error, the software prints the error status in the serial terminal and stops running.

## Running the Standalone CDMA Application Using SDK

1. Open SDK.
2. Check that the Target Communication Frame (TCF) (`hw_server.exe`) agent is running on your Windows machine. If it is not running, select **Xilinx Tools > XSDB Console**.
3. In the XSDB Console window, type **Connect**. You should see a message that states that the `hw_server` application started.



```

XSDB Console X
XSDB Process
xsadb% connect
attempting to launch hw_server

***** Xilinx hw_server v2015.1
**** Build date : Apr 7 2015-18:16:38
** Copyright 1986-1999, 2001-2015 Xilinx, Inc. All Rights Reserved.

INFO: hw_server application started
INFO: Use Ctrl-C to exit hw_server application

***** Xilinx hw_server v2015.1
**** Build date : Apr 7 2015-18:16:38
** Copyright 1986-1999, 2001-2015 Xilinx, Inc. All Rights Reserved.

INFO: hw_server application started
INFO: Use Ctrl-C to exit hw_server application

```

Figure 5-6: Hardware Server Message in XSDB Process Window

4. In SDK, **Select File > New > Application Project**.

The New Project wizard opens

5. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Application Project	Project Name	cdma_app
	Use Default Locations	Select this option
	Hardware Platform	system_hw_platform
	Processor	PS7_cortexa9_0
	OS Platform	Standalone
	Language	C
	Board Support Package	Select <b>Create New</b> and provide the name of cdma_app_bsp.
Templates	Available Templates	Empty Application

6. Click **Finish**.

The New Project wizard closes and SDK creates the cdma\_app application project and the cdma\_app\_bsp board support package (BSP) project under the project explorer. SDK also automatically compiles the project and generates the BSP.

7. In the Project Explorer tab, expand the **cdma\_app** project, right-click the **src** directory, and select **Import** to open the Import dialog box.
8. Expand **General** in the Import dialog box and select **File System**.
9. Click **Next**.
10. Select **Browse**.
11. In the design files for this guide (see [Design Files for This Tutorial, page 109](#)), navigate to the CDMA folder.
12. Select the CDMA folder, and click **OK**.
13. Add the `cdma_app.c` file and click **Finish**.

SDK automatically builds the application and displays the status in the console window.

**Note:** The Application software file name for the system is `cdma_app.c`. It is available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

14. Open the serial communication utility with baud rate set to **115200**.
- Note:** This is the baud rate that the UART is programmed to on Zynq devices.
15. Make sure that the hardware board is set up and turned on.
- Note:** Refer to [Example Project: Running the "Hello World" Application, page 26](#) for information about setting up the board.
16. Select **Xilinx Tools > Program FPGA** to open the Program FPGA dialog box. The dialog box shows the bitstream path.

17. Click **Program** to download the bitstream and program the PL Fabric.
  18. Run the project similar to the steps in [Example Project: Running the "Hello World" Application, page 26](#).
  19. Check the Status of the CDMA transfer in the Serial terminal. If the transfer is successful, the message "DMA Transfer is Successful" displays. Otherwise, the serial terminal displays an error message.
- 

## Linux OS Based Application Software for the CDMA System

In this section, you will create a Linux-based application software for CDMA using the **mmap()** system call provided by Linux and run it on the hardware to check the functionality of the CDMA IP.

The **mmap()** system call is used to map specified kernel memory area to the User layer, so that you can read or write on it depending on the attribute provided during the memory mapping. Details about the **mmap()** system call is beyond the scope of this guide.



**CAUTION!** *Use of the **mmap()** call might crash the kernel if it accesses, by mistake, some restricted area or shared resources of the kernel.*

---

The **main()** function in the application software is the entry point for the execution. It initializes the source array with the specified test pattern and clears the destination array. Then it copies the source array contents to the DDR memory starting at location **0x20000000** and makes the DMA register setting to initiate DMA transfer to the destination. After the DMA transfer, the application reads the status of the transfer and displays the result on the serial terminal.

### Application Software Creation Steps

Application software creation is composed of the following steps:

1. Initialize the whole source array, which is in the User layer with value **0xA5A5A5A5**.
2. Clear the whole destination buffer, which is in the User layer, by writing all zeroes.
3. Map the kernel memory location starting from **0x20000000** to the User layer with writing permission using **mmap()** system calls.

By doing so, you can write to the specified kernel memory.

4. Copy the source array contents to the mapped kernel memory.
5. Un-map the kernel memory from the User layer.

6. Map the AXI CDMA register memory location to the User layer with reading and writing permission using the `mmap()` system call. Make the following CDMA register settings from the User layer:
  - a. Reset DMA to stop any previous communication.
  - b. Enable interrupt to get the status of the DMA transfer.
  - c. Set the CDMA in simple mode.
  - d. Verify that the CDMA is idle.
  - e. Set the source buffer starting location, `0x20000000`, to the CDMA register.
  - f. Set the destination buffer starting location, `0x30000000`, to the CDMA register.
  - g. Set the number of bytes to be transferred in the CDMA register. Writing to this register starts the DMA transfer.
7. Continuously read the DMA transfer status until the transfer finishes.
8. After CDMA transfer finishes, un-map the CDMA register memory for editing from the User layer using the `mmap()` system call.
9. Map the kernel memory location starting from `0x30000000` to the User layer with reading and writing attributes.
10. Copy the kernel memory contents starting from `0x30000000` to the User layer destination array.
11. Un-map the kernel memory from the User layer.
12. Compare the source array with the destination array.
13. Display the comparison result in the serial terminal. If the comparison is successful, the message "DATA Transfer is Successful" displays. Otherwise, the serial terminal displays an error message.

---

## Running Linux CDMA Application Using SDK

Detailed steps on running Linux on the target board are outlined in [Chapter 6](#). If you are not comfortable running Linux, please run through the [Chapter 6](#) examples prior to running this example. Running a Linux OS based application is composed of the following steps:

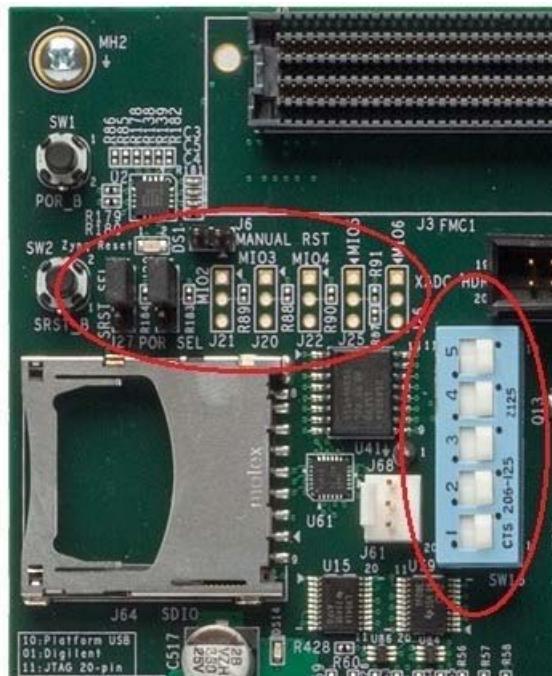
1. Booting Linux on the Target Board.
2. Building an Application and Running it on the Target Board Using SDK.

## Booting Linux on the Target Board

You will now boot Linux on the Zynq-7000 AP SoC ZC702 target board using JTAG mode.

**Note:** Additional boot options will be explained in [Chapter 6](#).

1. Check the following Board Connection and Setting for Linux booting using JTAG mode:
  - a. Ensure that the settings of Jumpers J27 and J28 are set as described in [Example Project: Running the "Hello World" Application, page 26](#).
  - b. Ensure that the SW16 switch is set as shown in [Figure 5-7](#).
  - c. Connect an Ethernet cable from the Zynq SoC board to your network.
  - d. Connect the Windows Host machine to your network.
  - e. Connect the power cable to the board.



*Figure 5-7: Ensure the SW16 Switch Setting*

2. Connect a Digilent cable between the Windows host machine and the target board with the following SW10 switch settings, as shown in [Figure 5-8, page 59](#).
  - Bit-1 is 0
  - Bit-2 is 1

**Note:** 0 = switch is open. 1 = switch is closed. The correct JTAG mode has to be selected, according to the user interface. The JTAG mode is controlled by switch SW10 on the zc702 and SW4 on the zc706.



Figure 5-8: SW4 on a ZC702 Set to use Digilent USB JTAG

3. Connect a USB cable to connector J17 on the target board with the Windows Host machine. This is used for USB to serial transfer.
4. Change Ethernet Jumper J30 and J43 as shown in [Figure 5-9](#).

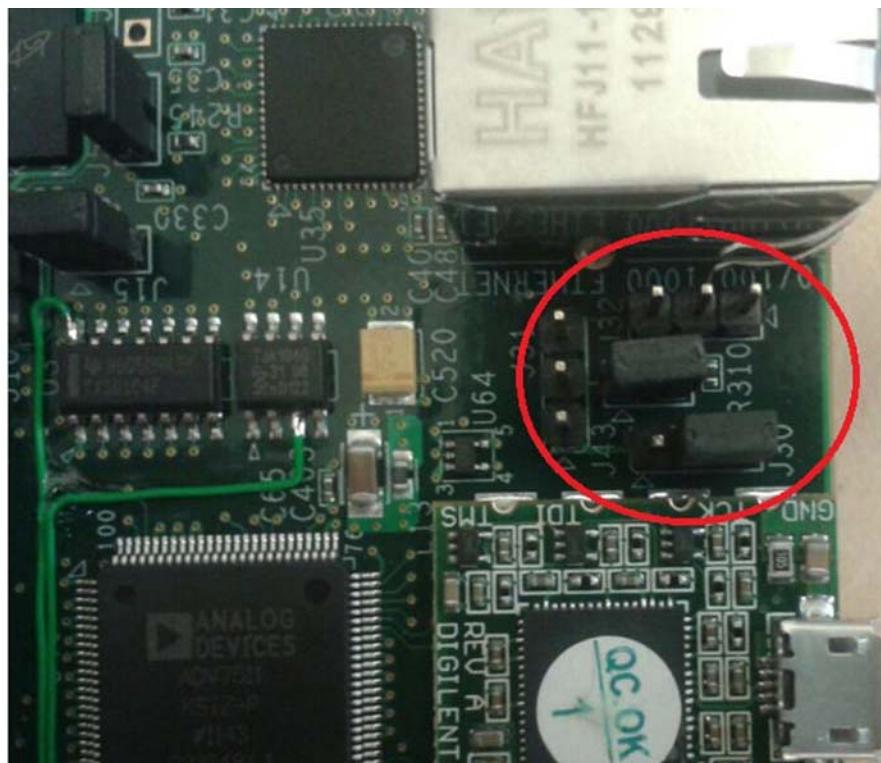


Figure 5-9: Change Jumpers J30 and J43

5. Power on the target board.
  6. Launch SDK and open same workspace you used in [Chapter 2](#) and [Chapter 3](#).
  7. If the serial terminal is not open, connect the serial communication utility with the baud rate set to **115200**.
- Note:** This is the baud rate that the UART is programmed to on Zynq devices.
8. Select **Xilinx Tools > Program FPGA**, then click **Program** to download the bitstream.
  9. Open the Xilinx System Debugger (XSDB) tool by selecting **Xilinx Tools > XSDB console**.
  10. At the XSDB prompt, do the following:
    - a. Type **connect** to connect with the PS section.
    - b. Type **targets** to get the list of target processors.
    - c. Type **ta 2** to select the processor CPU1.

```
xsdb% targets
 1 APU
 2 ARM Cortex-A9 MPCore #0 (Running)
 3 ARM Cortex-A9 MPCore #1 (Running)
 4 xc7z020
xsdb% ta 2
xsdb% targets
 1 APU
 2* ARM Cortex-A9 MPCore #0 (Running)
 3 ARM Cortex-A9 MPCore #1 (Running)
 4 xc7z020
```

- d. Type `source C:/designs/edt_tutorial/edt_tutorial.sdk/tutorial_bd_wrapper_hw_platform_0/ps7_init.tcl` and then type `ps7_init` to initialize the PS section (such as Clock PLL, MIO, and DDR initialization).
- e. Type **ps7\_post\_config** to enable level shifters between PS to PL and to clear fabric port resets.
- f. Type **dow <tutorial\_download\_path>/u-boot.elf** to download PetaLinux U-Boot.elf.
- g. Type **con** to start execution of U-Boot.

On the serial terminal, the autoboot countdown message appears:

Hit any key to stop autoboot: 3

- h. Press **Enter**.

Automatic booting from U-Boot stops and a command prompt appears on the serial terminal.

- i. At the XSDB Prompt, type **stop**.  
The U-Boot execution stops.
  - j. Type **dow -data image.ub 0x30000000** to download the Linux Kernel image at location `0x30000000`.
  - k. Type **con** to start executing U-Boot.
11. At the command prompt of the serial terminal, type **bootm 0x30000000**.  
The Linux OS boots.
12. If required, provide the Zynq login as **root** and the password as **root** on the serial terminal to complete booting the processor.  
After booting completes, # prompt appears on the serial terminal.
13. At the `root@Xilinx-ZC702-2014_4:#` prompt, make sure that the board Ethernet connection is configured:
- a. Check the IP address of the board by typing the following command at the `Zynq>` prompt: **ifconfig eth0**.  
This command displays all the details of the currently active interface. In the message that displays, the `inet addr` value denotes the IP address that is assigned to the Zynq SoC board.
  - b. If `inet addr` and `netmask` values do not exist, you can assign them using the following commands:
  - c. `root@Xilinx-ZC702-2014_4:# ifconfig eth0 inet 192.168.1.1`
  - d. `root@Xilinx-ZC702-2014_4:# ifconfig eth0 netmask 255.255.255.0`
14. Next, confirm that the IP address settings on the Windows machine are set up to match the board settings. Adjust the local area connection properties by opening your network connections.
- a. **Right click** the local area connection that is linked to the XC702 board and select **Properties**.
  - b. With the Local Area Connection properties window open, select **Internet Protocol Version 4 (TCP/IPv4)** from the item list and select **Properties**.
  - c. Select **Use the following IP address** and set the following values:  
IP address: 192.168.1.5  
Subnet mask: 255.255.255.0
  - d. Click **OK** to accept the values and then **close**.

15. In the Windows machine command prompt, check the connection with the board by typing **ping** followed by the board IP address. The ping response displays in a loop.

This response means that the connection between the Windows host machine and the target board is established.

16. Press **Ctrl+C** to stop displaying the ping response on windows host machine command prompt.

Linux booting completes on the target board and the connection between the host machine and the target board is complete.

## Building an Application and Running it on the Target Board Using SDK

1. Now that Linux is running on the board, we will create a linux application to utilize the CDMA. Select **File > New > Application Project**.
2. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Application Project	Project Name	linux_cdma_app
	Hardware Platform	system_hw_platform
	Processor	PS7_cortexa9_0
	OS Platform	Linux
	Language	C
Templates	Available Templates	Linux Empty Application

3. Click **Finish**.

The New Project wizard closes and SDK creates the `linux_cdma_app` project under the project explorer.

4. In the Project Explorer tab, expand `linux_cdma_app` project, right-click the `src` directory, and select **Import** to open the Import dialog box.
5. Expand **General** in the Import dialog box and select **File System**.
6. Click **Next**.
7. Add the `linux_cdma_app.c` file and click **Finish**.

SDK automatically builds the application and generates the `linux_cdma_app.elf` file. Check the console window for the status.

**Note:** The example application software file for the system is `linux_cdma_app.c`. This file is available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

8. Right-click `linux_cdma_app` and select **Run As > Run Configurations** to open the Run Configuration wizard.
9. In the Run Configuration wizard, right-click **Remote ARM Linux Application** and click **New**.
10. In the **Connection** drop-down list, click **New** to open the New Connection wizard.
11. Click the **SSH Only** tab and click **Next**.
12. In the **Host Name** tab, type the target board IP.  

**Note:** To determine the target IP, type `ifconfig eth0` at the **Zynq>** prompt in the serial terminal. The terminal displays the target IP that is assigned to the board.
13. Set the connection name and description in the respective tabs.
14. Click **Finish** to create the connection.
15. In the Run Configuration wizard, under **Remote Absolute File Path for C/C++ Application**, click the **Browse** button. The Select Remote C/C++ Application File wizard opens.
16. Do the Following:
  - a. Expand the root directory. The Enter Password wizard opens.
  - b. Provide the User ID and Password (`root/root`); select the **Save ID** and **Save Password** options.
  - c. Click **OK**.

The window displays the root directory contents because you already established the connection between the Windows host machine and the target board.

  - d. Right-click the "/" in the path name and create a new folder; name it **Apps**.
  - e. Provide an application absolute path, such as `/Apps/linux_cdma_app.elf`.
17. Click **Apply**.
18. Click **Run** to begin running the application.
19. Check the status of the CDMA transfer on the Serial terminal. If the transfer is successful, the message "DMA Transfer is Successful" displays. Otherwise, the serial terminal displays an error message.
20. After you finish debugging the Linux application, close SDK.

# Linux Booting and Debug in SDK

PetaLinux is a full Linux distribution, which includes the Linux OS as well as a complete configuration, build, and deployment environment for Xilinx silicon.

This chapter describes the steps to boot the Linux OS on the Zynq®-7000 AP SoC board with PetaLinux Tools. It also provides information about downloading images precompiled by Linux on the target memory using a JTAG interface.

The later part of this chapter covers programming the following non-volatile memory with the precompiled images, which are used for automatic Linux booting after switching on the board:

- On-board QSPI Flash
- SD card

This chapter also describes using the remote debugging feature in the Xilinx® Software Development Kit (SDK) to debug Linux applications running on the target board. The SDK tool software runs on the Windows host machine. For application debugging, SDK establishes an Ethernet connection to the target board that is already running the Linux OS.

For more information, refer to the Xilinx PetaLinux webpage [\[Ref 8\]](#).

# Requirements

In this chapter, the target platform refers to a Zynq SoC board. The host platform refers to a Windows machine that is running the Vivado® tools and PetaLinux installed on a Linux machine (either physical or virtual).

**Note:** The Das U-Boot universal bootloader is required for the tutorials in this chapter. It is included in the precompiled images that you will download next.

From the Xilinx documentation website, download the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#). It includes the following files:

- `BOOT.bin`: Binary image containing the FSBL and U-Boot images produced by [bootgen](#).
- `cdma_app.c`: Standalone Application software for the system you will create in [Chapter 6](#).
- `helloworld.c`: Standalone Application software for the system you created in [Chapter 3](#).
- `linux_cdma_app`: Linux OS based Application software for the system you will create in [Chapter 6](#).
- `README.txt`: Copyright and release information pertaining to the ZIP file.
- `u-boot.elf`: U-Boot file used to create the `BOOT.BIN` image.
- `Image.ub`: PetaLinux build Image (which have kernel image, ramdisk and dtb)
- `fsbl.elf`: FSBL image used to create `BOOT.BIN` image.

# Booting Linux on a Zynq SoC Board

This section covers the flow for booting Linux on the target board using the precompiled images that you downloaded in [Requirements, page 65](#).

**Note:** The compilations of the different images like Kernel image, U-Boot, Device tree, and root file system is beyond the scope of this guide.

## Boot Methods

The following boot methods are available:

- Master Boot Method
- Slave Boot Method

### ***Master Boot Method***

In the master boot method, different kinds of non-volatile memories such as QSPI, NAND, NOR flash, and SD cards are used to store boot images. In this method, the CPU loads and executes the external boot images from non-volatile memory into the Processor System (PS). The master boot method is further divided into Secure and Non Secure modes. Refer to the *Zynq-7000 Extensible Processing Platform Technical Reference Manual* (UG585) [\[Ref 6\]](#) for more detail.

The boot process is initiated by one of the ARM Cortex-A9 CPUs in the processing system (PS) and it executes on-chip ROM code. The on-chip ROM code is responsible for loading the first stage boot loader (FSBL). The FSBL does the following:

- Configures the FPGA with the hardware bitstream (if it exists)
- Configures the MIO interface
- Initializes the DDR controller
- Initializes the clock PLL
- Loads and executes the Linux U-Boot image from non-volatile memory to DDR

The U-Boot loads and starts the execution of the Kernel image, the root file system, and the device tree from non-volatile RAM to DDR. It finishes booting Linux on the target platform.

## **Slave Boot Method**

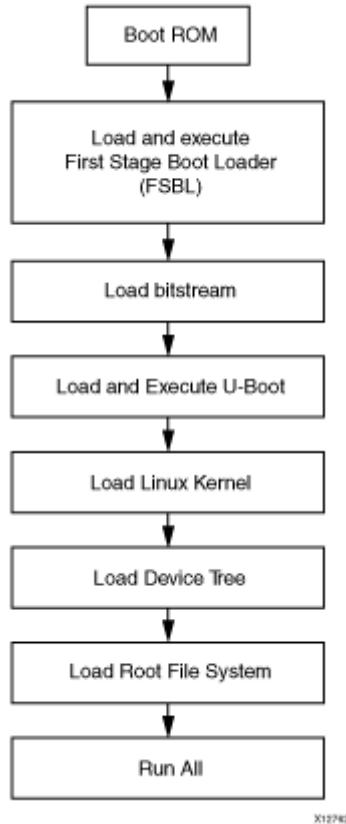
JTAG can only be used in slave boot mode. An external host computer acts as the master to load the boot image into the OCM using a JTAG connection.

Note: The PS CPU remains in idle mode while the boot image loads. The slave boot method is always a non-secure mode of booting.

In JTAG boot mode, the CPU enters halt mode immediately after it disables access to all security related items and enables the JTAG port. You must download the boot images into the DDR memory before restarting the CPU for execution.

## **Booting Linux from JTAG**

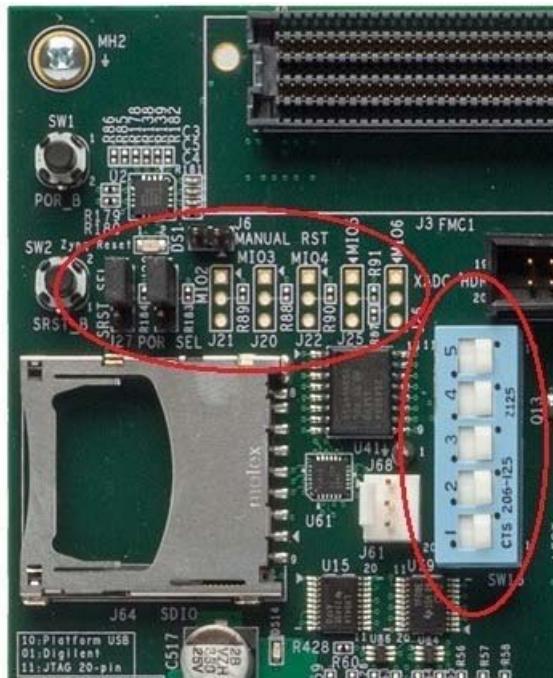
The flow chart in [Figure 6-1](#) describes the process used to boot Linux on the target platform.



*Figure 6-1: Linux Boot Process on the Target Platform*

## Booting Linux Using JTAG Mode

1. Check the following Board Connection and Setting for Linux booting using JTAG mode:
  - a. Ensure that the settings of Jumpers J27 and J28 are set as described in [Example Project: Running the "Hello World" Application, page 26](#).
  - b. Ensure that the SW16 switch is set as shown in [Figure 6-2](#).
  - c. Connect an Ethernet cable from the Zynq®-7000 All Programmable SoC board to your network.
  - d. Connect the Windows Host machine to your network.
  - e. Connect the power cable to the board.



*Figure 6-2: Ensure the SW16 Switch Setting*

2. Connect a Digilent cable between the Windows host machine and the target board with the following SW10 switch settings, as shown in [Figure 6-3, page 69](#).
  - Bit-1 is 0
  - Bit-2 is 1

**Note:** 0 = switch is open. 1 = switch is closed. The correct JTAG mode has to be selected, according to the user interface. The JTAG mode is controlled by switch SW10 on the zc702 and SW4 on the zc706.

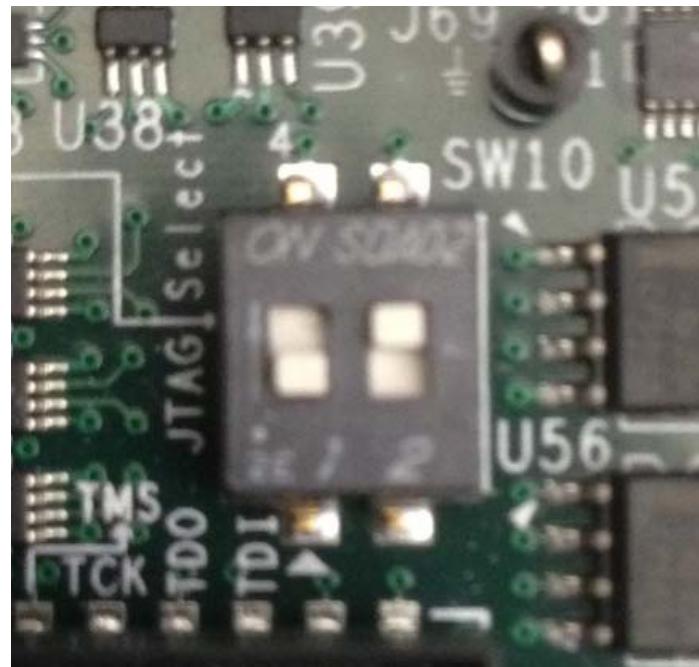


Figure 6-3: SW4 on a ZC706 Set to use Digilent USB JTAG

3. Connect a USB cable to connector J17 on the target board with the Windows Host machine. This is used for USB to serial transfer.
4. Change Ethernet Jumper J30 and J43 as shown in Figure 6-4.

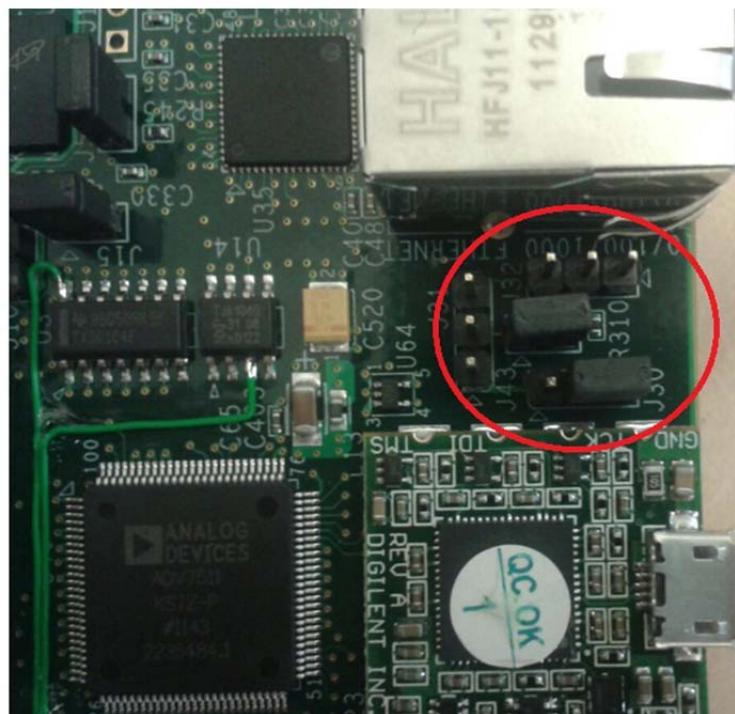


Figure 6-4: Change Jumpers J30 and J43

5. Power on the target board.
  6. Launch SDK and open same workspace you used in [Chapter 2](#) and [Chapter 3](#).
  7. If the serial terminal is not open, connect the serial communication utility with the baud rate set to **115200**.
- Note:** This is the baud rate that the UART is programmed to on Zynq devices.
8. Download the bitstream by selecting **Xilinx Tools > Program FPGA**, then clicking **Program**.
  9. Open the Xilinx System Debugger (XSDB) tool by selecting **Xilinx Tools > XSDB console**.
  10. At the XSDB prompt, do the following:
    - a. Type **connect** to connect with the PS section.
    - b. Type **targets** to get the list of target processors.
    - c. Type **ta 2** to select the processor CPU1.

```
xsdb% targets
 1 APU
 2 ARM Cortex-A9 MPCore #0 (Running)
 3 ARM Cortex-A9 MPCore #1 (Running)
 4 xc7z020
xsdb% ta 2
xsdb% targets
 1 APU
 2* ARM Cortex-A9 MPCore #0 (Running)
 3 ARM Cortex-A9 MPCore #1 (Running)
 4 xc7z020
```

- d. Type **source C:/designs/edt\_tutorial/edt\_tutorial.sdk/tutorial\_bd\_wrapper\_hw\_platform\_0/ps7\_init.tcl** and then type **ps7\_init** to initialize the PS section (such as Clock PLL, MIO, and DDR initialization).
- e. Type **ps7\_post\_config** to enable level shifters between PS to programmable logic (PL) and to clear fabric port resets.
- f. Type **dow <tutorial\_download\_path>/u-boot.elf** to download PetaLinux U-Boot.elf.
- g. Type **con** to start execution of U-Boot.

On the serial terminal, the autoboot countdown message appears:

Hit any key to stop autoboot: 3

- h. Press **Enter**.

Automatic booting from U-Boot stops and a command prompt appears on the serial terminal.

- i. At the XSDB Prompt, type **stop**.  
The U-Boot execution stops.
  - j. Type **dow -data image.ub 0x30000000** to download the Linux Kernel image at location 0x30000000.
  - k. Type **con** to start executing U-Boot.
11. At the command prompt of the serial terminal, type **bootm 0x30000000**.
- The Linux OS boots.
12. If required, provide the Zynq login as **root** and the password as **root** on the serial terminal to complete booting the processor.  
After booting completes, # prompt appears on the serial terminal.
13. At the `root@Xilinx-ZC702-2014_4:#` prompt, make sure that the board Ethernet connection is configured:
- a. Check the IP address of the board by typing the following command at the `Zynq>` prompt: **ifconfig eth0**.  
This command displays all the details of the currently active interface. In the message that displays, the `inet addr` value denotes the IP address that is assigned to the Zynq SoC board.
  - b. If `inet addr` and `netmask` values do not exist, you can assign them using the following commands:  

```
root@Xilinx-ZC702-2014_4:# ifconfig eth0 inet 192.168.1.1
root@Xilinx-ZC702-2014_4:# ifconfig eth0 netmask 255.255.255.0
```
14. Next, confirm that the IP address settings on the Windows machine are set up to match the board settings. Adjust the local area connection properties by opening your network connections.
- a. Right click the local area connection that is linked to the XC702 board and select **Properties**.
  - b. With the Local Area Connection properties window open, select **Internet Protocol Version 4 (TCP/IPv4)** from the item list and select **Properties**.
  - c. Select **Use the following IP address** and set the following values:  
 IP address: 192.168.1.5  
 Subnet mask: 255.255.255.0
  - d. Click **OK** to accept the values and close the window.

15. In the Windows machine command prompt, check the connection with the board by typing **ping** followed by the board IP address. The ping response displays in a loop.

This response means that the connection between the Windows host machine and the target board is established.

16. Press **Ctrl+C** to stop displaying the ping response on windows host machine command prompt.

Linux booting completes on the target board and the connection between the host machine and the target board is complete. The next Example Design describes using SDK to debug the Linux application.

## Example Design: Debugging the Linux Application Using SDK Remote Debugging

In this section, you will create an SDK default Linux hello world application and practice the steps for debugging the Linux application from the Windows host machine.

1. Open SDK.
2. Select **File > New > Application Project**.

The New Project wizard opens.

3. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Application Project	Project Name	linux_hello_world
	Use Default Location	Select this option
	Hardware Platform	system_hw_platform
	Processor	PS7_cortexa9_0
	OS Platform	Linux
	Language	C
Templates	Available Templates	Linux Hello World

4. Click **Finish**.

The New Project wizard closes and SDK creates the `linux_hello_world` project under the project explorer. SDK also automatically compiles the project and generates the file `linux_hello_world.elf`.

5. Right-click **linux\_hello\_world** and select **Debug as > Debug Configurations**.

The Debug Configuration wizard opens.

6. In the Debug Configuration wizard, right-click **Remote ARM Linux Application** and click **New**.

7. In the Connection drop-down list, click **New**.

The New Connection wizard opens

8. Click the **SSH Only** tab and click **Next**.

9. In the Host Name tab, type the target board IP.

**Note:** To determine the target IP, type **ifconfig eth0** at the **Zynq>** prompt in the serial terminal. The terminal displays the target IP that is assigned to the board.

10. Set the connection name and description in the respective tabs.

11. Click **Finish** to create the connection.

12. In the Debug Configuration wizard, under **Remote Absolute File Path for C/C++ Application**, click the **Browse** button. The Select Remote C/C++ Application File wizard opens.

13. In the wizard, do the following:

a. Expand the root directory to open the Enter Password wizard.

b. Provide the user ID and Password (root/root); select the **Save ID** and **Save Password** options.

c. Click **OK**.

**Note:** If a warning message appears, you can safely close it by clicking **YES**.

The window displays the root directory contents because you previously established the connection between the Windows host machine and the target board.

d. Right-click on the "/" in the path name and create a new folder; name it **Apps**.

e. Under "Remote Absolute File Path for C/C++ Application," type the path as `/Apps/linux_hello_world.elf`.

14. Click **Apply**.

15. Click **Debug**.

The Debug Perspective opens.

16. Follow the debugging procedure outlined in [Debugging with Software Using SDK, page 44](#).

**Note:** The Linux application output displays in the SDK console, not the Terminal window used for running Linux.

17. After you finish debugging the Linux application, close SDK.

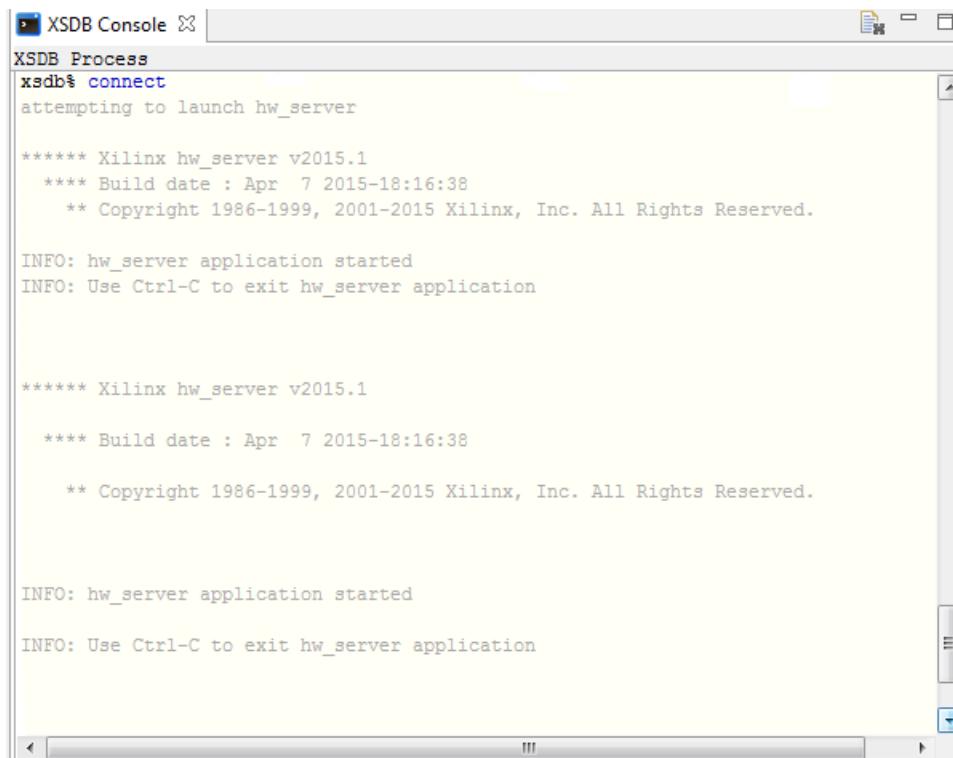
## Example Project: Booting Linux from QSPI Flash

This Example Project covers the following steps:

1. Create the First Stage Boot Loader Executable File.
2. Make a Linux Bootable Image for QSPI Flash.
3. Program QSPI Flash with the Boot Image Using JTAG and U-Boot Command.
4. Booting Linux from QSPI Flash.

### ***Create the First Stage Boot Loader Executable File***

1. Open SDK.
2. Check that the Target Communication Frame (TCF) (`hw_server.exe`) agent is running on your Windows machine. If it is not running, in SDK, Select **Xilinx Tools > XSDB Console**.
3. In the XSDB Console window, type **Connect**. You should see a message that states that the `hw_server` application started.



```

XSDB Console
XSDB Process
xsdb$ connect
attempting to launch hw_server

***** Xilinx hw_server v2015.1
**** Build date : Apr 7 2015-18:16:38
** Copyright 1986-1999, 2001-2015 Xilinx, Inc. All Rights Reserved.

INFO: hw_server application started
INFO: Use Ctrl-C to exit hw_server application


***** Xilinx hw_server v2015.1
**** Build date : Apr 7 2015-18:16:38
** Copyright 1986-1999, 2001-2015 Xilinx, Inc. All Rights Reserved.

INFO: hw_server application started
INFO: Use Ctrl-C to exit hw_server application

```

*Figure 6-5: XSDB Console: `hw_server` Application Started Message*

4. In SDK, select **File > New > Application Project**.

The New Project wizard opens.

5. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Application Project	Project Name	fsbl
	Use Default Location	Select this option
	Hardware Platform	system_hw_platform
	Processor	PS7_cortexa9_0
	OS Platform	Standalone
	Language	C
	Board Support Package	Select <b>Create New</b> and provide the name of fsbl_bsp.
Templates	Available Templates	Zynq FSBL

6. Click **Finish**.

The New Project wizard closes. SDK creates the fsbl application project and the fsbl\_bsp board support package (BSP) project under the project explorer. SDK also automatically compiles the project and generates the fsbl.elf file.

### ***Make a Linux Bootable Image for QSPI Flash***

1. In SDK, select **Xilinx Tools > Create Zynq Boot Image**.

The Create Zynq Boot Image wizard opens.

2. Provide the fsbl.elf path in the **FSBL ELF** tab.

**Note:** You can find fsbl.elf in  
 <project dir>/project/project.sdk/SDK/SDK\_Export/fsbl/Debug.  
 Alternately, you can use fsbl.elf from the file you downloaded in [Requirements, page 65](#).

**Note:** Files u-boot.elf, uImage.bin, devicetree.dtb, and uramdisk.image.gz are available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

3. Add the bitstream file, if any.
4. Add the U-Boot image, u-boot.elf.
5. Add the PetaLinux output image, uImage.bin, and provide the offset **0x520000**.  
 (image.ub: PetaLinux image consists of kernel image, device tree blob and minimal rootfs)

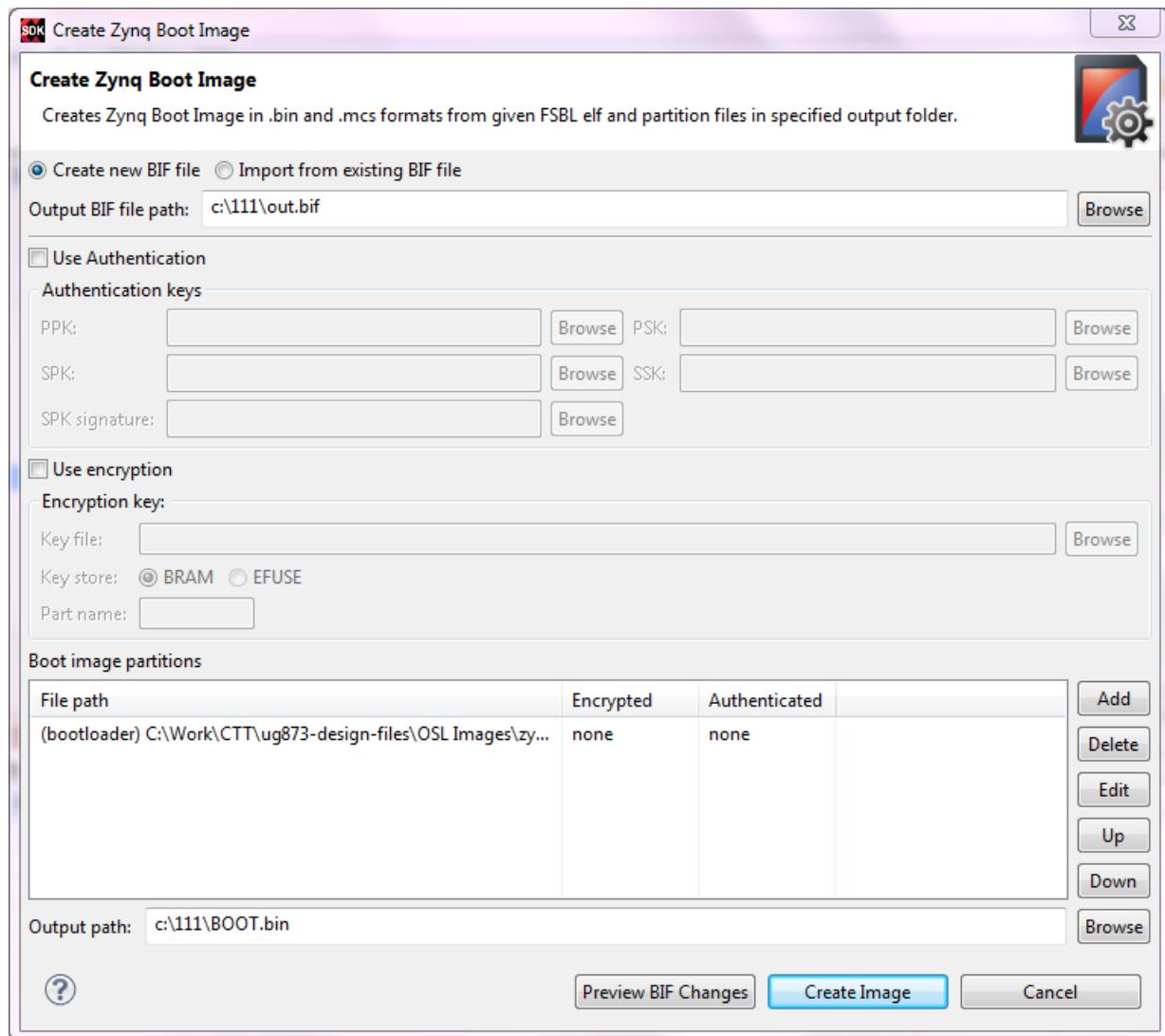



---

**IMPORTANT:** There is a Known Issue with the Bootgen command: it does not accept a file without a file extension. To work around this issue, change the downloaded ulmage file to uImage.bin.

---

6. Provide the output folder name in the **Output Folder** tab.



**Figure 6-6: Creating a Zynq Device Boot Image**

7. Click **Create Image**.

The Create Zynq Boot Image window creates following files in the specified output folder:

BOOT.bin

**Note:** If the BOOT.bin file is not found in the specified folder, run the above steps again. Instead of creating a new BIF file, import the existing one that was created the first time through.

## ***Program QSPI Flash with the Boot Image Using JTAG and U-Boot Command***

You can program QSPI Flash with the boot image using JTAG and the U-Boot command.

1. Power on the ZC702 Board.
2. If a serial terminal is not open, connect the serial terminal with the baud rate set to **115200**.

**Note:** This is the baud rate that the UART is programmed to on Zynq devices.

3. Select **Xilinx Tools > XSDB Console** to open the XSDB tool.
4. From the XSDB prompt, do the following:
  - a. Type **connect** to connect with the PS section.
  - b. Type **targets** to get the list of target processors.
  - c. Type **ta 2** to select the processor CPU1.
  - d. Type **source <Project Dir>/project\_1/project\_1.sdk/SDK/SDK\_Export/system\_hw\_platform/ps7\_init.tcl** and then type **ps7\_init** to initialize the PS section.
  - e. Type **ps7\_post\_config** to enable level shifters between PS to PL and clear fabric port resets.
  - f. Type **dow u-boot.elf** to download the Linux U-Boot to the QSPI Flash.
  - g. Type **dow -data BOOT.bin 0x08000000** to download the Linux bootable image to the target memory at location **0x08000000**.

**Note:** You just downloaded the binary executable to DDR memory. You can download the binary executable to any address in DDR memory.

- h. Type **con** to start execution of U-Boot.

U-Boot begins booting. On the serial terminal, the autoboot countdown message appears:

```
Hit any key to stop autoboot: 3
```

5. Press **Enter**.

Automatic booting from U-Boot stops and the U-Boot command prompt appears on the serial terminal.

6. Do the following steps to program U-Boot with the bootable image:
  - a. At the prompt, type **sf probe 0 0 0** to select the QSPI Flash.
  - b. Type **sf erase 0 0x01000000** to erase the Flash data.

This command completely erases 16 MB of on-board QSPI Flash memory.

- c. Type **sf write 0x08000000 0xFFFFFFF** to write the boot image on the QSPI Flash.

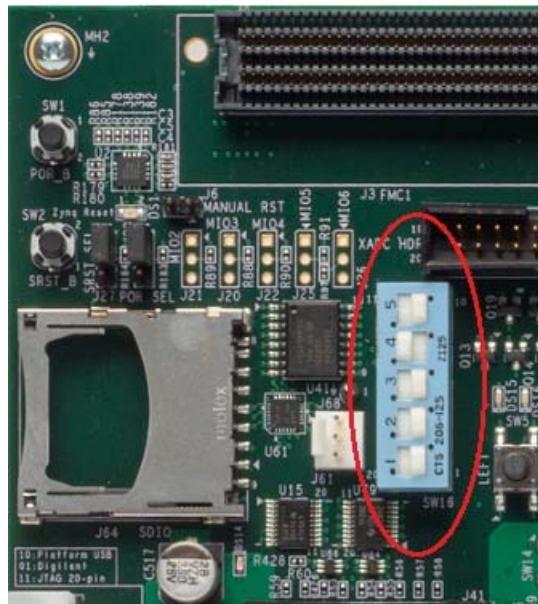
Note that you already copied the bootable image at DDR location 0x08000000. This command copied the data, of the size equivalent to the bootable image size, from DDR to QSPI location 0x0.

For this example, because you have 16 MB of Flash memory, you copied 16 MB of data. You can change the argument to adjust the bootable image size.

7. Power off the board.

### **Booting Linux from QSPI Flash**

1. After you program the QSPI Flash, set the SW16 switch on your board as shown in [Figure 6-7](#).



*Figure 6-7: Jumper Settings for Booting Linux from QSPI Flash*

2. Connect the Serial terminal using an **115200** baud rate setting.

**Note:** This is the baud rate that the UART is programmed to on Zynq devices.

3. Switch on the board power.

A Linux booting message appears on the serial terminal. After booting finishes, the `root@Xilinx-ZC702-2014_4: #` prompt appears.

4. Check the Board IP address connectivity as described in [Booting Linux Using JTAG Mode, page 68](#).

For Linux Application creation and debugging, refer to [Example Design: Debugging the Linux Application Using SDK Remote Debugging, page 72](#).

### Booting Linux from the SD Card

1. Change the SW16 switch setting as shown in [Figure 6-8](#).



*Figure 6-8: Jumper Settings for Booting Linux from SD Card*

2. Make the board settings as described in [Booting Linux Using JTAG Mode](#), page 68.
3. Create a first stage bootloader (FSBL) for your design as described in [Create the First Stage Boot Loader Executable File](#), page 74.

**Note:** If you do not need to change the default FSBL image, you can use the `fsbl.elf` file that you downloaded as part of the ZIP file for this guide. See [Design Files for This Tutorial](#), page 109.

4. In SDK, select **Xilinx Tools > Create Boot Image** to open the Create Zynq Boot Image wizard.
5. Add `fsbl.elf`, bit file (if any), and `u-boot.elf`.
6. Provide the output folder path in the Output folder field.

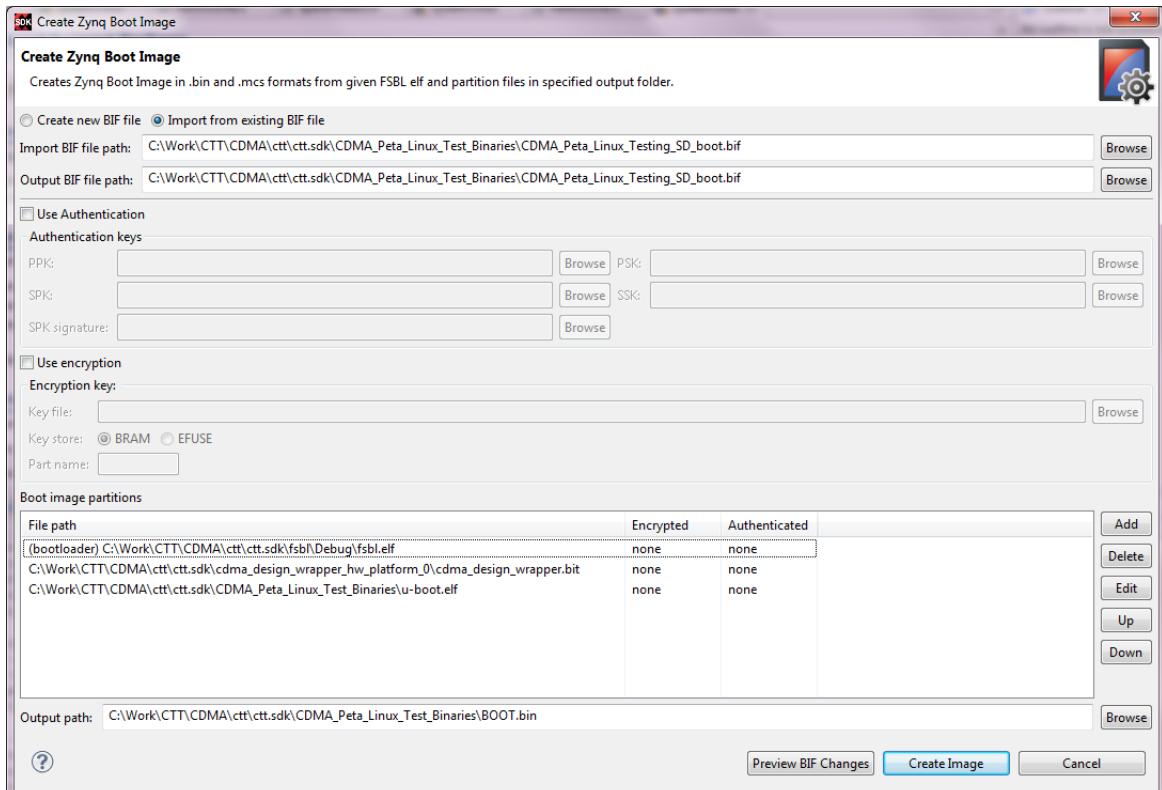


Figure 6-9: Creating the Zynq Device Boot Image

7. Click **Create Image**. SDK generates the **BOOT.bin** file in the specified folder.
8. Copy **BOOT.bin** and **image.ub** to the SD card.




---

**IMPORTANT:** Do not change the file names. U-Boot searches for these file names in the SD card while booting the system.

---

9. Turn on the power to the board and check the messages on the Serial terminal. The **Zynq>** prompt appears after Linux booting is complete on the target board.
10. Set the board IP address and check the connectivity as described in [Booting Linux Using JTAG Mode, page 68](#).

For Linux application creation and debugging, see [Example Design: Debugging the Linux Application Using SDK Remote Debugging, page 72](#).

# Software Profiling Using SDK

In this chapter, you will enable profiling features for the Standalone board support package (BSP) and the Application related to AXI CDMA, which you created in [Chapter 6](#).

---

## Profiling an Application in SDK with System Debugger

Profiling is a method by which the software execution time of each routine is determined. You can use this information to determine critical pieces of code and optimal code placement in a design. Routines that are frequently called are best suited for placement in fast memories, such as cache memory. You can also use profiling information to determine whether a piece of code can be placed in hardware, thereby improving overall performance.

You can use the system debugger in the Xilinx® Software Development Kit (SDK) to profile your application.

1. Select the application you want to profile.
2. Select **Run > Debug As > Launch on Hardware (System Debugger)**.
3. When the application stops at main, open the Target Communication Frame (TCF) profiler view by selecting **Window > Show View > Other > Debug > TCF Profiler**.

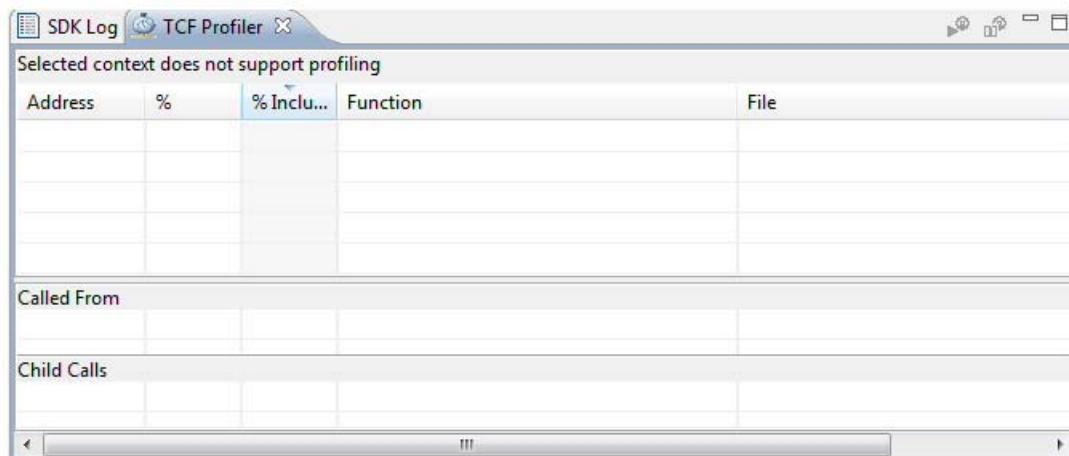


Figure 7-1: TCF Profiler View

4. Click the **Start**  button to begin profiling. Alternately, you can select the **Aggregate Per Function** option in the Profiler Configuration dialog box.

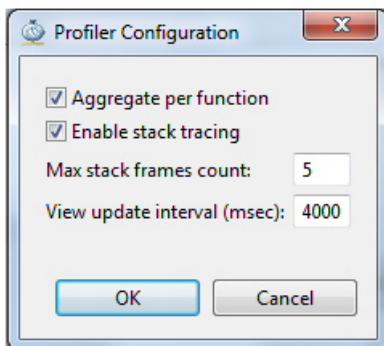


Figure 7-2: Profiler Configuration Dialog Box

5. Click the **Resume** button  to continue running the application.

You can wait for the application to complete, or you can stop the application by selecting the stop button in order to view the profile data in the TCF Profiler tab.

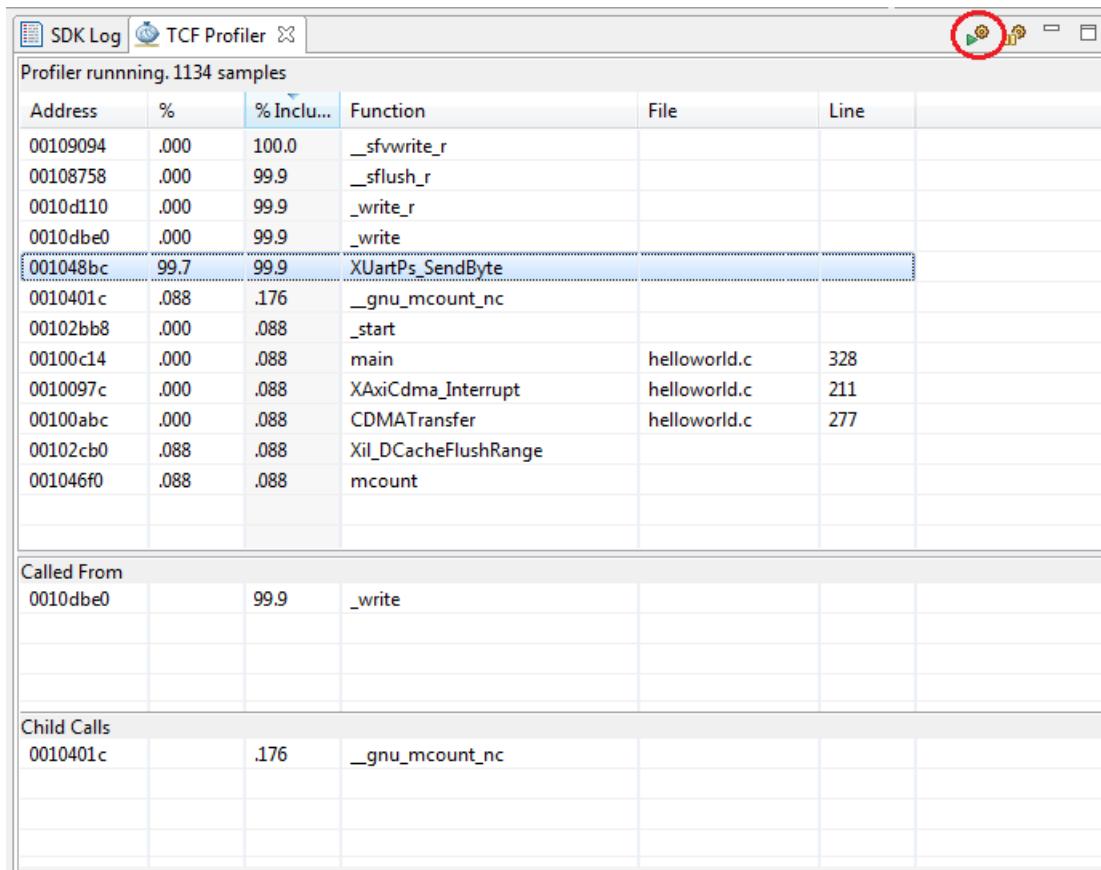


Figure 7-3: TCF Profiler Tab

## Application Software Profiling Using SDK

1. Launch SDK and open the same workspace you used in [Chapter 2](#) and [Chapter 3](#).
2. If the serial terminal is not open, connect the serial communication utility with the baud rate set to **115200**.

**Note:** This is the baud rate that the UART is programmed to on Zynq devices.

3. In SDK, select **File > New > Application Project**.

The New Project wizard opens.

4. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Application Project	Project Name	cdma_app_profile
	Use Default Location	Select this option
	Hardware Platform	system_hw_platform
	Processor	PS7_cortexa9_0
	OS Platform	Standalone
	Language	C
	Board Support Package	Select <b>Create New</b> and provide the name of cdma_app_profile_bsp
Templates	Available Templates	Empty Application

5. Click **Finish**.

The New Project wizard closes and SDK creates the `cdma_app` application project and the `cdma_app_bsp` BSP project under the project explorer. SDK also automatically generates the BSP.

6. In the Project Explorer tab, expand **cdma\_app\_profile** project, right-click the `src` directory, and select **Import** to open the Import dialog box.
7. Expand **General** in the Import dialog box and select **File System**.
8. Click **Next**.
9. Add `cdma_app.c` file and click **Finish**.

SDK automatically builds the application and displays the status in the console window.

**Note:** The Application software file name for the system is `cdma_app.c`. This file is available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

10. In the Project Explorer tab, right-click **cdma\_app\_profile\_bsp** and select **Board Support Package Settings** to open the Board Support Package Settings dialog box.

11. In the Board Support Package Settings dialog box, select **standalone** in the left navigation pane. Select the **enable\_sw\_intrusive\_profiling** option in the list and set its value to **true**.

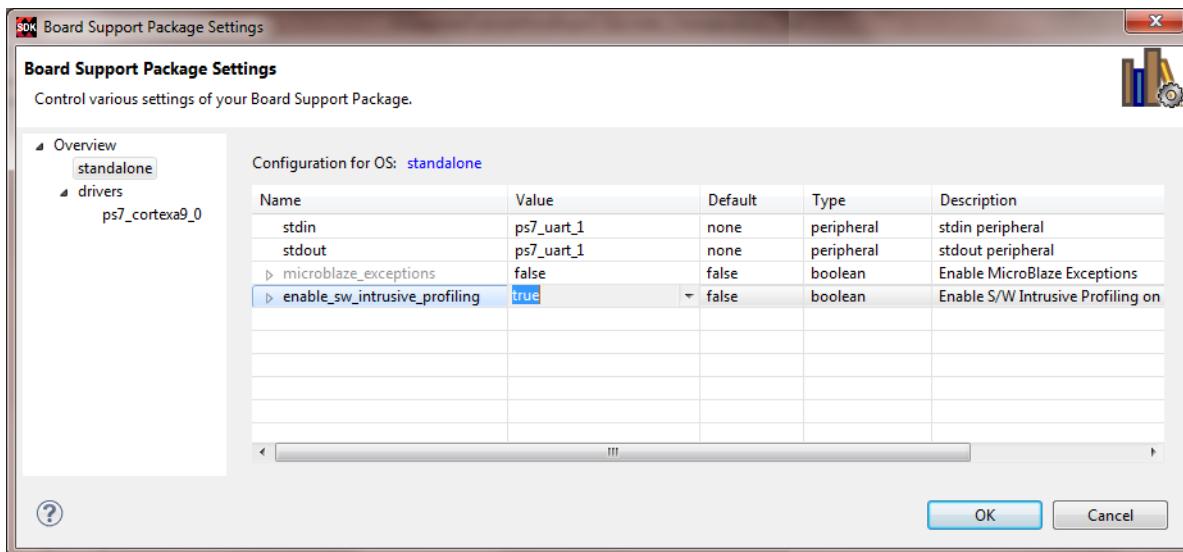


Figure 7-4: BSP Settings Standalone Configuration

This enables software intrusive profiling. It is considered intrusive because extra code is added to your code to make it work.

12. In the left navigation pane of the Board Support Package Settings dialog box, under drivers, select **cpu\_cortexa9**. In the **extra\_compiler\_flags** setting, type the value **-pg** as shown below.

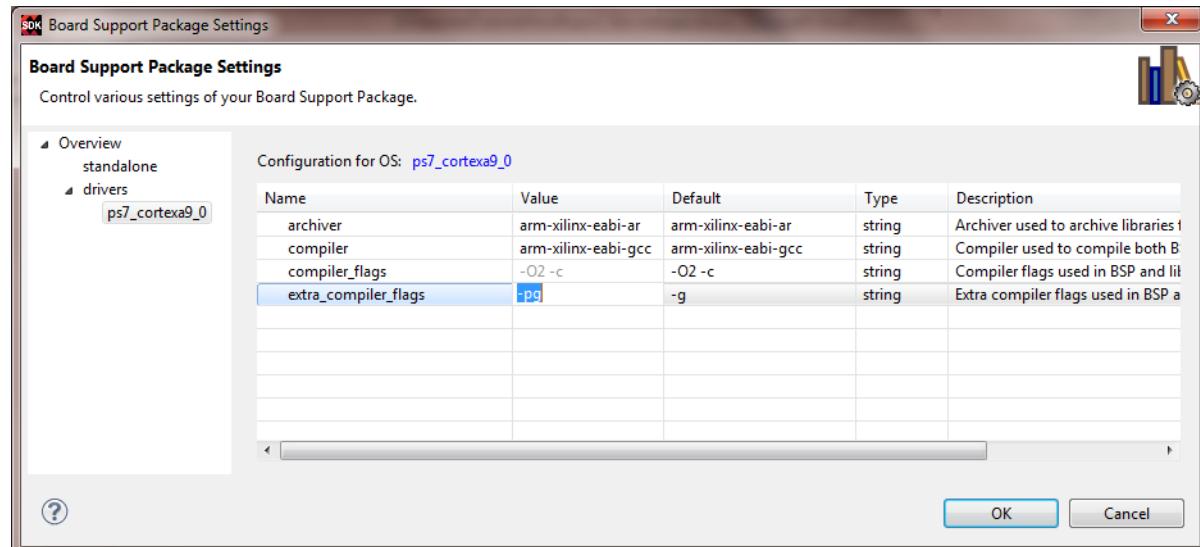


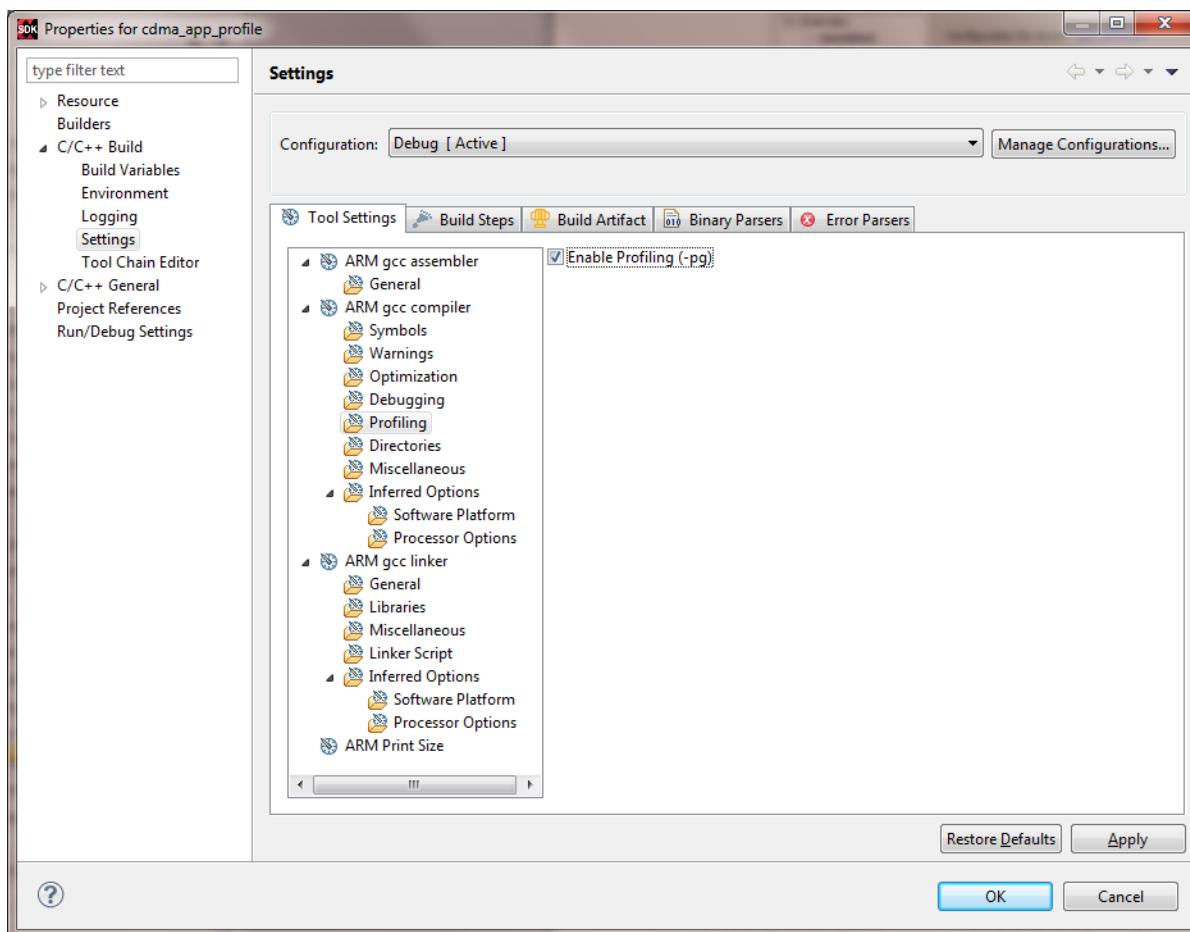
Figure 7-5: BSP Settings cpu\_cortexa9 Settings

13. Click **OK**.

SDK starts building BSP again with the new profiling options.

14. In the Project Explorer tab, right-click **cdma\_app\_profile** and select the **C/C++ Build** setting to open the Properties dialog box.

15. In the Properties dialog box, click the **Tool Settings** tab. Expand **ARM gcc compiler**, select **Profiling**, and select the **Enable Profiling (-pg)** option.



*Figure 7-6: Properties Dialog Box, Tool Settings Tab*

16. Select **Optimization** in the properties list and set the optimization level to **None (-O0)**.

17. Select **Debugging** in the properties list and set the debug level to **Default (-g)**.

18. Click **OK**.

SDK rebuilds the application again and generates the `cdma_app_profile.elf` file. Check the console window for the status.

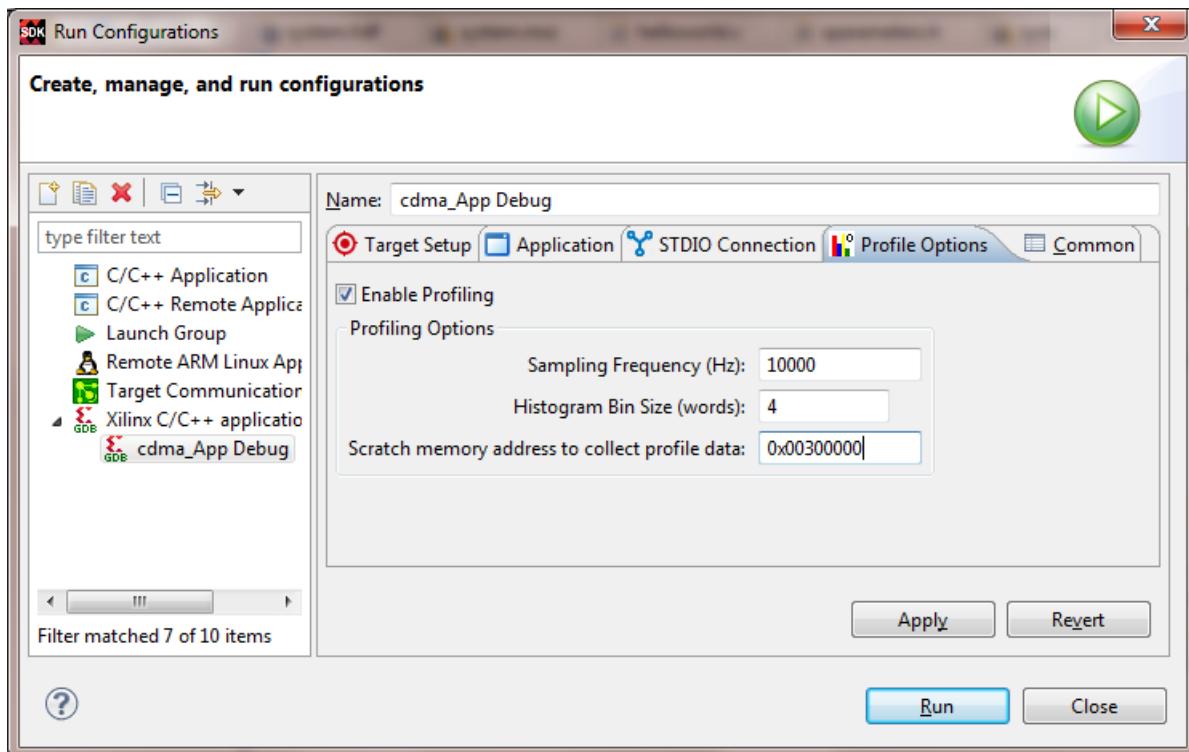
## Running the Application with the Profiling Option

1. Make sure that the hardware board is set up and turned on, as described in [Example Project: Running the "Hello World" Application, page 26](#).
2. In SDK, select **Xilinx Tools > Program FPGA** to open the Program FPGA dialog box, which shows the bitstream path.
3. Click **Program** to download the bitstream and program the programmable logic (PL) Fabric.
4. In the Project Explorer tab, right-click the **cdma\_app\_profile** project and select **Run As > Run Configurations** to open the **Run Configuration** dialog box.
5. In the Run Configuration dialog box, double-click **Xilinx C/C++ application (GDB)** to create a new **Configuration**.
6. Open the **Profile Options** tab and set the following parameters, as shown in [Figure 7-7, page 87](#):
  - a. Click to select the **Enable Profiling** check box.
  - b. Set the Sampling Frequency (Hz) to 10000.

The sampling frequency is the interrupt interval that the profiling routine uses to periodically check which function is currently being executed. The routine performs the sampling by examining the program counter at each interrupt.
  - c. Set the Histogram Bin Size (Words) to 4.

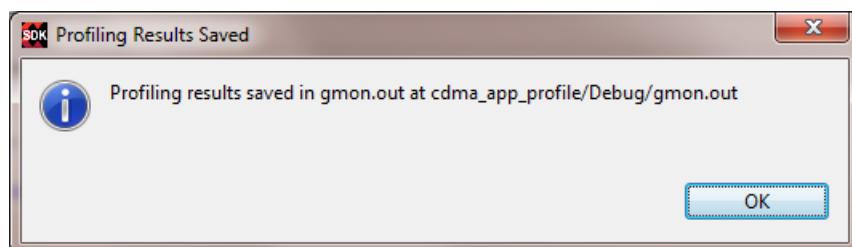
The histogram bin size is the resolution for examining the program counter location used to determine the function that is currently being executed.
  - d. Set the scratch memory address to 0x00300000.

The scratch memory address is the location in DDR3 memory that the BSP profiling services use for data collection. The application program should never touch this space.



*Figure 7-7: Enabling Profiling*

7. Click **Run** to create the configuration and run it.
8. Click **OK** in the Reset Status dialog box.
9. When profiling completes, a dialog box opens to indicate the location of the results file.



*Figure 7-8: Profiling Results Saved Dialog Box*

10. Click **OK**.

11. In the Project Explorer tab, expand the Debug folder under the cdma\_app\_profile project and double-click gmon.out to open the Gmon File Viewer dialog box.

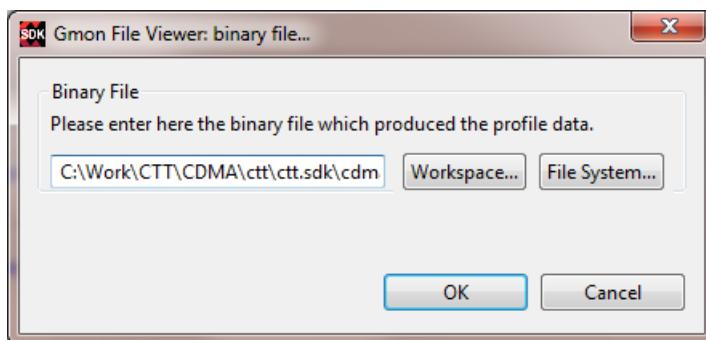


Figure 7-9: Gmon File Viewer Dialog Box

12. Click **OK** to open the profiling results (gmon.out) in a gprof tab in the right window area. It looks similar to [Figure 7-10](#).

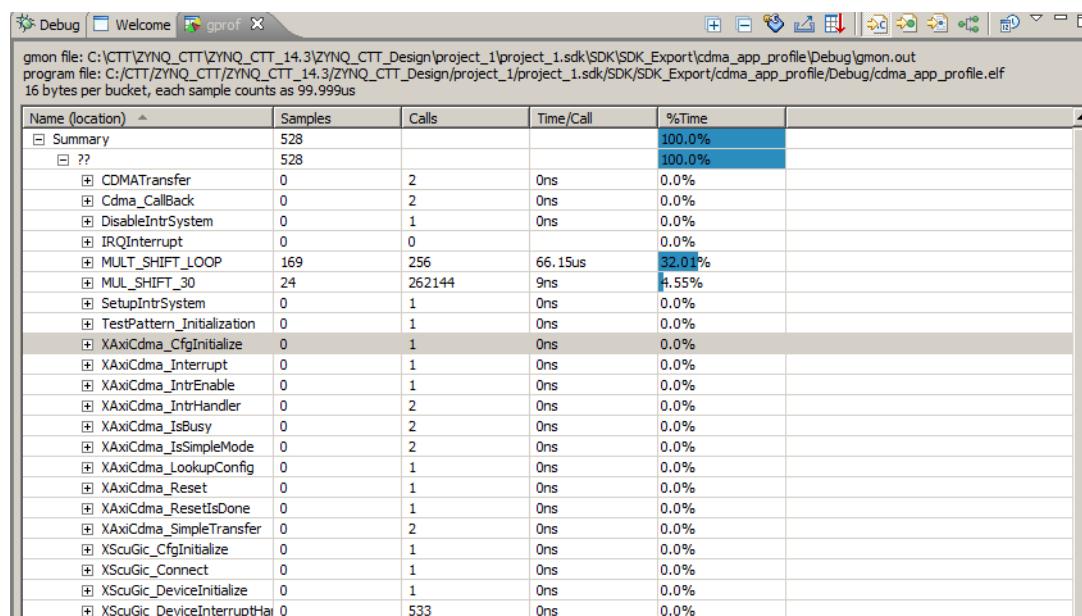


Figure 7-10: Viewing the gmon.out file

# Accelerator Coherency Port

The processing system accelerator coherency port (ACP) is an AXI3-compliant 64-bit slave port interface on the Snoop Control Unit (SCU) that provides an asynchronous cache-coherent access point directly from the processor logic (PL) to the processing system (PS) Cortex-A9 MP-Core processor subsystem.

The processor can mark transactions on the ACP as coherent or non-coherent. The AXI master on the fabric side indicates coherent read transactions by ARUSERS [0] and ARCACHE [1], and write transactions by AWUSERS [0] and AWCACHE [1] AXI bus related signals. Device or strongly ordered transactions are always treated as non-coherent.

**Note:** Device or strongly ordered transactions are types of transfers generated by the AXI master interface. They refer to non-cacheable and non-bufferable transactions. They always generate a fixed size and number of the transaction.

---

## Introduction

Non-coherent transactions pass through the SCU and are presented unchanged on the AXI master interface. Coherent AXI transactions on the ACP slave are changed into more or fewer transactions on the AXI master interface with some of their attributes changed appropriately.

When a coherent write request is received on the ACP from the external master, the SCU checks the L1 data caches of the cores for the address. If present, the coherency protocol cleans and invalidates the appropriate lines in the Cache and merges the cleaned data with the write request.

Read requests from the external master to a coherent region of memory interact with the SCU to test whether the required data is already stored within the processor L1 caches. If the data is present in L1 cache, the SCU returns the data directly to the requesting component. If the data is not present in the L1 cache, the SCU checks the L2 cache before sending the request to the main memory.

Figure 8-1 shows the possible connection between an AXI-4 compliant master and an ACP 64-bit port with the help of the AXI interconnect.

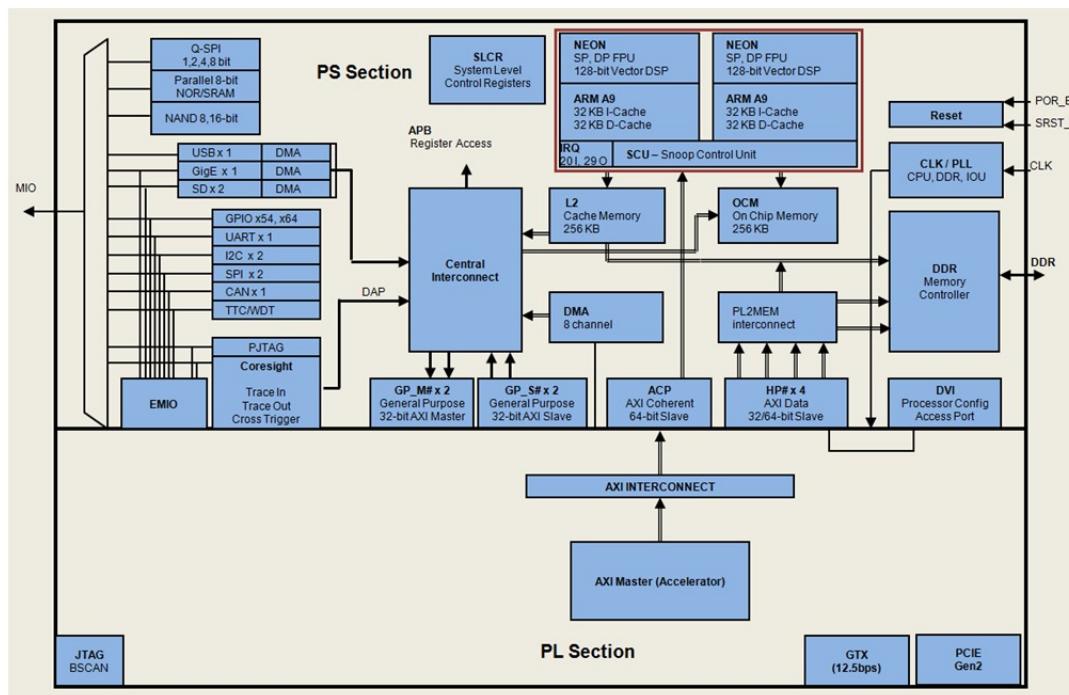


Figure 8-1: Possible Connections Between AXI-4 Compliant Master and ACP 64-bit Port

## ACP Requests

The read and write requests performed on the ACP behave differently with coherent requests than with non-coherent requests.

### ACP Coherent Read Requests

An ACP read request is coherent when both `ARUSER[0] = 1` and `ARCACHE[1] = 1` are alongside `ARVALID`. In this case, the SCU enforces coherency. When the data is present in the caches of one of the Cortex-A9 processors, the PS core reads the data directly from the relevant processor and returned to the ACP. When the data is not present in the cache of either of the Cortex-A9 processors, the read request is issued to either L2-cache or the main memory on one of the Cortex-A9 processors AXI master ports, along with all its AXI parameters, with the exception of the locked attribute.

## ACP Non-Coherent Read Requests

An ACP read request is non-coherent when either ARUSER[0] = 0 or ARCACHE[1] = 0 is alongside ARVALID. In this case, the SCU does not enforce coherency, and the read request is directly forwarded to one of the available SCU AXI master ports to the L2 cache controller or OCM.

## ACP Coherent Write Requests

An ACP write request is coherent when both AWUSER[0] = 1 and AWCACHE[1] = 1 are alongside AWVALID. In this case, the SCU enforces coherency. When the data is present in the L1-Cache of one of the Cortex-A9 processors, the PS section logic first cleans and invalidates the data from the relevant CPU. When the data is not present in any of the Cortex-A9 processors, or after it has been cleaned and invalidated, the write request is issued to either L2-Cache or the main memory on one of the Cortex-A9 processor AXI master ports. The write request is also issued to all corresponding AXI parameters, with the exception of the locked attribute.

**Note:** The transaction can optionally allocate into the L2 cache if the write parameters are set accordingly.

## ACP Non-Coherent Write Requests

An ACP write request is non-coherent when either AWUSER[0] = 1 or AWCACHE[1] = 0 is alongside AWVALID. In this case, the SCU does not enforce coherency, and the write request is forwarded directly to one of the available SCU AXI master ports.

---

## ACP Limitations

The accelerator coherency port (ACP) has the following limitations:

- Exclusive access is not allowed for coherent memory access.
- Locked access is not allowed for coherent memory access.
- Write transactions with length = 3, size = 3, and write strobe ≠ 11111111 can cause the cache line in the CPU to become corrupted.
- Continuous accesses to the OCM over the ACP can starve access from other AXI masters.

To allow access from other masters, the ACP bandwidth to OCM should be moderated to less than the peak OCM bandwidth. This can be accomplished by regulating burst sizes to fewer than eight 64-bit words.

**Note:** The PS processor cores can be used to flag the third limitation (cache lines being corrupted). If enabled, the Xilinx® ACP adapter watches for transactions that could potentially corrupt the cache and generates an error response to the master that requested the write request. The PS section allows the write transaction from master to proceed to the ACP interface, so the possibility of cache corruption is NOT eliminated. The PS section notifies the master of the possible problem in order to take the appropriate action. The ACP adapter can also generate an interrupt signal to the CPUs, which the software can use to detect such a situation.

Refer to the following for more information regarding the ACP:

- *Zynq®-7000 Extensible Processing Platform Technical Reference Manual* (UG585) [\[Ref 6\]](#)
- The Effect and Technique of System Coherence in ARM Multicore Technology by John Goodacre, Senior Program Manager, ARM Processor Division [\[Ref 11\]](#)
- ARM Cortex-A9 MPCore Technical Reference Manual, section 2.4, Accelerator Coherency Port [\[Ref 12\]](#)

# Creating Custom IP and Device Driver for Linux

In this chapter, you will create an Intellectual Property (IP) using the Create and Package New IP wizard. You will also design a system to include the new IP created for the Xilinx® Zynq®-7000 AP SoC device.

For the IP, you will develop a Linux-based device driver as a module that can be dynamically loaded onto the running kernel.

You will also develop Linux-based application software for the system to execute on the Zynq SoC ZC702 board.

---

## Requirements

In this chapter, the target platform points to a ZC702 board. The host platform points a Windows machine that is running the Vivado® Design Suite tools.

The requirements for Linux-based device driver development and kernel compilation are as follows:

- Linux-based Workstation. The workstation is used to build the kernel and the Device driver for the IP.
- CodeSourcery toolchain. An Eclipse-based Integrated Development Environment (IDE) that incorporates the GNU Toolchain for cross development for target architectures. For Tool related information and installation, refer to the Xilinx Zynq Tools Wiki Page [\[Ref 9\]](#).
- Kernel Source Code and build environment. Refer to the Xilinx Zynq Linux Wiki Page [\[Ref 10\]](#), which provides details about the Linux kernel specific to Zynq SoC FPGAs. You can download the Kernel Source files and also get the information for building a Linux kernel for the Zynq SoC FPGA.

**Note:** You can download kernel source files and u-boot source files with the tag "xilinx-14.4-build" from the Xilinx GitHub website [\[Ref 13\]](#).

- Device driver software file (blink.c) and the corresponding header file (blink.h). These files are available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

- Application software (`linux_blinkled_apps.c`) and corresponding header file (`blink.h`). These files are available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).
- If you want to skip the Kernel and device driver compilation, use the already compiled images that are required for this section. These images are available in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

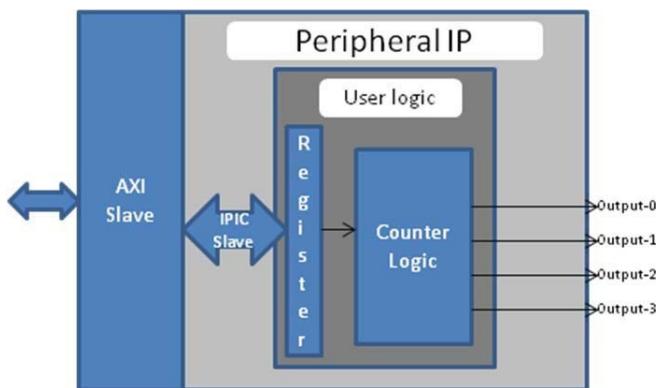


**CAUTION!** You must build Peripheral IP loadable kernel module (LKM) as part of the same kernel build process that generates the base kernel image. If you want to skip kernel or LKM Build process, use the precompiled images for both kernel and LKM module for this section provided in the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

## Creating Peripheral IP

In this section you will create an AXI4-Lite compliant slave peripheral IP framework using the Create and Package New IP wizard. You will also add functionality and port assignments to the peripheral IP framework.

The Peripheral IP you will create is an AXI4-Lite compliant Slave IP. It includes a 28-bit counter. The 4 MSB bits of the counter drive the 4 output ports of the peripheral IP. The Block Diagram is shown in [Figure 9-1](#).



*Figure 9-1: Block Diagram for Peripheral IP*

The block diagram includes the following configuration register:

Register Name	Control Register
Relative Address	0x0000_0000
Width	1 bit
Access Type	Read/Write
Description	Start/Stop the Counter

Field Name	Bits	Type	Reset Value	Description
Control Bit	0	R/W	0x0	1 : Start Counter 2 : Stop Counter

## Example Project: Creating Peripheral IP

In this section, you will create an AXI4-lite compliant slave peripheral IP.

1. Create a new project as described in [Example Project: Creating a New Embedded Project with Zynq SoC, page 14](#).
2. With the Vivado design open, select **Tools > Create and Package IP**. Click **Next** to continue.
3. Select **Create a new AXI4 peripheral** and then click **Next**.
4. Fill in the peripheral details as follows:

Wizard Screen	System Property	Setting or Comment to Use
Peripheral Details	Name	Blink
	Version	1.0
	Display Name	Blink_v1.0
	Description	My new AXI IP
	IP Location	C:/designs/ip_repro
	Overwrite existing	unchecked

5. Click **Next**.
6. In the Add Interfaces window, accept the default settings and click **Next**.
7. In the Create Peripheral window, select Edit IP and then click Finish. Upon completion of the new IP generation process, the Package IP tab opens ([Figure 9-2, page 96](#)).

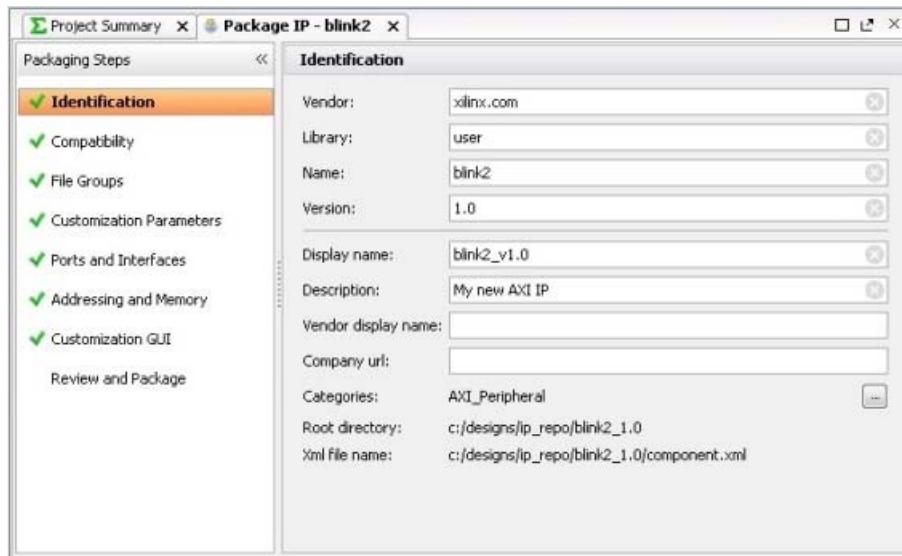


Figure 9-2: Package IP Tab

8. Under **Sources > Hierarchy > Design Sources**, right-click **blink\_v1\_0** and select **Open File**. We will need to add Verilog code that creates output ports to map to the external LEDs on the ZC702 board. With **blink\_v1\_0.v** open, navigate to the line `//Users` to add ports here and add the following code below this line:

```
//Users to add ports here
output wire [3:0] leds,
//User ports ends
```

9. Find the instance instantiation to the AXI bus interface and add the following code to map the port connections:

```
.S_AXI_RREADY(s00_axi_rready),
.LEDs(leds)
);
```

10. Save and close **blink\_v1\_0.v**.

11. Under **Sources > Hierarchy > Design Sources > blink\_v1\_0**, right-click **blink\_v1\_0\_S00\_AXI\_inst - blink\_v1\_0\_S00\_AXI** and select **Open File**.

Next, you will to add Verilog code that creates output ports to map to the external LEDs on the ZC702 board and also create the logic code to blink the LEDs when Register 0 is written to.

12. With **blink\_v1\_0\_S00\_AXI.v** open, navigate to the line `//Users` to add ports here and add the following code below this line.

```
//Users to add ports here
output wire [3:0] LEDs,
//User ports ends
```

13. Find the AXI4Lite signals section and add a custom register, which you will use as a counter. The added code is highlighted in red:

```
// AXI4LITE signals
reg [C_S_AXI_ADDR_WIDTH-1 : 0] axi_awaddr;
reg axi_awready;
reg axi_wready;
reg [1 : 0] axi_bresp;
reg axi_bvalid;
reg [C_S_AXI_ADDR_WIDTH-1 : 0] axi_araddr;
reg axi_arready;
reg [C_S_AXI_DATA_WIDTH-1 : 0] axi_rdata;
reg [1 : 0] axi_rrresp;
reg axi_rvalid;
// add 28-bit register to use as counter
reg [27:0] count;
```

14. Find the I/O connections assignments in each section. This is where we will assign the last 4 bits of the counter to the LED's. The added code is highlighted in red:

```
// I/O Connections assignments
assign S_AXI_AWREADY= axi_awready;
assign S_AXI_WREADY= axi_wready;
assign S_AXI_BRESP= axi_bresp;
assign S_AXI_BVALID= axi_bvalid;
assign S_AXI_ARREADY= axi_arready;
assign S_AXI_RDATA= axi_rdata;
assign S_AXI_RRESP= axi_rrresp;
assign S_AXI_RVALID= axi_rvalid;
// assign MSB of count to LED's
assign LEDs = count[27:24];
```

15. Toward the bottom of the file, find the section that states add user logic here. Add the following code, which will increment count while the slv\_reg0 is set to 0x1. If the register is not set, the counter does not increment. The added code is highlighted in red:

```
// Add user logic here
// on positive edge of input clock
always @( posedge S_AXI_ACLK )
begin
    //if reset is set, set count = 0x0
    if ( S_AXI_ARESETN == 1'b0 )
        begin
            count <= 28'b0;
        end
    else
        begin
            //when slv_reg_0 is set to 0x1, increment count
            if (slv_reg0 == 2'h01)
                begin
                    count <= count+1;
                end
            else
                begin
                    count <= count;
                end
        end
    end
// User logic ends
```

16. Save and close `blink_v1_0_S00_AXI.v`.
17. Open the **Package IP - blink** tab. Under **Packaging Steps**, select **Ports and Interfaces**.
18. Click the **Merge Changes from Ports and Interfaces Wizard** link.

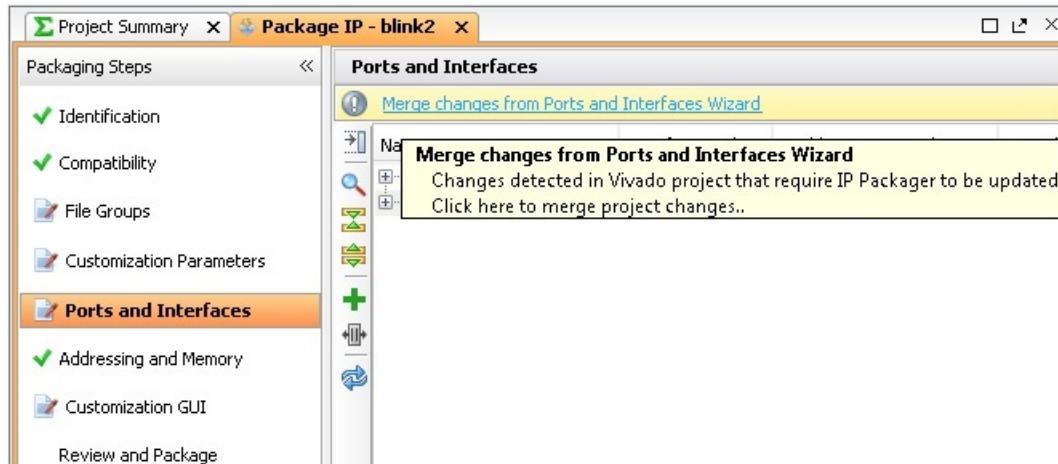


Figure 9-3: Merge Changes from Ports and Interfaces Wizard Link

19. Make sure that the window is updated and includes the LEDs output ports.

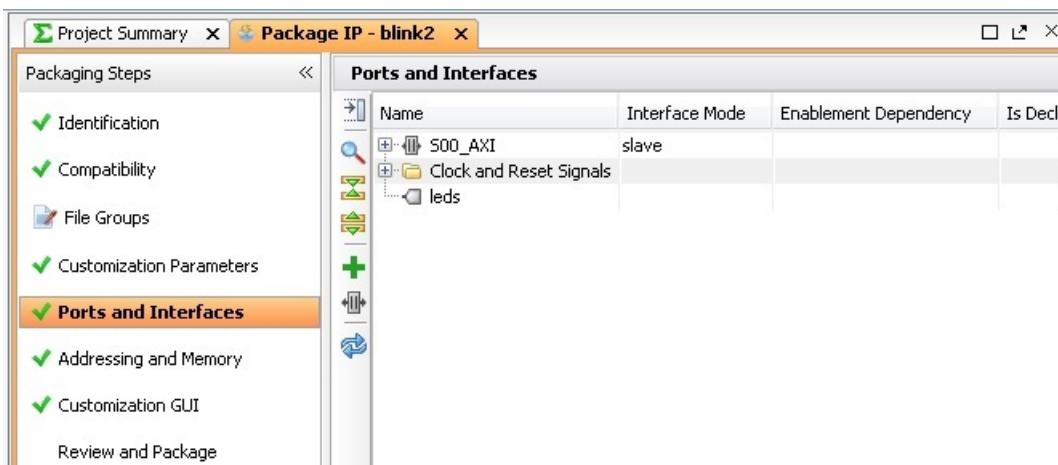


Figure 9-4: Package IP Tab: Ports and Interfaces Page

20. Under Packaging Steps, select **Review and Package**. At the bottom of the Review and Package window, click **Re-Packaging IP**.

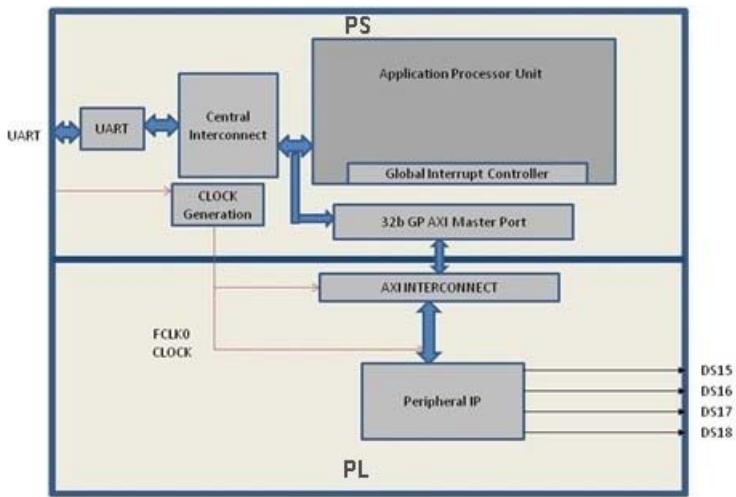
The dialog box that opens states that packaging is complete and asks if you would like to close the project.

21. Click **OK**.

**Note:** The custom core creation process that we have worked through is very simple with the example Verilog included in the IP creation process. For more complex debugging tips and tricks for custom Processor IP Cores, reference Xilinx Answer Record 55345 [Ref 7]. Another good reference is the GitHub Zynq Cookbook: How to Run BFM Simulation webpage [Ref 14].

## Integrating Peripheral IP with PS GP Master Port

Now, you will create a system for the ZC702 board by instantiating the peripheral IP as a slave in the Zynq SoC processing logic (PL) section. You will then connect it with the PS processor through the processing system (PS) general purpose (GP) master port. The block diagram for the system is shown in [Figure 9-5](#).



*Figure 9-5: Block Diagram*

This system covers the following connections:

- Peripheral IP connected to PS General Purpose master port 0 (M\_AXI\_GP0). This connection is used by the PS CPU to configure Peripheral IP register configurations.
- Four output ports of Peripheral IP connected to DS15, DS16, DS17, and DS18 on-board LEDs.

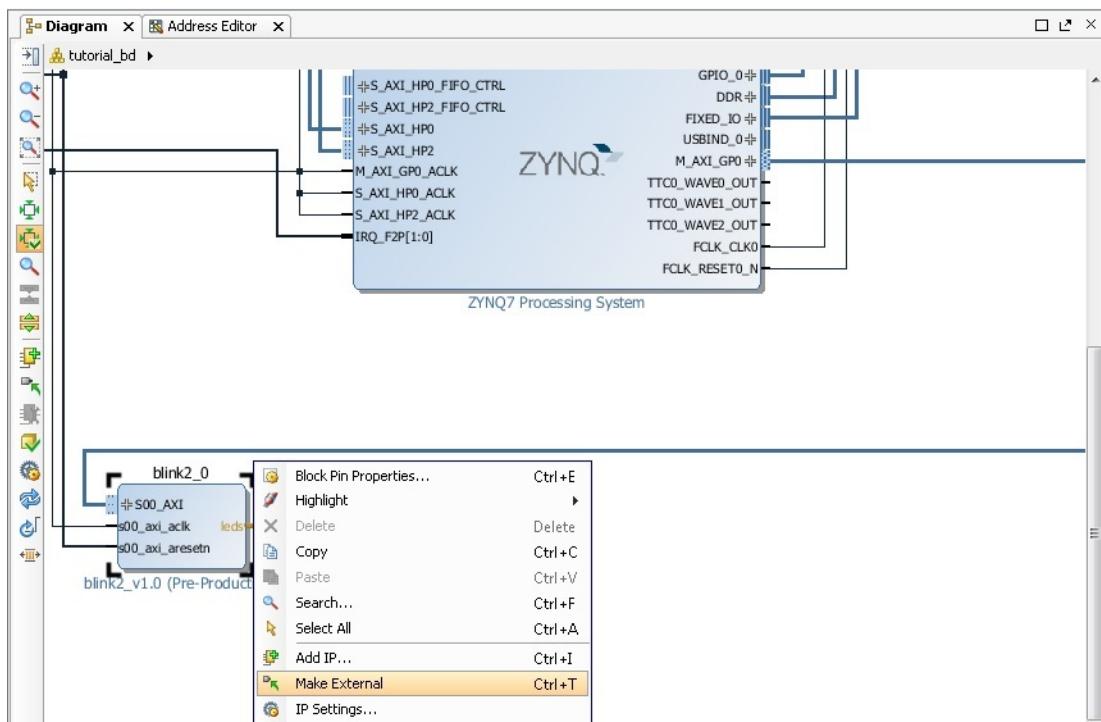
In this system, when you run application code, a message appears on the serial terminal and asks you to choose the option to make the LEDs start or stop blinking.

- When you select the start option on the serial terminal, all four LEDs start blinking.
- When you select the stop option, all four LEDs stop blinking and retain the previous state.

## Integrating Peripheral IP with the PS GP Master Port

In this section, you will connect an AXI4-lite compliant custom slave peripheral IP that you created in [Example Project: Creating Peripheral IP, page 95](#).

1. Open the Vivado project you previously created in [Example Project: Creating a New Embedded Project with Zynq SoC, page 14](#).
2. Add the custom IP to the existing design. Right-click the Diagram view and select **Add IP**.
3. Type **begin** into the search view. Blink\_v1.0 appears. **Double-click** the IP to add it to the design.
4. Click **Run Connection Automation** to make automatic port connections.
5. With the All Automation box checked by default, click **OK** to make the connections.
6. Your new IP is automatically connected but the leds output port is unconnected. Right-click the **leds** port and select **Make External**.



**Figure 9-6: Make the leds Port External**

7. In the Flow Navigator view, navigate to **RTL Analysis** and select **Elaborated Design**.

The message at the top of the screen states "Elaborated Design is out-of-date. Design sources were modified." Click **Reload**. The design must resynthesize in order to include the updated custom IP core that is added to the design.

8. After the elaborated design opens, click the **I/O Ports** tab and expand **All Ports > leds**.

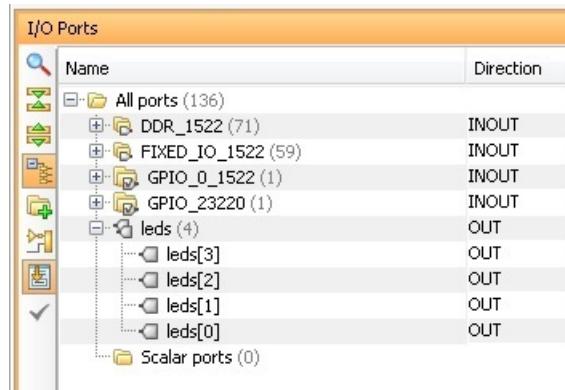


Figure 9-7: I/O Ports

9. Edit the led port settings as follows:

Port Name	Site	I/O Std
Leds[3]	LVCMOS18	P17
Leds[2]	LVCMOS18	P18
Leds[1]	LVCMOS18	W10
Leds[0]	LVCMOS18	V7

Figure 9-8 shows the completed led Port settings in the I/O Ports window.

Name	Direction	Board Part Pin	Board Part Interface	Neg Diff Pair	Site	Fixed	Bank	I/O Std	Vcco
All ports (136)						✓		(Multiple)*	1.50
DDR_1522 (71)	INOUT					✓		(Multiple)*	(Multiple)
FIXED_IO_1522 (59)	INOUT					✓		35 LVCMOS25*	2.50
GPIO_0_1522 (1)	INOUT					✓		35 LVCMOS25*	2.50
GPIO_23220 (1)	INOUT					✓		35 LVCMOS25*	2.50
leds (4)	OUT				P17	✓	(Multiple)	LVCMOS18	1.80
leds[3]	OUT				P18	✓	34	LVCMOS18	1.80
leds[2]	OUT				W10	✓	34	LVCMOS18	1.80
leds[1]	OUT				V7	✓	13	LVCMOS18	1.80
leds[0]	OUT					✓	13	LVCMOS18	1.80

Figure 9-8: led Port Settings

10. Select **Generate Bitstream**.

11. The Save Project dialog box opens. Ensure that the check box is selected and then click **Save**.

12. If a message appears stating that Synthesis is Out-of-date, click **Yes**.

13. After the Bitstream generation completes, export the hardware and launch the Xilinx Software Development Kit (SDK) as described in [Exporting to SDK, page 23](#).

## Linux-Based Device Driver Development

Modules in Linux are pieces of code that can be loaded and unloaded into the kernel on demand. A piece of code that you add in this way is called a loadable kernel module (LKM). These modules extend the functionality of the kernel without the need to reboot the system. Without modules, you would need to build monolithic kernels and add new functionality directly into the kernel image. Besides having larger kernels, this has the disadvantage of requiring you to rebuild and reboot the kernel every time you want new functionality.

LKMs typically are one of the following things:

- Device drivers. A device driver is designed for a specific piece of hardware. The kernel uses it to communicate with that piece of hardware without having to know any details of how the hardware works.
- Filesystem drivers. A filesystem driver interprets the contents of a file system as files and directories.
- System calls. User space programs use system calls to get services from the kernel.

On Linux, each piece of hardware is represented by a file named as a device file, which provides the means to communicate with the hardware. Most hardware devices are used for output as well as input, so device files provide input/output control (`ioctl`) to send and receive data to and from hardware. Each device can have its own `ioctl` commands, which can be of the following types:

- read `ioctl`. These send information from a process to the kernel.
- write `ioctl`. These return information to a process.
- Both read and write `ioctl`.
- Neither read nor write `ioctl`.

For more details about LKM, refer to The *Linux Kernel Module Programming Guide* [Ref 15].

In this section you are going to develop a Peripheral IP Device driver as a LKM, which is dynamically loadable onto the running Kernel. You must build Peripheral IP LKM as part of the same kernel build process that generates the base kernel image.

**Note:** If you don't want to compile the device driver, you can skip the example of this section and jump to [Loading Module into Running Kernel and Application Execution, page 104](#). In that section, you'll use a compiled kernel object image for the Peripheral IP, such as `blink.ko`, which is available in the `LKM` folder of the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

For kernel compilation and device driver development, you must use the Linux workstation. Before you start developing the device driver, the following steps are required:

1. Set the CodeSourcery toolchain path in your Linux Workstation.
2. Download kernel source code and compile it. For downloading and compilation, refer to the steps mentioned in Xilinx Zynq Linux Wiki Page [\[Ref 10\]](#).

## Example Project: Device Driver Development

You will use a Linux workstation for this example project. The device driver software and the make file are provided in the LKM folder of the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#).

1. Under the PetaLinux project directory, use the command below to create your module:

```
petalinux-create -t modules --name mymodule -enable
```

PetaLinux creates the module under <plnx-proj-root>/components/modules/.

2. For our exercise, create the "blink" module:

```
petalinux-create -t modules --name blink -enable
```

The default driver creation includes a make file, C-file, and Readme files. In our exercise, PetaLinux creates blink.c, Makefile, and README files.

3. Change the C-file (driver file) and the make file as per your driver.

4. Take the LKM folder (reference files) and copy blink.c and blink.h into this directory.

5. Run the command:

```
'petalinux build'
```

After successful compilation the .ko file is created under:

```
/lib/modules/<KERNELRELEASE>/extra/mymodule.ko
```

6. You can install the driver using the modprobe command, which will be explained in further detail in the next section.

# Loading Module into Running Kernel and Application Execution

In this section you will boot Linux onto the Zynq SoC Board and load the peripheral IP as a LKM onto it. You will develop the application for the system and execute it onto the hardware

## Loading Module into Kernel Memory

The basic programs for inserting LKMs are modprobe. The modprobe command makes an `init_module` system call to load the LKM into kernel memory. The `init_module` system call invokes the LKM initialization routine immediately after it loads the LKM. As part of its initialization routine, `insmod` passes to the address of the subroutine to `init_module`.

In the peripheral IP device driver, you already set up `init_module` to call a kernel function that registers the subroutines. It calls the kernel's `register_chrdev` subroutine, passing the major and minor number of the devices it intends to drive and the address of its own "open" routine among the arguments. The subroutine `register_chrdev` specifies in base kernel tables that when the kernel wants to open that particular device, it should call the open routine in your LKM.

## Application Software

The `main()` function in the application software is the entry point for the execution. It opens the device file for the peripheral IP and then waits for the user selection on the serial terminal.

If you select the start option on the serial terminal, all four LEDs start blinking. If you select the stop option, all four LEDs stop blinking and retain the previous state.

## Example Project: Loading a Module into Kernel and Executing the Application

### *Booting Linux on the Target Board*

Boot Linux on the Zynq SoC ZC702 target board, as described in [Booting Linux on a Zynq SoC Board, page 66](#).

## ***Loading Modules and Executing Applications***

**Note:** In this section, you'll use the SDK tool installed on a Windows machine.

1. Open SDK.

For SDK, you must run the Target Communication Frame (TCF) agent on the host machine.

2. Select **XSDB** and then **connect** to connect to the Xilinx System Debugger (XSDB).
3. In SDK, select **File > New > Application Project**.

The New Project wizard opens.

4. Use the information in the table below to make your selections in the wizard screens.

Wizard Screen	System Property	Setting or Command to Use
Application Project	Project Name	linux_blinkled_app
	Use Default Location	Select this option
	Hardware Platform	system_hw_platform
	Processor	PS7_cortexa9_0
	OS Platform	Linux
	Language	C
Templates	Available Templates	Linux Empty Application

5. Click **Finish**.

The New Project wizard closes and SDK creates the `linux_blinkled_app` project under the project explorer.

6. In the Project Explorer tab, expand the **linux\_blinkled\_app** project, right-click the **src** directory, and select **Import**.

The Import dialog box opens.

7. Expand **General** in the Import dialog box and select **File System**.
8. Click **Next**.
9. Add the `linux_blinkled_app.c` and `blink.h` files.

**Note:** The Application software file name for the system is `linux_blinkled_app.c` and the header file name is `blink.h`. These files are available in the `LKM` folder of the ZIP file that accompanies this guide. See [Design Files for This Tutorial, page 109](#). Add the `linux_blinkled_app.c` and `blink.h` files.

10. Click **Finish**.

SDK automatically builds the application and generates the `linux_blinkled_app.elf` file. Check the console window for the status of this action.

## 11. Connect the board.

12. Because you have a bitstream for the PL Fabric, you must download the bitstream. Select **Xilinx Tools > Program FPGA**.

The Program FPGA dialog box opens. It displays the bitstream exported from Vivado.

13. Click **Program** to download the bitstream and program the PL Fabric.14. Follow the steps described in [Chapter 6](#) to load the Linux image and start it.

After the Kernel boots successfully, in a serial terminal, navigate to `/lib/modules/<kernel-version>/extra` and run the command:

```
modprobe blink.ko
```

You will see the following message:

```
<1>Hello module world.
```

```
<1>Module parameters were (0xdeadbeef) and "default"
```

```
blink_init: Registers mapped to mmio = 0x80954000
```

```
Registration is a success the major device number is 245.
```

If you want to talk to the device driver, create a device file by following command:

**mknod /dev/blink\_Dev c 245 0**

The device file name is important, because the ioctl program assumes that's the file you'll use

15. Create a device node by running the **mknod** command. Pick the string from the print messages.

For example, the command **mknod /dev/blink\_Dev c 245 0** creates the `/dev/blink_Dev` node.

16. Select **Window > Open Perspective > Other**.

The list of Perspective windows appears.

17. Select **Remote System Explorer** and click **OK**.

SDK opens the Remote Systems Perspective explorer.

18. In the Remote Systems Perspective, do the following:

- a. Right-click and select **New > Connection** to open the New Connection wizard.
- b. Click the **SSH only** tab and click **Next**.
- c. In the Host Name tab, type the target board IP.  
**Note:** To determine the target IP, type **ifconfig eth0** at the **Zynq>** prompt in the serial terminal. The target IP assigned to the board displays.
- d. Set the connection name as **blink** and type a description.
- e. Click **Finish** to create the connection.
- f. Expand **blink > sftp Files > Root**. The Enter Password wizard opens.
- g. Provide the user ID and Password (**root/root**); select the **Save ID** and **Save Password** options.
- h. Click **OK**.

The window displays the root directory content, because you previously established the connection between the Windows host machine and the target board.

- i. Right-click the "/" in the path name and create a new directory; name it **Apps**.
- j. Using the Remote Systems Perspective explorer, copy the `linux_blinkled_app.elf` file from the `<project-dir>/project_1/project_1.sdk/SDK/SDK_Export/linux_blinkled_apps/Debug` folder and paste it into the `/Apps` directory under **blink connection**.
- k. Copy the `blink.ko` file, which you already moved from the Linux workstation to the windows machine, and paste it in the `/Apps` folder under **blink connection**.

19. In the Serial terminal, type **cd Apps** at the **Zynq>** prompt to open the `/Apps` directory.

20. Go to Apps directory at the `root@Xilinx-ZC702-2014_4:/#` Linux prompt, and type **chmod 777 Linux\_blinkled\_app.elf** to change the `linux_blinkled_app.elf` file mode to executable mode.

21. At the `root@Xilinx-ZC702-2014_4:/#` prompt, type **./Linux\_blinkled\_app.elf** to execute the application.

22. Follow the instruction printed on the serial terminal to run the application. The Application asks you to enter 1 or 0 as input.

- Type 1, and observe the LEDs DS15, DS16, DS17, and DS18. They start glowing.
- Type 0, and observe that LEDS stop at their state. No more blinking changes.

You can repeat your inputs and observe the LEDs

23. After you finish debugging the Linux application, close SDK.

# Additional Resources and Legal Notices

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## Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see [Xilinx Support](#).

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## Solution Centers

See the [Xilinx Solution Centers](#) for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

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## Xilinx Documentation Navigator

The Xilinx Documentation Navigator is a free tool that you can use to access documentation while using Xilinx products. The Documentation Navigator is available as part of the Vivado Installer. When it is installed on your system, you can access it by going to **Start > Programs > Xilinx Design Tools > DocNav** and clicking the **DocNav** icon.

For detailed information about using the Xilinx Documentation Navigator, refer to [this link](#) in *Vivado Design Suite User Guide: Getting Started (UG910)* [Ref 12].

## Related Design Hubs

Design hubs provide quick access to documentation, training, and information for specific design tasks. The following design hubs are applicable to embedded development and the methods described in this guide:

- PetaLinux Tools Design Hub
- Software Development Kit Design Hub

## Design Files for This Tutorial

The ZIP file associated with this document contains the design files for the tutorial. You can download this file from [this link](#).

## Xilinx Resources

The following Xilinx® Vivado® Design Suite guides are referenced in this document.

1. *Vivado Design Suite Tutorial: Embedded Processor Hardware Design* ([UG940](#))
2. *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* ([UG973](#))
3. *PetaLinux Tools Documentation Reference Guide* ([UG1144](#))
4. *Vivado Design Suite User Guide: Using Constraints* ([UG903](#))
5. *Zynq-7000 Software Developers Guide* ([UG821](#))
6. *Zynq-7000 Extensible Processing Platform Technical Reference Manual* ([UG585](#))

## Support Resources

7. [Xilinx Answer Record 55345](#)
8. Xilinx PetaLinux Webpage: <http://www.xilinx.com/PetaLinux>
9. Xilinx Zynq Tools Wiki Page: <http://wiki.xilinx.com/zynq-tools>
10. Xilinx Zynq Linux Wiki page: <http://wiki.xilinx.com/zynq-linux>

## Additional Resources

11. The Effect and Technique of System Coherence in ARM Multicore Technology by John Goodacre, Senior Program Manager, ARM Processor Division  
(<http://www.mpsoc-forum.org/previous/2008/slides/8-6%20Goodacre.pdf>)
12. ARM Cortex-A9 MPCore Technical Reference Manual, section 2.4, Accelerator Coherency Port  
(<http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0407e/CACGGBCF.html>)
13. Xilinx GitHub website: <https://github.com/xilinx>
14. GitHub ZYNQ Cookbook: How to Run BFM Simulation:  
<https://github.com/imrickysu/ZYNQ-Cookbook/wiki/How-to-run-BFM-simulation>
15. The Linux Kernel Module Programming Guide:  
<http://tldp.org/LDP/lkmpg/2.6/html/index.html>

## Training Resources

Xilinx provides a variety of training courses and QuickTake videos to help you learn more about the concepts presented in this document. Use these links to explore related videos:

1. [Vivado Design Suite QuickTake Video: How to Create a Zynq Boot Image Using Xilinx SDK](#)
  2. [Vivado Design Suite QuickTake Video Tutorials](#)
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