EEE3096S Tutorial 2

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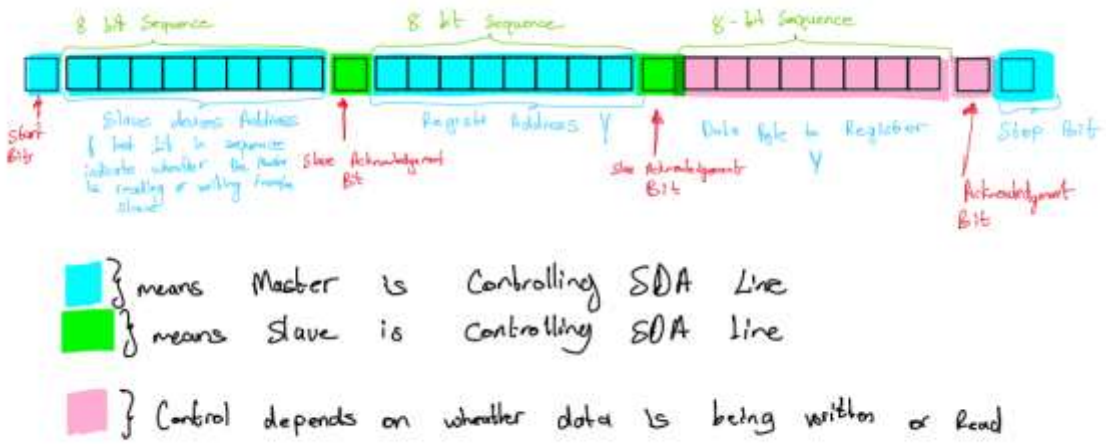
1. I2C

1.1. The message structure for I2C protocol is as follows:

- The data signal is transferred in 3 sequences of 8-bits
- A start bit initiates the first sequence of 8-bits (initiation occurs when the start bit is pulled low because SDA & SCL are high during Idle)
- A series of 8 slave address bits then follow (the first 8 bits indicates the address of the slave to which data is being sent)
- An acknowledge bit then precedes the second sequence of 8-bits (indicates that the slave is ready to communicate with master when pulled low)
- A second series of 8 bits containing the address of the internal register that is to be interacted with on the slave then follows
- A second acknowledgement bit follows
- A third series of 8-bits containing the data being read/written then follows
- A third acknowledgment bit follows
- Then the Stop bit follows
- Below is a visual representation of the message structure



1.2. <u>Advantages of I2C over SPI:</u>

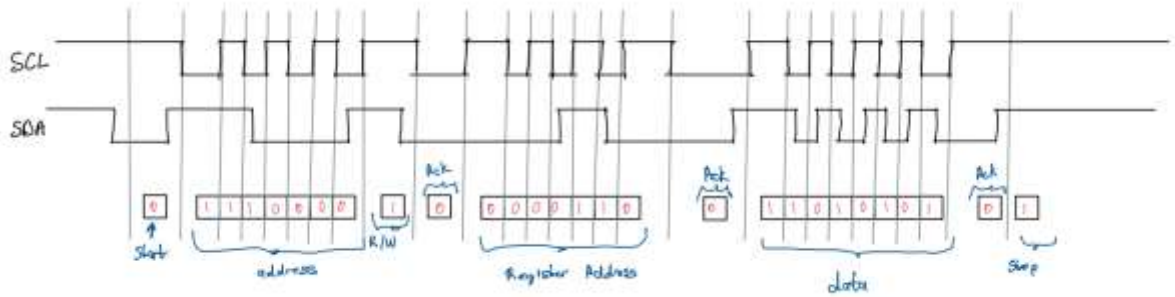
- I2C only requires 2 wires whereas SPI requires 4 or more.
- More than one master device can be used in the circuit whereas only 1 can be used for SPI.

1.3. <u>Start Condition:</u>
The SDA line is pulled low while SCL is high (this is because SCL & SDA are in Idle, therefor high state)

<u>Stop Condition:</u>

The SDA line stop-bit is pulled high (to put communication in Idle)

1.4.



2. <u>Binary Coded Decimal (BCD)</u>

2.1. BCD is a way of writing decimal numbers using their 4-bit or 8-bit binary coded equivalent. An example: The BCD of 252 is 0b11111100. (3 – 0011, 5 – 0101, 2 – 0010)

2.2. Advantage of BCD: It allows for easy conversions between machine readable and human readable numbers, so it makes for a faster approach.
Disadvantage of BCD: It requires more bits of storage in memory than the standard binary system making it inefficient at storing numbers.

3. Unix Epoch

3.1. Unix epoch time is the total amount of seconds that have passed since 1st January 1970, 00:00:00 UTC. Unix epoch time is used because it is all stored in a signed 32-bit. So, the time is stored as a single number of seconds instead of having to store for different values for year, hour, day etc.

3.2. 1 January 2023 12:00:00 am GMT +2 unit epoch time is: 1672524000.

4. RTS and RISC/CISC

4.1. A "Dynamic Synchronous Hard Real-time System" is a system that is designed to respond to situations with strict timing requirements. Dynamic means that the timing requirements can adapt based on various factors during runtime and maintain real-time guarantees. Synchronous means that tasks adhere to a predetermined schedule. For Hard Real-time systems the most import thing is meeting the specified time limits as not meeting that time limits could lead to horrible consequences. These systems are mostly used for safety and time critical applications.

4.2. RISC:
RISC has a smaller instruction set size.
In RISC, memory access is more controlled through load and store instructions. Only specific load and store instructions can directly access memory. These instructions transfer data between memory and registers.
CISC:
CISC has a larger instruction set size.
For CISC there are memory-to-memory operations that perform operations using data in memory without loading it into registers first. These instructions are more complex than those of RISC.

References

Jack, B. (2021, February 13). *What Is Unix Time and When Was the Unix Epoch?* Retrieved from Makeuseof: https://www.makeuseof.com/what-is-unix-time-and-when-was-the-unix-epoch/

Kanade, V. (2023, February 14). *RISC vs. CISC: 20 Key Comparisons*. Retrieved from spiceworks: https://www.spiceworks.com/tech/tech-general/articles/risc-vs-cisc/