CSE 140L Lab 2

A16389707, NG Zhe Wee

Academic Integrity

Your work will not be graded unless the signatures of all members of the group are present beneath the honor code.

To uphold academic integrity, students shall:

- Complete and submit academic work that is their own and that is an honest and fair representation of their knowledge and abilities at the time of submission.
- Know and follow the standards of CSE 140L and UCSD.

Please sign (type) your name(s) below the following statement:

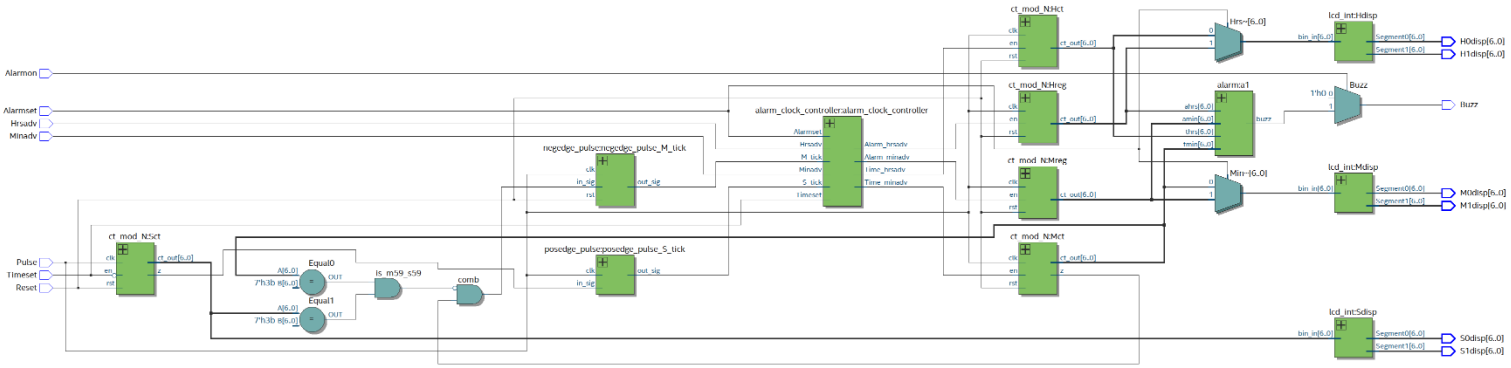
I pledge to be fair to my classmates and instructors by completing all of my academic work with integrity. This means that I will respect the standards set by the instructor and institution, be responsible for the consequences of my choices, honestly represent my knowledge and abilities, and be a community member that others can trust to do the right thing even when no one is watching. I will always put learning before grades, and integrity before performance. I pledge to excel with integrity.

NG Zhe Wee

Screenshots

Part 1

Screenshot of the RTL viewer top level schematic/block diagram in Quartus
Or submit your Mentor Precision netlist file if using EDA Playground (3 pts)

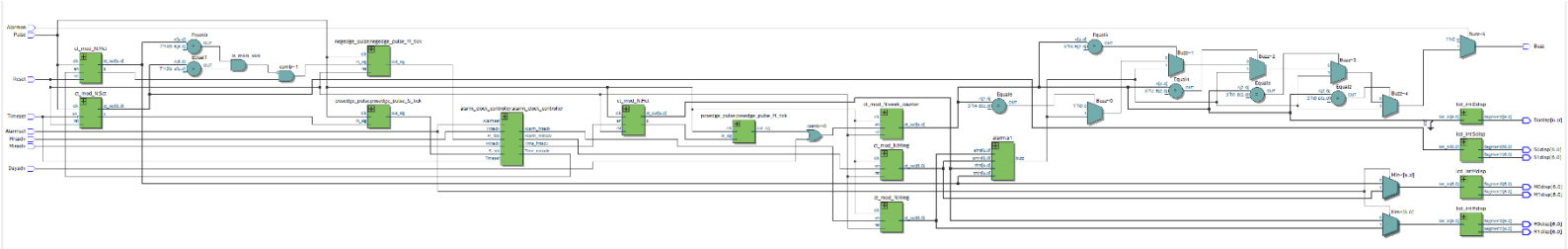


Please include the output file of part 1 testbench in your submission, and name it “output1.txt” (3 pts)

We will be looking for a text file with that name specifically, so be sure to rename it from “list.txt”. Nothing is required in the writeup for this question.

Part 2

Screenshot of the RTL viewer top level schematic/block diagram in Quartus
Or submit your Mentor Precision netlist file if using EDA Playground (3 pts)

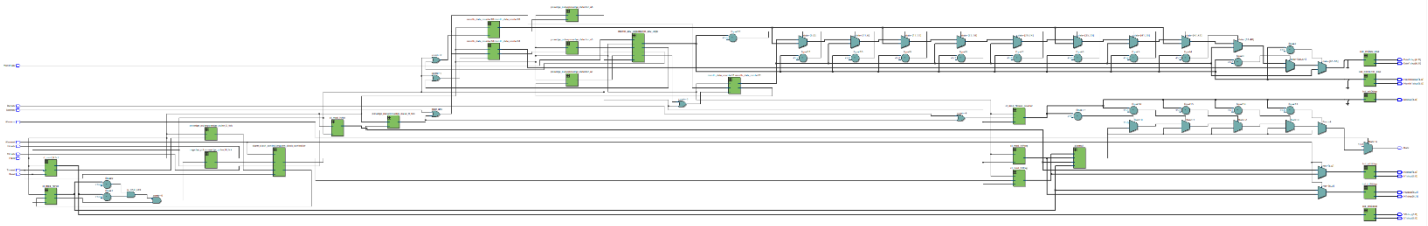


Please include the output file of part 2 testbench in your submission, and name it “output2.txt” (3 pts)

We will be looking for a text file with that name specifically, so be sure to rename it from “list.txt”. Nothing is required in the writeup for this question.

Part 3

Screenshot of the RTL viewer top level schematic/block diagram in Quartus
Or submit your Mentor Precision netlist file if using EDA Playground (3 pts)



Please include the output file of part 3 testbench in your submission, and name it “output3.txt” (3 pts)

We will be looking for a text file with that name specifically, so be sure to rename it from “list.txt”. Nothing is required in the writeup for this question.

Free Response

Please answer the following questions.

1. Please write a summary paragraph explaining how you tested your alarm clock in part 1. (4 pts)

To test my alarm clock in part 1, I first instantiated the alarm clock module and initialized the corresponding signals. Then, I simulated the behavior of the alarm clock which included setting time and alarm, advancing the time, turning on and off the alarm for a specified duration of time period. Meanwhile, I was able to take advantage of the “display_tb” task to visualize the prodcedure of the simulation via the 7-segment display. Note that I delibrately included some edge cases for incrementing hour, minutes, and seconds to demonstrate the comprehensiveness of my designated tests.

2. Please write a summary paragraph explaining the day of the week enhancement and how it was implemented. (4 pts)

The day of the week enhancement at its core is orientated by a week counter that is connected to “ct_mod_N” module with a parameter value of 7. It is also connected to the “lcd_int” module to allow itself to be displayed correctly in 7-sefment display. Additionally, the day of the week enhancement influences the previous implementation of the alarm such that alarmon on is only set to be on for weekdays in “struct_diag” module. With corresponding tests similar but more comprehensive than the previous one, the enhancement passed its functionality test with several cases.

3. Please write a summary paragraph explaining the date enhancement and how it was implemented. (4 pts)

The date enhancement at its core is orientated by ‘month_date_counter28’, ‘month_date_counter30’, ‘month_date_counter31’. Each of them, as their names suggest, increment the date and increment the date up to their specified celling where the date is reset to 1. These modules are included into the top level design ‘struct_diag’ module, where these modules are selected based on which month it is. This is determined by month value and the trivial conditional statements. Finally, It is also connected to the “lcd_int” module to allow itself to be displayed correctly. With test that increments it from January to May, the enhancement passed its functionality test with several cases.