# CSE 140L Lab 1

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## Academic Integrity

Your work will not be graded unless the signatures of all members of the group are present beneath the honor code.

To uphold academic integrity, students shall:
● Complete and submit academic work that is their own and that is an honest and fair representation of their knowledge and abilities at the time of submission.
● Know and follow the standards of CSE 140L and UCSD.

Please sign (type) your name(s) below the following statement:

I pledge to be fair to my classmates and instructors by completing all of my academic work with integrity. This means that I will respect the standards set by the instructor and institution, be responsible for the consequences of my choices, honestly represent my knowledge and abilities, and be a community member that others can trust to do the right thing even when no one is watching. I will always put learning before grades, and integrity before performance. I pledge to excel with integrity.

Type full names of teammates:

NG Zhe Wee, A16389707
_____

_____

_____

Please include the following screenshots:

1. Screenshot of Modelsim/Questa output (last page of transcript/console).

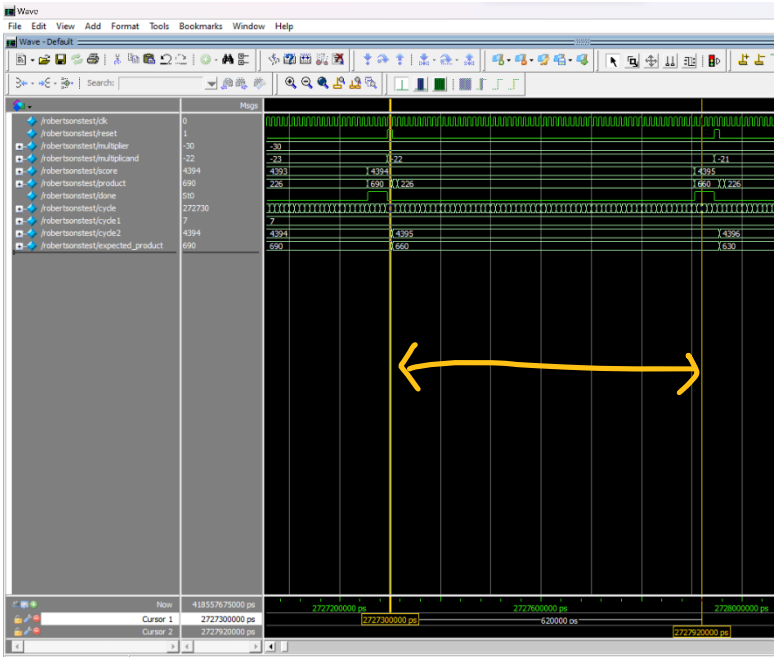
   The screenshot should show your output vs the expected output. It should also show the score.

```
VSIM 2> run -all
# Simulation succeeded 0000 = 0000 = 00 * 00
# Simulation succeeded      0 =      0 =    0 *    0
# Simulation succeeded 001e = 001e = 05 * 06
# Simulation succeeded     30 =     30 =    5 *    6
# Simulation succeeded ffdd = ffdd = 07 * fb
# Simulation succeeded    -35 =    -35 =    7 *   -5
# Simulation succeeded ffe2 = ffe2 = fb * 06
# Simulation succeeded    -30 =    -30 =   -5 *    6
# Simulation succeeded ffc8 = ffc8 = f9 * 08
# Simulation succeeded    -56 =    -56 =   -7 *    8
# Simulation succeeded 001e = 001e = fb * fa
# Simulation succeeded     30 =     30 =   -5 *   -6
# Simulation succeeded 0024 = 0024 = f7 * fc
# Simulation succeeded     36 =     36 =   -9 *   -4
# ** Note: $stop    : D:/OneDrive/UCSD/(9) 2023 Spring/CSE 140L/[Labs for CSE 140L] (20%x5)/Lab 1/robertsonstest.sv(72)
#    Time: 4315 ns  Iteration: 0  Instance: /robertsonstest
# Break in Module robertsonstest at D:/OneDrive/UCSD/(9) 2023 Spring/CSE 140L/[Labs for CSE 140L] (20%x5)/Lab 1/robertsonstest.sv line 72
add wave -position insertpoint sim:/robertsonstest/*
VSIM 4> run -all
# clock cycles =     1008051, test cycles =           7, score =       16384 /       16384
# ** Note: $stop    : D:/OneDrive/UCSD/(9) 2023 Spring/CSE 140L/[Labs for CSE 140L] (20%x5)/Lab 1/robertsonstest.sv(79)
#    Time: 10080515 ns  Iteration: 0  Instance: /robertsonstest
# Break in Module robertsonstest at D:/OneDrive/UCSD/(9) 2023 Spring/CSE 140L/[Labs for CSE 140L] (20%x5)/Lab 1/robertsonstest.sv line 79
```

2. Be sure to upload all of your source code (.sv files), including any associated .txt files for $readmem statements.

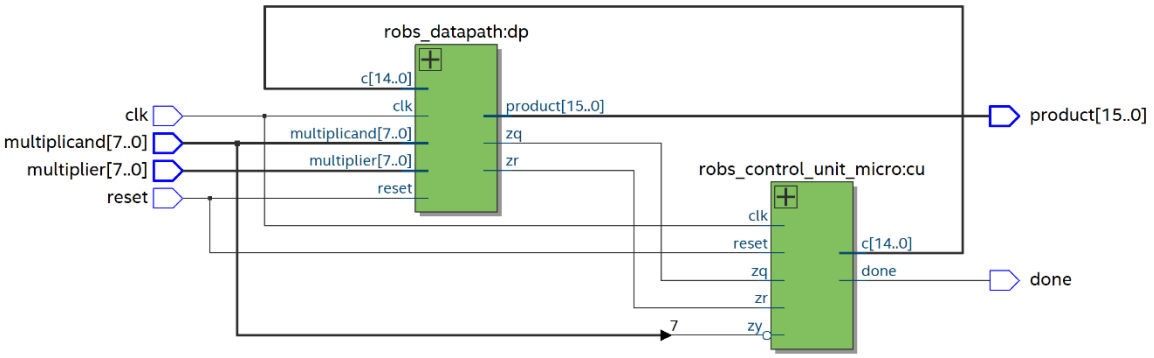
3. Waveforms.

   Include screenshot of waveform for one entire multiplication cycle (i.e. the waveform should include the portion where reset is 1 until the portion where the done flag is 1)

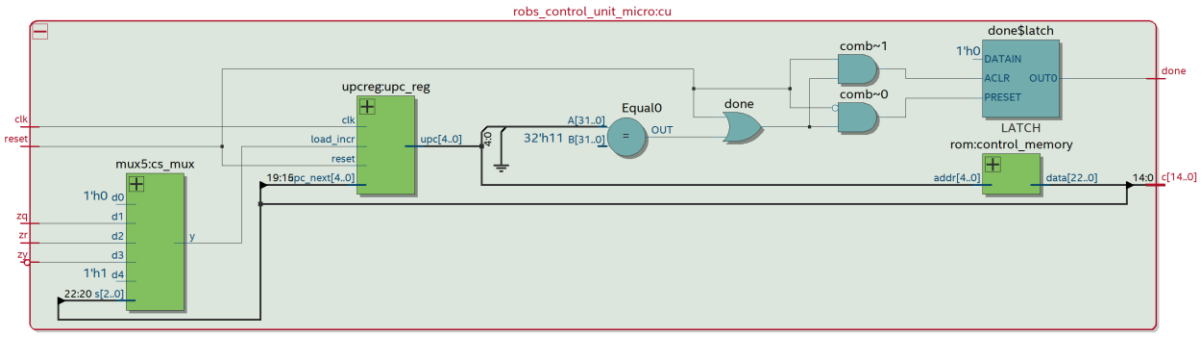



4. RTL diagrams of the following

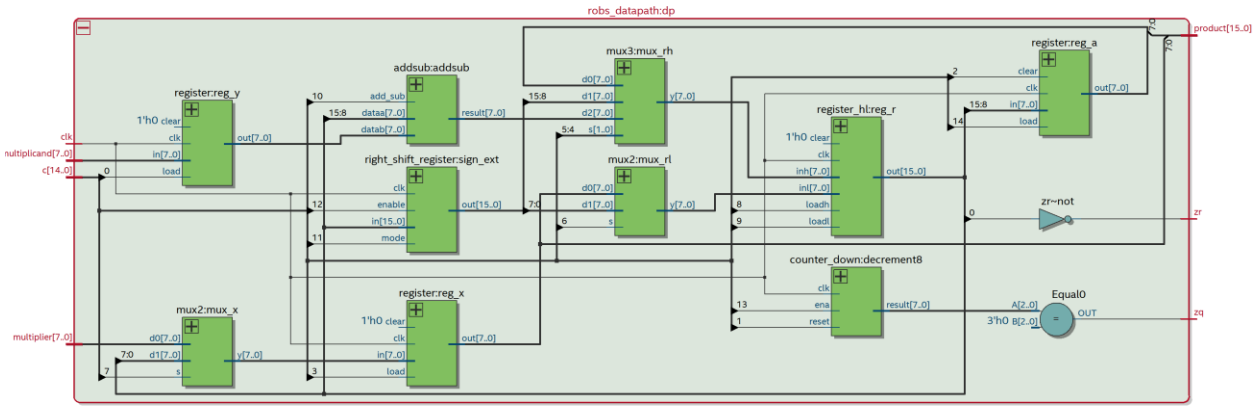
a. Quartus RTL view of top level of the multiplier (it should show the connections between data path and control path).




b. Quartus RTL view of the control unit.




c. Quartus RTL view of the data path.



These questions won't be graded but it would be helpful to know the answers to these for future labs.

On combinational & sequential logic

1. Which always_* keyword do you use for combinational logic of a single line of code?
2. Which keywords would you use along with the above answered always_* keyword if there are multiple lines of code in the combinational logic?
3. Is there any other keyword you can use for combinational logic with a single line of code?
4. Which keyword is used to denote sequential logic?
5. What's the difference between sequential and combinational logic?

On blocking & nonblocking assignment

1. Which symbol indicates the blocking assignment?
2. Which symbol indicates the nonblocking assignment?
3. Why do we need blocking assignments?
4. Why do we need non-blocking assignments?
5. What's the difference between blocking and non-blocking assignments?

On logic and wire

1. What's the difference between keywords : logic and wire?
2. Would you prefer to assign the output of sequential logic to wire or logic? Explain why.