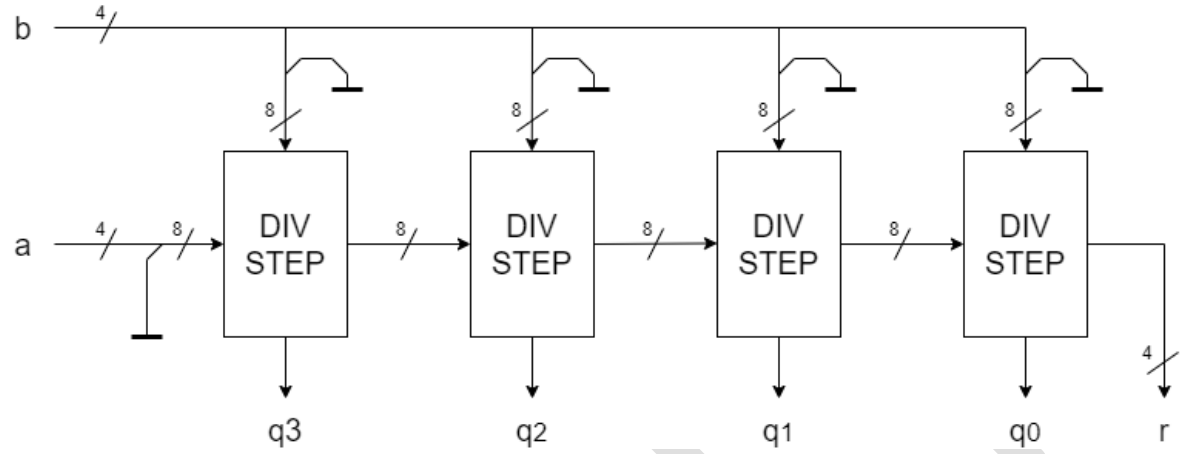
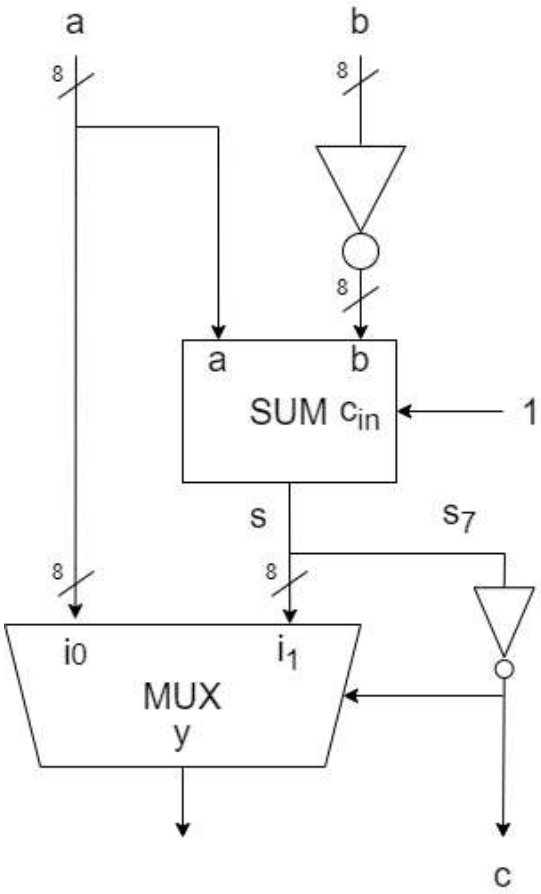
# ASSIGNMENT 1

## Description

This circuit, **div**, is an integer divider that computes the quotient and the remainder of the input dividend, a, divided by the divider, b. It implements the basic division algorithm, using one instance of **div_step** block for each step of the algorithm:




The **div_step** bloc subtracts the shifted dividend from the partial result. If the result of the subtraction is negative ($s_7 = 1$), the partial result is kept, otherwise ($s_7 = 0$) the new partial result goes to the next step of the algorithm.




For each step of the division, the divider is properly alligned. For the first step it is shifted to the left with 3 positions, for the second step with 2 positions, for the third step with one position.

The 4 bit inputs of the **div** block are extended with 4 zeros to 8 bits.

## Requirements

- The **div_step** module is described structurally as in the second figure.
- The **sum** module is described behaviorally with a continuous assignment.
- The **mux** module is described behaviorally using an always process.
- The top-level design module, **div**, is described structurally as in the first figure.
- All modules must have the names and pin names as in the list below. The widths of the pins are shown in the block schematics.

```
div (a, b, q, r)
div_step (a, b, c, y)
sum (a, b, cin, s)
mux (sel, in1, in0, y)
div_tb
```

## Grading

2 – sum

2 – mux

8 – div_step

5 – div

2 – div_tb

1 – coding style