EE 320 COURSE

DESIGN PROJECT REPORT

Design Project II

**December 08, 2015**

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# Introduction

*Design an audio amplifier using Bipolar Junction Transistors. The input signal comes from a communications receiver which has a 100mVpp signal that can range from 200Hz to 2000Hz and a series resistance of 1kΩ. The maximum output current of the receiver is 1.5μA. The output of the amplifier is to be connected to an 8Ω speaker. The* *required output power of the amplifier’s signal is to be 3W ±5%. The output signal may be time-shifted (up to 90°), but you must keep the signal distortion minimal (the output must still be a clear sinusoid).*

# Procedure

The amplifier design was split into four parts. The general circuit is the same, Fig. 1, for each of the designs but the amplifier grows as more components are added. It may be helpful to read the procedure and the results and analysis of one part together. The results and analysis of part 1 was done before the procedure of part 2.

The output voltage must be within a range of values set by the load resistance and the required output power range. By using this relationship (1) the required output voltage range is determined to be: to , or equivalently to .

(1)

Given the input signal then the required closed loop gain range of the circuit was determined by using the definition of closed loop gain (2). Using the average required voltage, 4.9 V, the closed loop gain of the system must be approximately .

(2)

The full circuit is assembled; note the use of net aliases to modularize components, Fig. 1. It is important to evaluate how the input signal’s parameters were chosen. The design of the problem defines the input signal as . The parameter “VAMPL” is the amplitude of the sine wave and half of the peak to peak voltage. The parameter “AC” is the root mean square (RMS) value of the sinusoidal wave; it is utilized during simulations that do a frequency sweep. Any circuit with active components requires a power source; initially a simulated 30 VDC source was used, Fig. 2

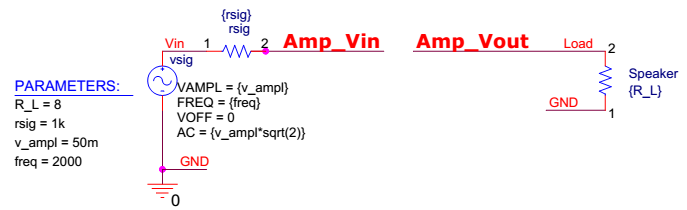


Figure : PSpice circuit connecting input and output to amplifier.

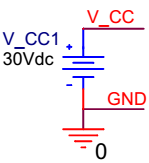


Figure : Simulated power supply.

## Part 1: Initial design.

*Determine the required output voltage. Determine ICQ which provides the best β (in your calculations, use a β midway between the typical and maximum values). Show the hand calculations to determine the bias (DC) network and calculate the expected gain (AC). Build the system in Pspice using 0.1mF coupling caps.*

The best beta value is the largest beta value; other names for this parameter are DC Current Gain and . From the datasheet for the 2N3904 NPN transistor (produced by KEC on Sept 12, 2002) the greatest DC current gain is 300. More specifically the beta value can be expected to be from 100 to 300 when and .

The bias network was designed to have a current of 10 mA through the emitter and a beta value of 200 was assumed. The design was created so that was divided equally among , , and . The handwork to design the bias network for the common emitter is included in the appendix but the results are presented, Table 1.

Table : Resistances used for common emitter bias network.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name |  |  |  |  |
| Value | 1000 | 995 | 50.847 | 32.967 |

Using these resistance values the initial design for the first common emitter was created, Fig. 3. The percentage of the emitter resistance that is AC coupled can be set by the parameter ‘CE1\_CP’. The AC coupling of is defined as percentage of the common emitter resistance that is not in shunt with a capacitor. The common emitter has coupling capacitors on either side to isolate the DC signal, Fig. 4.

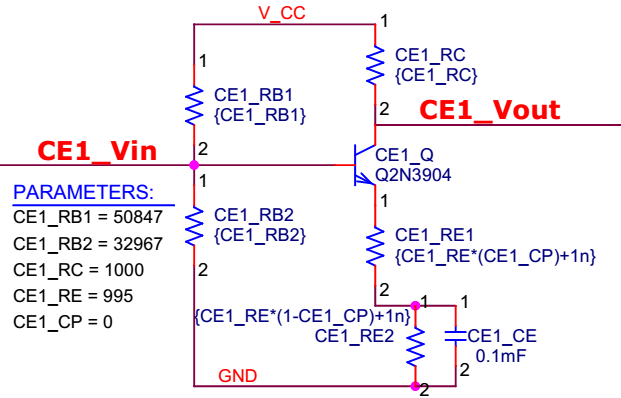


Figure : PSpice circuit of common emitter amplifier.

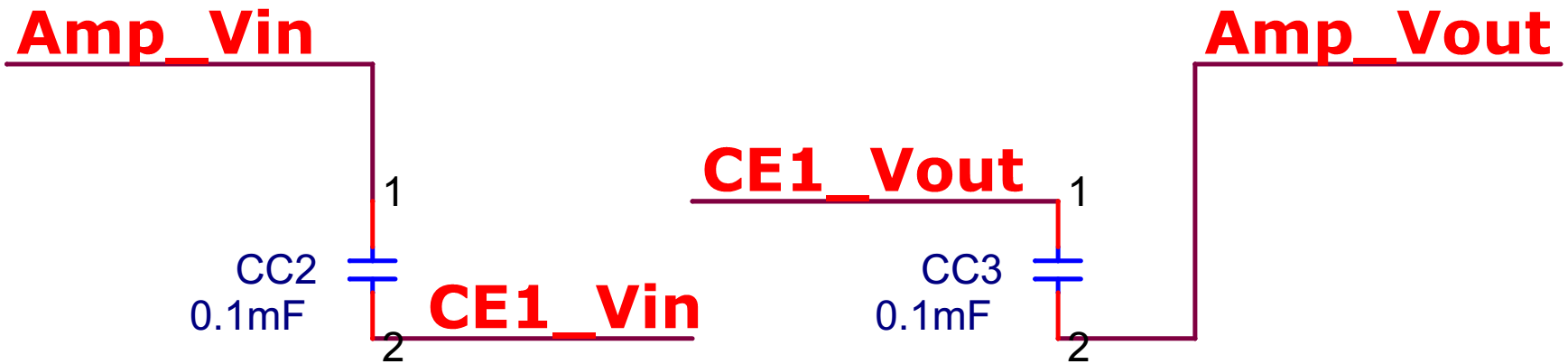


Figure : Initial design for amplifier created in PSpice.

By considering the small signal model, Fig. 5, of this circuit the relationship between the input and output signal can be determined. The closed loop gain of the common emitter amplifier was found to be by using equation (3), handwork for determining this equation is in the appendix.

(3)

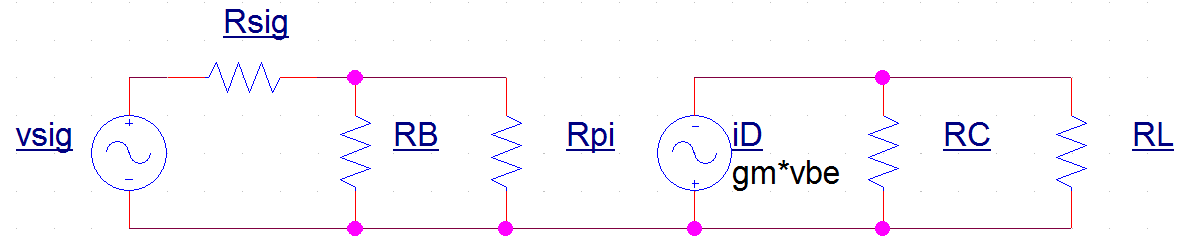


Figure : Small signal model of common emitter amplifier

## Part 2: Improve the design.

*Analyze the input voltage divider and discuss its effect upon the output. Clearly justify the need for an input stage. Design the appropriate input circuit. Show the hand calculations to determine the bias network. This bias network should not include an RC (think about the appropriate R.O.T for this network).*

The expected closed loop gain of the initial design is significantly lower than the expected intrinsic gain of the amplifier (4), . The difference between these gains is that accounts for the voltage drop across . To determine the effect of each resistance the voltage divider is analyzed.

(4)

(5)

In order to decrease the difference between the intrinsic and closed loop gains either the signal’s resistance must decrease or the amplifiers resistances must increase. This is a very common issue in signal amplification and has a well-known solution. The common collector amplifier, also known as a buffer amplifier, has unity gain but has the ability to decrease resistance of the input signal as seen by the following amplifiers.

The bias network was designed to have a current of 10 mA through the emitter and a beta value of 200 was assumed. The design was created so that was divided equally among , and . The handwork to design the bias network for the common collector is included in the appendix but the results are presented in Table 2. The common collector amplifier, Fig. 6, is added to the circuit, Fig. 7, before the common emitter.

Table : Resistances in common collector amplifier.

|  |  |  |  |
| --- | --- | --- | --- |
| Name |  |  |  |
| Value | 1000 | 995 | 50.847 |

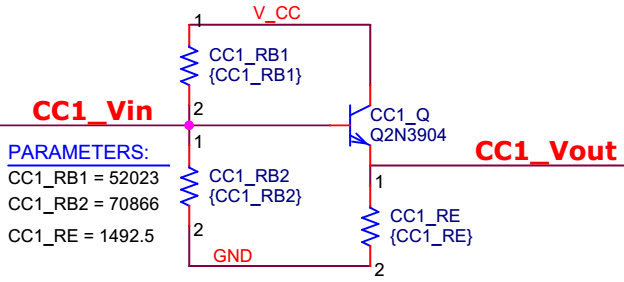


Figure : PSpice circuit of common collector amplifier.

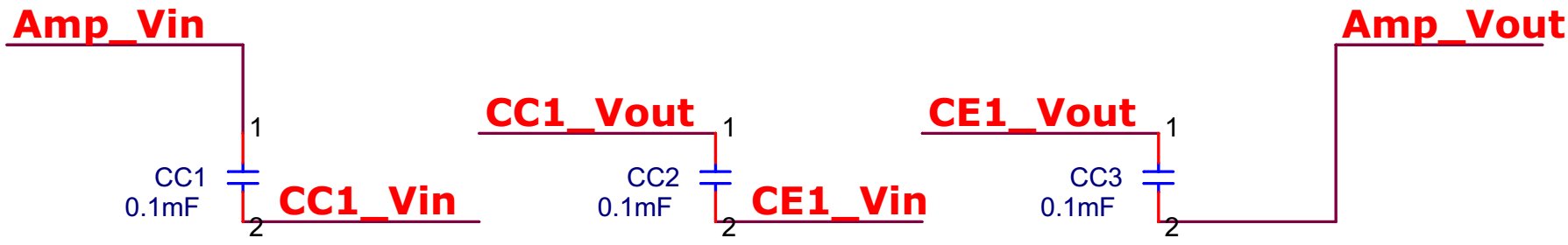


Figure : Second design of amplifier.

## Part 3: Finalize your design.

*You may add 1 more gain stage if you require it. Consider both Vout and Isig.*

The gain of the system is under the specifications. In order to increase the gain a second common emitter was added, Fig. 8, with an identical bias network as the first common emitter, Fig. 6. The bypass capacitor of both common emitters was increase to 10mF to lower , the lower break frequency.

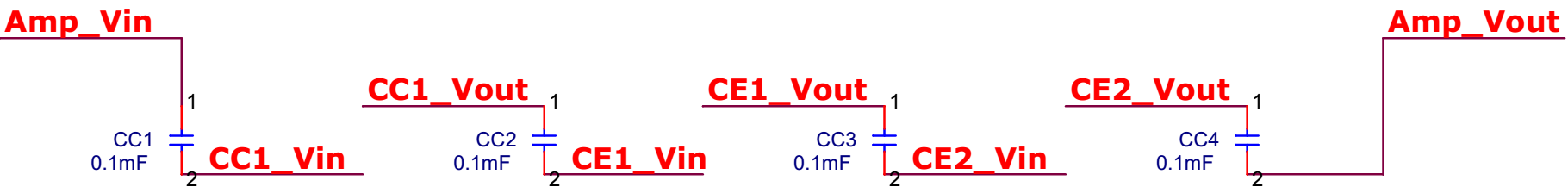


Figure : Third design of amplifier.

## Part 4: Testing your design.

*A 30V power supply is required for this amplifier. You have access to the 120 Vrms, 60Hz wall voltage. To prevent an audible 60Hz noise, the ripple must be less than 40mV. You must minimize the number of diodes used in this design. Capacitor size is of no concern. (The free version of Pspice limits the number of components allowed in a single project. You should design the power supply and amplifier separately. When you are sure they work individually, attempt to integrate the designs.)*

This part of the procedure introduces a new output stage, a new power supply to replace the simulated one, and small changes to parameters of the current amplifiers. The specifications of the design were then examined and modifications were made so that it met the required specifications.

The output stage, Fig. 9, was given to us by Mr. Mettler to solve the issue of a small load resistance. It effectively lowers the output resistance of the amplifier. It is placed at the end of the current amplifier and does not have a coupling capacitor separating it from the output, Fig. 10; note that the resister is required for PSpice but ultimately can be ignored. This improves the amplifier because an ideal amplifier should have very high output resistance just like an ideal source.

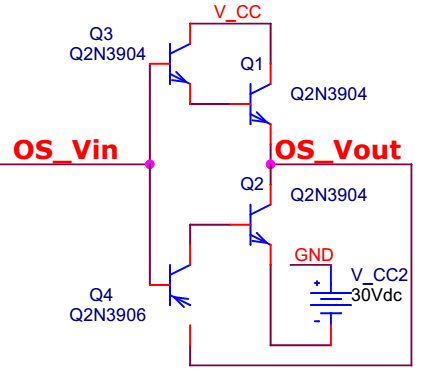


Figure : PSpice circuit of output stage of amplifier.

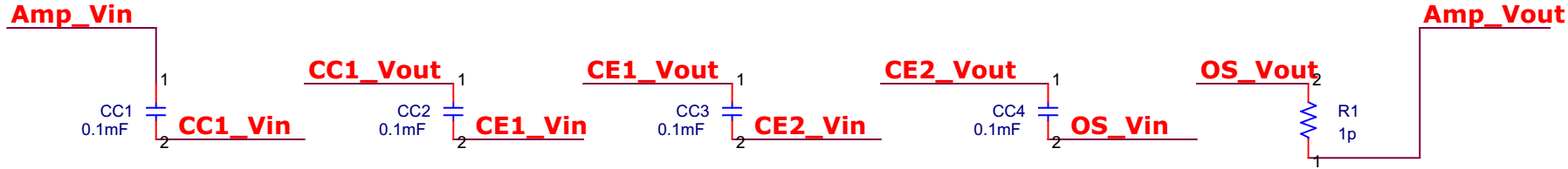


Figure : Fourth design of amplifier.

The power supply should be designed to step down the magnitude of a AC signal and then convert it to a DC voltage. The load of this power supply will be the entire circuit designed in the above work; the thevenin resistance can be found by considering the current draw from . While this would be very complicated to determine analytically it was easily determined by using a PSpice simulation; the value found during part 1 of results and analysis will be used.

The transformer was designed so that the AC signal steps down to a AC signal. This assumes the voltage drop across the diode is negligible. The turns ratio is determined by primary and secondary voltage (6).

(6)

The number of turns required on each side of the transformer can be used to determine the inductance values to use (7). An inductance of was chosen for and then was determined to be .

(7)

The resistance of the rectifier is determined by the load but the capacitance is designed to obtain the desired voltage ripple. The required capacitance to obtain ripple was found to be by using the equation for the half-wave rectifier (8).

(8)

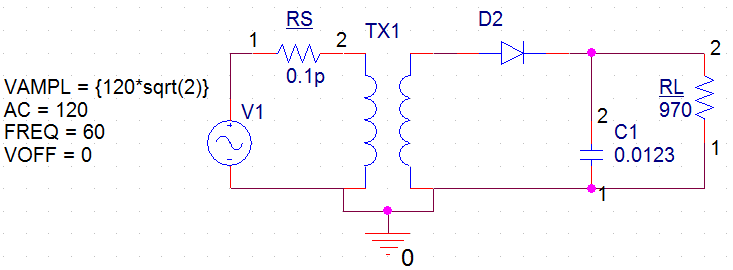


Figure : Designed Voltage source for (30 VDC).

# Results and Analysis

The following sections demonstrate the progression of the signals as the amplifier is improved. The input and output of the amplifier is analyzed as both a function of time and frequency. The results are used to verify the specifications are met.

## Part 1: Initial design.

*Discuss the output with and without RE AC coupled and with RE partially AC coupled. What is the current draw of the simulated source?*

The graphs, Fig. 12 and Fig. 13, of the three voltages (Green),(Blue) and (Red) accurately describe the behavior of the circuit for a 200 Hz and 2000 Hz input signal respectively. A significant drop over causes the amplifier to only receive a portion (blue) of the input signal. There it is a noticeable time shift from the input to the output (red) but this is not a major concern. This circuit had 0% coupling of with AC; coupling is defined as percentage of the common emitter that is not in shunt with a capacitor. The input signal has been attenuated, not amplified, by the amplifier.

It is important to note the difference in the response for the 200Hz input signal and the 2000 Hz input signal. It is clear that the 0.1 mF bypass capacitor is affecting the frequency response of the amplifier. The lower break frequency is too high and is interfering for the lower portion of the desired frequency range.



Figure : Voltage vs time for common emitter amplifier with 200 Hz input signal.



Figure : Voltage vs time for common emitter amplifier with 2000 Hz input signal.

The input and output voltages plotted against frequency provides insight on the gain across a range of frequency, Fig. 14. The input is consistently at (not labeled), but the output is dependent on frequency and is labeled for various AC coupling percentages. It reveals that the gain is less at the lower frequencies; which could prove to be a design flaw. The output voltage of the circuits with some AC coupling of was more consistent for the full range of frequency, from 200 Hz to 2000 Hz. AC Coupling of quickly diminishes the gain; even 2% coupling results in only about a third of the gain as 0% coupling for the higher frequencies.



Figure : Voltage vs Frequency for and with various percent AC coupling on emitter resistance.

The current response was only analyzed for the 200 Hz input, Fig. 15. The current draw from the simulated source was approximately , Fig 15. Considering the voltage of this source is then the thevenin resistance is . The maximum current draw from is , but the load draws .



Figure : Current vs time for 200 Hz input signal.

## Part 2: Improve the design.

Adding the buffer amplifier between the input signal and the common emitter increased the portion of the signal that reaches the common emitter amplifier, Fig. 16. This lead to a significant increase in the gain of the amplifier. The closed loop gain of the amplifier is still significantly less than the required gain.



Figure : Voltage vs time for 2000 Hz input signal.

The percentage of the emitter resistance that is seen by the AC circuit affects the gain of the circuit. The gain is highest for 2000 Hz with no coupling but the gain at lower frequencies is significantly lower, Fig. 17. The circuit with 1% coupling has a relatively consistent gain over the entire frequency range but only slightly higher than a 0.5 gain. The percent coupling can also be used to fine tune the gain of the system.



Figure : Voltage vs Frequency for and with various percent AC coupling on emitter resistance.

The size of the common emitter’s capacitor effects the low break frequency of the amplifier. A parametric sweep of CE reveals that a large value should be used to avoid inconsistent gains at lower frequencies, Fig. 18. This option was overlooked in the early design steps because of a misunderstanding of the constraints; it was assumed that only 0.1mF capacitors could be used. Higher emitter capacitor in shunt with provides a more consistent result across the range of frequency from 200 Hz to 2 kHz because it lowers the break frequency . The next part of the design will introduce a higher capacitance.



Figure : Load voltage vs time for various bypass capacitor values.

## Part 3: Finalize your design.

*Re-analyze the effect of coupling RE on this stage. Explain the effects and justify them with calculations. The load resistor is very small. Discuss what the output resistance must be for a well-designed amplifier. What is the output resistance of your amplifier? We have not discussed the “solution” to this problem; I will provide it to you if you can clearly state what is wrong with your design so far and what you require from the “solution.”*

The load resistance of the designed problem is only ; when compared against the and other resistances in the design it is very small. This becomes an issue since the output resistance of the designed amplifier has a large resistance in parallel with the load, and this causes the load to be supplied with a low percentage of the current. The consequence of the current design would be a power inefficient amplifier and would require higher gain of the input signal. The solution to this problem would be decreasing the output impedance of our amplifier.

The percent of AC coupling on emitter resistance was revisited to observe the effect it has on the multi stage amplifier. The gain was still significantly higher for less percent coupling, Fig. 19 and Fig. 20. The signal is more distorted at the lower frequencies and the 0% coupling no long has the highest gain.



Figure : Voltage vs time for with various percent (0%, 1%, 5%, 7%, 10%) AC coupling on emitter resistance with 2000Hz input.



Figure : Voltage vs time for with various percent (0%, 1%, 5%, 7%, 10%) AC coupling on emitter resistance with 200Hz input..

Clearly there needs to be some AC coupling or there is deformation of the signal, Fig. 21. Comparing the response with 0% and 6% coupling shows that it is more than a clipping of the peaks of the signal. There is a visible narrowing of the sinusoid. The 6% coupling circuit has less gain but the shape of the sinusoid is not distorted, Fig. 22.



Figure : Voltage vs time for 200 and 2000 Hz input signal with 0% RE coupling.



Figure : Voltage vs time for 200 and 2000 Hz input signal with 6% RE coupling.

## Part 4: Testing your design.

The designed was observed over 10 seconds, Fig. 23. The output contains ripples as large as 100 mV; this indicates that a larger capacitance should be used. The average output voltage was only 28.84 V; this indicates that the transformer’s turn ratio must decrease.

The first design of the voltage source did not meet the specifications, Fig 13. The voltage on the secondary side of the transformer was lower than desired; this can be attributed to the efficiency of the transformer. Reasons for this inefficiency are Eddy currents, hysteresis loss, heating, and flux transport failure. The primary inductance was increased slightly to account for this.

The turns ratio was adjusted until the voltage was 30 VDC; the inductance on the primary side was . The power supply ripple was improved by increasing the capacitance; there was significant ripple in the output and so the capacitance increases significantly. A capacitance of was chosen because it achieved slightly under ripple; it was desired to exceed the specification, Fig. 24. There was little effect of using too large of a capacitance, but the transient response does take longer.



Figure : Voltage vs time for first design of voltage source, C=12.3mF, =320 H.



Figure : Voltage vs time for second design of voltage source, C=500mF, =300 H.

The voltage at the load was observed as the value of percent coupling was finely modified until the desired specifications were met, Fig. 25. The value of achieved a peak voltage of 6.98 V for 200 Hz and 7.05 for 2000 Hz. This was the first major requirement of the design.



Figure : Voltage vs Time for 6.6% RE coupled circuit and the min max specifications for Vpeak.

The next constraint required that the current from be less than . The circuit currently draws 1.8, Fig. 26; this can be reduced by increasing the bias resistors used for the common collector amplifier. Currently the resistances are and; the voltage divider created by them must output the same resistance. After observing the effect on current and fine tuning the parameters, the values of and were chosen. These resistances result in peak currents of 1.43 for , Fig. 27. This change caused the peak output voltage for 200 Hz input to rise to 7.113 V, and so the coupling percent was increased slightly to accommodate.



Figure : Current of vs time for original current collector resistances.



Figure : Current of vs time, after increasing bias resistors.

After both portions of the circuit had been successfully tested individually – they were combined. The output voltage of the source decreased slightly to around 29.6 V. The gain observed in the amplifier circuit was much larger. It exceeded the desired by a factor of 10.

The transient portion of the source’s signal had a significant effect on the amplifier circuit. When the signals are observed over a large period of time there is a definite trend. This shows that analyzing the circuit in the first 10 seconds would result in different results then minutes later. This would be a fatal design flaw in any audio amplifier; the transient portion of the signal would have to be decreased.



Figure : Voltage across load vs time during the transient portion of the source.

# Conclusion

The amplifier designed for the specified problem started with a single stage common emitter amplifier. A buffer amplifier was added at the beginning so that the high resistance of did not negatively affect the gain. The gain of the system was still lower than required and so another common emitter was added. The output signal had noticeable “clipping” or limiting of the peaks of the signal, but this was fixed by increasing the fraction of the emitter resistance that is not in parallel with the capacitor. The stacked Darlington array was added to deal with the issue of a small load resistance.

The design did not succeed in meeting all the required specs. The way the PSpice design was constructed made it very easy to jump in-between the four parts mentioned above (Screen-shots are included in the appendix. The current that was sourced by was very hard to measure; it may have been better to consider the power draw from each component individually.

# Appendix - Handwork

## Part 1: Initial design.

### Show the hand calculations to determine the bias (DC) network.

was chosen to be the test condition’s current which was used to determine the range of beta from 100 to 300. A value of 200 was used for beta in all calculations. The equations below were used as the exact steps from lecture were followed. Calculations were performed in Matlab.

function [bias] = create\_ce\_bias\_network(V\_CC, I\_CQ, beta )

% 1. Consider that the voltage V\_CC is divided equally.

V\_RC = V\_CC / 3;

V\_CE = V\_CC / 3;

V\_RE = V\_CC / 3;

% 2. Use beta and I\_CQ to find I\_EQ:

I\_EQ = I\_CQ \* ((beta +1)/beta);

% 3. Use V\_RE and I\_EQ to find R\_E:

% Use V\_RC and I\_CQ to find R\_C:

bias.R\_C = V\_RC / I\_CQ;

bias.R\_E = V\_RE / I\_EQ;

% 4. Find thevenin Equivalent Circuit to obtain V\_B

r\_th = bias.R\_E \* (beta+1)/10;

v\_th = r\_th \* (I\_EQ / (beta +1)) + V\_BE + I\_EQ \* bias.R\_E;

% 5. Determine RB1 and RB2

bias.R\_B2 = V\_CC \* (r\_th / (V\_CC-v\_th));

bias.R\_B1 = bias.R\_B2 \* ((V\_CC / v\_th) - 1);

end

### Show the hand calculations to calculate the expected gain (AC).

Find

Relate to

Find the closed loop gain

Find the intrinsic gain

E.f\_A\_vo =@(self) -self.gm \* self.R\_C;

E.f\_A\_v =@(self) -self.gm \*parallel([self.R\_C; self.R\_L]);

E.f\_G\_v =@(self) -self.beta \* parallel([self.R\_C; self.R\_L]) / (self.rsig + (self.beta +1)\*self.R\_E);

## Part 2: Improve the design.

### Show the hand calculations to determine the bias network.

Pick beta and :

Consider that the voltage is divided equally.

Use beta and to find :

Use and to find :

function [bias] = create\_cc\_bias\_network(V\_CC, I\_CQ, beta )

% 1. Consider that the voltage V\_CC is divided equally.

V\_CE = V\_CC / 2;

V\_RE = V\_CC / 2;

% 2. Use beta and I\_CQ to find I\_EQ:

I\_EQ = I\_CQ \* ((beta +1)/beta);

% 3. Use V\_RE and I\_EQ to find R\_E:

bias.R\_E = V\_RE / I\_EQ;

% 4. Find thevenin Equivalent Circuit to obtain V\_B

r\_th = bias.R\_E \* (beta+1)/10;

v\_th = r\_th \* (I\_EQ / (beta +1)) + V\_BE + I\_EQ \* bias.R\_E;

% 5. Determine RB1 and RB2

bias.R\_B2 = V\_CC \* (r\_th / (V\_CC-v\_th));

bias.R\_B1 = bias.R\_B2 \* ((V\_CC / v\_th) - 1);

end

# Appendix - PSpice Simulation

## 

## 

**Scoring Rubric**

#### **20 points --** Attendance:

#### (1) Attended on time: 100%

(2) Attended, but was late: 80%

(3) Made up lab due to an excused absence: 80%

#### **10 points --** Introduction:

#### Accurate, exceptional writing: 100%

#### Accurate, well written: 90%

#### Attempted, complete, but 1 inaccuracy: 70%

#### Attempted, not complete or accurate: 40%

#### **20 points –** Procedure:

* + - * 1. Accurate, exceptional writing, thoughtful personal investigation: 100%
        2. Accurate, well written, thoughtful personal investigation: 90%
        3. Accurate, well written, includes personal investigation: 80%
        4. Accurate, well written, does not include personal investigation: 65%
        5. Attempted, poorly written or inaccurate, no personal investigation: 50%

#### **40 points –** Results/Analysis:

#### Worked out in completion, accurate, exceptional writing: 100%

#### Worked out in completion, accurate, well written: 90%

#### Worked out in completion, almost accurate: 70%

#### Attempted, not complete or accurate: 40%

#### **10 points –** Conclusion:

#### Worked out in completion, accurate: 100%

#### Worked out in completion, almost accurate: 70%

#### Attempted, not complete or accurate: 40%

Total:

**Scoring Rubric to be used 3 times by the instructor**

#### Report Format:

#### (1) Follows guidelines exactly, no mistakes: +2

(2) Follows guidelines, but a few mistakes: -2

(3) Did not follow guidelines or lots of mistakes: -5

Guidelines refers to verb tense, use of first person, and data formatting

#### Grammar, punctuation:

#### No Mistakes: +2

#### Three or fewer minor mistakes: 0

#### Between 3 and 5 minor mistakes or 1 significant mistake: -2

#### More than 1 significant mistake or more than 5 minor mistakes: -5

#### Quality of writing:

#### No significant critiques: +2

#### Between 1 – 3 critiques: 0

#### Between 3 – 5 critiques: -2

#### More than 5 critiques: -5