# ESP32-S2-WROOM & ESP32-S2-WROOM-I

**Datasheet** 



## **About This Document**

This document provides the specifications for the ESP32-S2-WROOM and ESP32-S2-WROOM-I module.

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### 1. Module Overview

#### 1.1 Features

#### MCU

- ESP32-S2 embedded, Xtensa<sup>®</sup> single-core 32-bit LX7 microprocessor, up to 240 MHz
- 128 KB ROM
- 320 KB SRAM
- 16 KB SRAM in RTC

#### Wi-Fi

- 802.11 b/g/n
- Bit rate: 802.11n up to 150 Mbps
- A-MPDU and A-MSDU aggregation
- 0.4 μs guard interval support
- Center frequency range of operating channel:
   2412 ~ 2484 MHz

#### Hardware

- Interfaces: GPIO, SPI, LCD, UART, I<sup>2</sup>C, I<sup>2</sup>S, Camera interface, IR, pulse counter, LED PWM, USB OTG 1.1, ADC, DAC, touch sensor, temperature sensor
- 40 MHz crystal oscillator
- 4 MB SPI flash
- Operating voltage/Power supply: 3.0 ~ 3.6 V
- Operating temperature range: -40 ~ 85 °C
- Dimensions: (18 × 31 × 3.3) mm

#### Certification

Green certification: RoHS/REACH

• RF certification: FCC/CE-RED/SRRC

#### Test

• HTOL/HTSL/uHAST/TCT/ESD

## 1.2 Description

ESP32-S2-WROOM and ESP32-S2-WROOM-I are two powerful, generic Wi-Fi MCU modules that have a rich set of peripherals. They are an ideal choice for a wide variety of application scenarios relating to Internet of Things (IoT), wearable electronics and smart home.

ESP32-S2-WROOM comes with a PCB antenna, and ESP32-S2-WROOM-I with an IPEX antenna. They both feature a 4 MB external SPI flash. The information in this datasheet is applicable to both modules.

The ordering information of the two modules is listed as follows:

Table 1: Ordering Information

Module	Chip embedded	Flash	Module dimensions (mm)
ESP32-S2-WROOM (PCB)	ESP32-S2	4 MB	(18.00±0.15)×(31.00±0.15)×(3.30±0.15)
ESP32-S2-WROOM-I (IPEX)	L3F32-32	4 1010	(10.00±0.13)×(31.00±0.13)×(3.30±0.13)

#### Notes:

- 1. These modules can be shipped with different flash sizes.
- 2. Modules that operate at higher temperature (-40 °C ~+105 °C) are available for order, embedded with 4 MB flash.
- 3. For dimensions of the IPEX connector, please see Section 7.3.

At the core of this module is ESP32-S2 \*, an Xtensa® 32-bit LX7 CPU that operates at up to 240 MHz. The chip has a low-power co-processor that can be used instead of the CPU to save power while performing tasks that do not require much computing power, such as monitoring of peripherals. ESP32-S2 integrates a rich set of peripherals, ranging from SPI, I²S, UART, I²C, LED PWM, LCD, Camera interface, ADC, DAC, touch sensor, temperature sensor, as well as up to 43 GPIOs. It also includes a full-speed USB On-The-Go (OTG) interface to enable USB communication.

#### Note:

\* For more information on ESP32-S2, please refer to ESP32-S2 Datasheet.

## 1.3 Applications

- Generic Low-power IoT Sensor Hub
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- Over-the-top (OTT) Devices
- USB Devices
- Speech Recognition
- Image Recognition
- Mesh Network
- Home Automation
- Smart Home Control Panel

- Smart Building
- Industrial Automation
- Smart Agriculture
- Audio Applications
- Health Care Applications
- Wi-Fi-enabled Toys
- Wearable Electronics
- Retail & Catering Applications
- Smart POS Machines

## **Contents**

<b>1</b> 1.1 1.2 1.3	Module Overview Features Description Applications	3 3 4
2	Block Diagram	8
<b>3</b> 3.1 3.2 3.3	Pin Definitions Pin Layout Pin Description Strapping Pins	9 9 10 11
<b>4</b> 4.1 4.2 4.3 4.4 4.5	Electrical Characteristics  Absolute Maximum Ratings  Recommended Operating Conditions  DC Characteristics (3.3 V, 25 °C)  Current Consumption Characteristics  Wi-Fi RF Characteristics  4.5.1 Wi-Fi RF Standards  4.5.2 Transmitter Characteristics  4.5.3 Receiver Characteristics	13 13 13 14 15 15 15
5	Schematics	18
6	Peripheral Schematics	20
<b>7</b> 7.1 7.2 7.3	Physical Dimensions and PCB Land Pattern Physical Dimensions Recommended PCB Land Pattern U.FL Connector Dimensions	21 21 22 23
7.1 7.2	Physical Dimensions Recommended PCB Land Pattern	21 22
7.1 7.2 7.3 <b>8</b> 8.1 8.2 8.3	Physical Dimensions Recommended PCB Land Pattern U.FL Connector Dimensions  Product Handling Storage Condition ESD	21 22 23 24 24 24
7.1 7.2 7.3 <b>8</b> 8.1 8.2 8.3 <b>9</b> 10.1	Physical Dimensions Recommended PCB Land Pattern U.FL Connector Dimensions  Product Handling Storage Condition ESD Reflow Profile	21 22 23 24 24 24

## **List of Tables**

1	Ordering Information	3
2	Pin Definitions	10
3	Strapping Pins	11
4	Absolute Maximum Ratings	13
5	Recommended Operating Conditions	13
6	DC Characteristics (3.3 V, 25 °C)	13
7	Current Consumption Depending on RF Modes	14
8	Current Consumption Depending on Work Modes	14
9	Wi-Fi RF Standards	15
10	Transmitter Characteristics	15
11	Receiver Characteristics	16

# **List of Figures**

1	ESP32-S2-WROOM Block Diagram	8
2	ESP32-S2-WROOM-I Block Diagram	8
3	Module Pin Layout (Top View)	9
4	ESP32-S2-WROOM Schematics	18
5	ESP32-S2-WROOM-I Schematics	19
6	Peripheral Schematics	20
7	Physical Dimensions	21
8	Recommended PCB Land Pattern	22
9	U.FL Connector Dimensions	23
10	Reflow Profile	24

# 2. Block Diagram

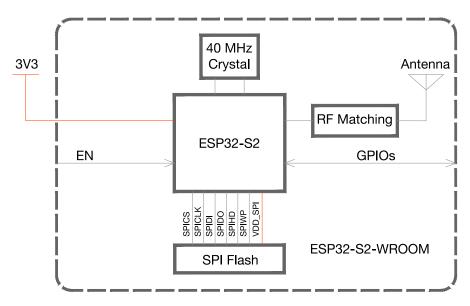


Figure 1: ESP32-S2-WROOM Block Diagram

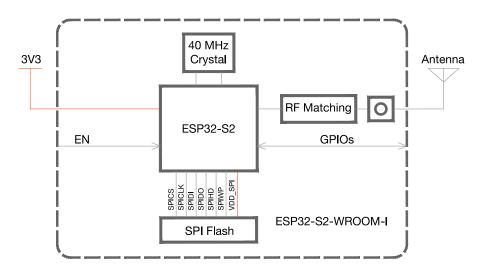


Figure 2: ESP32-S2-WROOM-I Block Diagram

## 3. Pin Definitions

## 3.1 Pin Layout

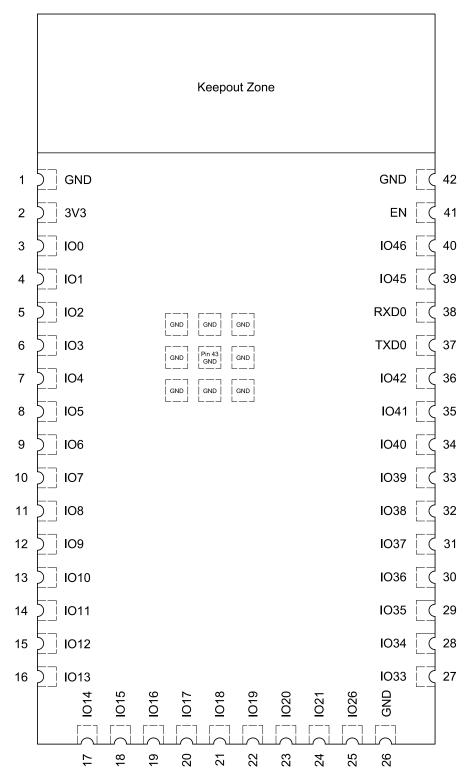


Figure 3: Module Pin Layout (Top View)

#### Note:

The pin diagram shows the approximate location of pins on the module. For the actual mechanical diagram, please refer to Figure 7.1 *Physical Dimensions*.

## 3.2 Pin Description

The module has 42 pins. See pin definitions in Table 2.

Table 2: Pin Definitions

Name	No.	Туре	Function
GND	1	Р	Ground
3V3	2	Р	Power supply
IO0	3	I/O/T	RTC_GPIO0, GPIO0
IO1	4	I/O/T	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
IO2	5	I/O/T	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
IO3	6	I/O/T	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
IO4	7	I/O/T	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
IO5	8	I/O/T	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
106	9	I/O/T	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
107	10	I/O/T	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
IO8	11	I/O/T	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
109	12	I/O/T	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
IO10	13	I/O/T	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
IO11	14	I/O/T	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5
IO12	15	I/O/T	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6
IO13	16	I/O/T	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7
IO14	17	I/O/T	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
IO15	18	I/O/T	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
IO16	19	I/O/T	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
IO17	20	I/O/T	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
IO18	21	I/O/T	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
IO19	22	I/O/T	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
1020	23	I/O/T	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
IO21	24	I/O/T	RTC_GPIO21, GPIO21
IO26	25	I/O/T	SPICS1, GPIO26
GND	26	Р	Ground
IO33	27	I/O/T	SPIIO4, GPIO33, FSPIHD
IO34	28	I/O/T	SPIIO5, GPIO34, FSPICS0
IO35	29	I/O/T	SPIIO6, GPIO35, FSPID
IO36	30	I/O/T	SPIIO7, GPIO36, FSPICLK
IO37	31	I/O/T	SPIDQS, GPIO37, FSPIQ
IO38	32	I/O/T	GPIO38, FSPIWP
1039	33	I/O/T	MTCK, GPIO39, CLK_OUT3

Name	No.	Type	Function
IO40	34	I/O/T	MTDO, GPIO40, CLK_OUT2
IO41	35	I/O/T	MTDI, GPIO41, CLK_OUT1
IO42	36	I/O/T	MTMS, GPIO42
TXD0	37	I/O/T	U0TXD, GPIO43, CLK_OUT1
RXD0	38	I/O/T	U0RXD, GPIO44, CLK_OUT2
IO45	39	I/O/T	GPIO45
IO46	40	I	GPIO46
			High: on, enables the chip.
EN	41	I	Low: off, the chip powers off.
			Note: Do not leave the EN pin floating.
GND	42	Р	Ground

#### Notice:

For peripheral pin configurations, please refer to ESP32-S2 Datasheet.

## 3.3 Strapping Pins

ESP32-S2 has three strapping pins: GPIO0, GPIO45, GPIO46. The pin-pin mapping between ESP32-S2 and the module is as follows, which can be seen in Chapter 5 *Schematics*:

- GPIO0 = IO0
- GPIO45 = IO45
- GPIO46 = IO46

Software can read the values of corresponding bits from register "GPIO\_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

IO0, IO45 and IO46 are connected to the internal pull-up/pull-down. If they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S2.

After reset, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration of the strapping pins.

**Table 3: Strapping Pins** 

VDD_SPI Voltage <sup>1</sup>						
Pin	Default	3.3 V	1.8 V			
IO45 <sup>2</sup>	Pull-down	0	1			

Booting Mode						
Pin	Default SPI Boot Download Boot					
100	Pull-up	1	0			
IO46	Pull-down	Don't-care	0			
Enabling/Disabling ROM Code Print During Booting <sup>3 4</sup>						
Pin	Default	Enabled	Disabled			
IO46	Pull-down	See the fourth note	See the fourth note			

#### Note:

- 1. Firmware can configure register bits to change the settings of "VDD\_SPI Voltage".
- 2. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
- 3. Internal pull-up resistor (R1) for IO45 is not populated in the module, as the flash in the module works at 3.3 V by default (output by VDD\_SPI). Please make sure IO45 will not be pulled high when the module is powered up by external circuit.
- 4. ROM code can be printed over TXD0 (by default) or DAC\_1 (IO17), depending on the eFuse bit.
- 5. When eFuse UART\_PRINT\_CONTROL value is:
  - 0, print is normal during boot and not controlled by IO46.
  - 1 and IO46 is 0, print is normal during boot; but if IO46 is 1, print is disabled.
  - 2 and IO46 is 0, print is disabled; but if IO46 is 1, print is normal.
  - 3, print is disabled and not controlled by IO46.

## 4. Electrical Characteristics

## 4.1 Absolute Maximum Ratings

**Table 4: Absolute Maximum Ratings** 

Symbol	Parameter	Min	Max	Unit
VDD33	Power supply voltage	-0.3	3.6	V
$T_{STORE}$	Storage temperature	-40	85	°C

## 4.2 Recommended Operating Conditions

**Table 5: Recommended Operating Conditions** 

Symbol	Parameter	Min	Тур	Max	Unit
VDD33	Power supply voltage	3.0	3.3	3.6	V
$I_{VDD}$	Current delivered by external power supply	0.5	_		А
Т	Operating temperature	-40	_	85	°C
Humidity	Humidity condition	_	85	_	%RH

## 4.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Тур	Max	Unit
$C_{IN}$	Pin capacitance	_	2	_	рF
$V_{IH}$	High-level input voltage	0.75 × VDD	_	VDD + 0.3	V
$V_{IL}$	Low-level input voltage	-0.3	_	0.25 × VDD	V
$  \cdot  _{IH}$	High-level input current	_	_	50	nA
$I_{IL}$	Low-level input current	_	_	50	nA
$V_{OH}^2$	High-level output voltage	0.8 × VDD	_	_	V
$V_{OL}^2$	Low-level output voltage	_	_	0.1 × VDD	V
1	High-level source current (VDD = $3.3 \text{ V}$ , $\text{V}_{OH} >=$		40		mA
OH	2.64 V, PAD_DRIVER = 3)		10		111/-3
Lor	Low-level sink current (VDD = 3.3 V, $V_{OL}$ =		28		mA
OL	0.495 V, PAD_DRIVER = 3)		20		ША
$R_{PU}$	Pull-up resistor	_	45	_	kΩ
$R_{PD}$	Pull-down resistor	_	45	_	kΩ
$V_{IH\_nRST}$	Chip reset release voltage	0.75 × VDD	_	VDD + 0.3	V
$V_{IL\_nRST}$	Chip reset voltage	-0.3		0.25 × VDD	V

#### Note:

- 1. VDD is the I/O voltage for a particular power domain of pins.
- 2.  $V_{OH}$  and  $V_{OL}$  are measured using high-impedance load.

## 4.4 Current Consumption Characteristics

With the use of advanced power-management technologies, the module can switch between different power modes. For details on different power modes, please refer to Section RTC and Low-Power Management in ESP32-S2 Datasheet.

Table 7: Current Consumption Depending on RF Modes

Work mode	Description		Average	Peak
	TX RX	802.11b, 20 MHz, 1 Mbps, @19.5 dBm	190 mA	310 mA
		802.11g, 20 MHz, 54 Mbps, @15 dBm	145 mA	220 mA
Active (RF working)		802.11n, 20 MHz, MCS7, @13 dBm	135 mA	200 mA
		802.11n, 40 MHz, MCS7, @13 dBm	120 mA	160 mA
		802.11b/g/n, 20 MHz	63 mA	63 mA
		802.11n, 40 MHz	68 mA	68 mA

#### Note:

- The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 50% duty cycle.
- The current consumption figures for in RX mode are for cases when the peripherals are disabled and the CPU idle.

Table 8: Current Consumption Depending on Work Modes

Work mode	Description		Current consumption (Typ)
Modem-sleep	The CPU is powered on	240 MHz	22 mA
		160 MHz	17 mA
		Normal speed: 80 MHz	14 mA
Light-sleep	_		550 μA
Deep-sleep	The ULP co-processor is powered on.		235 μΑ
	ULP sensor-monitored pattern		22 μA @1% duty
	RTC timer + RTC memory		25 μA
	RTC timer only		20 μA
Power off	CHIP_PU is set to low level, the chip is powered off.		1 μΑ

#### Note:

- The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.
- · When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consump-

tion changes accordingly.

- In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.
- During Deep-sleep, when the ULP co-processor is powered on, peripherals such as GPIO and I<sup>2</sup>C are able to operate.
- The "ULP sensor-monitored pattern" refers to the mode where the ULP coprocessor or the sensor works periodically. When touch sensors work with a duty cycle of 1%, the typical current consumption is 22  $\mu$ A.

#### 4.5 Wi-Fi RF Characteristics

#### 4.5.1 Wi-Fi RF Standards

Table 9: Wi-Fi RF Standards

Name		Description	
Center frequency range of operating channel note1		2412 ~ 2484 MHz	
Wi-Fi wireless standard		IEEE 802.11b/g/n	
	20 MHz	11b: 1, 2, 5.5 and 11 Mbps	
Data rate		11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps	
Data rate		11n: MCS0-7, 72.2 Mbps (Max)	
	40 MHz	11n: MCS0-7, 150 Mbps (Max)	
Antenna type		PCB antenna, IPEX antenna	

- 1. Device should operate in the center frequency range allocated by regional regulatory authorities. Target center frequency range is configurable by software.
- 2. For the modules that use IPEX antennas, the output impedance is 50  $\Omega$ . For other modules without IPEX antennas, users do not need to concern about the output impedance.

#### 4.5.2 Transmitter Characteristics

**Table 10: Transmitter Characteristics** 

Parameter	Rate	Тур	Unit
	11b, 1 Mbps	19.5	dBm
	11b, 11 Mbps	19.5	
	11g, 6 Mbps	18	
TX Power note1	11g, 54 Mbps	15	
1771 64761	11n, HT20, MCS0	18	
	11n, HT20, MCS7	13.5	
	11n, HT40, MCS0	18	
	11n, HT40, MCS7	13.5	

1. Target TX power is configurable based on device or certification requirements.

## 4.5.3 Receiver Characteristics

**Table 11: Receiver Characteristics** 

Parameter	Rate	Тур	Unit	
	1 Mbps	-97		
	2 Mbps	-95		
	5.5 Mbps	-93		
	11 Mbps	-88		
	6 Mbps	-92		
	9 Mbps	-91		
	12 Mbps	-89		
	18 Mbps	-86		
	24 Mbps	-83		
	36 Mbps	-80		
	48 Mbps	-76		
	54 Mbps	-74		
	11n, HT20, MCS0	-92		
DV Caraciti it .	11n, HT20, MCS1	-88	-ID:	
RX Sensitivity	11n, HT20, MCS2	-85	dBm	
	11n, HT20, MCS3	-82		
	11n, HT20, MCS4	-79		
	11n, HT20, MCS5	-75		
	11n, HT20, MCS6	-73		
	11n, HT20, MCS7	-72		
	11n, HT40, MCS0	-89		
	11n, HT40, MCS1	-85		
	11n, HT40, MCS2	-83		
	11n, HT40, MCS3	-79		
	11n, HT40, MCS4	-76		
	11n, HT40, MCS5	-72		
	11n, HT40, MCS6	-70		
	11n, HT40, MCS7	-68		
	11b, 1 Mbps	5		
	11b, 11 Mbps	5		
	11g, 6 Mbps	5		
RX Maximum Input Level	11g, 54 Mbps	0	dBm	
TIX Maximum input Level	11n, HT20, MCS0	5	аын	
	11n, HT20, MCS7	0		
	11n, HT40, MCS0	5		
	11n, HT40, MCS7	0		
	11b, 11 Mbps	35		
	11g, 6 Mbps	31		
	11g, 54 Mbps	14		
Adjacent Channel Rejection	11n, HT20, MCS0	31	dB	
	11n, HT20, MCS7	13		

Parameter	Rate	Тур	Unit
	11n, HT40, MCS0	19	
	11n, HT40, MCS7	8	

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## 5. Schematics

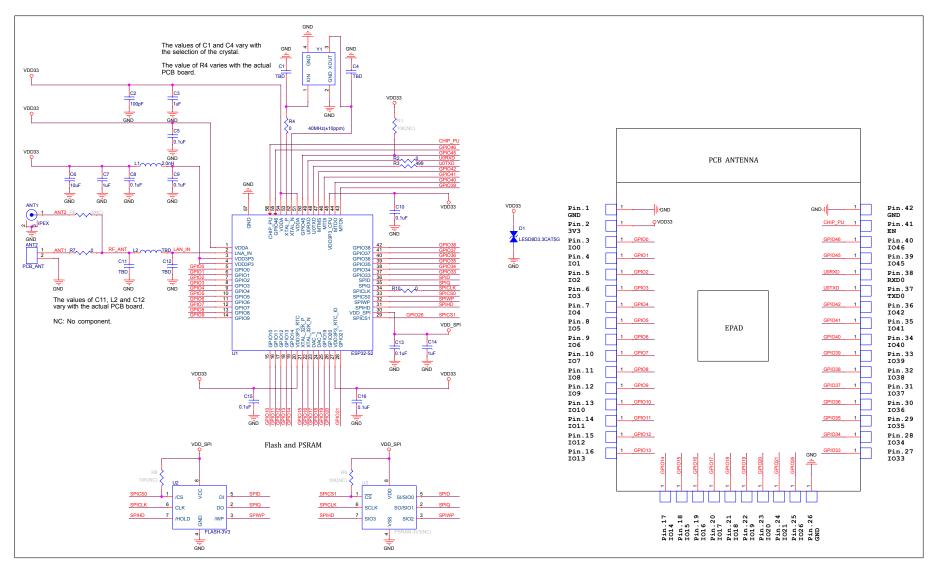


Figure 4: ESP32-S2-WROOM Schematics

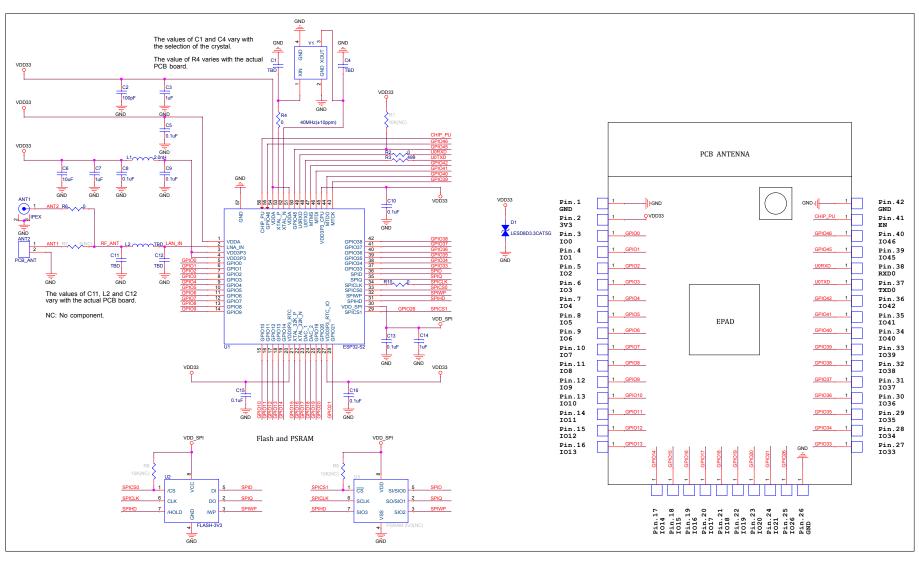


Figure 5: ESP32-S2-WROOM-I Schematics

## 6. Peripheral Schematics

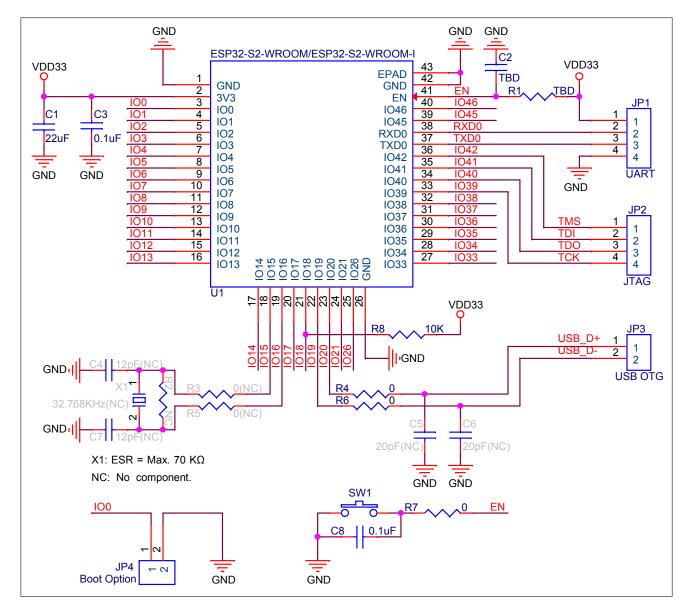


Figure 6: Peripheral Schematics

#### Note:

- Soldering the EPAD to the ground of the base board is not a must, though doing so can get optimized thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.
- To ensure the power supply to the ESP32-S2 chip during power-up, it is advised to add an RC delay circuit at the EN pin. The recommended setting for the RC delay circuit is usually R = 10 k $\Omega$  and C = 0.1  $\mu$ F. However, specific parameters should be adjusted based on the power-up timing of the module and the power-up and reset sequence timing of the chip. For ESP32-S2's power-up and reset sequence timing diagram, please refer to Section *Power Scheme* in *ESP32-S2 Datasheet*.
- GPIO18 works as U1RXD and is in an uncertain state when the chip is powered on, which may affect the chip's entry into download boot mode. To solve this issue, add an external pull-up resistor.

# 7. Physical Dimensions and PCB Land Pattern

## 7.1 Physical Dimensions

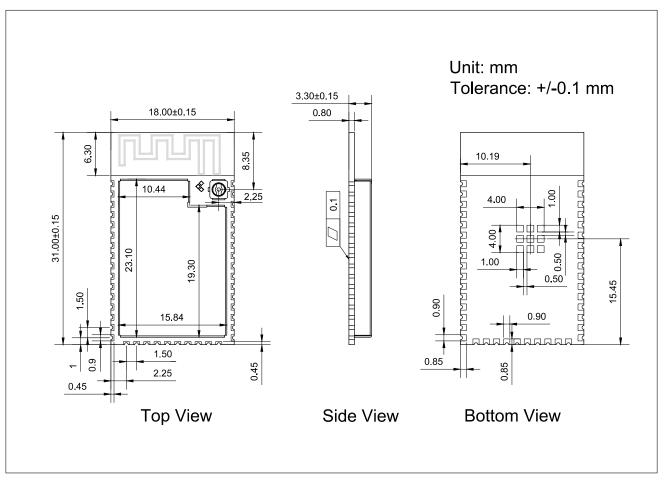


Figure 7: Physical Dimensions

## 7.2 Recommended PCB Land Pattern

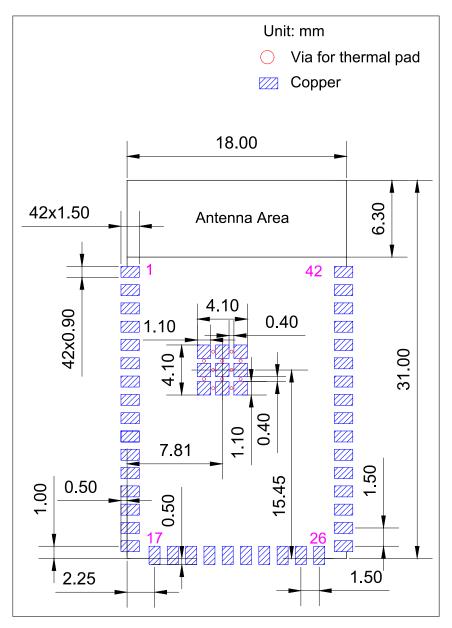


Figure 8: Recommended PCB Land Pattern

## 7.3 U.FL Connector Dimensions

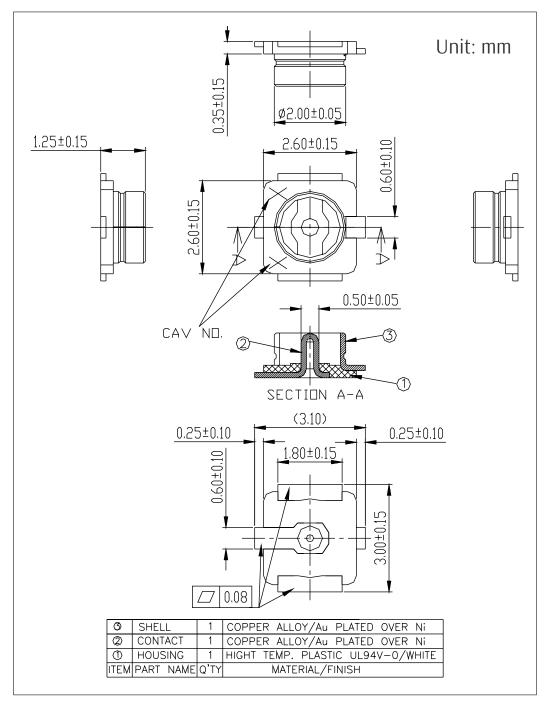


Figure 9: U.FL Connector Dimensions

## 8. Product Handling

## 8.1 Storage Condition

The products sealed in Moisture Barrier Bag (MBB) should be stored in a noncondensing atmospheric environment of < 40 °C/90%RH.

The module is rated at moisture sensitivity level (MSL) 3.

After unpacking, the module must be soldered within 168 hours with factory conditions 25±5 °C and /60%RH. The module needs to be baked if the above conditions are not met.

#### 8.2 **ESD**

• Human body model (HBM): 2000 V

• Charged-device model (CDM): 500 V

• Air discharge: 6000 V

• Contact discharge: 4000 V

#### 8.3 Reflow Profile

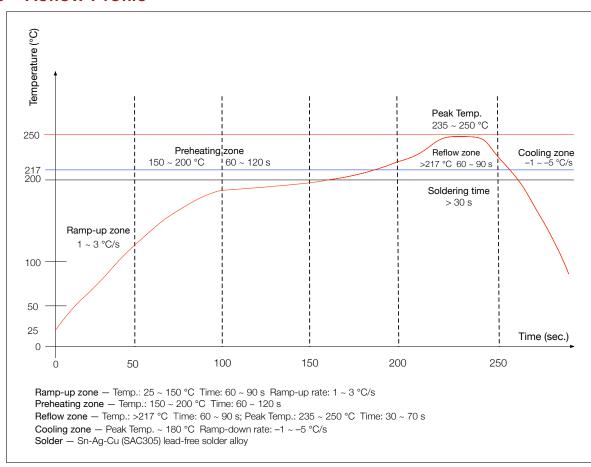


Figure 10: Reflow Profile

#### Note:

Solder the module in a single reflow. If the PCBA requires multiple reflows, place the module on the PCB during the final reflow.

## 9. MAC Addresses and eFuse

The eFuse in ESP32-S2 has been burnt into 48-bit mac\_address. The actual addresses the chip uses in station or AP modes correspond to mac\_address in the following way:

- Station mode: mac\_address
- AP mode: mac\_address + 1

There are seven blocks in eFuse for users to use. Each block is 256 bits in size and has independent write/read disable controller. Six of them can be used to store encrypted key or user data, and the remaining one is only used to store user data.

## 10. Learning Resources

#### 10.1 Must-Read Documents

The following link provides documents related to ESP32-S2.

• ESP32-S2 Datasheet

This document provides an introduction to the specifications of the ESP32-S2 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.

• ESP-IDF Programming Guide

It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.

• ESP32-S2 Technical Reference Manual

The manual provides detailed information on how to use the ESP32-S2 memory and peripherals.

• Espressif Products Ordering Information

#### 10.2 Must-Have Resources

Here are the ESP32-S2-related must-have resources.

• ESP32-S2 BBS

This is an Engineer-to-Engineer (E2E) Community for ESP32-S2 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

# **Revision History**

Date	Version	Release notes
2020-07-31	V1.1	Updated notes in table 1.
2020-06-01	V1.0	Official release.
2020-03-10	V0.5	Preliminary release.