

**ESPRESSIF**

**TRAINING**

Going In-Depth



# Objective

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- Hardware Subsystems
- Software Modules

# Memory Architecture



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- ```
graph TD
    PRO_CPU[PRO_CPU]
    APP_CPU[APP_CPU]
    DMA[DMA]
    EM[Embedded Memory]
    C[Cache]
    MMU[MMU]
    EXM[External Memory]
    P[Peripheral]

    DMA --> EM
    EM <--> C
    C <--> MMU
    MMU --> EXM
    EM <--> PRO_CPU
    EM <--> APP_CPU
    C <--> PRO_CPU
    C <--> APP_CPU
    MMU <--> PRO_CPU
    MMU <--> APP_CPU
    EXM <--> PRO_CPU
    EXM <--> APP_CPU
    P <--> PRO_CPU
    P <--> APP_CPU
```





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# Embedded Memory

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- Internal 448K ROM
  - 1st stage bootloader and ROM libs
- Internal 520K SRAM
  - 192K Instruction SRAM
    - 32K cache memory for *each* core
    - 128K code memory
    - Only 32-bit aligned accesses
  - 328K Data SRAM
    - DMA capable
    - Fastest access





# Embedded Memory

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- RTC Memory
  - RTC fast memory 8K
    - Only PRO CPU accessible
    - Operates on APB clock (80MHz)
    - Retention purpose
  - RTC slow memory 8K
    - Both CPU can access
    - Operates on fast clock (8MHz)
    - ULP execution and retention purpose



# Embedded Memory

| Bus Type         | Boundary Address |              | Size   | Target          | Comment      |
|------------------|------------------|--------------|--------|-----------------|--------------|
|                  | Low Address      | High Address |        |                 |              |
| Data             | 0x3FF8_0000      | 0x3FF8_1FFF  | 8 KB   | RTC FAST Memory | PRO_CPU Only |
|                  | 0x3FF8_2000      | 0x3FF8_FFFF  | 56 KB  | Reserved        | -            |
| Data             | 0x3FF9_0000      | 0x3FF9_FFFF  | 64 KB  | Internal ROM 1  | -            |
|                  | 0x3FFA_0000      | 0x3FFA_DFFF  | 56 KB  | Reserved        | -            |
| Data             | 0x3FFA_E000      | 0x3FFD_FFFF  | 200 KB | Internal SRAM 2 | DMA          |
| Data             | 0x3FFE_0000      | 0x3FFF_FFFF  | 128 KB | Internal SRAM 1 | DMA          |
| Bus Type         | Boundary Address |              | Size   | Target          | Comment      |
|                  | Low Address      | High Address |        |                 |              |
| Instruction      | 0x4000_0000      | 0x4000_7FFF  | 32 KB  | Internal ROM 0  | Remap        |
| Instruction      | 0x4000_8000      | 0x4005_FFFF  | 352 KB | Internal ROM 0  | -            |
|                  | 0x4006_0000      | 0x4006_FFFF  | 64 KB  | Reserved        | -            |
| Instruction      | 0x4007_0000      | 0x4007_FFFF  | 64 KB  | Internal SRAM 0 | Cache        |
| Instruction      | 0x4008_0000      | 0x4009_FFFF  | 128 KB | Internal SRAM 0 | -            |
| Instruction      | 0x400A_0000      | 0x400A_FFFF  | 64 KB  | Internal SRAM 1 | -            |
| Instruction      | 0x400B_0000      | 0x400B_7FFF  | 32 KB  | Internal SRAM 1 | Remap        |
| Instruction      | 0x400B_8000      | 0x400B_FFFF  | 32 KB  | Internal SRAM 1 | -            |
| Instruction      | 0x400C_0000      | 0x400C_1FFF  | 8 KB   | RTC FAST Memory | PRO_CPU Only |
| Bus Type         | Boundary Address |              | Size   | Target          | Comment      |
|                  | Low Address      | High Address |        |                 |              |
| Data Instruction | 0x5000_0000      | 0x5000_1FFF  | 8 KB   | RTC SLOW Memory | -            |



# Memory Architecture: External Memory



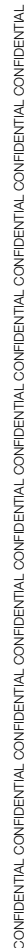
- Supports up-to 16M off-chip SPI flash
- Allows eXecute-In-Place (XIP)
- Accessed using 32K internal cache

- Supports up-to 8M off-chip SPI SRAM
- Can be 10x slower compared with internal memory when accessed using cache
- No DMA capability



# External Memory

| Bus Type    | Boundary Address |              | Size     | Target         | Comment        |
|-------------|------------------|--------------|----------|----------------|----------------|
|             | Low Address      | High Address |          |                |                |
| Data        | 0x3F40_0000      | 0x3F7F_FFFF  | 4 MB     | External Flash | Read           |
| Data        | 0x3F80_0000      | 0x3FBF_FFFF  | 4 MB     | External SRAM  | Read and Write |
| Bus Type    | Boundary Address |              | Size     | Target         | Comment        |
|             | Low Address      | High Address |          |                |                |
| Instruction | 0x400C_2000      | 0x40BF_FFFF  | 11512 KB | External Flash | Read           |





# Memory Speed

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- **Embedded Memory**
  - ROM/SRAM clocked at CPU frequency, single cycle access possible
  - RTC fast memory clocked at APB clock (80MHz)
  - RTC slow memory from fast clock (8MHz)
  - Upto 400 Mbyte/s for memcpy operation
- **DMA uses APB clock to access memory**
- **External Flash/SPIRAM at 40/80 MHz**
  - Dual/Quad mode of operation for flash
  - Upto 32 Mbyte/s for memcpy operation for SPIRAM



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# Security Architecture





# Security Overview

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- eFUSE/OTP
- Secure Boot
- Flash Encryption
- Considerations



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# **Security Architecture : eFUSE/OTP**



## eFUSE/OTP

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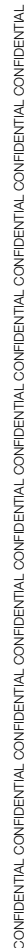
- The eFUSE can be used to program certain information into the SoC
- By default all bits of the eFUSE are 1. Once a bit is flipped to 0, it cannot go back to 1.
- Only software running on the ESP32 can program the eFUSE
- Parts of the eFUSE can even be locked from read-out or writes by the software

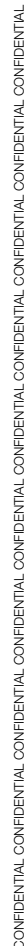




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# **Security Architecture : Secure Boot**







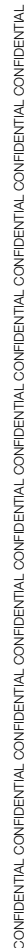
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# Security Architecture : Flash Encryption





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# **Security Architecture : UART Download**



# UART Download

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- Strap pins can trigger UART download mode of ESP32 to be triggered
- This mode can be triggered even when Secure Boot and Flash Encryption are enabled
- Can execute code on MCU, but cannot decrypt flash, or tamper with the firmware





# Firmware Anatomy and Boot-up



# Flash Layout

Fixed

|   |                           |          |
|---|---------------------------|----------|
| { | Secure boot IV and Digest | — 0x0000 |
|   | 2nd Stage Boot Loader     | — 0x1000 |
|   |                           | — 0x8000 |
|   | Partition Table           | — 0x9000 |

User Defined  
(Partition Table)

|   |                       |
|---|-----------------------|
| { | NVS                   |
|   | OTA Data              |
|   | App Slot 0            |
|   | App Slot 1            |
|   | NVS (mfg)             |
|   | Filesystem (Optional) |

| Name    | Type | Sub-type | Offset  | Size     | Flags |
|---------|------|----------|---------|----------|-------|
| nvs     | data | nvs      | 0x9000  | 0x4000   |       |
| otadata | data | ota      | 0xd000  | 0x2000   |       |
| ota_1   | app  | ota_1    | 0x10000 | 0x180000 |       |
| ota_2   | app  | ota_2    | 0x19000 | 0x180000 |       |
| mfg     | data | nvs      | 0x31000 | 0x4000   |       |

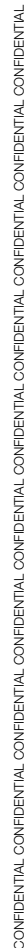


# Flash Components

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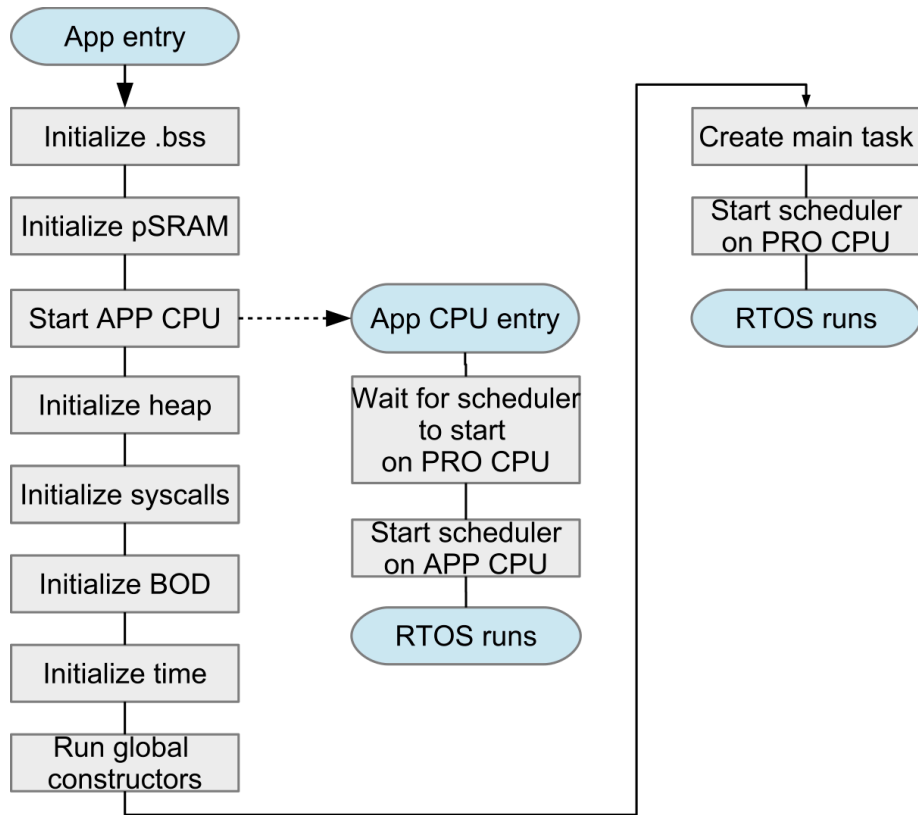
- NVS
  - Non-volatile storage for configuration data
- OTA Data
  - Used internally by the OTA module to identify the latest active partition
- App Slot 0 and 1
  - Active-Passive partition for OTA updates
- NVS (Mfg) (Optional)
  - NVS partition for manufacturing data





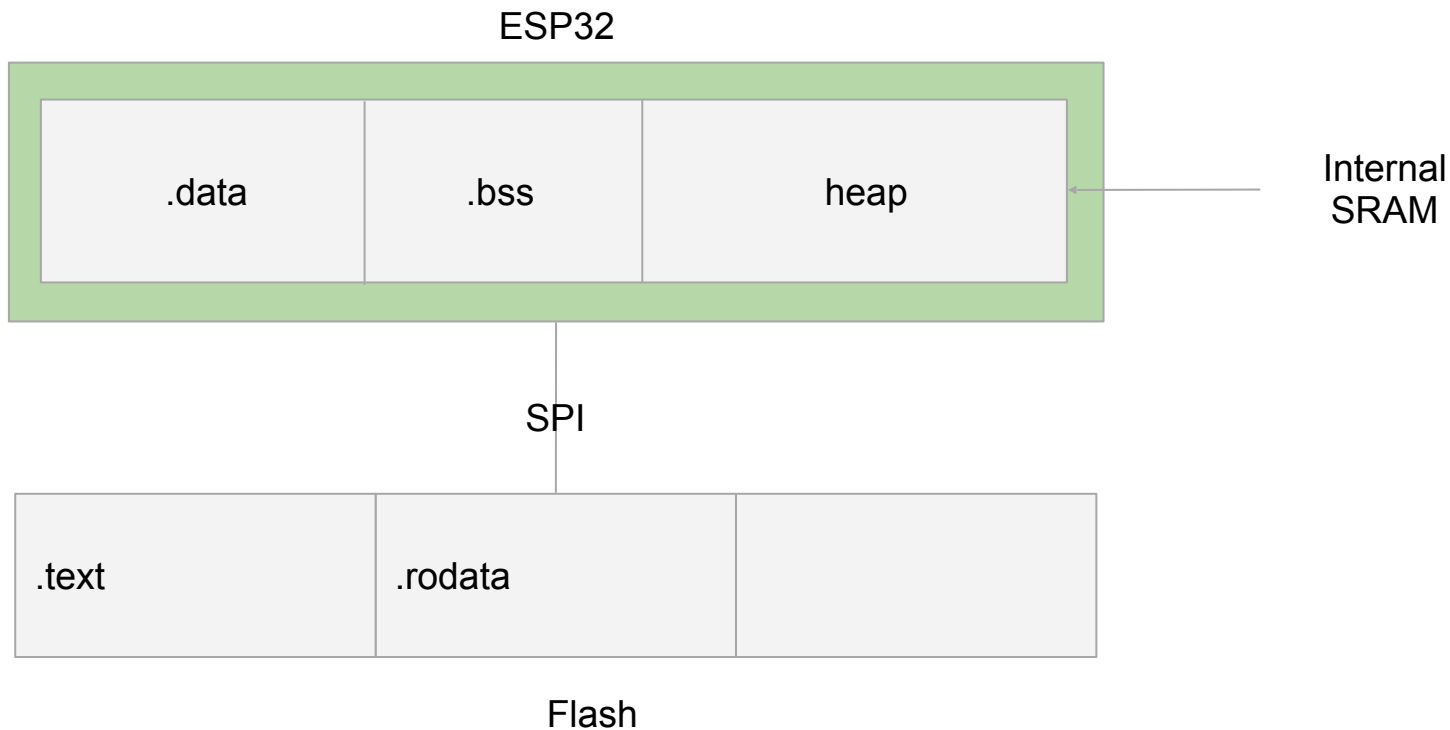


# Application Startup Flow





# Memory Layout during execution





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# Storage



# Storage Overview

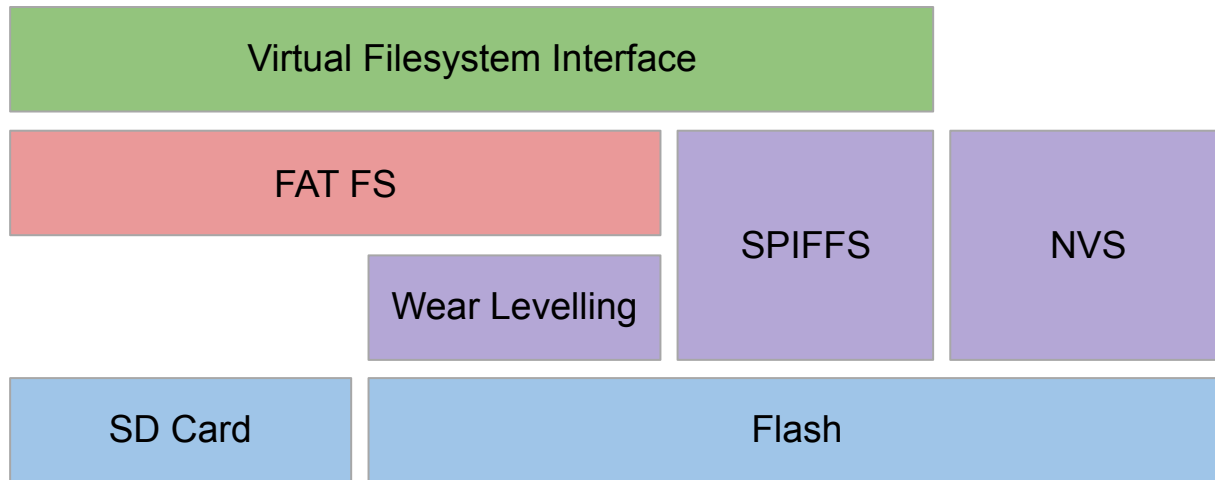
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- NVS
- Virtual File System Interface
- FAT
- SPIFFS
- SD Card
- Wear Levelling



# Storage Options

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- Key-Value store in flash
- Power loss resilient
- Wear-levelling: Log based structure
- Support namespaces
- Used for: Manufacturing settings, User's configuration, Maintaining state across resets



- ChaN's FATFS library R0.12b (to be updated to R.013)
  - [http://elm-chan.org/fsw/ff/00index\\_e.html](http://elm-chan.org/fsw/ff/00index_e.html)
- Works on SD Card or Wear-Levelling Driver





# SPIFFS

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- SPIFFS is a popular filesystem used in many ESP8266 based projects
  - <https://github.com/pellepl/spiffs>
- Flat filesystem
- Not compatible with flash encryption
- Supports filesystem image sizes from 64KB upwards





# Networking Overview

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- Application Protocols:
  - HTTP (Server, Client),
  - HTTP2 Client,
  - MQTT Client
  - mDNS/DNS-SD Bonjour
  - COAP (Server, Client)
- TLS (Transport Layer Security)
- LWIP
- Wi-Fi
- Bluetooth
- Ethernet



# LWIP

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Light Weight IP ([http://www.nongnu.org/lwip/2\\_1\\_x/index.html](http://www.nongnu.org/lwip/2_1_x/index.html))

- Modified with ESP's patches
- TCP/UDP, IPv4/v6, DHCP, ICMP, IGMP
- BSD Socket API



# Networking: Wi-Fi



# Wi-Fi Features

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- 802.11b/g/n
- Modes: Station, SoftAP, Promiscuous, Simultaneous (STA & SoftAP)
- Security: WPA/WPA2/WPA2-Enterprise, WPS
- 802.11-compliant power management
- Adaptive rate fallback algorithm
- Antenna diversity
- Up to 20 Mbps TCP and 30Mbps UDP OTA throughput





# Typical Wi-Fi Programming Sequence

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- Initialize Wi-Fi stack using *esp\_wifi\_init* API
  - Allocates internal structures, buffers
  - Registers an event handler and starts wifi task
- Set mode using *esp\_wifi\_set\_mode* API
  - STA, AP, STA + AP
- Set mode specific configuration using *esp\_wifi\_set\_config* API
  - SSID, Password, Beacon Interval, Channel etc
- Start WiFi using *esp\_wifi\_start* API as per previous config
- Perform mode specific operations and handle events
  - For example, start STA scan using *esp\_wifi\_scan\_start* and handle *SYSTEM\_EVENT\_SCAN\_DONE*
- Stop and deinit wifi using *esp\_wifi\_stop* & *esp\_wifi\_deinit* APIs





# Wi-Fi Protocol Modes

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- Call `esp_wifi_set_protocol` to set any of the following Wi-Fi protocol modes
  - 802.11 B
  - 802.11 BG
  - 802.11 BGN
  - 802.11 BGNLR
  - 802.11 LR
- 802.11 LR
  - This mode is an Espressif-patented mode which can achieve a one-kilometer line of sight range.

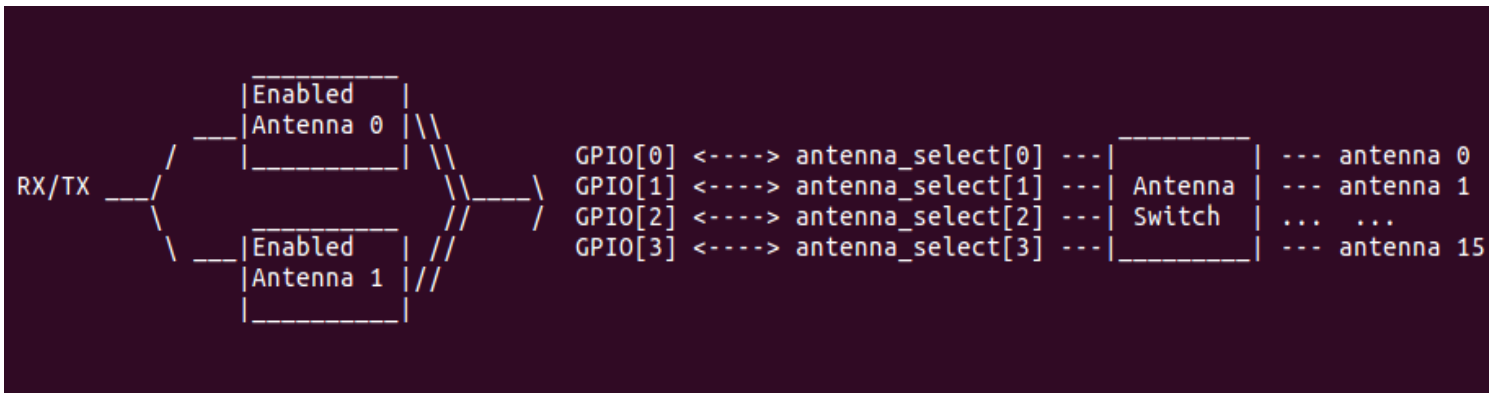


# Wi-Fi Channel & Tx Power Management

- Call `esp_wifi_set_country` to set the country code which limits the channel range. The following policies can be configured.
  - `WIFI_COUNTRY_POLICY_AUTO`
    - When connected, the country info of the AP to which the station is connected is used.
    - When not connected, the configured country info is used.
  - `WIFI_COUNTRY_POLICY_MANUAL`
    - Configured country info is used regardless of the connection state
- Max Tx power can be configured by
  - “`menuconfig: component => PHY => Max Wi-Fi TX Power`” to set the default
  - Call `esp_wifi_set_max_tx_power` in the application if the default value is not desirable.
- **Note** - The APIs do not validate the per-country rules. It is up to the user to fill in all fields according to local regulations.



# Wi-Fi Multiple Antennas



- Up to 16 antennas through external antenna switch controlled by 4 address pins
  - antenna\_select[0:3].
- Use **esp\_wifi\_set\_ant\_gpio** to configure which GPIOs are connected to antenna\_selects.
- Only one or two antennas can be simultaneously enabled for RX/TX.
- Use **esp\_wifi\_set\_ant**
  - To configure which antennas are enabled.
  - To configure antenna selection mode (which enabled antenna is used for Tx and Rx)
    - WIFI\_ANT\_MODE\_ANT0, WIFI\_ANT\_MODE\_ANT1, WIFI\_ANT\_MODE\_AUTO



# Wi-Fi Power Saving Modes

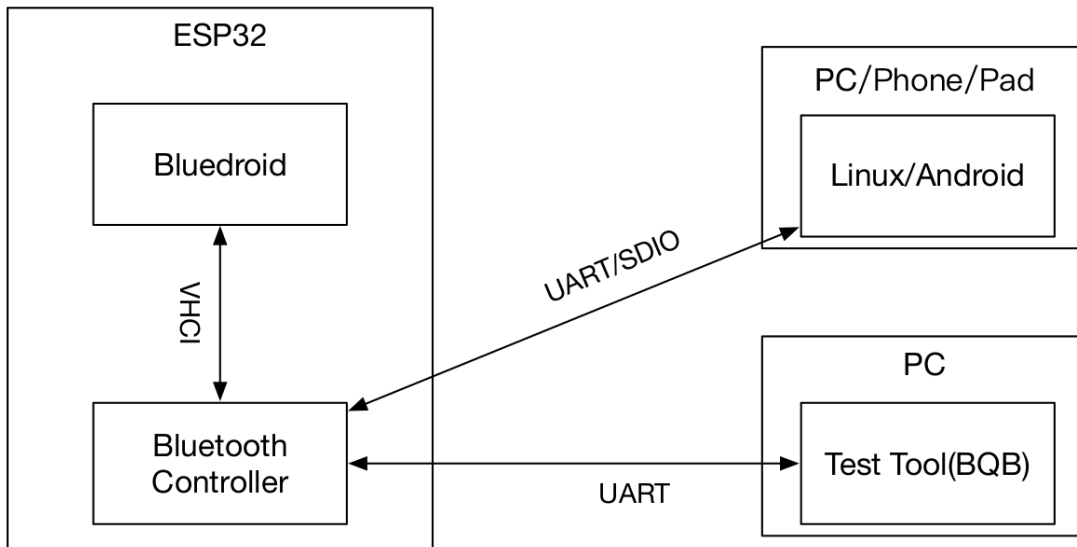
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- Modem-sleep mode
  - Refers to the legacy power-saving mode in the IEEE 802.11 protocol
  - Works in STA only mode
  - When connected to AP STA switches between ACTIVE and SLEEP states
  - In SLEEP state, RF, PHY and BB are turned off in order to reduce power consumption
  - Connection is maintained
  - Current reduces from average ~120mA to ~40mA
- Types of Modem-sleep (chosen using *esp\_wifi\_set\_ps*)
  - WIFI\_PS\_MIN\_MODEM
    - STA wakes up every DTIM
  - WIFI\_PS\_MAX\_MODEM
    - STA wakes up every LISTEN\_INTERVAL configured by *esp\_wifi\_set\_config*





- ESP32 supports dual-mode Bluetooth
- Bluetooth Host and Controller Architecture





# Architecture

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- ESP IDF uses significantly modified Bluedroid as the Bluetooth Host (Classic BT + BLE)
- Layers
  - BTU - Bluetooth Adaptation Layer
  - BTC - Bluetooth Control Layer
  - HCI - Host Controller Interface
- Design Principles
  - Minimize the load on user tasks
  - Streamline the structure by handling over Bluetooth related tasks to the BTC layer



# Classic Bluetooth

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- To exchange large data over a small range
- Applications
  - Wireless Headsets and Speakers
  - Wireless Keyboards and Printers
  - Files transfer
- Supported Profiles
  - GAP, A2DP, AVRCP (CT), SPP, HFP Client





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- Legacy Pairing (v2.0 devices and before)
  - Static Pin Code
- Secure Simple Pairing (v2.1 devices)
  - Just Works
  - Passkey Entry
  - Numeric Comparison



## Cont'd...

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- LE Legacy Pairing (v4.0, 4.1 and 4.2 devices)
  - Just Works
  - Passkey Entry
- LE Secure Connections (v4.2 devices)
  - Just Works
  - Passkey Entry
  - Numeric Comparison



# Bluetooth Mesh

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- Enables many-to-many device communications
- Operates on BLE and is compatible with core specification version 4.0 or higher
- Supported Features
  - Node and Provisioner Roles
  - PB-ADV and PB-GATT Bearers
  - Relay and Proxy support
  - Foundation Models
    - Configuration Server and Client Models
    - Health Server and Client Models



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# Application Protocols

---

- Application Protocols:
  - HTTP (Server, Client),
  - HTTP2 Client,
  - MQTT Client
  - mDNS/DNS-SD Bonjour
  - COAP (Server, Client)
- TLS (Transport Layer Security)



# Thank You!



# Backup







- A2DP Sink
  - Advanced Audio Distribution Profile
  - How multimedia audio can be streamed over a Bluetooth connection
  - Can be used in conjunction with AVRCP for remote control on devices



# Demo - Bluetooth Low Energy

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- BLE Peripheral
  - BLE Advertisement
  - GATT Service - Light (custom)
  - Custom Characteristic - State (custom)
  - Control the light using BLE



- Data transfer speeds upto 2Mbps
- Extended range
- Increased maximum Tx Power
- Increased broadcast message capacity