



NVT TCON Tool User Manual





Outline

- Tool Installation
- FTDI JIG Connection
- TCON Tool User Manual
- Save and Program



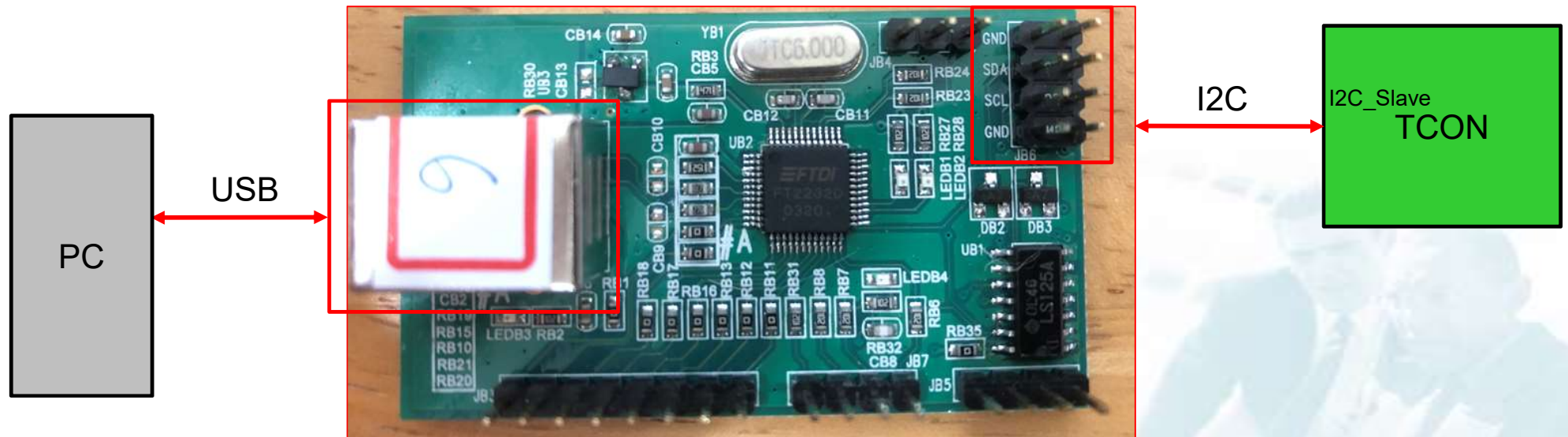


Tool Installation

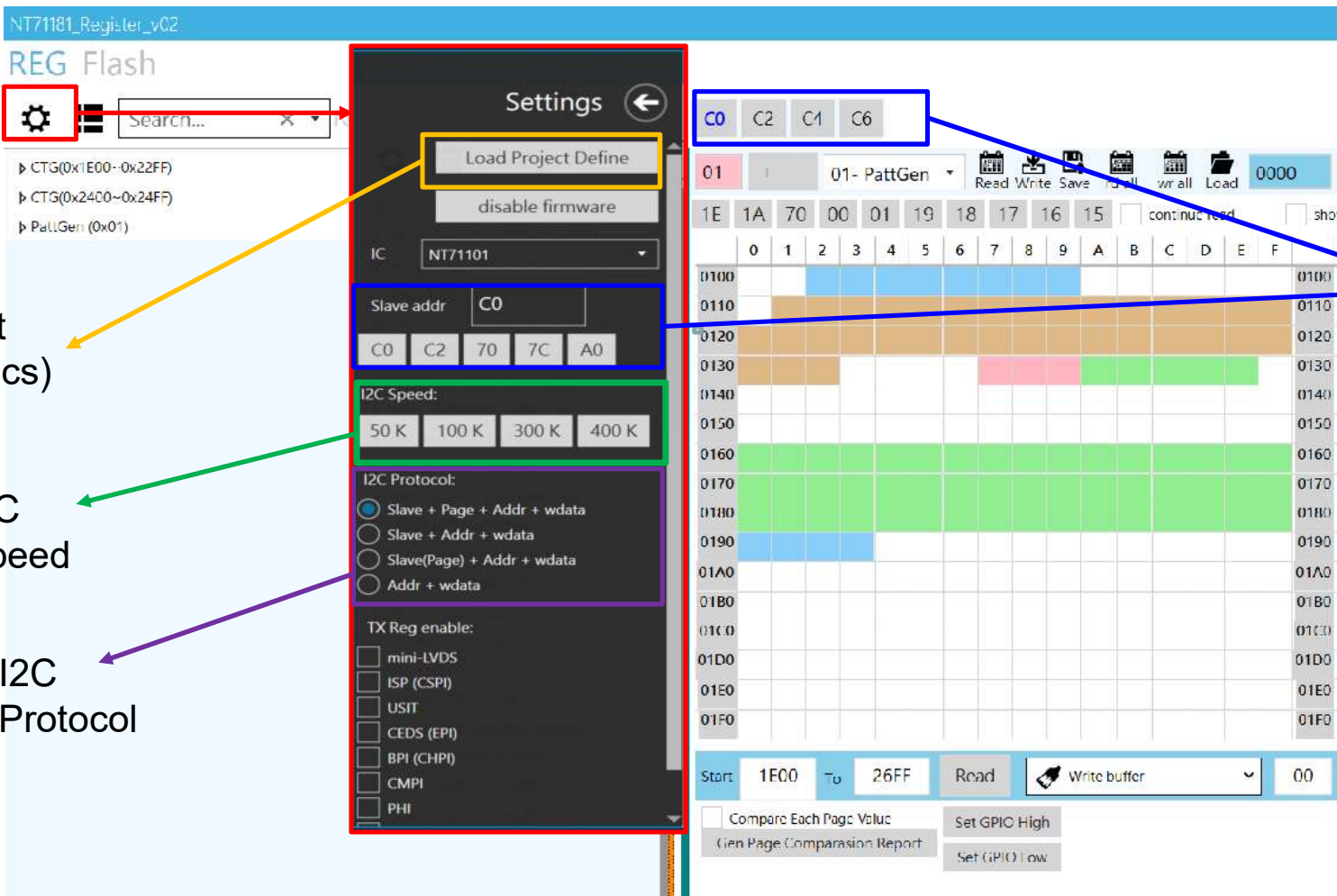
- Install the FTDI JIG Driver “Jig driver (FTDI) / CDM v2.08.30 WHQL Certified.exe”
- Install the TCON TOOL “TCON setup Customer(x64).exe”



FTDI JIG Connection



TCON Tool User Manual - 1



NT71181_Register_v02

REG Flash

Search...

CTG(0x1E00~0x22FF)
CTG(0x24C0~0x24FF)
PattGen (0x01)

Settings

Load Project Define

disable firmware

IC: NT71101

Slave addr: C0

C0 C2 70 7C A0

I2C Speed:
50 K 100 K 300 K 400 K

I2C Protocol:
☒ Slave + Page + Addr + wdata
☐ Slave + Addr + wdata
☐ Slave(Page) + Addr + wdata
☐ Addr + wdata

TX Reg enable:
☐ mini-LVDS
☐ ISP (CSPI)
☐ USIT
☐ CEDS (EPI)
☐ BPI (CHPI)
☐ CMPI
☐ PHI

C0 C2 C1 C6

01 01- PattGen Read Write Save Full wr all Load 0000

1E	1A	70	00	01	19	18	17	16	15	contin read		show value 00		hide table	
0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0100															
0110															
0120															
0130															
0140															
0150															
0160															
0170															
0180															
0190															
01A0															
01B0															
01C0															
01D0															
01E0															
01F0															

Slave Address NVT TCON 0xC0

bit 7
bit 6
bit 5
bit 4
bit 3
bit 2
bit 1
bit 0

decimal 0 + -

Start 1E00 To 26FF Read Write buffer 00

Compare Each Page Value (Gen Page Comparison Report)

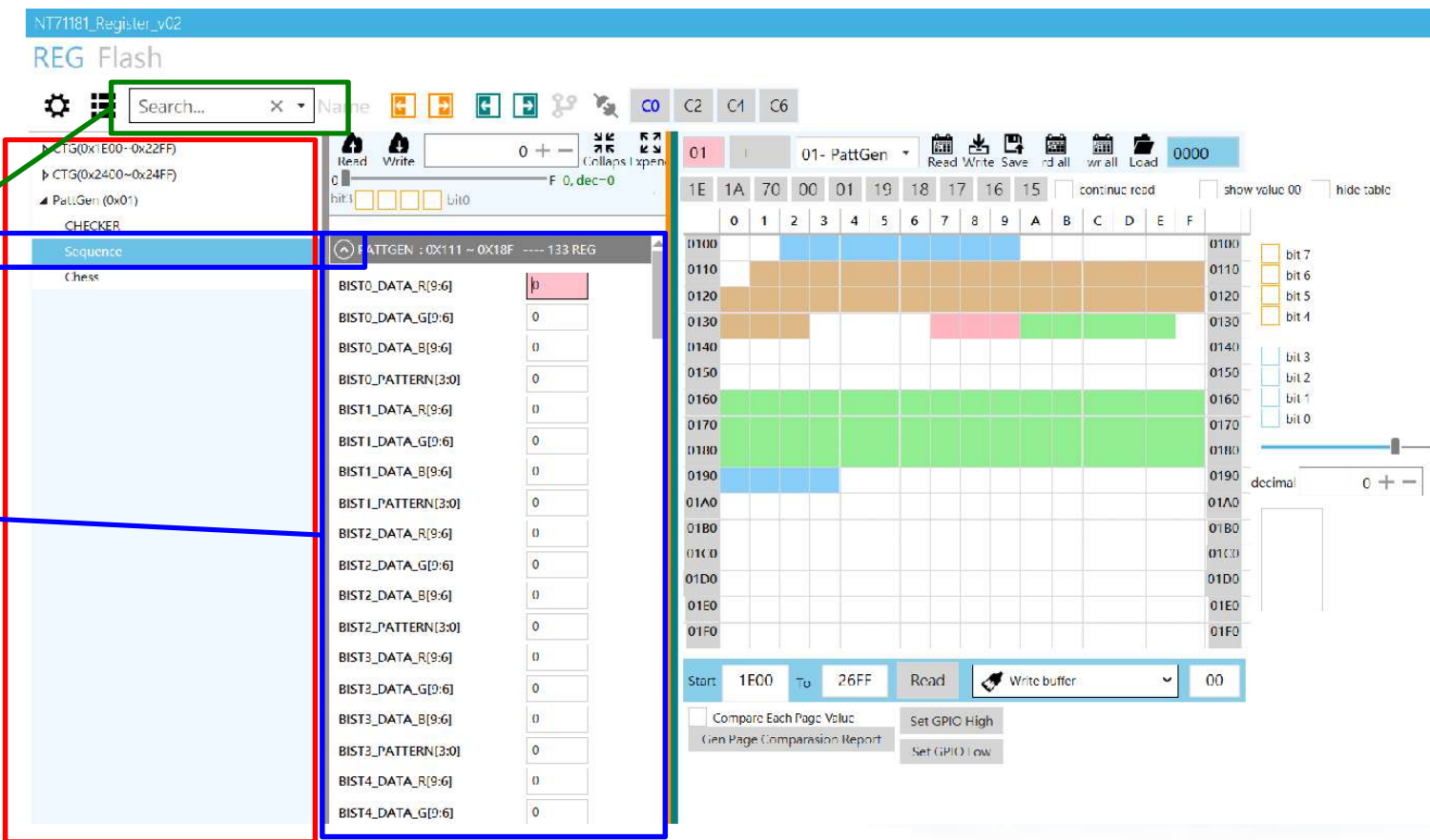
Set GPIO High
Set GPIO Low

Load Project Model File (.cs)

I2C Speed

I2C Protocol

TCON Tool User Manual - 2



The screenshot shows the TCON Tool interface with the following components and annotations:

- Register Search:** Indicated by a green arrow pointing to the search bar at the top left of the interface.
- Register Sub-Group:** Indicated by a blue arrow pointing to the 'Sequence' tab in the left sidebar.
- Register Group:** Indicated by a red arrow pointing to the 'CTG(0x2400~0x24FF)' group in the left sidebar.

The interface displays a list of registers on the left, including:

- CTG(0x1E00~0x22FF)
- CTG(0x2400~0x24FF)
- PattGen(0x001)
- CHECKER
- Sequence
- Chess

The main area shows a detailed view of the 'PattGen' register group, displaying a list of registers and their values:

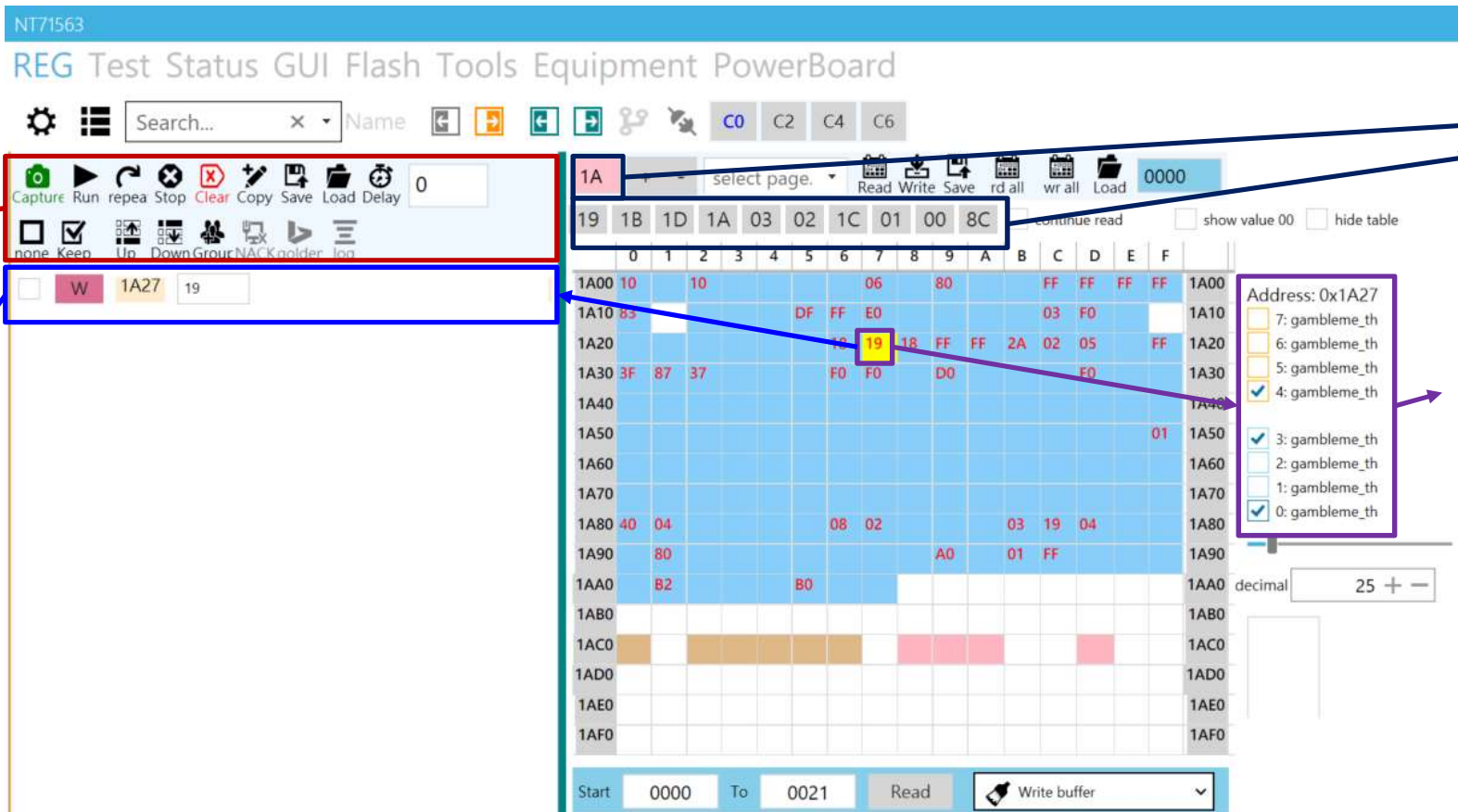
Register Name	Value
BIST0_DATA_R[9:6]	h
BIST0_DATA_G[9:6]	0
BIST0_DATA_B[9:6]	0
BIST0_PATTERN[3:0]	0
BIST1_DATA_R[9:6]	0
BIST1_DATA_G[9:6]	0
BIST1_DATA_B[9:6]	0
BIST1_PATTERN[3:0]	0
BIST2_DATA_R[9:6]	0
BIST2_DATA_G[9:6]	0
BIST2_DATA_B[9:6]	0
BIST2_PATTERN[3:0]	0
BIST3_DATA_R[9:6]	0
BIST3_DATA_G[9:6]	0
BIST3_DATA_B[9:6]	0
BIST3_PATTERN[3:0]	0
BIST4_DATA_R[9:6]	0
BIST4_DATA_G[9:6]	0

The right side of the interface shows a memory map visualization with a grid of addresses and data values. The address range is from 01E00 to 01F00. The data values are displayed in hexadecimal and decimal formats.

TCON Tool User Manual - 3

Macro Manual

Register History



The screenshot shows the TCON Tool interface with the following components and annotations:

- Page Setting:** Indicated by a blue arrow pointing to the 'select page.' dropdown menu.
- Macro Manual:** Indicated by a red arrow pointing to the top toolbar containing icons for Capture, Run, repeat, Stop, Clear, Copy, Save, Load, and Delay.
- Register History:** Indicated by a blue arrow pointing to the 'W' (Write) button and the address '1A27' in the register history list.
- Select Register Show description:** Indicated by a purple arrow pointing to the 'gambleme_th' checkbox in the right-hand panel.

The main display area shows a memory map with addresses from 1A00 to 1AF0. The value at address 1A27 is highlighted in yellow and is '19'.

TCON Tool User Manual - 4

Enter the Modified register to write immediately

Page Read Page Write All Page Read All Page Write

Read Write Save rd all wr all Load 0000

03 02 01 0A 09 00 08 07 3F 0D continue read show value 00 hide table

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0100		10			0F	FF			0F	FF						
0110		FF	FF	0F		FF	88	80			FF	FF	FF	FF	FF	
0120	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	FF	
0130	FF	B4		44			0C	FF								
0140																
0150	0B		FF		FF		FF		FF		FF		FF			
0160	3F	3F	3F		3F			3F								
0170																
0180																
0190					01											
01A0	01	30	FF		03		FF			FF	01	F4	03	E8		
01B0	FF	FF	FF				FF	5A	FF			FF	FF	FF		
01C0			FF	FF	FF			03	FF					01	0F	
01D0	0F	0F	0F	03		FF	03	E8	A1	F4	10		64	32	14	0A
01E0	C8	C8	64	64	10	01	10	05	AF							
01F0																

Address: 0x0111

- ☒ 7: BIST0DATA_R [9]
- ☒ 6: BIST0DATA_R [8]
- ☒ 5: BIST0DATA_R [7]
- ☒ 4: BIST0DATA_R [6]
- ☒ 3: BIST0DATA_G [9]
- ☒ 2: BIST0DATA_G [8]
- ☒ 1: BIST0DATA_G [7]
- ☒ 0: BIST0DATA_G [6]

decimal 255 + -

Start 08A0 To 08AF Read Write buffer 00

Register bit check



Save and Program - 1

Load – Load Flash Rom Code file , It can load these format : .bin 、 .hex 、 .design_hex_rom,
Program/Save – select the file to Program or Save

REG Flash

ISP on Read Program Chip Erase → list register diff

Remove files Load Save ISP slave= C0

Blocks Read Program/Save

☒ read back buffer

☒ NT71181Sharp_2024x2560_Test_20210713_v001.bin

Firmware

2021-07-02, ver= 00.00.01, Checksum= 0x478976

0000 7FFF

Registers

☒ read back buffer

☐ Reg from grid

NT71181Sharp_2024x2560_Test_2021

Reg start_addr	end_addr	offset_addr
0000	FFFF	0000
0000	FFFF	0000
0000	FFFF	0000

CRC= 5F4C

0000 FFFF

LUTs

☐ read back buffer

☐ LUT from grid

NT71181Sharp_2024x2560_Test_2021

Flash start_addr	end_addr	offset_addr
1_8000	3F_FFFF	1_8000
1_8000	3F_FFFF	1_8000
1_8000	6_6FFF	1_8000

01_8000 06_6FFF



Save and Program - 2

Load – load many files once

Load – Load EDID to change the original rom code

REG Flash

ISP on Read Program Chip Erase → list register diff

Remove files Load Save ISP slave= C0

Blocks Read Program/Save

☒ Read back buffer

☒ NT71181Sharp_2024x2560_Test_20210713_v001.bin

☐ NT71181FW_NVT_V253_00_TEST02_20210310.bin

2021-07-02, ver= 00.00.01, Checksum= 0x478976

0000 7FFF

Registers

☒ read back buffer

☐ Reg from grid

	Reg start_addr	end_addr	offset_addr
<input type="checkbox"/> read back buffer	0000	FFFF	0000
<input type="checkbox"/> Reg from grid	0000	FFFF	0000
<input checked="" type="checkbox"/> NT71181Sharp_2024x2560_Test_2021	0000	FFFF	0000
<input checked="" type="checkbox"/> EDID.designhex_rom	0500	05FF	0500

CRC= 5F4C

0000 FFFF

LUTs

☐ read back buffer

☐ LUT from grid

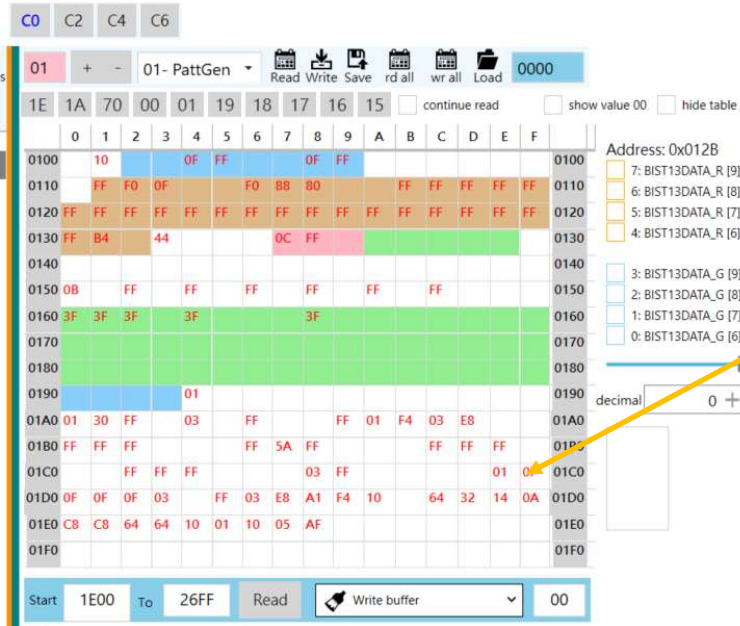
	Flash start_addr	end_addr	offset_addr
<input type="checkbox"/> read back buffer	1_8000	3F_FFFF	1_8000
<input type="checkbox"/> LUT from grid	1_8000	3F_FFFF	1_8000
<input checked="" type="checkbox"/> NT71181Sharp_2024x2560_Test_2021	1_8000	6_6FFF	1_8000

01_8000 06_6FFF



Save and Program - 3

To REG – HW rom code paste to REG



REG Flash

ISP on Read Program Chip Erase → list register diff

Remove files Load Save ISP slave= C0

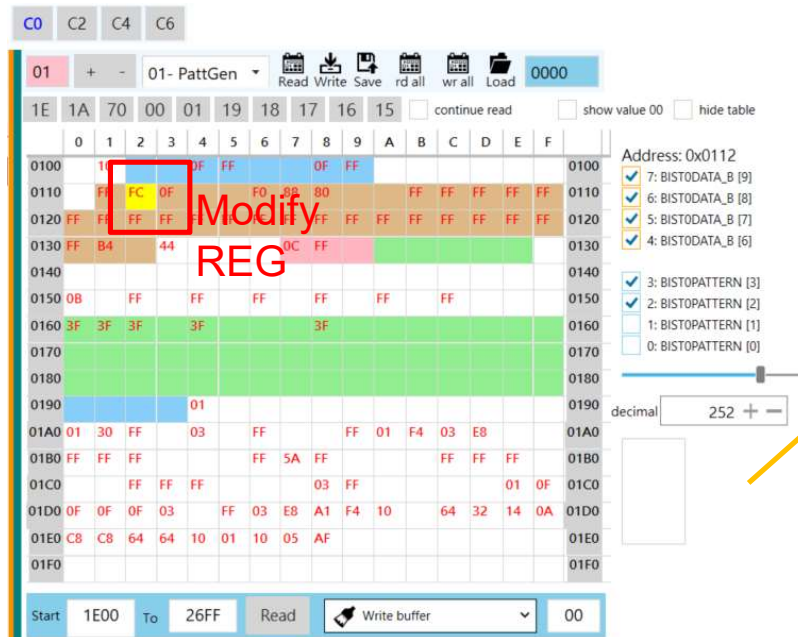
Blocks	Read	Program/Save
<input checked="" type="checkbox"/>	<input type="checkbox"/> read back buffer	<input checked="" type="checkbox"/> NT71181Sharp_2024x2560_Test_20210713_v001.bin
Firmware		
2021-07-02, ver= 00.00.01, Checksum= 0x478976		
0000 7FFF		
<input checked="" type="checkbox"/>	<input type="checkbox"/> read back buffer	Reg start_addr - end_addr offset_addr
<input type="checkbox"/> Reg from grid	0000 - FFFF	0000
<input checked="" type="checkbox"/> NT71181Sharp_2024x2560_Test_2021	0000 - FFFF	0000
CRC= 5F4C		
0000 FFFF		
<input type="checkbox"/>	<input type="checkbox"/> read back buffer	Flash start_addr - end_addr offset_addr
<input type="checkbox"/> LUT from grid	1_8000 - 3F_FFFF	1_8000
<input checked="" type="checkbox"/> NT71181Sharp_2024x2560_Test_2021	1_8000 - 6_6FFF	1_8000
01_8000 06_6FFF		

Paste
to
REG



Save and Program - 4

from REG – HW rom code copy from REG after rom code modify



Copy from REG

