ELECTRONIC PACKAGING

PROJECT

TEAM NO: 12

TEAM MEMBERS:

SRINIDHI M – S20210020323

BHANU PRANASWI P – S20210020309

TRISANDHYA DEVI G – S20210020276

PROJECT TITLE: **CYTRON-10A MOTOR DRIVER**

ABSTRACT:

This project focuses on the design and development of a printed circuit board (PCB) for the Cytron 10A Motor Driver using Autodesk Eagle. The goal of this project is to create a customized and compact PCB layout that integrates all the essential components required for motor control applications.

The project begins with a comprehensive review of the Cytron 10A Motor Driver datasheet and schematic, followed by component selection and placement to ensure optimal performance and compatibility. Schematic capture and PCB layout are performed using Autodesk Eagle, taking into consideration signal routing, power distribution, and thermal management. The final PCB design is tailored to meet the specific needs of motor control applications, with careful attention to signal integrity and optimization.

CONTRIBUTION

- SRINIDHI M
  - B Channel circuit
  - Step Up circuit
  - Error Correction
- BHANU PRANASWI
  - A Channel circuit
  - Signal circuit
  - Error Correction
- TRISANDHYA DEVI G
  - Timer circuit
  - Connector circuit
  - Power circuit
  - Error Correction

SOFTWARES USED:

WHAT ELSE DID WE DO?

Optimizations:

HEAT SINK – We removed the heat sink(quite a area consuming component), and have increased the PCB board thickness by a factor of 0.2mm as a replacement. So that increased core width would contribute in the heat regulation.

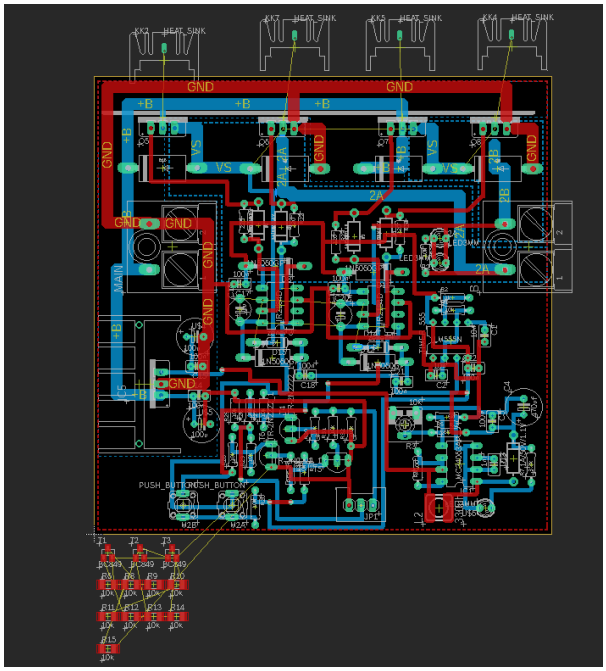
PCB dimensions – have decreased the PCB dimensions despite of having a large circuit that takes up a lot of space.

Size optimisation in schematic circuit.

Did the entire circuit again in EASY EDA to get a 3D view of the circuit.

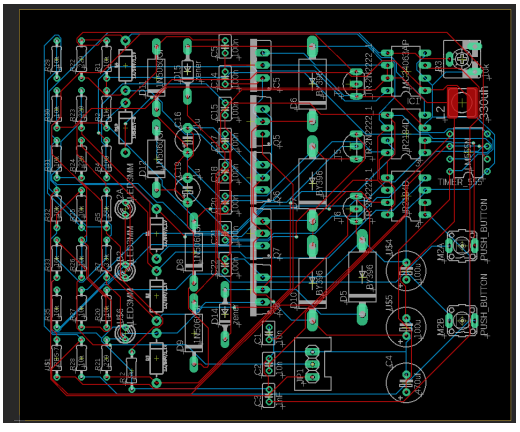
Have added resistors for the purpose of current division and voltage regulation.

Have immplemented IR2184 has a single input plus inverting shut down, which is a half bridge syncronous driver.

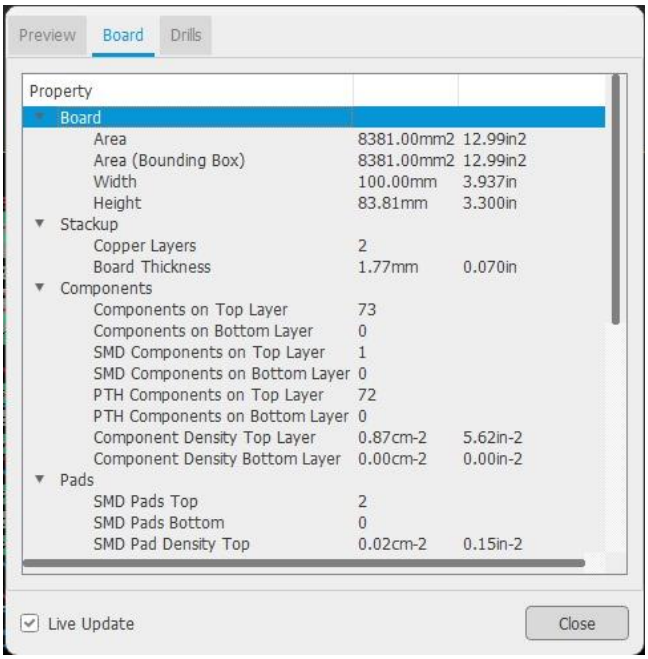


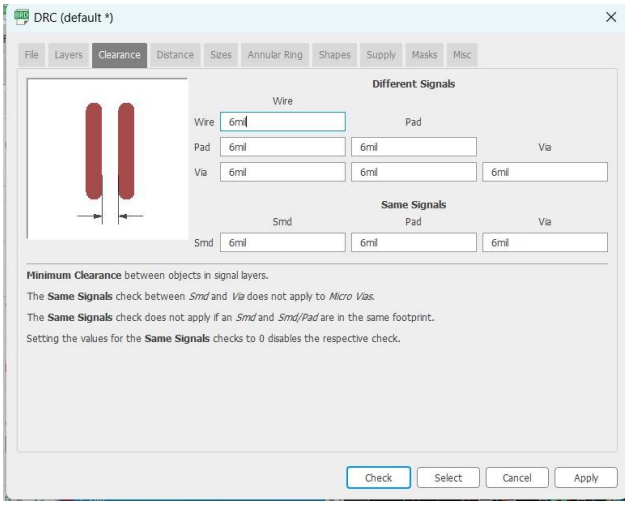
NORMAL ONE

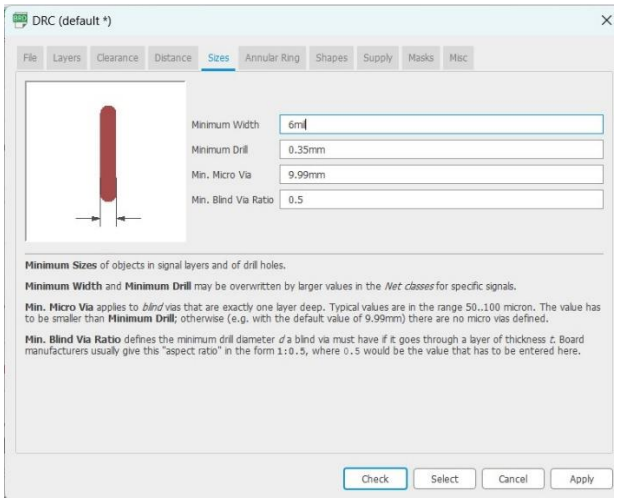
OPTIMISED ONE



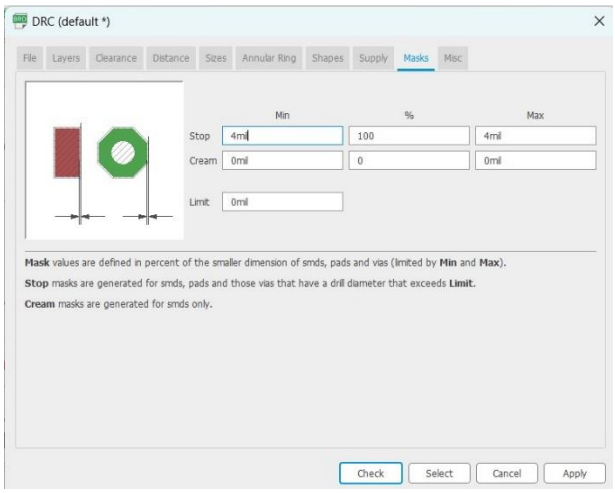
DIMENSIONS:


Preview
Board
Drills
Property
Board
Area 8381.00mm2 12.99in2
Area (Bounding Box) 8381.00mm2 12.99in2
Width 100.00mm 3.937in
Height 83.81mm 3.300in
Stackup
Copper Layers 2
Board Thickness 1.77mm 0.070in
Components
Components on Top Layer 73
Components on Bottom Layer 0
SMD Components on Top Layer 1
SMD Components on Bottom Layer 0
PTH Components on Top Layer 72
PTH Components on Bottom Layer 0
Component Density Top Layer 0.87cm-2 5.62in-2
Component Density Bottom Layer 0.00cm-2 0.00in-2
Pads
SMD Pads Top 2
SMD Pads Bottom 0
SMD Pad Density Top 0.02cm-2 0.15in-2
Live Update
Close

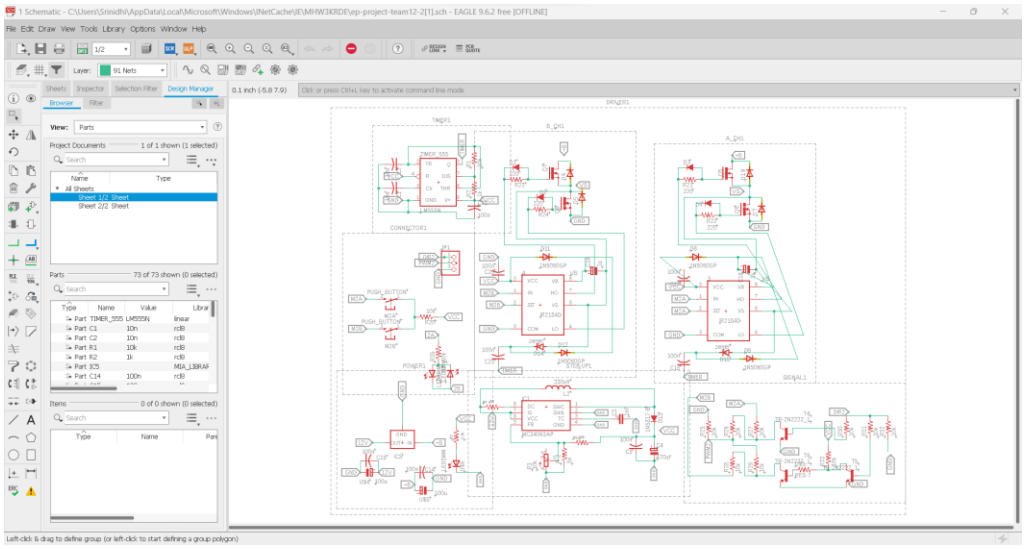

DRC (default *)
File
Layers
Clearance
Distance
Sizes
Annular Ring
Shapes
Supply
Masks
Misc
Different Signals
Wire
Pad
Via
6mil
Same Signals
Smd
Minimum Clearance between objects in signal layers.
The Same Signals check between Smd and Via does not apply to Micro Vias.
The Same Signals check does not apply if an Smd and Smd/Pad are in the same footprint.
Setting the values for the Same Signals checks to 0 disables the respective check.
Check
Select
Cancel
Apply

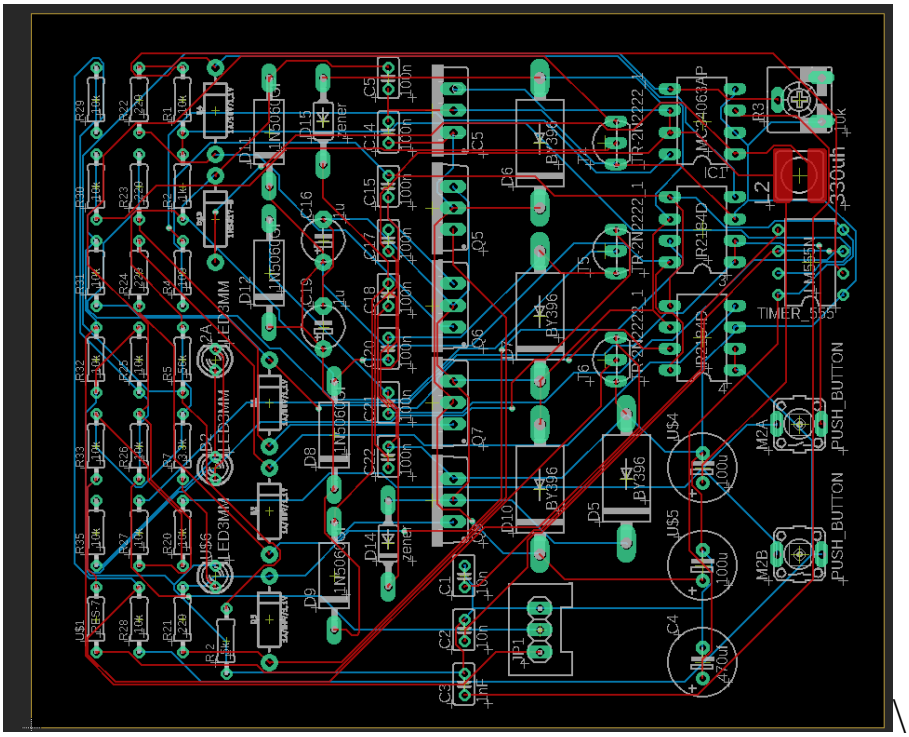

DRC (default *)
File
Layers
Clearance
Distance
Sizes
Annular Ring
Shapes
Supply
Masks
Misc
Minimum Width
6mil
Minimum Drill
0.35mm
Min. Micro Via
9.99mm
Min. Blind Via Ratio
0.5
Minimum Sizes of objects in signal layers and of drill holes.
Minimum Width and Minimum Drill may be overwritten by larger values in the Net classes for specific signals.
Min. Micro Via applies to blind vias that are exactly one layer deep. Typical values are in the range 50..100 micron. The value has to be smaller than Minimum Drill; otherwise (e.g. with the default value of 9.99mm) there are no micro vias defined.
Min. Blind Via Ratio defines the minimum drill diameter d a blind via must have if it goes through a layer of thickness t. Board manufacturers usually give this "aspect ratio" in the form 1:0.5, where 0.5 would be the value that has to be entered here.
Check
Select
Cancel
Apply

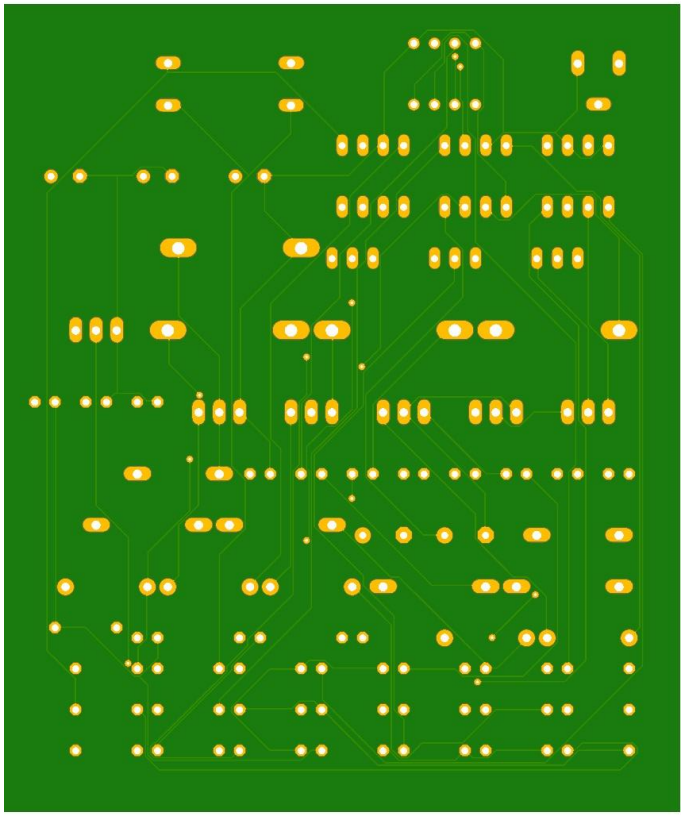

DRC (default *)
File
Layers
Clearance
Distance
Sizes
Annular Ring
Shapes
Supply
Masks
Misc
Min
%
Max
Diameter
Pads
Top
10mil
25
20mil
Inner
10mil
25
20mil
Bottom
10mil
25
20mil
Vias
Outer
8mil
25
20mil
Inner
8mil
25
20mil
Micro Vias
Outer
4mil
25
20mil
Inner
4mil
25
20mil
Annular Rings for pads and vias are defined in percent of the drill diameter (limited by Min and Max). If the diameter of an actual pad or via would result in a larger Annular Ring, that value will be used in the outer layers.
If the Diameter option is checked the actual pad or via diameter will be taken into account in the inner layers, too.
Micro Vias are blind vias that are exactly one layer deep and have a drill diameter that is smaller than the Minimum Drill value defined under Sizes (which may be overwritten by a larger Drill value in the Net classes).
Check
Select
Cancel
Apply

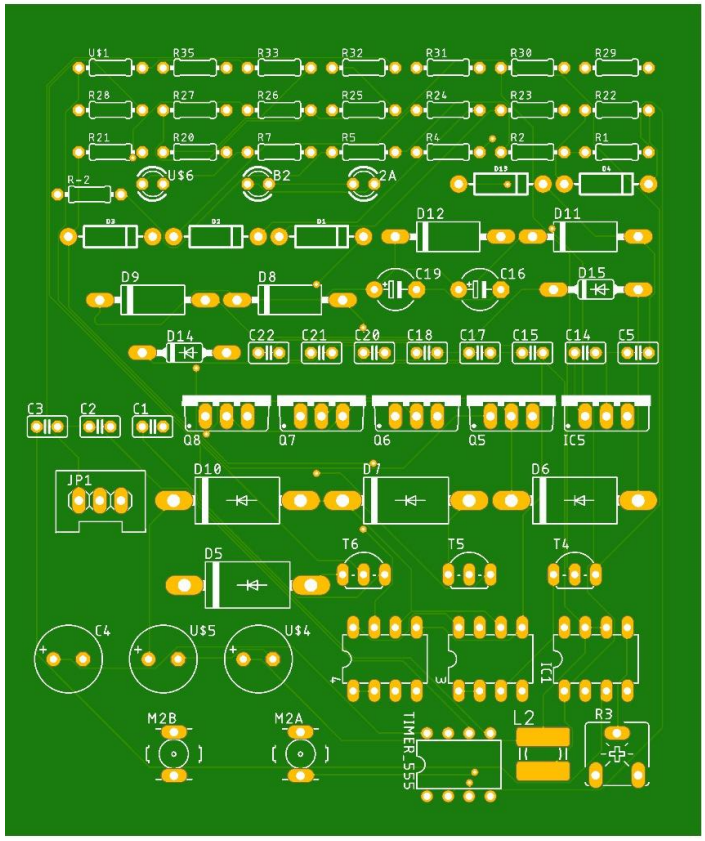

DRC (default *)
File
Layers
Clearance
Distance
Sizes
Annular Ring
Shapes
Supply
Masks
Misc
Min
%
Max
Stop
4mil
100
4mil
Cream
0mil
0
0mil
Limit
0mil
Mask values are defined in percent of the smaller dimension of smds, pads and vias (limited by Min and Max).
Stop masks are generated for smds, pads and those vias that have a drill diameter that exceeds Limit.
Cream masks are generated for smds only.
Check
Select
Cancel
Apply

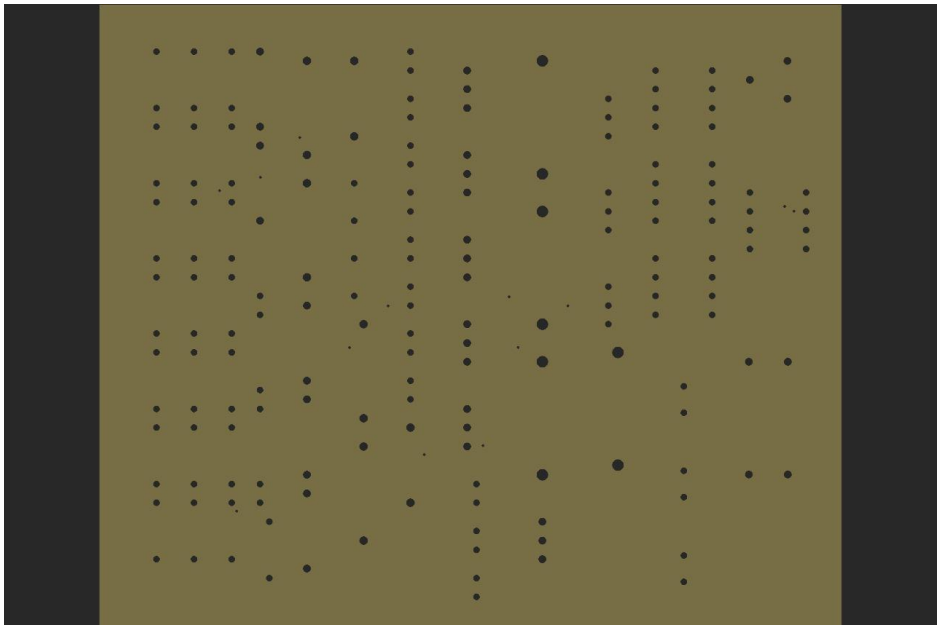
SCHEMATIC:



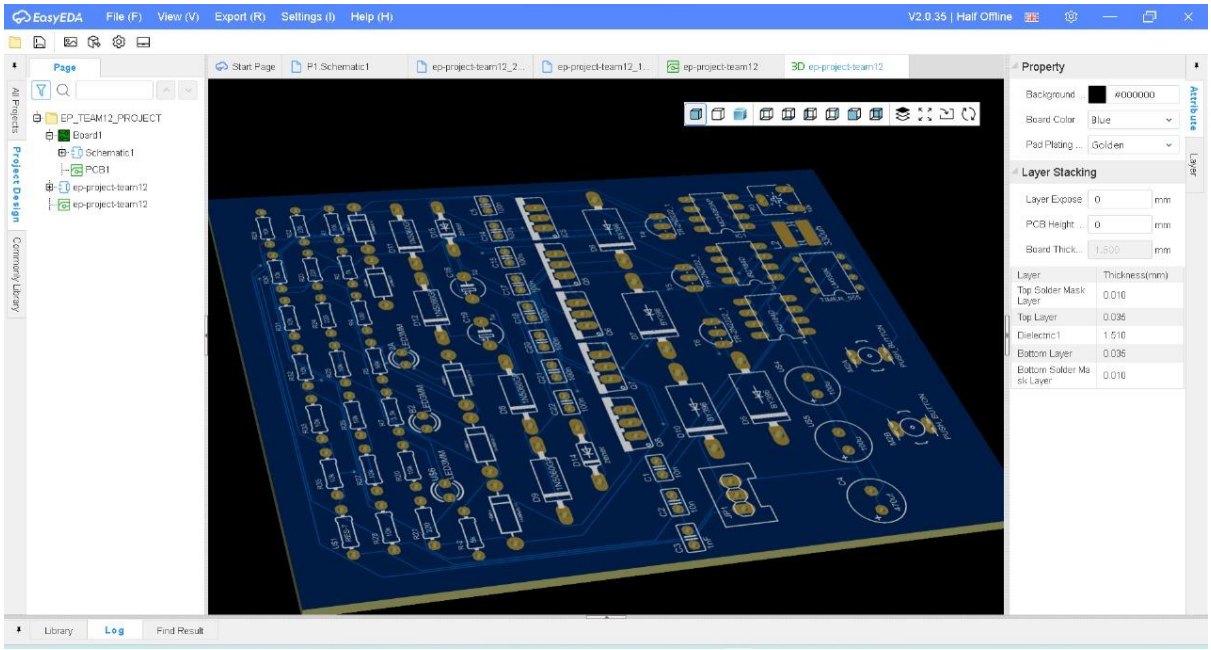


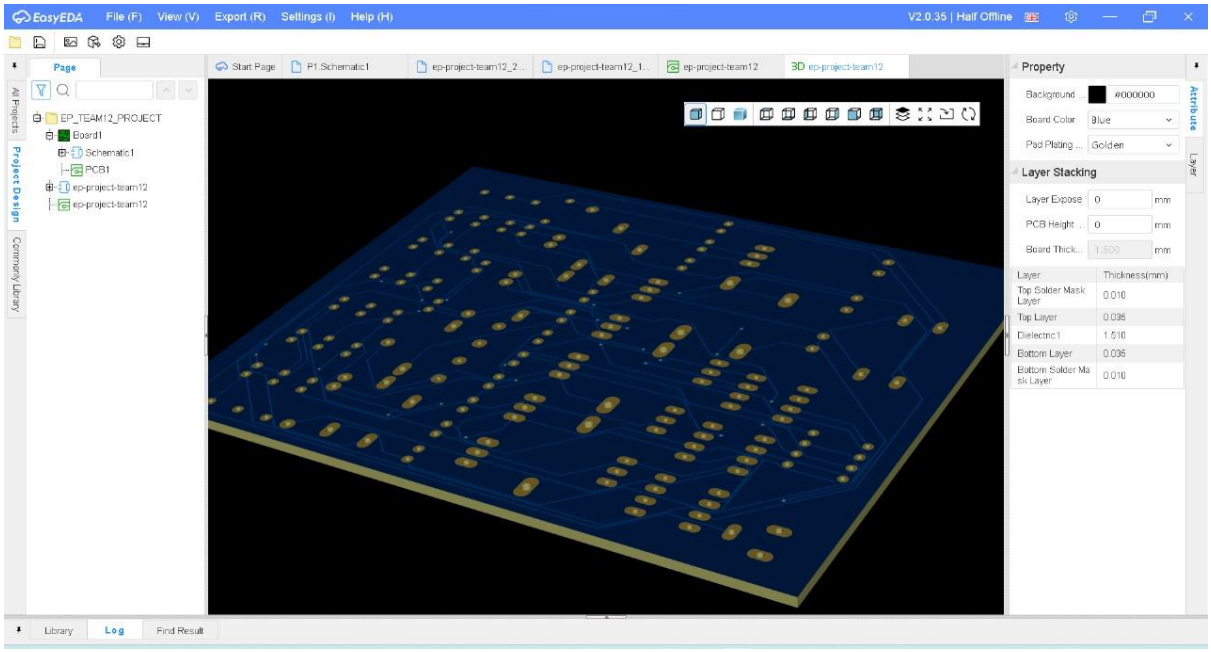


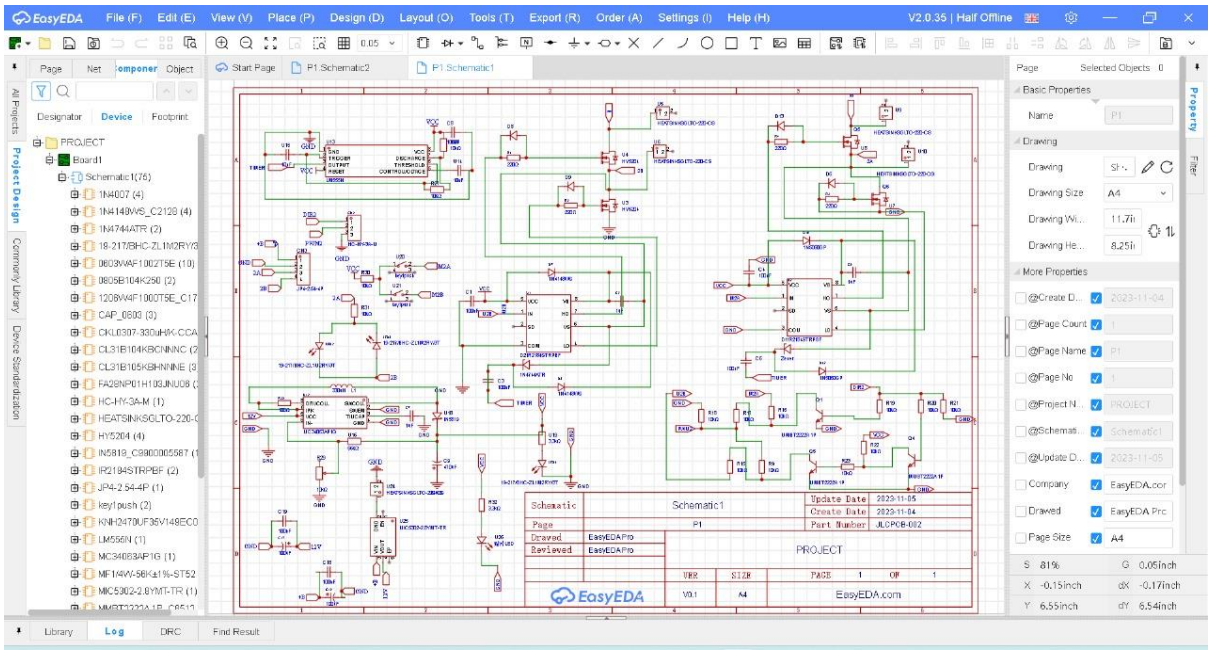

U$1
R35
R33
R32
R31
R30
R29
R28
R27
R26
R25
R24
R23
R22
R21
R20
R7
R5
R4
R2
R1
R-2
U$6
B2
2A
D13
D4
D3
D2
D1
D12
D11
D9
D8
C19
C16
D15
D14
C22
C21
C20
C18
C17
C15
C14
C5
C3
C2
C1
Q8
Q7
Q6
Q5
IC5
JP1
D10
D7
D6
T6
T5
T4
D5
C4
U$5
U$4
IC1
M2B
M2A
TIMER_555
L2
R3

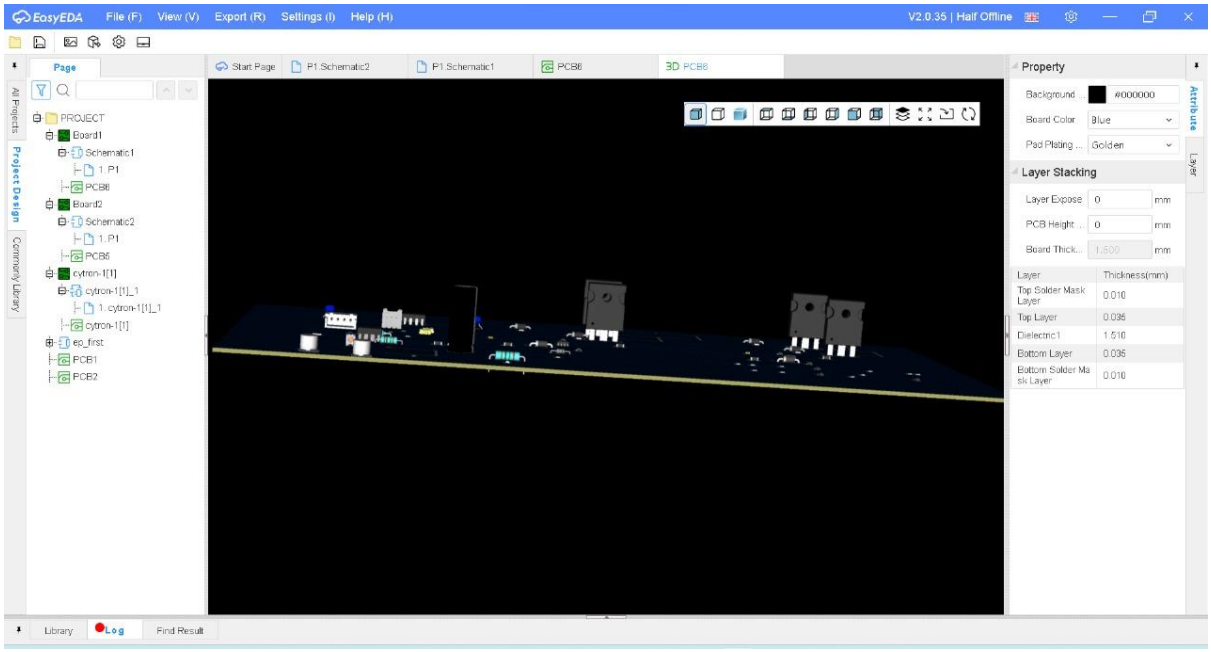


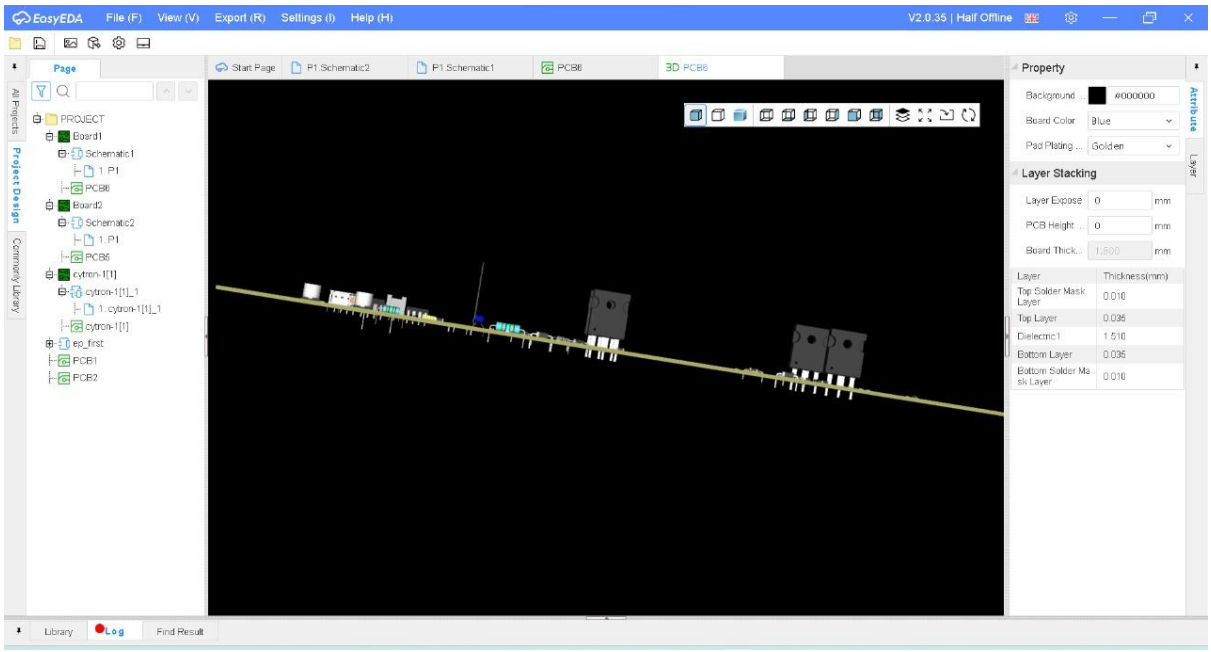
EASY EDA


EasyEDA
File (F)
View (V)
Export (E)
Settings (I)
Help (H)
V2.0.35 | Half Offline
Page
EP_TEAM12_PROJECT
Board1
Schematic1
PCB1
ep-project-team12
Start Page
P1 Schematic1
3D ep-project-team12
Property
Background ...
#000000
Board Color
Blue
Pad Plating ...
Golden
Layer Stacking
Layer Expose
PCB Height ...
Board Thick...
Layer
Thickness(mm)
Top Solder Mask Layer
0.010
Top Layer
0.035
Dielectric1
1.510
Bottom Layer
0.035
Bottom Solder Mask Layer
0.010
Library
Log
Find Result

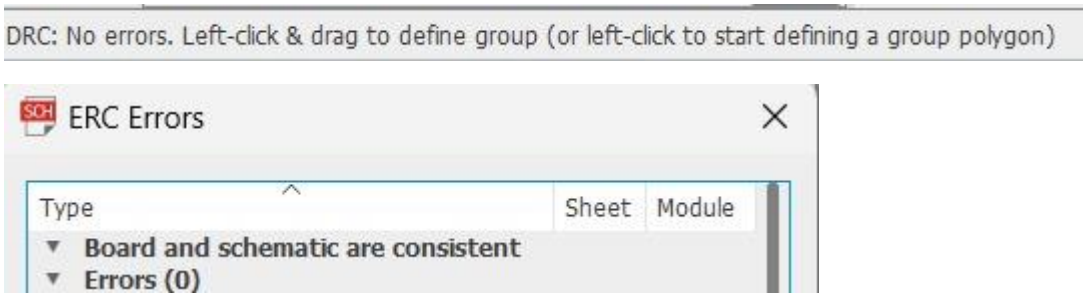

EasyEDA
File (F)
View (V)
Export (R)
Settings (I)
Help (H)
V2.0.35 | Half Offline
Start Page
P1.Schematic1
ep-project-team12_2...
ep-project-team12_1...
ep-project-team12
3D ep-project-team12
Property
Background ...
#000000
Board Color
Blue
Pad Plating ...
Golden
Layer Stacking
Layer Expose
PCB Height ...
Board Thick...
Layer
Thickness(mm)
Top Solder Mask Layer
0.010
Top Layer
0.035
Dielectric1
1.510
Bottom Layer
0.035
Bottom Solder Mask Layer
0.010
EP_TEAM12_PROJECT
Board1
Schematic1
PCB1
ep-project-team12
Library
Log
Find Result


EasyEDA
File (F)
Edit (E)
View (V)
Place (P)
Design (D)
Layout (O)
Tools (T)
Export (R)
Order (A)
Settings (I)
Help (H)
V2.0.35 | Half Offline
Start Page
P1.Schematic2
P1.Schematic1
Page
Selected Objects 0
Basic Properties
Name
P1
Drawing
Drawing Size
A4
More Properties
PROJECT
Board1
Schematic1(76)
Schematic
Schematic1
Page
P1
Drawed
EasyEDA Pro
Reviewed
EasyEDA Pro
Update Date
2023-11-05
Create Date
2023-11-04
Part Number
JLCPCB-002
PROJECT
VER
SIZE
PAGE
1
OF
1
V0.1
A4
EasyEDA.com
Library
Log
DRC
Find Result


EasyEDA
File (F)
View (V)
Export (R)
Settings (I)
Help (H)
V2.0.35 | Half Offline
Page
Start Page
P1:Schematic2
P1:Schematic1
PCB8
3D PCB8
PROJECT
Board1
Schematic1
1_P1
PCB8
Board2
Schematic2
1_P1
PCB6
cytron-1[1]
cytron-1[1]_1
1_cytron-1[1]_1
cytron-1[1]
eo_first
PCB1
PCB2
Property
Background ...
#000000
Board Color
Blue
Pad Plating ...
Golden
Layer Stacking
Layer Expose
0
mm
PCB Height ...
0
mm
Board Thick...
1.600
mm
Layer
Thickness(mm)
Top Solder Mask Layer
0.010
Top Layer
0.035
Dielectric1
1.510
Bottom Layer
0.035
Bottom Solder Mask Layer
0.010
Attribute
Layer
All Projects
Project Design
Commonly Library
Library
Log
Find Result


EasyEDA
File (F)
View (V)
Export (R)
Settings (I)
Help (H)
V2.0.35 | Half Offline
Page
Start Page
P1:Schematic2
P1:Schematic1
PCB8
3D PCB8
PROJECT
Board1
Schematic1
1_P1
PCB8
Board2
Schematic2
1_P1
PCB6
cytron-1[1]
cytron-1[1]_1
1_cytron-1[1]_1
cytron-1[1]
eo_first
PCB1
PCB2
Property
Background ...
#000000
Board Color
Blue
Pad Plating ...
Golden
Layer Stacking
Layer Expose
0
mm
PCB Height ...
0
mm
Board Thick...
1.600
mm
Layer
Thickness(mm)
Top Solder Mask Layer
0.010
Top Layer
0.035
Dielectric1
1.510
Bottom Layer
0.035
Bottom Solder Mask Layer
0.010
Attribute
Layer
All Projects
Project Design
Commonly Library
Library
Log
Find Result

NO ERRORS DETECTED!



SOURCE IS ATTACHED ON THE SOURCE_TEAM12 FOLDER

THANK YOU!