

Mod-N Synchronous Counter using a Novel Structure of T Flip-Flop in QCA Technology

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ABSTRACT

The development of electronic devices, in terms of size and speed, depends on manufacturing technology, which is based mainly on CMOS technology. There are several challenges in CMOS technology, particularly in terms of short channel effects. It is expected that CMOS technology will soon reach the scaling-down limit due to dissipated power, which prevents an increase in the number of devices on a single chip. In contrast, QCA technology is considered an alternative solution to CMOS, among several technologies. Due to its many features, this technology has attracted the attention of scientists, who have built different logic circuits using this technique. In this paper, a new QCA T Flip-Flop structure has been built which is used to create effective synchronous counters of various sizes. The proposed flip-flop achieved a 17 % and 5 % improvement in terms of cell count and area, respectively, while a 25 % and 13 % delay reduction were observed in the proposed 2-bit and 3-bit synchronous counters, respectively.

1. Introduction

Quantum-dot Cellular Automata (QCA) is a promising technology for constructing electronic circuits that utilize quantum dots as nanoscale structures for storing and manipulating data [1]. In comparison to traditional electronic technologies such as Complementary Metal-Oxide-Semiconductor (CMOS), QCA has numerous benefits, including smaller size, higher energy efficiency, faster operation, and greater resistance to radiation and temperature changes [2]. These advantages make QCA suitable for use in supercomputers. However, the QCA technology is still in the early stages of development and has not yet been widely adopted in commercial electronic devices. In this paper, we propose a new structure of T Flip-Flop in QCA technology. The proposed design can be used to build multi-level counters that offer improvements in performance compared to traditional circuits and can be utilized in various applications. This paper will follow a structured path, beginning with Section 2 where the origins of the technology, its basic building blocks, and how the signal is transmitted and moved

between cells will be discussed. Moving on to Section 3, we will conduct a review of related work, emphasizing the gaps we aim to address. Section 4 will unveil our innovative T Flip-Flop design tailored for QCA technology, elucidating design principles and methodology. Section 5 will present simulation results and comparative analysis against existing methods. Finally, Section 6 will serve as the conclusion, summarizing our contributions, discussing implications, and outlining potential future research directions.

2. Preliminaries

In 1993, the concept of QCA technology is first time introduced by Lent [3] as a CMOS alternative technology. The basic building block in this technique is a square container [4]. This container contains four dots injected by a couple of electrons [5]. The cell's electrons are unrestricted in their movement between the dots. Because there are only two permitted configurations of these electrons within the cell, the technology can represent the binary numbers, as seen in Fig. 1 [6].

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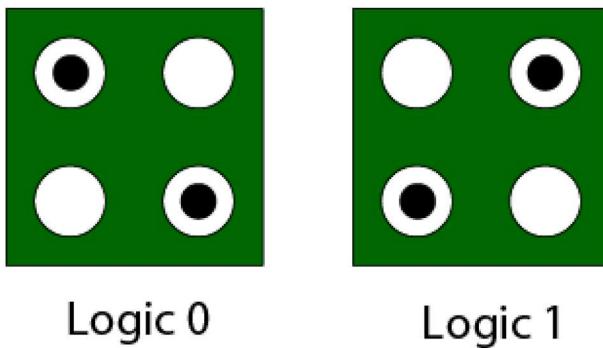


Fig. 1. Binary representation by QCA cell.

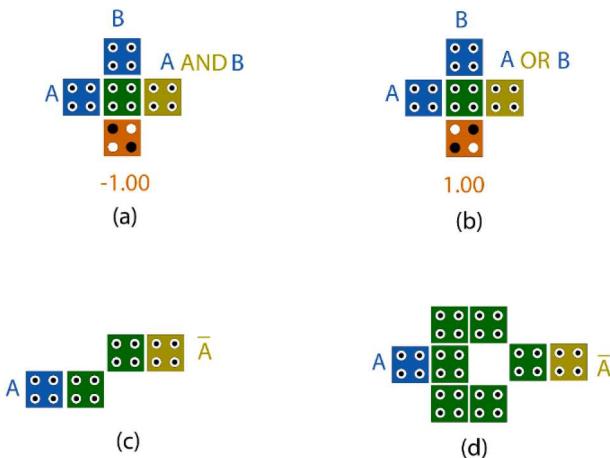


Fig. 2. Basic blocks in QCA (a) AND gate, (b) OR gate, (c) corner inverter (d) robust inverter [17].

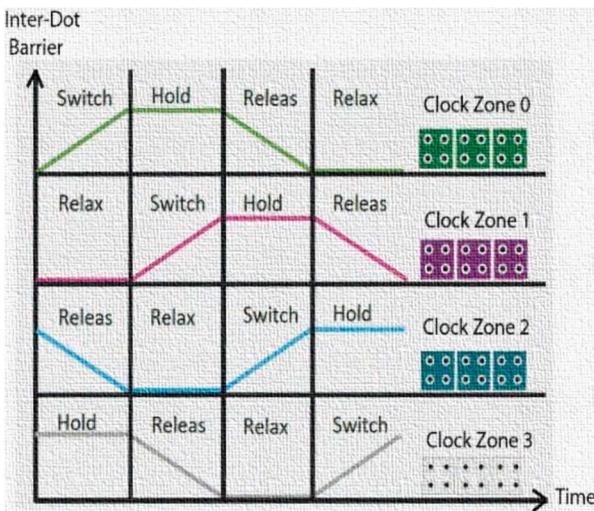


Fig. 3. Clock signal phases in four zones.

To construct logic circuits in this technology, it is important to build the basic logical blocks AND, OR and NOT gates. AND and OR gates can be designed using five cells whereas the simple inverter can be constructed by four cells as shown in Fig. 2 [7]. In QCA technology, the information is transmitting between cells using the principle of electronic repulsion, so there is no current flow in this technology [8]. The direction of the information flow is controlled using a clock signal [9]. The topic of clock signals and the movement of electrons within cells

was studied in detail in many previous researches [10–13]. In general, large circuits are divided into multiple zones [14]. The clock signal in each zone passes through four phases (switching phase, holding phase, releasing phase and relaxation phase) as shown in Fig. 3 [15]. These phases are important for the circuit to remain near the ground state [16].

3. Related work

The development and optimization of QCA-based T Flip-Flops have received a lot of attention in the fields of Quantum-dot Cellular Automata (QCA) technology and counter design. These T Flip-Flops are essential parts of the design of synchronous counters and have been the subject of extensive research in the QCA setting. Researchers have looked into many different facets of QCA-based counters, including fundamental components like flip-flops and gate structures, clocking strategies for synchronization, and various counter types like ripple counters, Johnson counters, and rings counters, each of which presents particular opportunities and challenges in terms of performance. Important challenges including robustness against environmental disturbances, fault tolerance, and error correction have also been addressed in this subject. The practical uses of QCA-based counters have increased as a result of recent developments in fabrication methods, materials, and multi-layer QCA architectures. Studies comparing QCA technology to its traditional CMOS counterparts have highlighted its advantages and disadvantages, and synthesis tools and design approaches have been created to simplify QCA circuit design. New paradigms like DNA-based QCA and molecular QCA give new opportunities for designing nanoscale counters. The development of QCA-based T Flip-Flops and counters is still being optimized, which is expected to lead to the development of extremely fast and efficient digital circuits.

The digital counter can be designed if a series of flip-flops are connected in a certain way. Counters are classified into two basic classes (synchronous and asynchronous) based on the way they are connected. Synchronous counters connect all flip-flops to a common clock source to overcome the delay problem faced by the other type (asynchronous) [18]. The synchronous counter is one of the most widely used counters, where n flip flops can be used to count from 0 to $2n-1$.

Despite the advantages of using T Flip-Flops in (QCA) technology, it's important to recognize the drawbacks of their application. One particular issue is the insertion of rotated cells into the QCA array or their demand for a comparatively higher number of cells. The benefits of QCA technology's famed compactness and density may be jeopardized as a result of the increased area overhead. Additionally, the practical scalability and manufacturability of the use of rotating cells may provide difficulties. There is a need for alternate designs and tactics that may fully utilize this nanoscale paradigm while minimizing cell count because the widespread use of T Flip-Flops in QCA-based counters may undermine the efficiency improvements promised by QCA technology. Different structures of T Flip-Flops were introduced in the literature as shown in Fig. 4.

4. Proposed structure

Flip-flop circuits need to be highlighted as they are essential components of a sequential circuit. A counter circuit, which is a type of sequential circuit and typically built using a set of flip-flops, samples data on just one clock edge (rising or falling clock edge). This section is dedicated to explaining the proposed structure of an edge-sensitive T Flip-Flop (EST Flip-Flop), which will be used later as a basic building block in the construction of synchronous counters. An edge-sensitive flip-flop, also known as a "edge-triggered flip-flop," is a basic digital electronic circuit used in sequential circuit design and digital logic. Its main job is to store and synchronize binary data according to a particular edge of a clock signal, usually either the rising edge (transition from low to high voltage) or the falling edge (transition from high to low voltage). Edge-sensitive flip-flops are essential parts of sequential logic

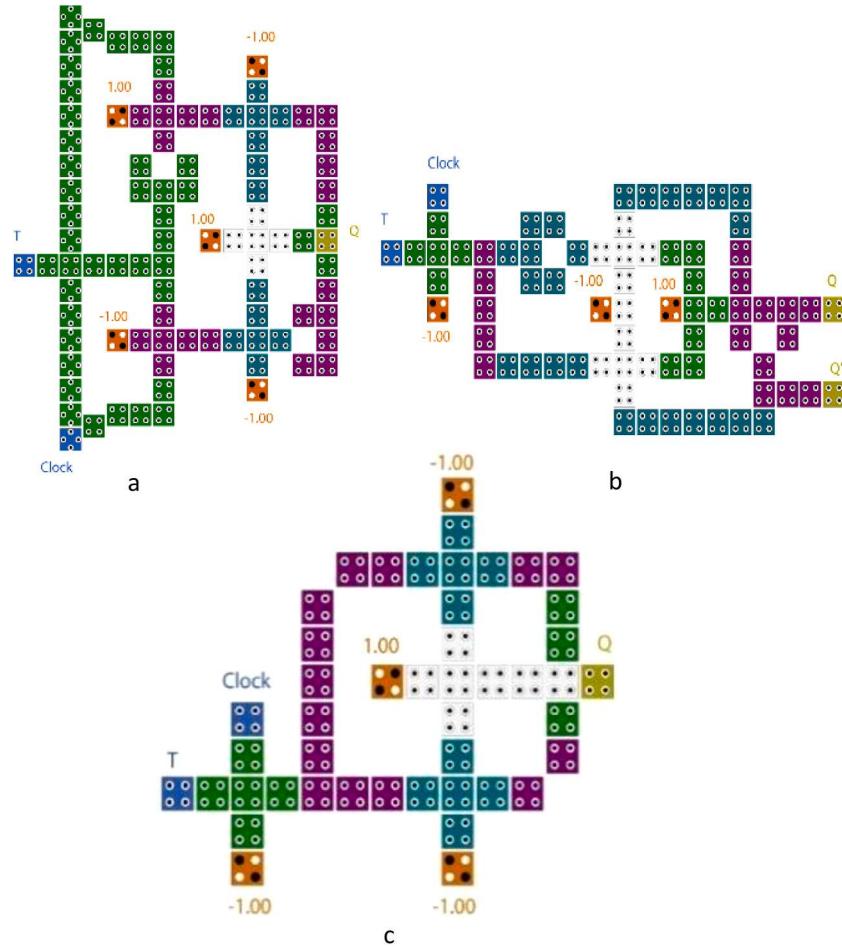


Fig. 4. Previous QCA form of T Flip-Flop introduced by (a) [19] (b) [20] (c) [21].

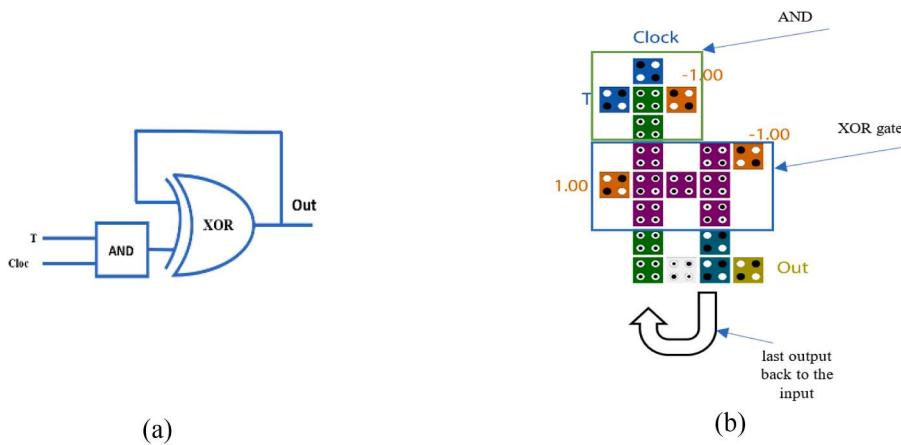


Fig. 5. T Flip-Flop (a) block diagram (b) proposed QCA structure.

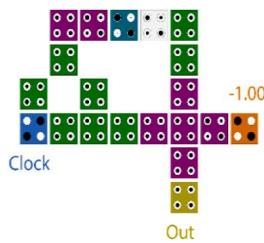


Fig. 6. The proposed structure of the CP generator.

circuits because they allow data to be synchronized and stored in a way that makes it easier to process information sequentially. When compared to existing circuits, the proposed layout shows many improvements in terms of complexity and area reduction, which further reduces the implementation cost. The block diagram followed in this paper is shown in Fig. 5(a), and the proposed QCA architecture of EST-FF is depicted in Fig. 5(b). The proposed flip-flop structure consists of an AND gate and an XOR gate connected in a particular configuration.

The EST Flip-Flop is composed of 20 cells and occupies an area of approximately $0.015\mu\text{m}^2$. It generates the true output after passing through only three clock phases. The Clock Pulse (CP) module produces a sequence of pulses, generated every rising edge of the clock signal, which is used to drive the circuit. Fig. 6 depicts the QCA configuration of the CP generator. Then, 2-bit, 3-bit, and 4-bit synchronous counters are configured using the EST Flip-Flop. Fig. 7 shows the QCA layout for these counters. The consistent arrangement of the proposed structures is distinguished from its peers. All proposed circuits are simulated using the coherence vector engine of the QCADesigner software [22].

The (CP) module is a crucial component in synchronous counter circuits. It is responsible for generating a pulse signal from an input clock signal. This pulse signal is generated every time the clock signal experiences a rising edge, and then it is fed into all the EST (Edge-Triggered Flip-Flop) circuits in the system. This ensures that all the flip-flops in the circuit are triggered at the same time, thereby guaranteeing that the counter operates in a synchronous manner.

The T-type flip-flop circuit plays a crucial role in this work, as the focus is primarily on building it in an optimal structure. When both the input (T) and the clock signal are in the HIGH state, the output signal flips instantly. It is worth noting that all the proposed circuits in this work do not use a corner inverter, making the proposed structures more robust. The XOR block utilized to build the proposed flip-flop was introduced in [23].

In summary, the CP module generates a pulse signal from the input clock signal, which is then used to trigger all EST Flip-Flops in the circuit simultaneously, ensuring synchronous operation.

5. Simulation results and comparison

QCA technology has gained significant attention in recent years due to its potential for ultra-low power and high-speed digital circuits. One of the key tools used in the development and analysis of QCA circuits is QCADesigner, a popular simulation and design platform. In this study, QCADesigner was utilized to design, simulate, and verify the proposed QCA circuits. One of the key features of QCADesigner is its use of advanced simulation engines, which allow for accurate and efficient analysis of QCA circuits. In particular, this application offers both bistable and coherence vector simulation engines, each with its own unique capabilities. The bistable engine is suitable for simulating QCA circuits with bistable elements, such as flip-flops and latches, while the coherence vector engine is more suitable for circuits with high-complexity behavior.

For this study, the coherence vector simulation engine was chosen due to its higher level of precision [24]. This engine is able to simulate the coherence and phase information of quantum-dot states, allowing

for a more accurate representation of circuit behavior. The input/output waveforms of the EST Flip-Flop, a key component of the proposed circuits, are shown in Fig. 8.

The use of a coherence vector simulation engine in the simulation tool allowed for the thorough analysis and verification of the proposed QCA circuits [24]. The results of these simulations were crucial in the development and optimization of the circuits, and helped to ensure their performance and reliability. In addition to its simulation capabilities, QCADesigner also offers a range of design and layout tools for the creation of QCA circuits. These tools allow for the quick and easy placement and routing of QCA cells and interconnects, reducing the design time and effort required.

Overall, the use of QCADesigner was essential for simulation and analysis the proposed circuits in this study. Its advanced simulation engines and comprehensive design tools allowed for the efficient and accurate design and verification of the circuits and played a critical role in their success.

The output waveform for the proposed structure of the CP Module is illustrated in Fig. 9, where the CP represents a pulse generator as it converts level to edge. For the 2-bit, 3-bit and 4-bit synchronous counter, the output results are depicted in Figs. 10, 11 and 12. It is clear from the simulated output that the proposed circuits are error-free.

Table 1 presents the results of comparing the suggested flip-flop structure with previous similar circuits. The EST Flip-Flop demonstrated a 5 % improvement in area and a 17 % improvement in complexity compared to the previous best structure. The proposed 2-bit and 3-bit synchronous counters showed a reduction in delay of 25 % and 13 %, respectively. Additionally, there was a slight improvement in cell count and area, as shown in Table 2. Based on these results, it is possible to estimate the approximate values of counters of different sizes, as illustrated in Fig. 13. These findings highlight the efficacy of the proposed circuits and their potential to improve QCA technology.

The QCAPro software [25] is used to examine the power dissipation for the proposed flip flop in this work. At three tunneling energies (0.5 Ek, 1 Ek, and 1.5 Ek) and temperature equal 2 Kelvin, the energy needed for switching and clocking cells is calculated separately. Ek is the kink energy. Fig. 14 shows the proposed EST Flip Flop dissipated power map at three energy levels. Table 3 details the dissipated power values of the proposed design at three levels.

6. Conclusion

In this paper, new forms of Quantum-dot Cellular Automata (QCA) circuits were introduced, including a level-to-edge converter and a T Flip-Flop. These structures were used to construct synchronous counters in modes 2, 3, and 4, and their performance was demonstrated through simulation results. The proposed structures showed superior performance compared to other designs, as evidenced by the results of the comparison presented in Table 1 and Table 2.

One of the key contributions of this work is the ability to predict the properties of mod-N synchronous counters based on the results obtained from the first three levels. This allows for the extrapolation of the performance of these circuits to larger sizes, providing valuable insights for their potential use in real-world applications.

Another notable aspect of this paper is the lack of reliance on the corner inverter, which is known to be a weak point in QCA architectures. The proposed circuits were able to achieve their performance without utilizing this element, making them more robust and reliable.

Overall, the new QCA forms of the level-to-edge converter and T Flip-Flop presented in this work show promising performance and have the potential for use in a range of applications. The ability to predict the properties of mod-N synchronous counters based on the results from the first three levels is a valuable contribution, and the absence of the corner inverter makes the proposed circuits more robust and reliable.

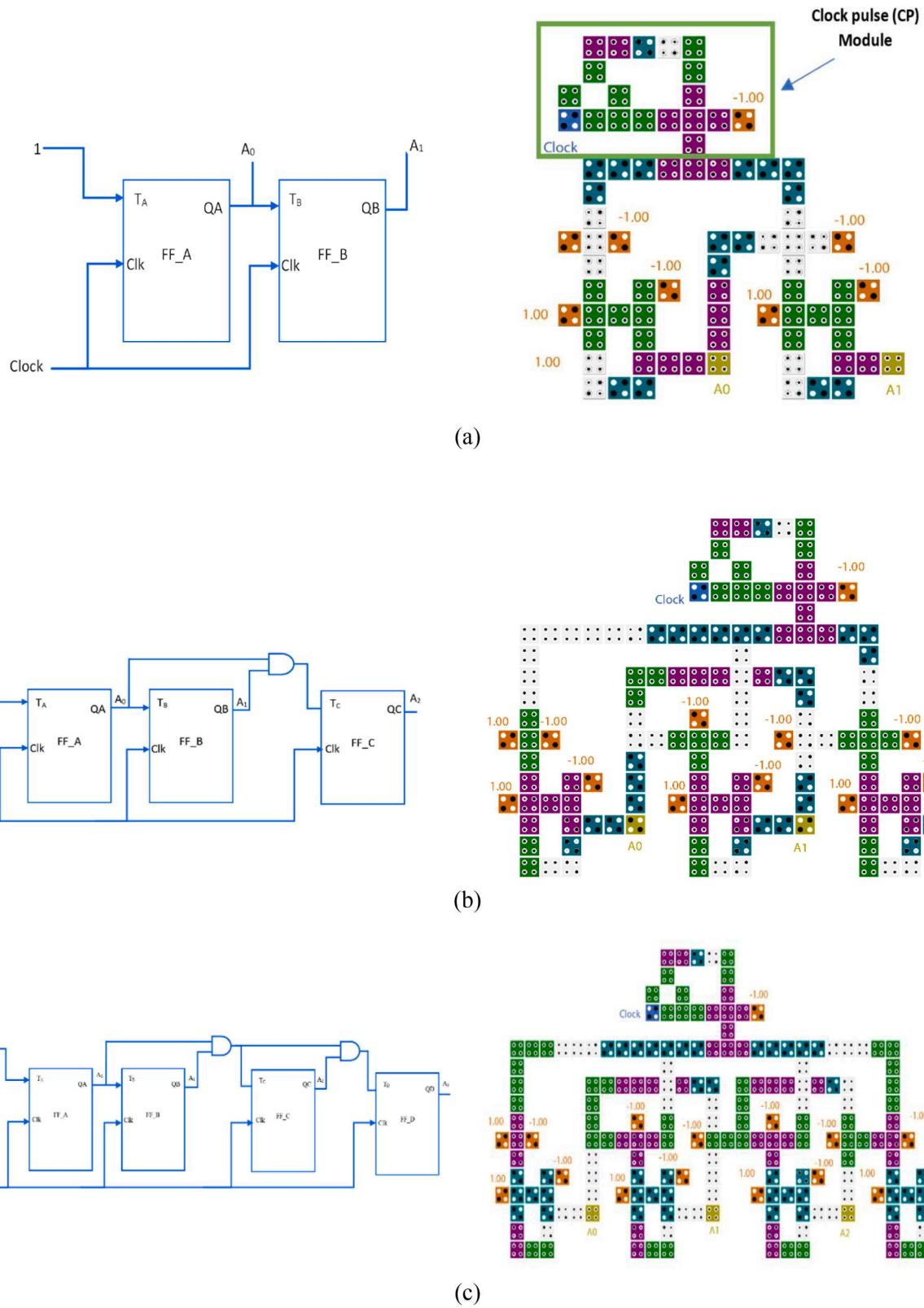


Fig. 7. The proposed diagram and QCA layout of (a) 2-bit counter (b) 3-bit counter and (c) 4-bit counter.

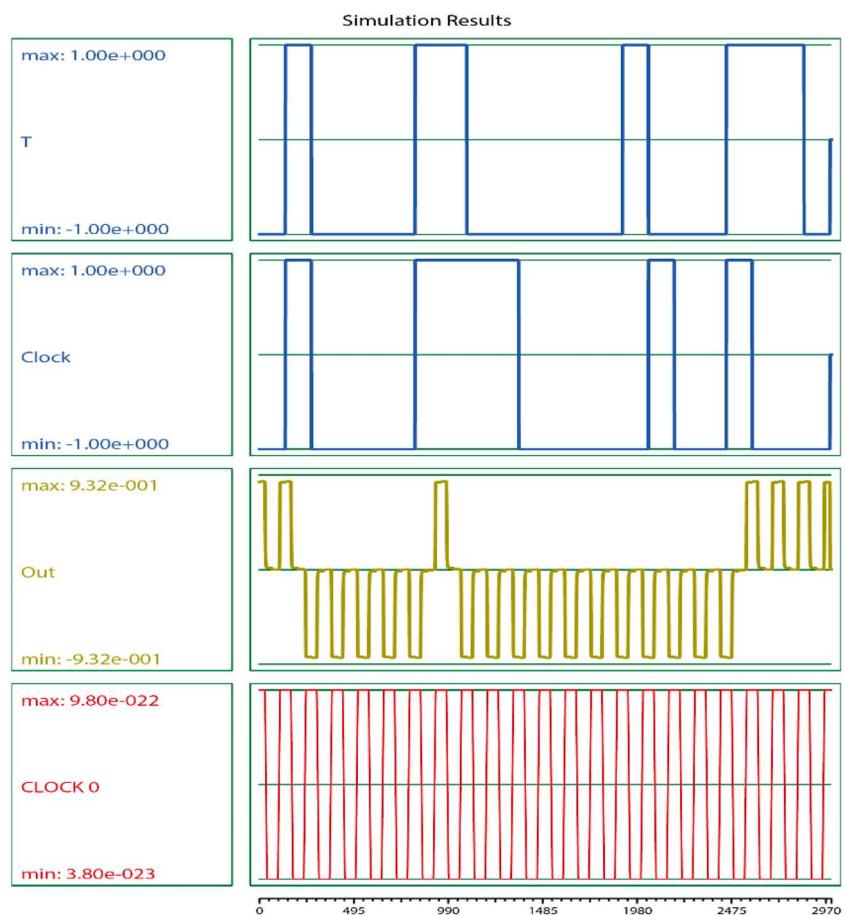


Fig. 8. The simulation result of the proposed layout of T Flip-Flop.

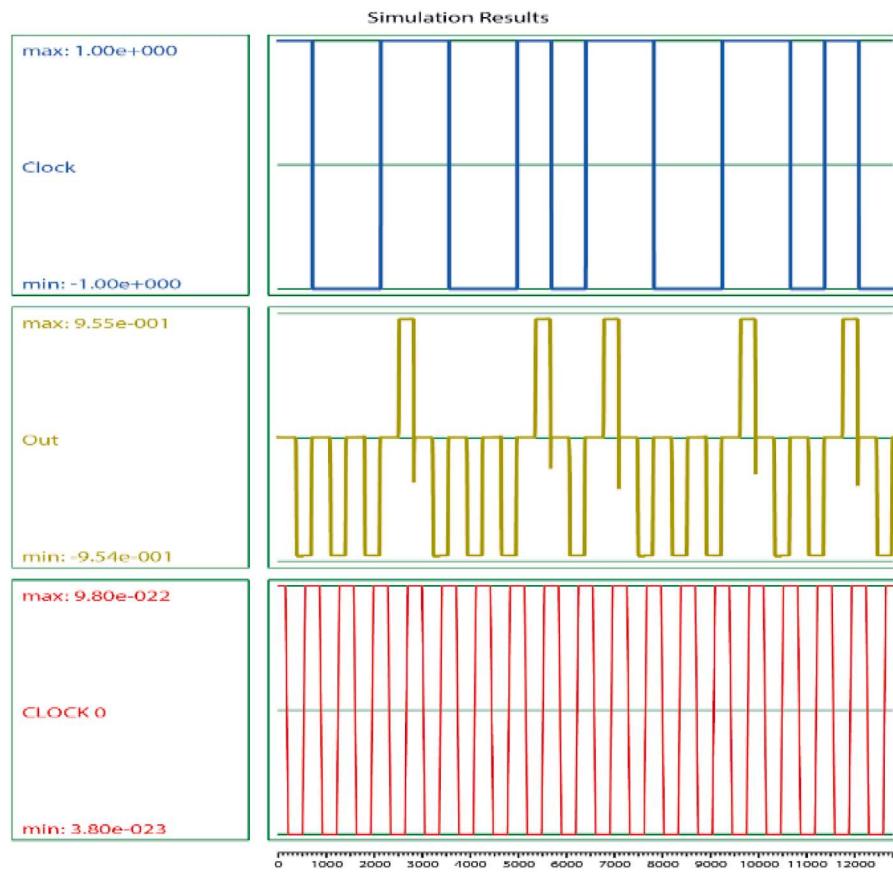


Fig. 9. The output result of the proposed CP module.

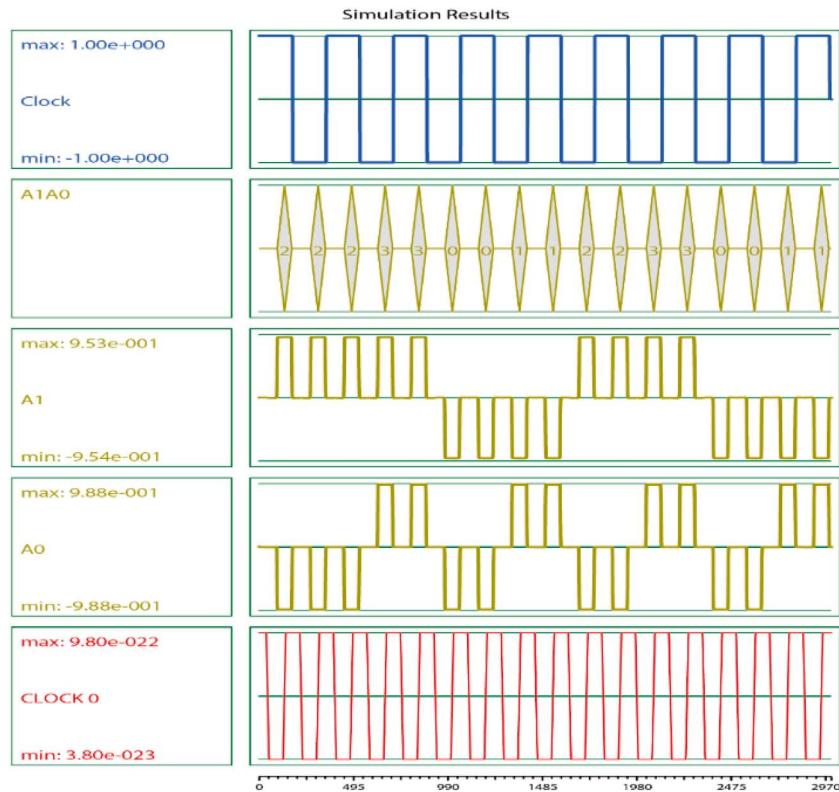


Fig. 10. Simulation output of the proposed 2-bit counter structure.

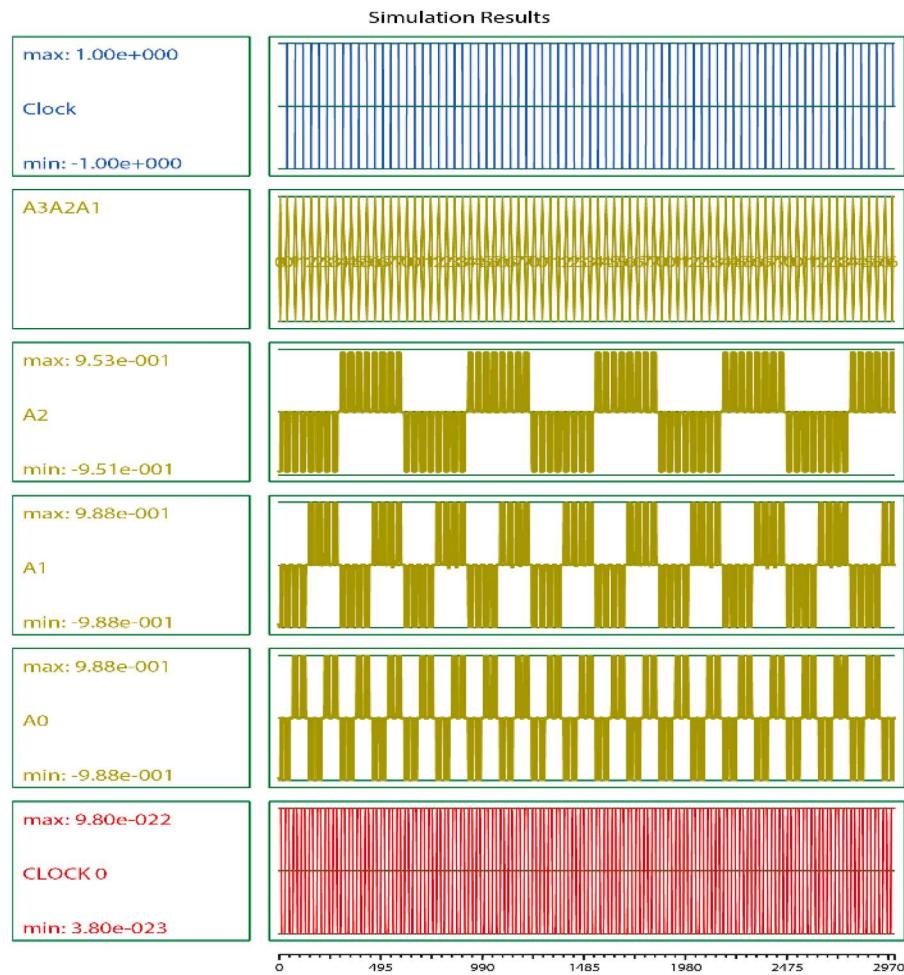


Fig. 11. Simulation output of the proposed 3-bit counter structure.

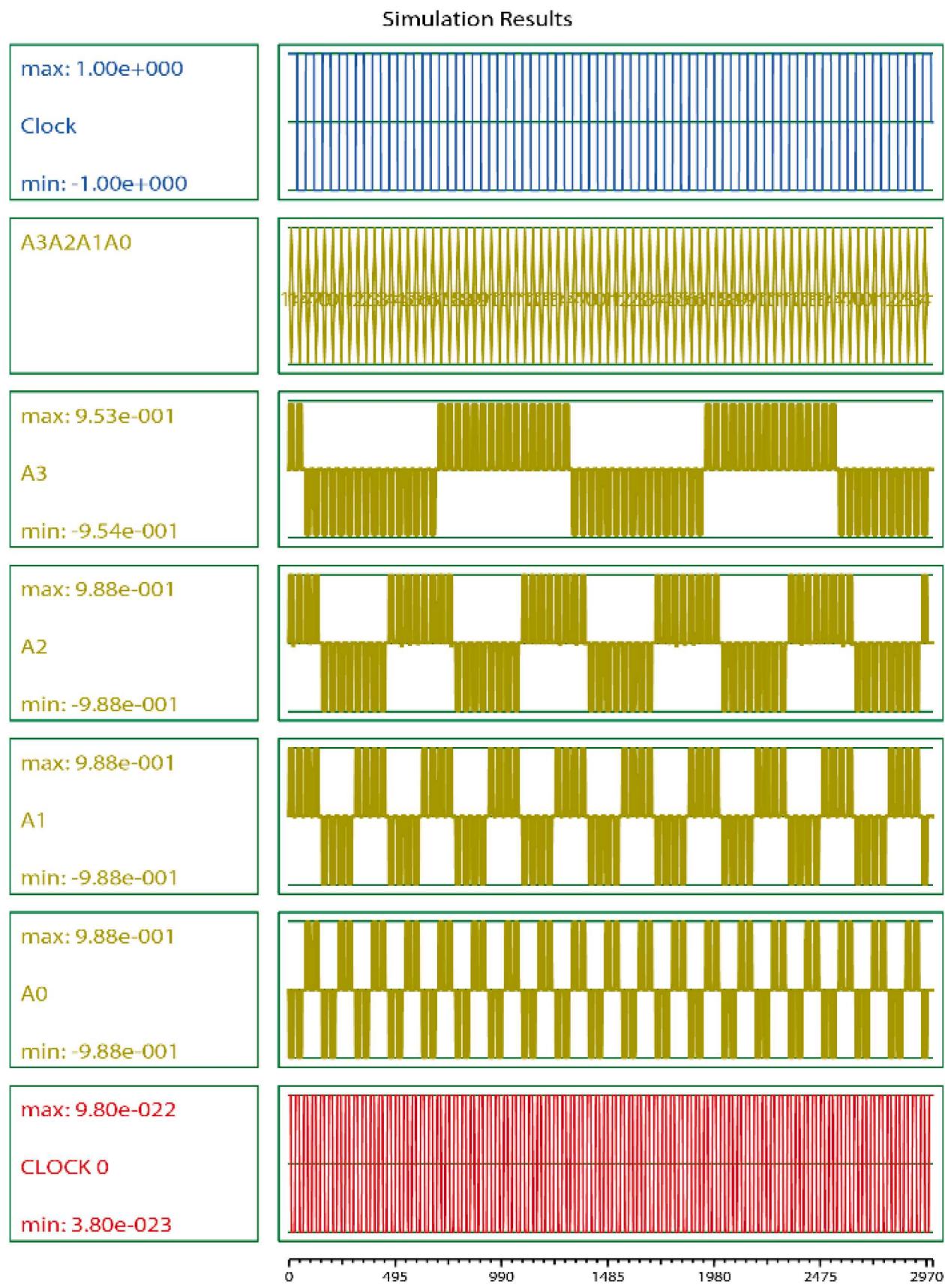


Fig. 12. Simulation output of the proposed 4-bit counter structure.

Table 1

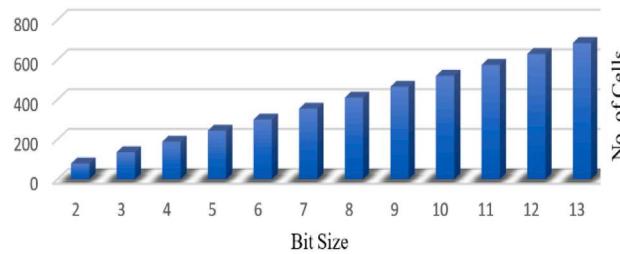
The comparison of the proposed flip-flop with the counterparts.

Flip-Flop Presented in	Cell counts	Area (μm^2)	Latency (Delay)
[26]	184	0.32	1.25
[19]	92	0.10	1.25
[27]	81	0.07	1.5
[28]	55	0.06	1.5
[21]	46	0.06	1
[18]	21	0.0186	0.5
Proposed	20	0.0154	0.5

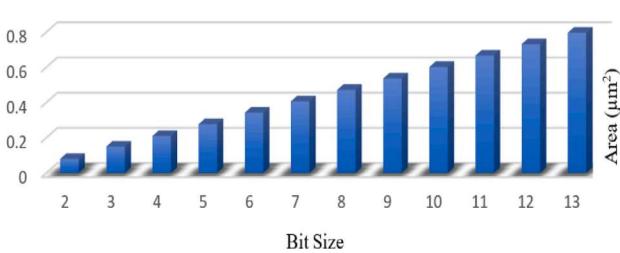
Table 2

The comparison of the proposed counters with the counterparts.

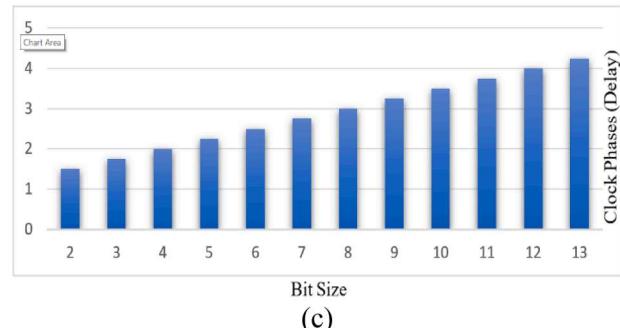
Counter presented in	Bit size	No. of cells (Complexity)	Area (μm^2)	Latency (Delay)
[29]	2	328	0.62	3
	3	616	1.2	5
	4	1130	2.2	7
[21]	2	141	0.22	2.25
	3	238	0.36	2.25
[30]	4	354	0.49	2.25
	3	174	0.20	3
[18]	4	258	0.25	4
	2	80	0.09	2
Proposed	3	140	0.16	2
	4	196	0.24	2
	2	79	0.08	1.5
Proposed	3	136	0.15	1.75
	4	189	0.21	2



(a)



(b)



(c)

Fig. 13. Mod-N synchronous counter properties in terms of cell count, area and delay.

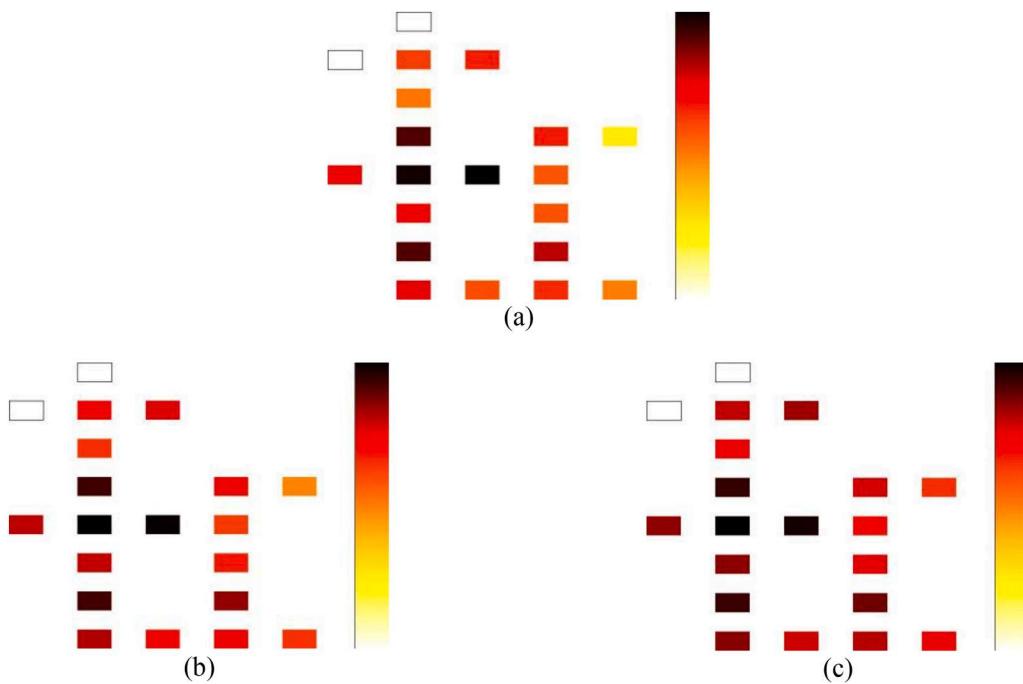


Fig. 14. The proposed EST Flip Flop dissipated power map at a 0.5 Ek, (b) 1 Ek, and (c) 1.5 Ek.

Table 3
The energy dissipation values of EST Flip Flop at three-level.

Circuit	No. of QCA cells	Leakage & energy dissipation (eV)			Switching energy dissipation (eV)			Total Energy dissipation (eV)		
		0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek
EST FF	20	0.00493	0.01604	0.02950	0.02481	0.02144	0.01821	0.02974	0.03749	0.04771

CRediT authorship contribution statement

Ali H. Majeed: Methodology, Project administration, Software, Validation, Writing – original draft, Writing – review & editing. **Ghasan Ali Hussain:** Supervision. **Adnan Sabbar:** Supervision. **Hassan Falah Fakhruddin:** Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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