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A unique universal block in QCA technology

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ABSTRACT

The limitations of Complementary Metal Oxide Semiconductor (CMOS) such as high-power dissipation, short channel effects, and high lithography has prompted scientists to look forward to alternatives. Many nanotechnologies were emerged and still in the competition such as Fin Field-Effect Transistor (FinFET), Carbon Nanotube Field-Effect Transistor (CNFET), Quantum-dot Cellular Automata (QCA). QCA is a new nanoelectronics technology used a new method for calculations and it is a promising technology in terms of power dissipation. In QCA, circuit complexity is depending on cell count, area and latency. For commercial purposes a universal gate is necessary, this gate can be used alone to design any Boolean function, where in CMOS technology, the NAND or NOT gates have the ability to be a universal gate. The dominant gates in QCA are the majority gate with inverter where QCA circuits cannot be designed using only a universal gate. Because the structure of the gate is important in QCA, this paper introduces a new low complexity singular block that can be used as a universal block. The proposed block can be used to form AND, OR, NOT, Exclusive-OR (XOR) and Multiplexer (MUX). So, this block not just used to design any circuit but also it can be used to form other important functions XOR and MUX to build large circuits in an optimum form.

1. Introduction

Quantum-dot cellular automata (QCA) is a technology that uses quantum dots to store and manipulate information. QCA technology was first proposed in the mid-1990s [12] as a potential alternative to traditional semiconductor technologies, such as complementary metal-oxide-semiconductor (CMOS) [19]. One of the main advantages of QCA technology is that it can potentially operate at much higher speeds and with lower power consumption compared to traditional semiconductor technologies [23]. This is because QCA technology relies on quantum mechanical phenomena, such as electron tunneling, to perform logic operations, which can be much faster than the electrical charges used in CMOS technology [1]. QCA technology has the potential to revolutionize the field of computing by enabling the creation of ultra-fast, low-power devices with a high level of integration. However, it is still in the early stages of development and there are many challenges that need to be overcome before it can be widely used in commercial applications. Despite these challenges, QCA technology has attracted significant interest from researchers and industry, and is an active area of research and development in the field of nanoelectronics [2]. For electronic circuit design, different gate is required like (AND, OR, NOT, XOR, MUX). These blocks have different topologies in QCA technology. The universal gate gives the designer flexibility and make a revolution in terms of manufacturing and production costs.

2. Background

The main building block of the QCA circuit is a square cell. This cell has four dots with two electrons arranged in regular form. The QCA cell has two stable states to represent binary values as shown in Fig. 1.

The cell state is controlled by the adjacent cell where the cell electrons are affected by other nearby electrons even if they fall outside the cell. Cell electrons can be tunneling between the dots inside the cell, but they can not escape outside. Majority voter is an important block in QCA where it consists of 5 cells (three as inputs, one voter cell and one as output) and it has the ability to form AND and OR gates by fixing one of the input cells to logic 0 or 1 respectively. The structure of majority gate is illustrated in Fig. 2. Majority gate has interest many researchers where some of them introduce multi input majority gate [3,10,13,17,20] and others discus the reliability of it [5]. Another important block in QCA is inverter as depicted in Fig. 3, where any Boolean function will be easy to form with the majority gate and inverter.

QCA circuits did not need current flow to work but it required moving the cell state to the adjacent cell. So, it is important to control

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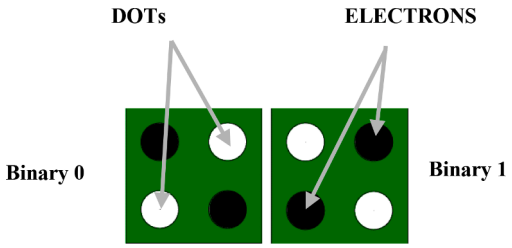


Fig. 1. QCA cell configuration.

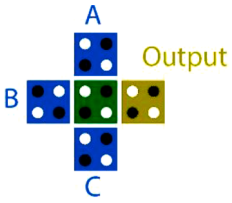


Fig. 2. QCA 3-input majority gate.

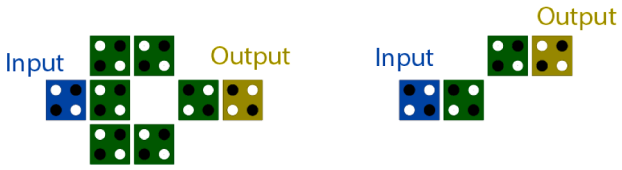


Fig. 3. QCA Inverter configurations (a) Robust (b) Corner.

the data flow from the input cell toward the output [7]. The controlling mechanism is done by the clock signal. The clock signal controls the barrier between dots to give electrons the ability to tunnel between cell dots or prevent it. In the large QCA circuits, the circuit divided into four zones each zone has four phases (switch phase, hold phase, release phase and relax phase) as illustrated in Fig. 4 [11]. If these phases work consequently we can say the circuit runs near to the ground state [4,14].

3. Related study

The potential of Quantum-dot Cellular Automata (QCA) technology, with its advantages of ultra-low power consumption, high-speed operation, and scalability, has attracted significant interest among researchers. Previous studies in the field of QCA have primarily focused on optimizing individual components such as majority gates, adders, and multiplexers. However, a major challenge that remains is the development of a versatile universal block capable of performing diverse functions. To address this challenge, researchers have explored various approaches.

SQUARES design: SQUARES is a methodology proposed in an earlier work that uses a 5 × 5 QCA cell grid as the basic building block [6]. However, the paper shows that SQUARES results in a high area overhead and complex timing.

Tile-based design: A tile is a square grid of cells with input/output cells [9]. Tiles can be fully populated (FP) or non-fully populated (NFP). The paper proposes a new type of tile called the "MV-like tile" that combines the logic functions of the Majority Voter (MV) and Inverter (INV) blocks. The MV-like tile is area efficient and can be used as a basic primitive for logic design.

A universal logic gate is pre-suggested in [22], the proposed gate is complex and required 77 cells and two types of cells (normal and rotated) while another design suggested by [8] required 30 cells and it required multi-layer for implementation.

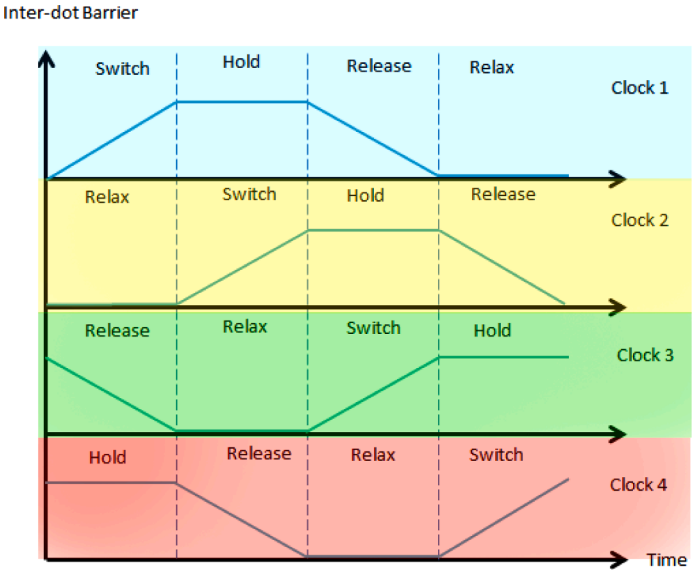


Fig. 4. Clock signal phased in 4 zones.

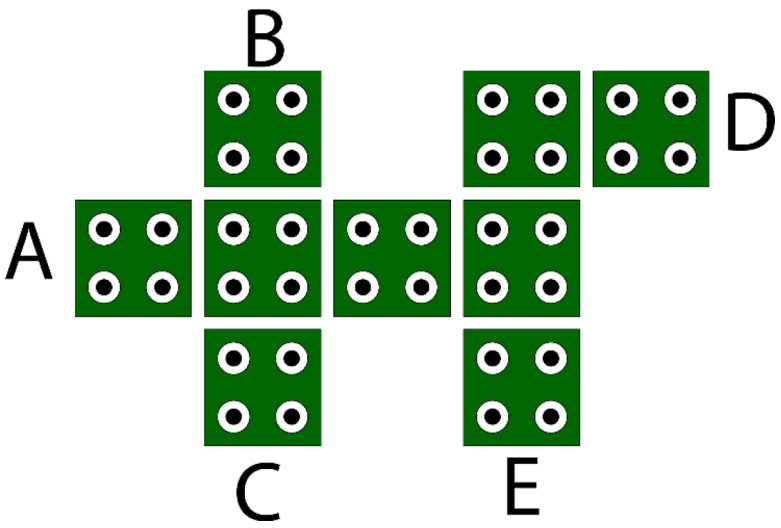


Fig. 5. Proposed universal block.

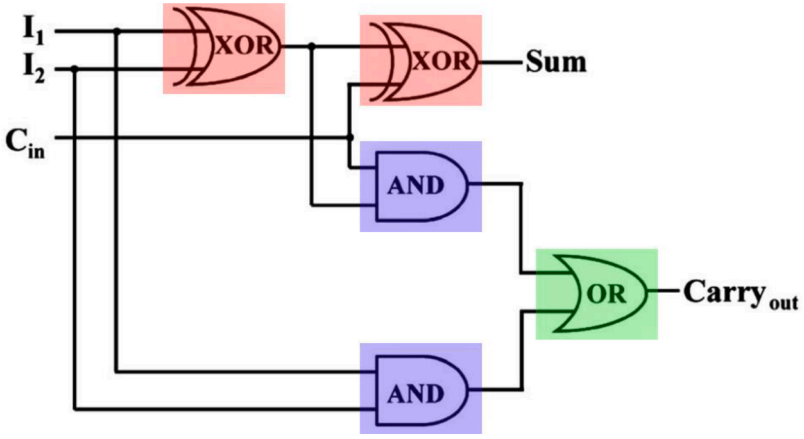


Fig. 6. Block diagram of full-adder [18].

This paper contributes to existing research by conducting a comprehensive survey and analysis of previous and current studies. It proposes a new universal block design in QCA that aims to address the limitations and challenges observed in prior approaches.

4. Proposed block

The main contribution of this work is to proposed a new block consists of only 9 cells, the proposed block can be programmed to work as AND, OR, NOT, MUX and XOR gate. This feature is very important commercially in future of this technology. Beside these features, the proposed block designed in an optimal form in terms of area and cell count as illustrated in Fig. 5.

Programming the proposed block is done by following the procedure as below:

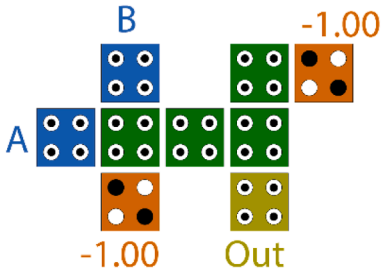
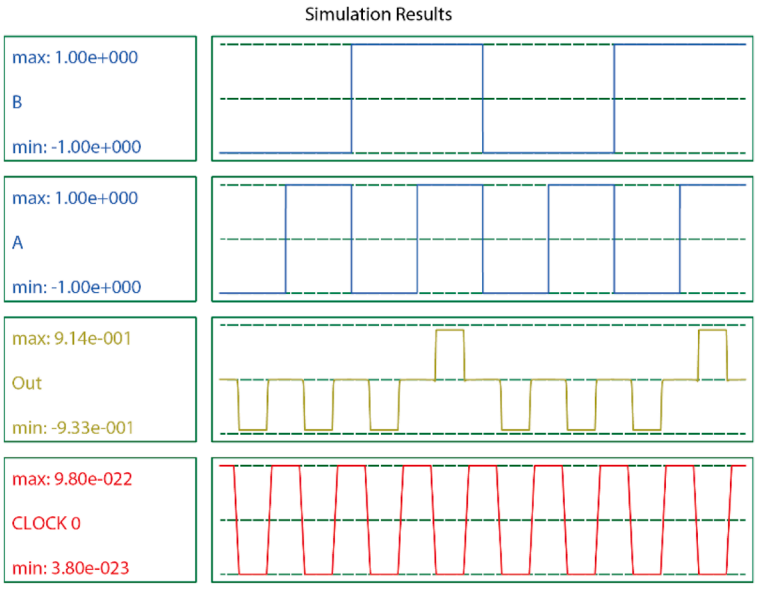
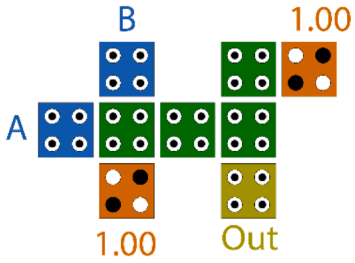
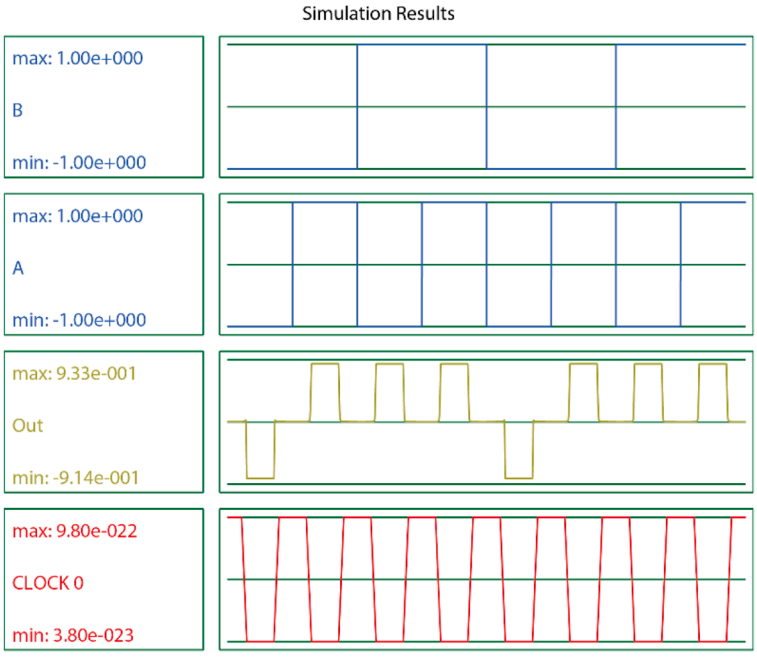
To realize AND gate: A and B to the inputs, connect C & D to logic 0 and E represents the output cell.

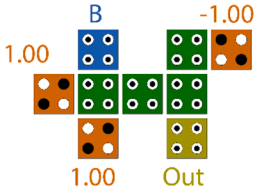
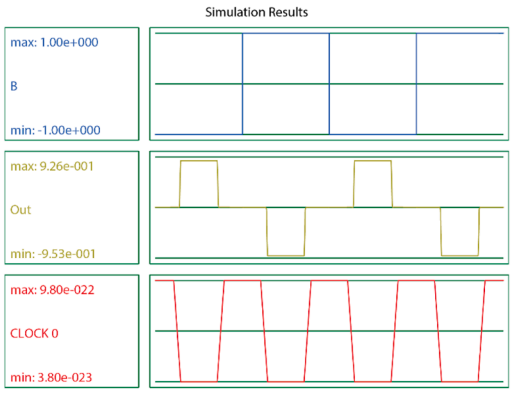
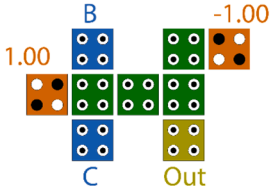
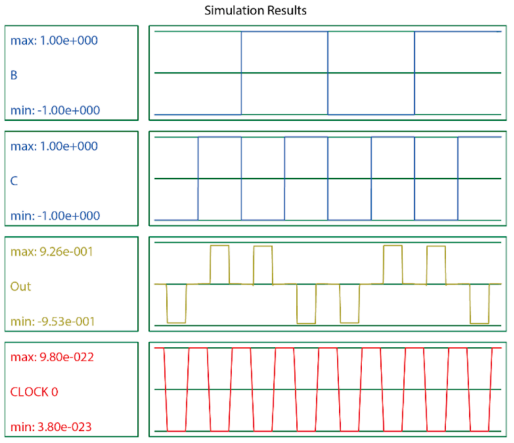
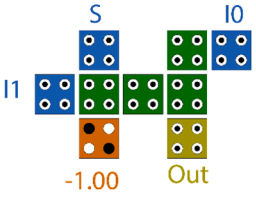
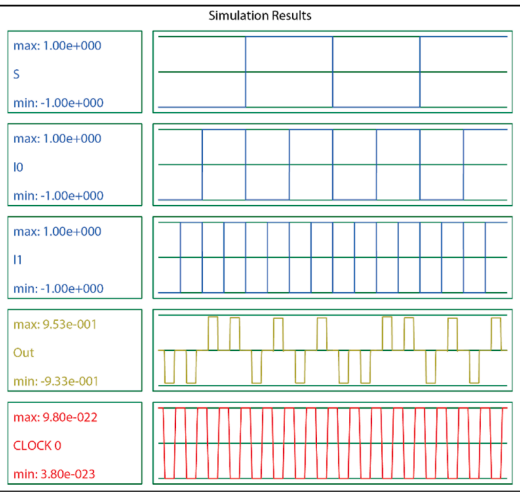
To realize OR gate: connect A and B to the inputs, connect C & D to logic 1 and E represents the output cell.

To realize NOT gate: B as input cell, A & C fixed as logic 1, D fixed as logic 0 and E as output cell.

To realize XOR gate: A fixed as logic 1 B & C act as input cells, D fixed as logic 0 and E as output cell. It's important to mention that this gate has already been proposed in our previous work [16].

To realize MUX gate: B work as selector, D as I0, A as I1, C fixed as logic 0 and E as output cell. It's important to mention that this gate has already been proposed in our previous work with small change [15].

Programming gate as	Reforming the universal block	simulation output
AND		
OR		

NOT	 B -1.00 1.00 1.00 Out	 Simulation Results max: 1.00e+000 B min: -1.00e+000 max: 9.26e-001 Out min: -9.53e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023
XOR	 B -1.00 1.00 C Out	 Simulation Results max: 1.00e+000 B min: -1.00e+000 max: 1.00e+000 C min: -1.00e+000 max: 9.26e-001 Out min: -9.53e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023
MUX	 S I0 I1 -1.00 Out	 Simulation Results max: 1.00e+000 S min: -1.00e+000 max: 1.00e+000 I0 min: -1.00e+000 max: 1.00e+000 I1 min: -1.00e+000 max: 9.53e-001 Out min: -9.33e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023

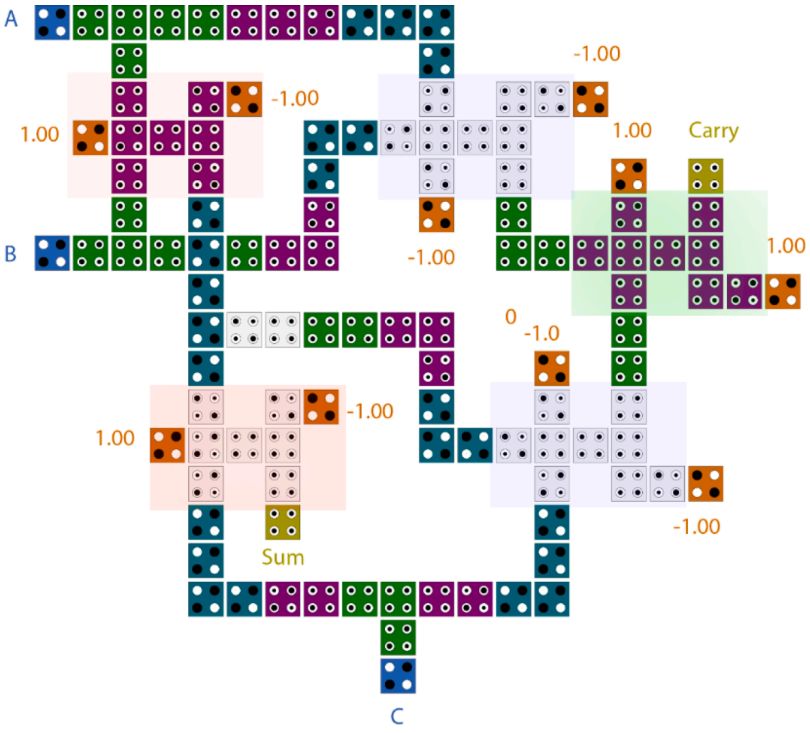


Fig. 7. QCA full adder using the proposed block.

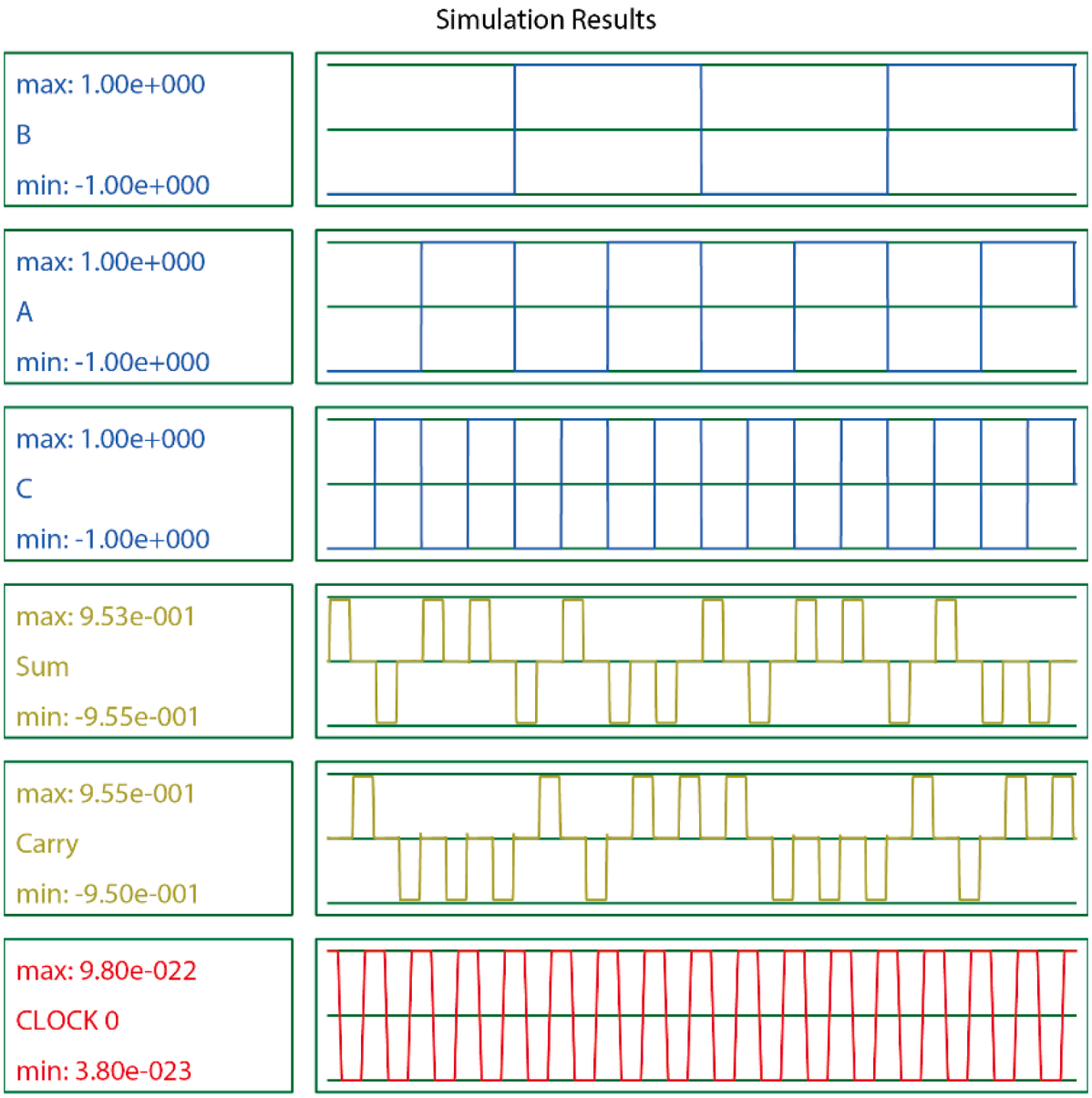


Fig. 8. Output simulation of the proposed QCA-full adder.

5. Circuit design using proposed block

To prove the ability of the proposed block, it is important to use it in a circuit with different functions. Fig. 6 represents the block diagram of a full-adder that will be using it to carry out in the QCA technology using the proposed block only.

By carrying out the same circuit in QCA technology using the proposed block only by QCADesigner software [21], the circuit layout are as in Fig. 7 and the simulation result as in Fig. 8. It is obvious from the simulation output that the proposed block work correctly without error when it connected in big circuits.

The circuit shown in Fig. 7 is designed using the proposed Universal gate only as a building block and compared to the previous designs, it is clear from Table 1 that the proposed Universal gate solved the previous designs problems since it has single layer layout design, with only normal cells needed, and with reduced complexity.

6. Conclusion

In quantum-dot cellular automata (QCA) technology, a universal block is a component that is capable of performing a wide range of logic functions, such as AND, OR, and NOT. Universal blocks are important in QCA technology because they allow designers to build complex circuits using a small number of basic components. One of the main advantages of using universal blocks in QCA technology is that they can reduce the complexity and size of QCA circuits, which can lead to lower power consumption and faster operation. Additionally, another advantage of universal blocks is that they can be easily reprogrammed or reconfigured to perform different logic functions, which makes them flexible and adaptable. This allows designers to easily modify QCA circuits to meet changing requirements or to add new features. This paper proposes a unique structure that can play a universal block in the next generation of IC technology. The proposed block has been tested in a new full adder

Table 1
Full adder circuits designed with universal gates comparison.

No.	Full Adder circuit designed in	Structure\Block cells count	Occupied layout cells count
1	The approach given in [6] while the circuit design by [9]	SQUARES-based\25 cells	1400
2	[9]	Tile-based\9 cells	576
3	[22]	Universal Logic Gate#1\77 cells	432
4	[8]	Universal Logic Gate#2\ 30 cells	Multi-layer design
5	Proposed in this work	Universal Block\ 9 cells	304

circuit to prove it is fault free. The proposed design caused around 30% complexity reduction in the full adder circuit compared to previous designs

Declaration of Competing Interest

All authors certify that they have no affiliations with or involvement in any organization or entity with any financial interest or non-financial interest in the subject matter or materials discussed in this manuscript, and they did not receive any financial support regarding this work.

Data availability

No data was used for the research described in the article.

References

[1] S.S. Ahmadpour, M. Mosleh, S. Rasouli Heikalabad, Efficient designs of quantum-dot cellular automata multiplexer and RAM with physical proof along with power analysis, J. Supercomput. 78 (2022) 1672–1695.
[2] D. Ajitha, K.V. Ramanaiah, V. Sumalatha, An Efficient Design of XOR Gate And Its Applications Using QCA, i-manager's J. Electron. Eng. 5 (2015) 22–29.
[3] H.M. Ali, E. Alkaldy, M.S. Zainal, B.N. Danial, A new 5-input majority gate without adjacent inputs crosstalk effect in QCA technology, Indones. J. Electr. Eng. Comput. Sci. 14 (2019) 1159–1164.
[4] E. Alkaldy, A.H. Majeed, M.S. Bin Zainal, D. Bin Md Nor, Optimum multiplexer design in quantum-dot cellular automata, Indones. J. Electr. Eng. Comput. Sci. 17 (2020) 148–155.
[5] E. Alkaldy, K. Navi, Reliability study of single stage multi-input majority function for QCA, Int. J. Comput. Appl. 83 (2013) 2.
[6] D. Berzon, T.J. Fountain, A memory design in QCAs using the SQUARES formalism, in: Proceedings of the Ninth Great Lakes Symposium on VLSI, 1999, pp. 166–169, 4-6 Mar 1999.
[7] F. Deng, G. Xie, R. Zhu, Y. Zhang, A matrix representation method for decoders using majority gate characteristics in quantum-dot cellular automata, J. Supercomput. 76 (2020) 2842–2859.
[8] M. Hayati, A. Rezaei, Design of a new optimized universal logic gate for quantum-dot cellular automata, IETE J. Res. 68 (2022) 1141–1147.
[9] J. Huang, M. Momenzadeh, L. Schiano, M. Ottavi, F. Lombardi, Tile-based QCA design using majority-like logic primitives, J. Emerg. Technol. Comput. Syst. 1 (2005) 163–185.
[10] C. Labrado, H. Thapliyal, Design of adder and subtractor circuits in majority logic-based field-coupled QCA nanocomputing, Electron. Lett. 52 (2016) 464–466.
[11] C.S. Lent, P.D. Tougaw, A device architecture for computing with quantum dots, Proc. IEEE 85 (1997) 541–557.
[12] C.S. Lent, et al., Quantum cellular automata, Nanotechnology 4 (1993) 49–57.
[13] A. Majeed, E. Alkaldy, S. Albermany, An energy-efficient RAM cell based on novel majority gate in QCA technology, SN Appl. Sci. 1 (2019) 1–8. $V.
[14] A.H. Majeed, E. Alkaldy, M.S. Bin Zainal, D. Bin Md Nor, Synchronous counter design using novel level sensitive T-FF in QCA technology, J. Low Power Electron. Appl. 9 (2019) 1–13.
[15] A.H. Majeed, E. Alkaldy, M. Zainal, K. Navi, D. Nor, Optimal design of RAM cell using novel 2:1 multiplexer in QCA technology, Circuit World 46 (2) (2019) 147–158.
[16] A.H. Majeed, M.S.B. Zainal, E. Alkaldy, D.M. Nor, Full adder circuit design with novel lower complexity XOR Gate in QCA technology, Trans. Electr. Electron. Mater. 21 (2020) 198–207.
[17] V.K. Mishra, Cost aware majority logic synthesis for emerging technologies, in: Proceedings of the IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), 2017.
[18] R. Orbach, F. Wang, O. Lioubashevski, R.D. Levine, F. Remacle, I. Willner, A full-adder based on reconfigurable DNA-hairpin inputs and DNAzyme computing modules, Chem. Sci. 5 (2014) 3381–3387.
[19] A. Srivastava, R. Chandel, A novel co-planar five input majority gate design in quantum-dot cellular automata, IETE Tech. Rev. 39 (4) (2022) 850–864.
[20] M.A. Tehrani, K. Navi, A. Kia-Kojoori, Multi-output majority gate-based design optimization by using evolutionary algorithm, Swarm Evol. Comput. 10 (2013) 25–30.
[21] K. Walus, T.J. Dysart, G.A. Jullien, R.A. Budiman, QCADesigner: a rapid design and Simulation tool for quantum-dot cellular automata, IEEE Trans. Nanotechnol. 3 (2004) 26–31.
[22] Y. Xia, K. Qiu, Design and application of universal logic gate based on quantum-dot cellular automata, in: Proceedings of the 11th IEEE International Conference on Communication Technology, 2008, pp. 335–338, 10-12 Nov. 2008.
[23] Y. Zhang, G. Xie, J. Han, A robust wire crossing design for thermostability and fault tolerance in quantum–dot cellular automata, Microprocess. Microsyst. 74 (2020), 103033.

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