NOVEL NEGATIVE EDGE TRIGGER T FLIP FLOP AND COMPARATOR USING PROPOSED UNIQUE UNIVERSAL GATES

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Abstract: This report delves into the limitations of CMOS technology and the emergence of Quantum-dot Cellular Automata (QCA) as a viable alternative. It introduces a novel low-complexity singular block serving as a universal gate in QCA circuits, facilitating versatile logic functions including AND, OR, NOT, and XOR. The report incorporates a novel comparator circuit using the unique universal logic gates. Furthermore, it presents a new QCA negative edge trigger T Flip-Flop design aimed at enhancing the circuit's efficiency. Leveraging these advancements, the novel proposed designs of comparator and T flip flop is compared with two other counter parts and the difference in parameters are tabulated, contributing to the ongoing pursuit of efficient nanoelectronics systems.

Keywords: Novel comparator circuit, Novel T flip flop, Quantum-dot Cellular Automata (QCA).

1. Introduction

Quantum-dot Cellular Automata (QCA) stands at the forefront of nanoelectronics, promising revolutionary advancements in electronic circuit design. First conceived in the mid-1990s as a potential successor to traditional semiconductor technologies like Complementary Metal-Oxide-Semiconductor (CMOS), QCA harnesses the unique properties of quantum dots to store and manipulate information [1]. Unlike CMOS, which relies on the movement of electrical charges, QCA leverages quantum mechanical phenomena such as electron tunneling for logic operations, enabling the potential for higher speeds and lower power consumption [1].

The allure of QCA lies in its ability to create ultra-fast, low-power devices with remarkable integration capabilities, presenting a tantalizing prospect for the future of computing. However, despite its immense potential, QCA is still in its nascent stages of development, facing numerous challenges before widespread commercial adoption can be realized. Nonetheless, the technology has garnered significant interest from both academia and industry, fueling an active landscape of research and development in the field of nanoelectronics.

One crucial aspect of QCA circuit design is the utilization of different logic gates, including AND, OR, NOT, XOR, and MUX, each with unique topologies optimized for QCA technology. The universal gate holds particular importance, offering designers the flexibility to construct complex circuits while potentially revolutionizing manufacturing and production costs [2].

In this paper, I proposed a novel structure for the Comparator circuit and T flipflop using universal logic gates [1] in QCA technology, aiming to address existing limitations and push the boundaries of performance. Our latter design offers enhancements over traditional circuits, particularly in multi-level counters, showcasing the transformative potential of QCA in practical applications. This paper unfolds with an exploration of QCA fundamentals, followed by a review of related work and an in-depth presentation of our innovative T Flip-Flop design. Simulation results and comparative analyses validate our approach, culminating in a discussion of implications and future research directions. Through this endeavor, we contribute to the ongoing evolution of QCA technology and its journey towards realizing its full potential in the realm of nanoelectronics.

2. Background

In QCA technology, the information is transmitting between cells using the principle of electronic repulsion, so there is no current flow in this technology, but it required moving the cell state to the adjacent cell. So, it is important to control the data flow from the input cell toward the output. The direction of the information flow is controlled using a clock signal. The clock signal controls the barrier between dots to give electrons the ability to tunnel between cell dots or prevent it. 1n general, large circuits are divided into multiple zones. The clock signal in each zone passes through four phases (switching phase, holding phase, releasing phase and relaxation phase) as shown in Fig. 3. These phases are important for the circuit to remain near the ground state, so if these phases work consequently, we can say the circuit runs near to the ground state. [1,2]

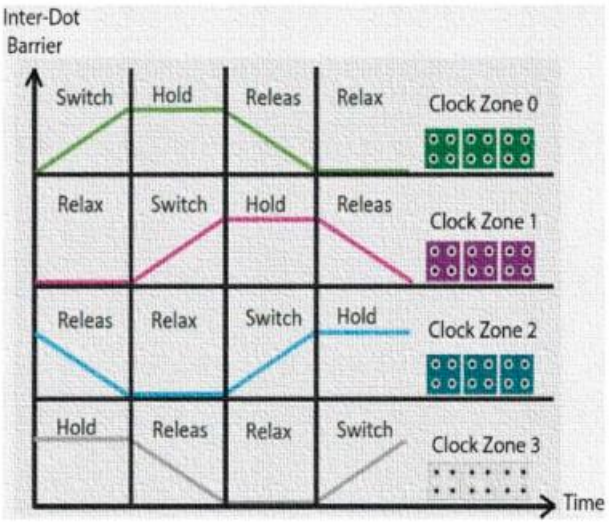


Fig. 3. Clock signal phases in four zones.

3. Related Work

Several studies have focused on enhancing the functionality and efficiency of Quantum-dot Cellular Automata (QCA) circuits, particularly in the realm of logic design and counter optimization. The SQUARES methodology proposed in previous work attempted to establish a 5 × 5 QCA cell grid as a fundamental building block, yet encountered challenges related to area overhead and timing complexity. Another approach, the tile-based design, introduced novel "MV-like tiles" that combined the logic functions of Majority Voter (MV) and Inverter (INV) blocks, demonstrating improved area efficiency and applicability as basic primitives for logic design [2].

In the pursuit of developing versatile universal blocks for QCA circuits, various proposals have emerged. Prior studies introduced complex universal gates, such as the pre-suggested gate requiring 77 cells and two types of cells, and another design demanding 30 cells and multi-layer implementation. These endeavours underscore the ongoing exploration of efficient and scalable solutions in QCA circuit design.[2]

Within the domain of counter design, significant attention has been devoted to optimizing QCA-based T Flip-Flops, essential components for synchronous counters. Researchers have investigated diverse aspects, including clocking strategies for synchronization, fault tolerance, and error correction mechanisms. Despite the advantages offered by T Flip-Flops in QCA technology, concerns persist regarding the insertion of rotated cells and increased cell count, potentially undermining the compactness and efficiency promised by QCA technology.[1]

Overall, the literature reflects a concerted effort to advance QCA technology through innovative designs and methodologies, laying the groundwork for further exploration and refinement in the field of nanoelectronics.

4. Proposed Universal Logic gate

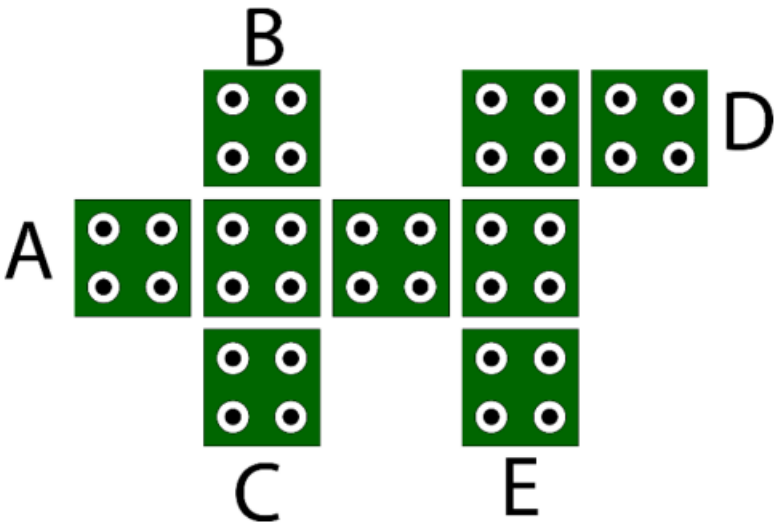


Fig. 5. Proposed universal block.

The primary contribution of this work lies in the introduction of a novel block comprising only 9 cells, capable of functioning as AND, OR, NOT, MUX, and XOR gates. This versatile feature holds significant commercial potential for the future of Quantum-dot Cellular Automata (QCA) technology. The proposed block is designed optimally, emphasizing efficiency in terms of both area and cell count, as depicted in Fig. 5.

Programming the proposed block is achieved through a straightforward procedure: [2]

- For AND gate functionality: Connect inputs A and B, set C and D to logic 0, with E representing the output cell.

- For OR gate functionality: Connect inputs A and B, set C and D to logic 1, with E representing the output cell.

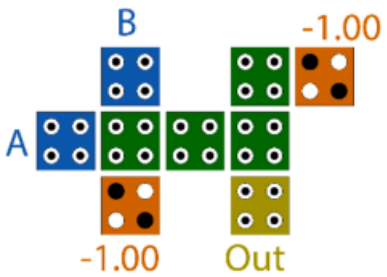
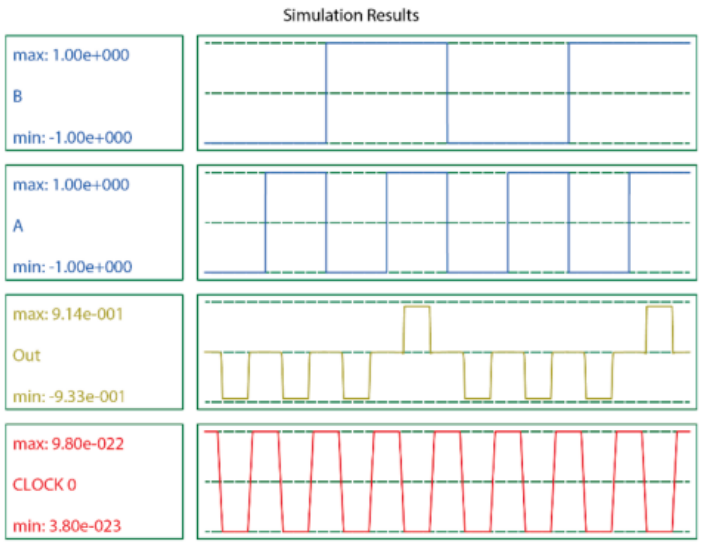
- For NOT gate functionality: Utilize B as the input cell, fix A and C as logic 1, set D as logic 0, and designate E as the output cell.

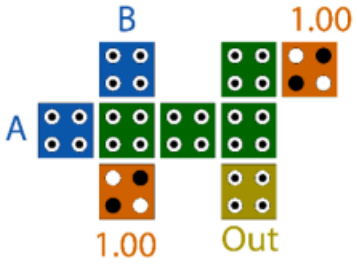
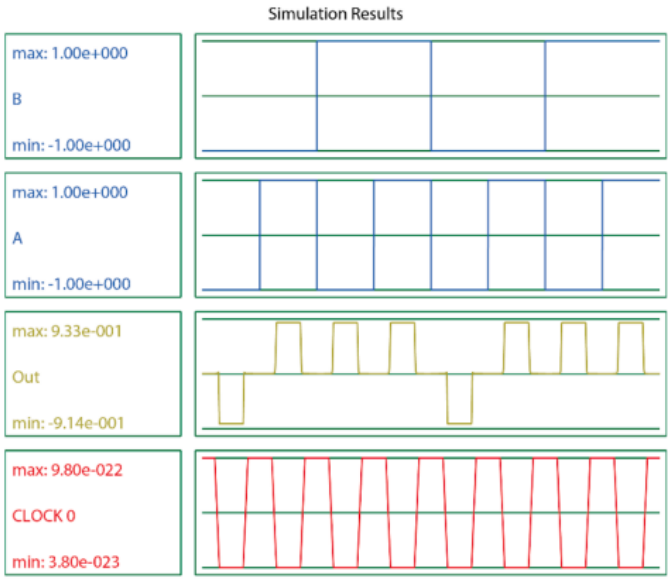
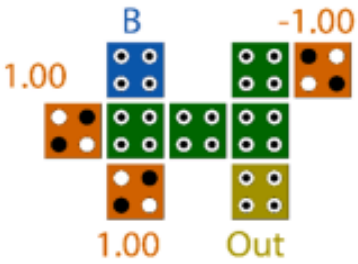
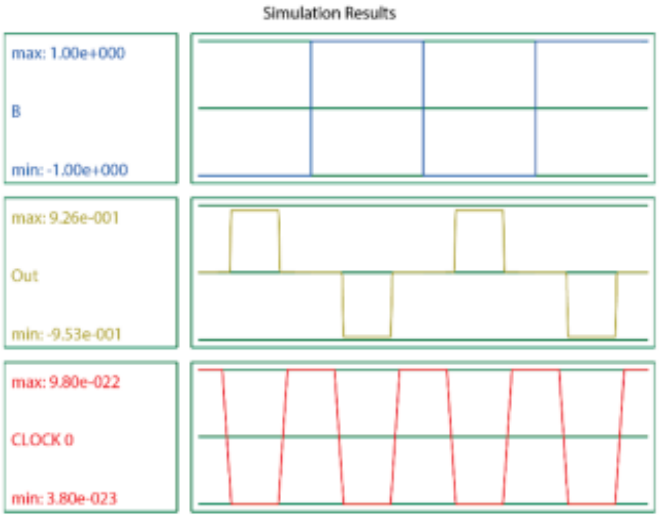
- For XOR gate functionality: Fix A as logic 1, employ B and C as input cells, set D as logic 0, and designate E as the output cell (previously proposed in [16]).

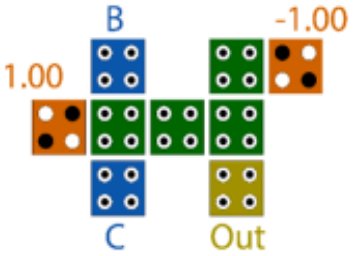
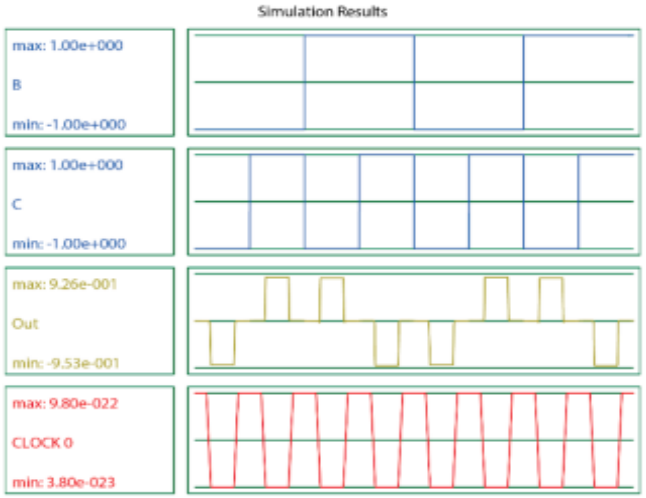
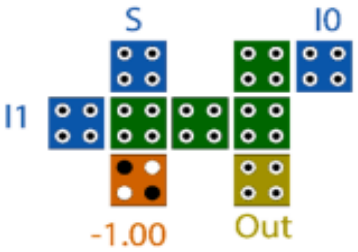
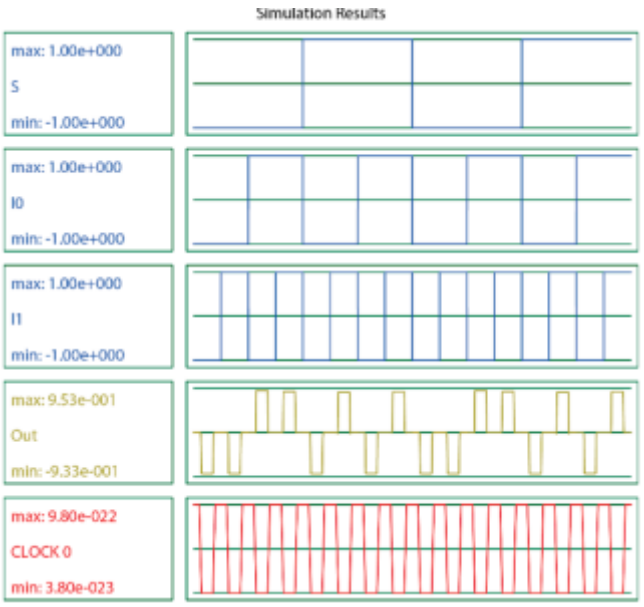
- For MUX gate functionality: Utilize B as the selector, set D as I0, designate A as I1, fix C as logic 0, and designate E as the output cell (previously proposed with minor modifications in [2]).

This novel block not only offers versatile functionality but also addresses commercial viability and efficiency concerns, making it a noteworthy advancement in QCA circuit design.

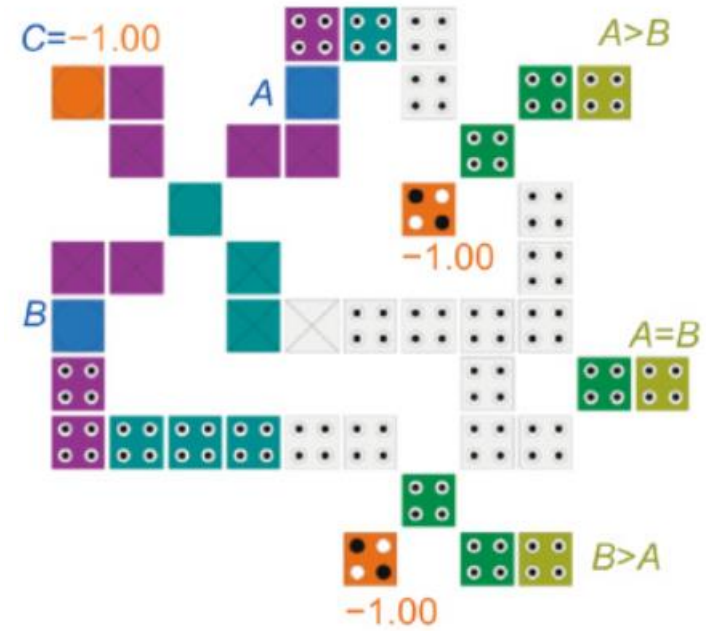
Proposed Universal gates

GATES	QCA CELLS	OUTPUT WAVEFORM
AND		

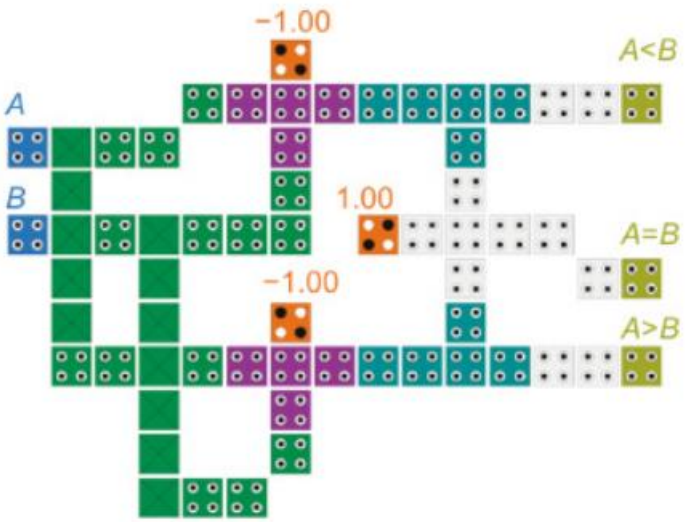
OR	 B 1.00 A 1.00 Out	 Simulation Results max: 1.00e+000 B min: -1.00e+000 max: 1.00e+000 A min: -1.00e+000 max: 9.33e-001 Out min: -9.14e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023
NOT	 B -1.00 1.00 1.00 Out	 Simulation Results max: 1.00e+000 B min: -1.00e+000 max: 9.26e-001 Out min: -9.53e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023

XOR	 B -1.00 1.00 C Out	 Simulation Results max: 1.00e+000 B min: -1.00e+000 max: 1.00e+000 C min: -1.00e+000 max: 9.26e-001 Out min: -9.53e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023
MUX	 S I0 I1 -1.00 Out	 Simulation Results max: 1.00e+000 S min: -1.00e+000 max: 1.00e+000 I0 min: -1.00e+000 max: 1.00e+000 I1 min: -1.00e+000 max: 9.53e-001 Out min: -9.33e-001 max: 9.80e-022 CLOCK 0 min: 3.80e-023

Other 1-bit comparators for comparison



[8]



[9]

5. Proposed structure of 1 bit comparator

1 BIT COMPARATOR CIRCUIT USING PROPOSED UNIVERSAL LOGIC GATES

CIRCUIT DIAGRAM

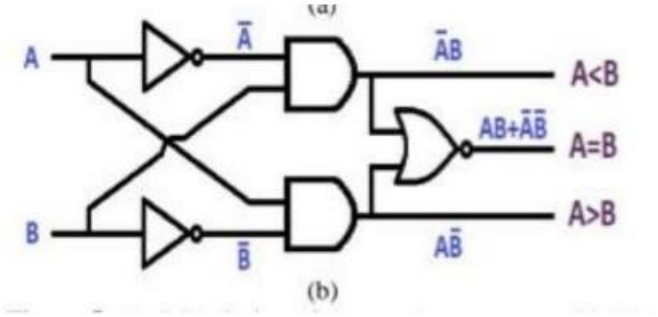


Fig. Circuit diagram of Comparator

QCA CELL STRUCTURE OF COMPARATOR

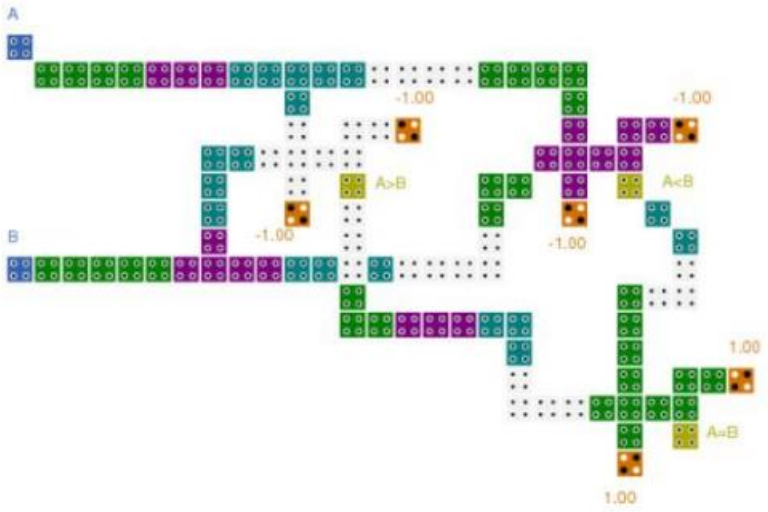


Fig. Proposed Comparator circuit

Result

Output Waveform of Comparator

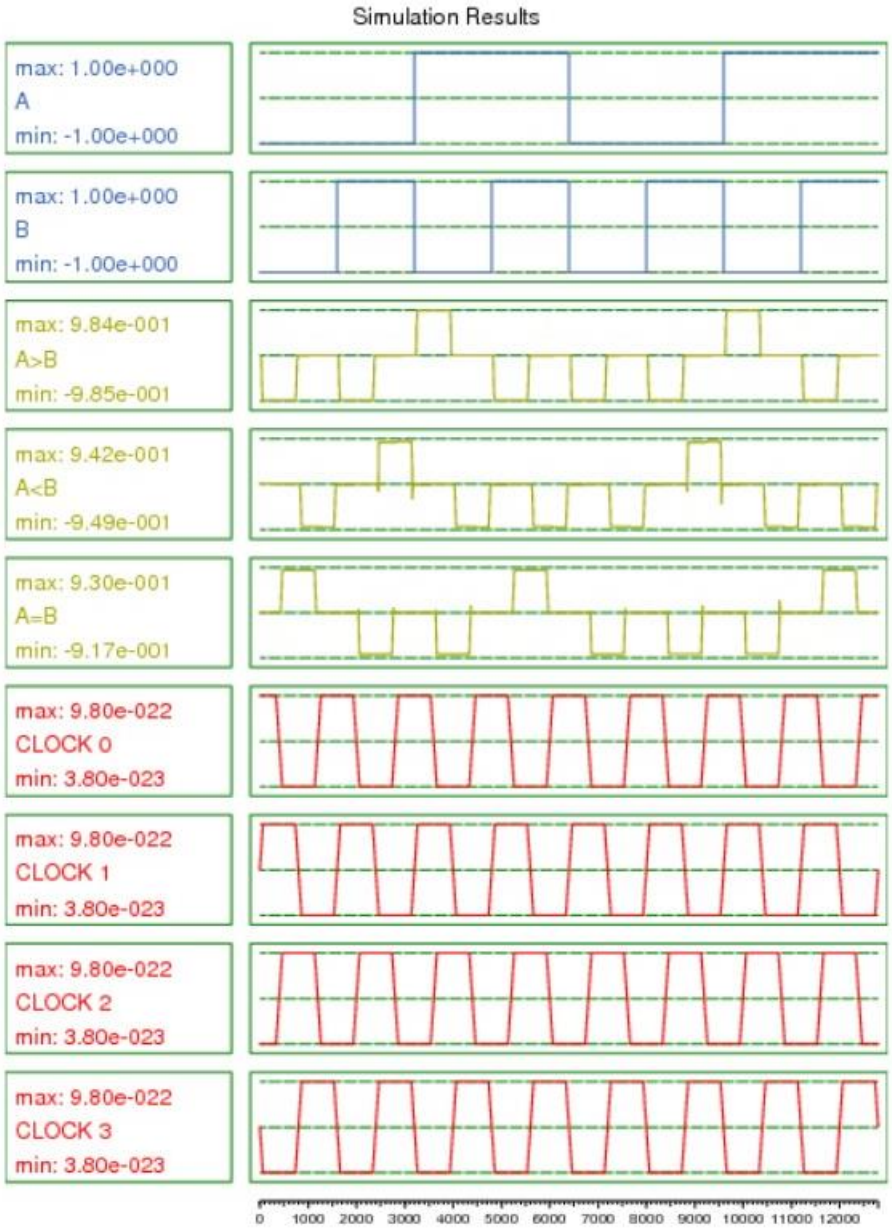
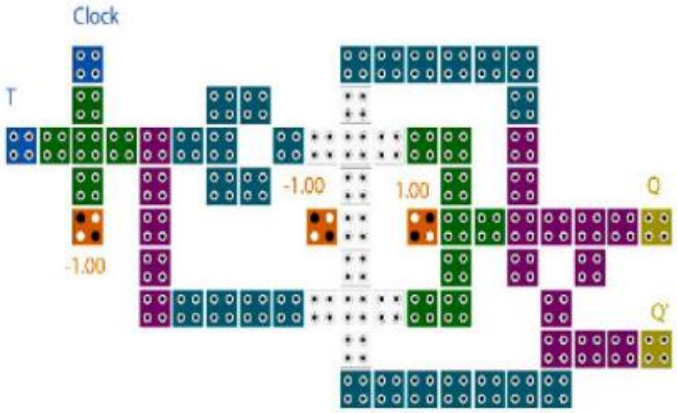
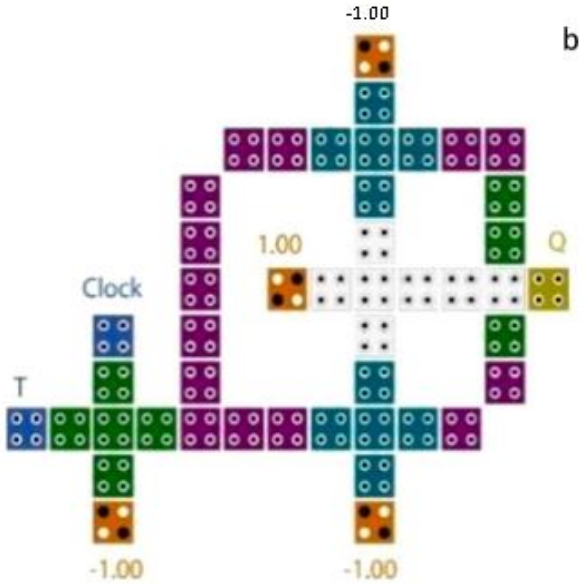


Fig. Simulated output waveform of Comparator

Other T Flip Flop circuits for comaprison



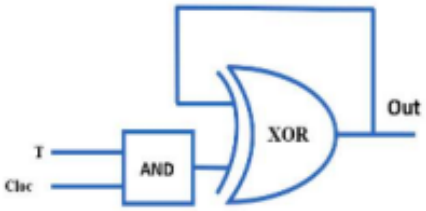
[6]



[7]

5. Proposed structure of T flip flop

CIRCUIT DIAGRAM AND QCA CELLS REPRESENTATION OF PROPOSED T FLIP FLOP



T Flip Flop Circuit diagram

[1]

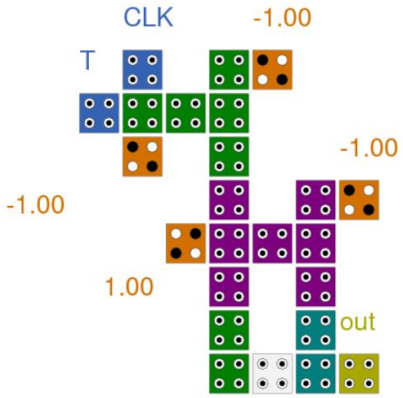


Fig. Proposed Novel Negative Edge Trigger T Flip Flop

Mechanism of negative edge trigger T flip flop

- A negative-edge-triggered T Flip-Flop is a digital circuit that changes its output state (out) only when it detects a falling edge on its clock input (CLK).
- The proposed circuit has two inputs namely T and CLK and one output state (out).
- The output of the T flip flop is toggled every time the falling edge of the clock is encountered.

Result

Output Waveform of negative edge trigger T flip flop

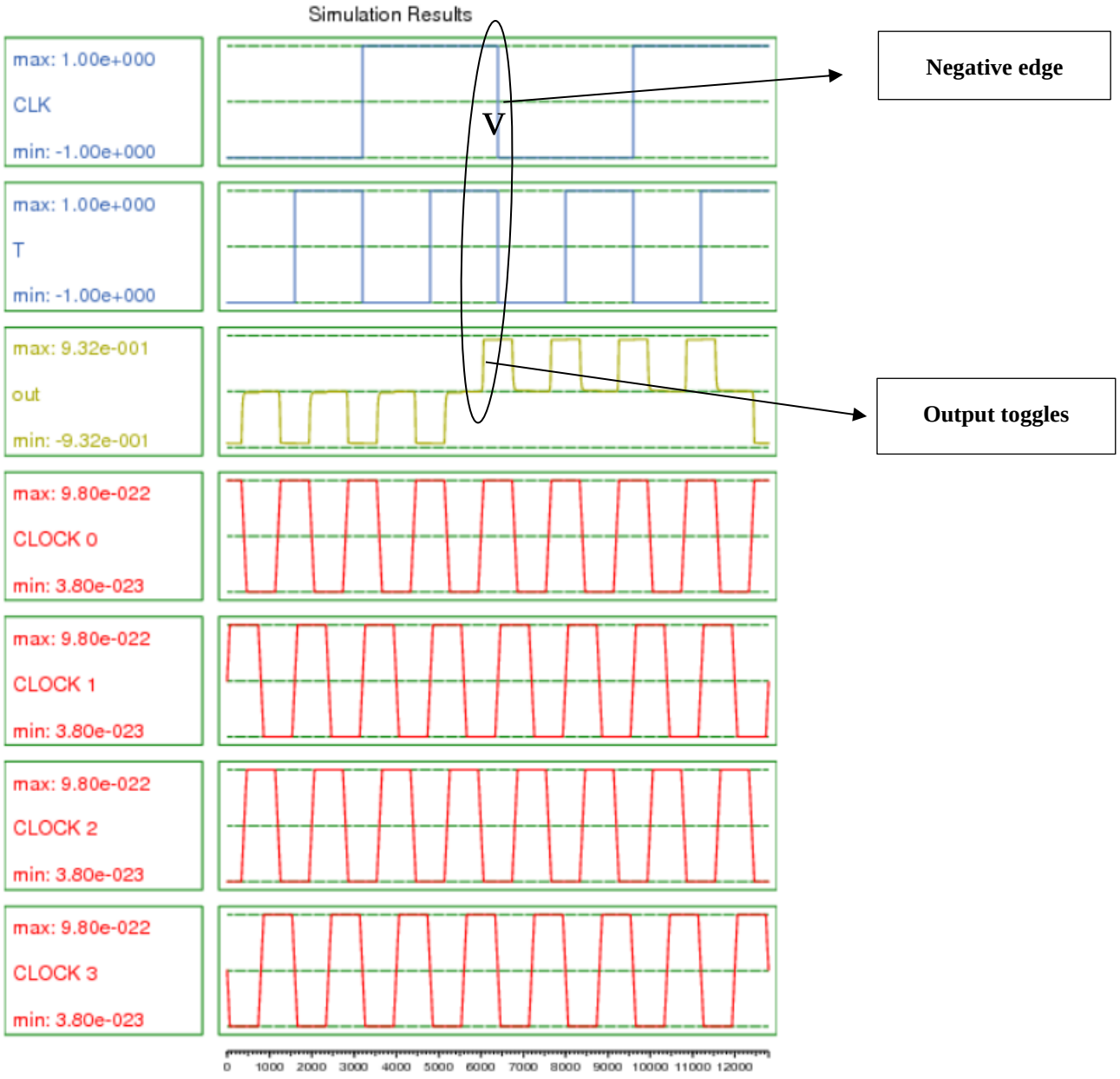


Fig. Simulated output waveform of negative edge trigger T flip flop

Tabulated Results and Observation of 1-bit comparator

PARAMETERS	NO OF CELLS	APPROX. AREA	LATENCY	ENERGY DISSIPATED IN ONE CYCLE	TEMPERATURE ANALYSIS OBSERVATION
[8]	43 CELLS	0.05mu m^2	1s	Total energy dissipation (Sum_Ebath): 9.09e-003 eV (Error: +/- -7.47e-004 eV) Average energy dissipation per cycle (Avg_Ebath): 8.27e-004 eV (Error: +/- -6.79e-005 eV)	Clearer at 1K, and flatlines at 21K Decrease in Energy Dissipation and in error rate as temperature increase, observed due to lack of waveform.
[9]	63 CELLS	0.08mu m^2	2.7 s	Total energy dissipation (Sum_Ebath): 2.04e-002 eV (Error: +/- -1.78e-003 eV) Average energy dissipation per cycle (Avg_Ebath): 1.86e-003 eV (Error: +/- -1.61e-004 eV)	Clearer at 1K, and flatlines at 15K Decrease in Energy Dissipation and in error rate as temperature increase, observed due to lack of waveform.
PROPOSED COMPARATOR CIRCUIT	106 CELLS	2.120 mu m^2	1s	Total energy dissipation (Sum_Ebath): 2.43e-002 eV (Error: +/- -1.85e-003 eV) Average energy dissipation per cycle (Avg_Ebath): 2.21e-003 eV (Error: +/- -1.68e-004 eV)	Clearer at 1K, and flatlines at 45K Decrease in Energy Dissipation and in error rate as temperature increase, observed due to lack of waveform.

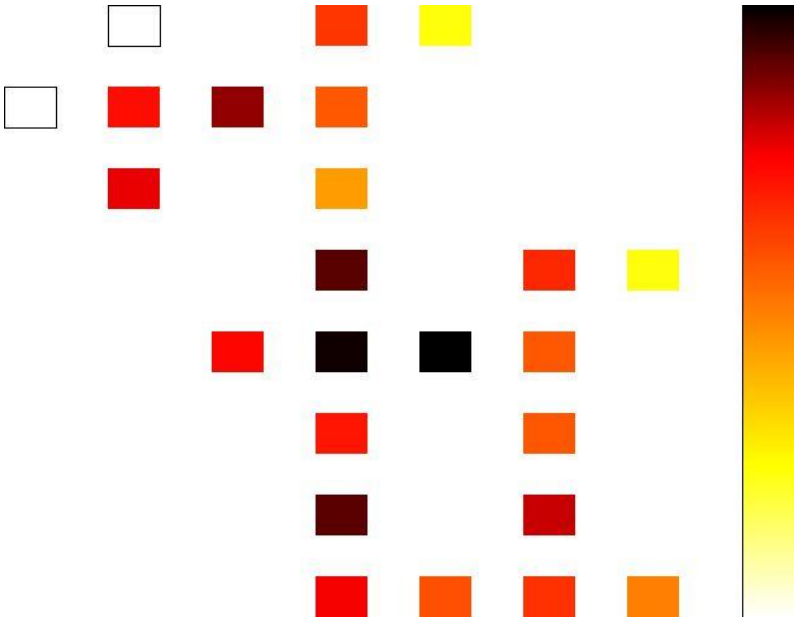
Tabulated Results and Observation of T Flip Flop

PARAMETERS	NO OF CELLS	APPROX. AREA	LATENCY	ENERGY DISSIPATED IN ONE CYCLE	TEMPERATURE ANALYSIS OBSERVATION
[6]	73 CELLS	0.08 mu^2	1s	Total energy dissipation (Sum_Ebath): 2.18e-002 eV (Error: +/- -1.84e-003 eV) Average energy dissipation per cycle (Avg_Ebath): 1.98e-003 eV (Error: +/- -1.67e-004 eV)	Clearer at 1K, and flatlines at 23K Decrease in Energy Dissipation and in error rate as temperature increase, due to lack of waveform.
[7]	46 CELLS	0.06 mu^2	1s	Total energy dissipation (Sum_Ebath): 1.95e-002 eV (Error: +/- -1.84e-003 eV) Average energy dissipation per cycle (Avg_Ebath): 1.78e-003 eV (Error: +/- -1.67e-004 eV)	Clearer at 1K, and flatlines at 20K Decrease in Energy Dissipation and in error rate as temperature increase, due to lack of waveform.
PROPOSED NEGATIVE EDGE TRIGGER T FLIP FLOP	24 CELLS	0.05 mu^2	0s	Average energy dissipation per cycle (Avg_Ebath): 6.59e-004 eV Error: +/- -6.25e-005 eV Total simulation time: 7 s For calculating energy dissipation	Clearer at 1K, and flatlines at 45K Decrease in Energy Dissipation and in error rate as temperature increase, due to lack of waveform.

POWER DISSIPATION ANALYSIS AT 0.5 Ek

FOR 1 BIT COMPARATOR

FOR NEGATIVE EDGE TRIGGER T FLIP FLOP



7. Conclusion

In conclusion, the integration of the proposed universal logic gates in the design of a negative edge trigger T Flip-Flop and comparator, represents a significant advancement in QCA technology. The reduced complexity, demonstrated fault-free operation, and around 30% reduction in complexity compared to prior designs highlight the efficiency and practicality of the proposed approach. Additionally, the absence of reliance on the corner inverter enhances the robustness and reliability of the circuits, further reinforcing their potential for real-world applications. Overall, the successful implementation of the T Flip-Flop and Comparator circuits underscores the promising trajectory of QCA technology in advancing digital circuitry.

8. Future Work

- To develop a more robust circuit with further analysis
- Optimize performance metrics like power consumption and speed, and assess scalability.
- Can implement n-bit counters using the novel T flip flop.

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