Indian Institute of Information Technology, Sri City, Chittoor

Name of the Exam: Digital Design SET2 Duration: 60+30 mins (for uploading) Max. Marks: 18

Question 1 to 4: 4 marks each, Question 5: 2 marks

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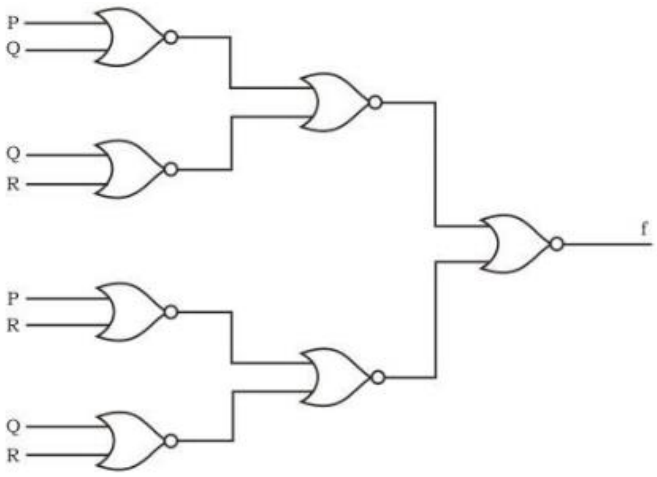
1. For the given circuit diagram (NOR gates), applying Boolean algebra find the minimized expression for ouput F=



2. Design a Full subtractor using two half subtractors (include truth table, K-maps, logic expression and diagram)

3. Write the truth table of 8x3 enoder by encoding single bit 0. Include logic expression and circuit diagram. Represent inputs D0 to D7, and outputs X, Y and Z.

4. 1) Simplify into SOP using K-maps and draw the logic diagram for simplified expression
   i) F(a,b,c,d)=∑(0,1,2,5,8,9,10) ii) F(a,b,c,d)=∑(0,2,4,5,6,7,8,10,13,15)

5. Write the complete truth table of BCD to 7 segment decoder. (K-maps and circuit diagram not required)