Indian Institute of Information Technology Sri City Chittoor

Name of the Exam: Embedded Systems (ES) Duration: 90 mins Max. Marks: 30 Marks

Instructions:

1. Closed book exam
2. Must turn on video and mic throughout the exam.
3. Please keep enough A4 sheets to write answers. Each A4 should have your Name, Roll number and page number on the top right corner.
4. Charge your laptops and mobiles ahead of exam to avoid issues during the exam. Suggested to keep alternate mobile phones in case of network issues
5. Total Exam session will be recorded.
6. Each student should start scanning the answer scripts in the order from 12:30 PM and should submit before 12:40 PM as a single pdf document through the shared google classroom link. File name: **Roll_No_Name_Set2_ES_21.pdf**
7. Assumptions made should be clearly stated
8. All sub-parts of the question should be written together

I. a) Explain SAR ADC with block diagram? Derive the bit pattern Step by step following the algorithm for
i) 4 bit and ii) 6 bits. for Vref = 5 volts, Vin = 2.32 volts?
iii)Calculate the errors for both 4 bit and 6 bit? [2 +2+2M]

b) Explain the Top down approach (5 phases) of a Bluetooth speaker with a display to show the song details and options to attach a pen drive/sd card [4M]
Note: State the assumptions clearly

II.

a) Write Embedded C code to calculate the RMS value of a signal with an 10 bit ADC of a Arduino Uno board? [4M]

b) Write Embedded C code to configure two channels (voltage V and Current I) of an single ADC of an Arduino UNO board for computing power of the given signals? Mention the difficulties when you have to sample DC signals and AC signals? (6M)

Note: Power -- $\mathrm{P} = (\sum_{k=1}^{n} \mathrm{V(k)} * \mathrm{I(k)})/\mathrm{n}$

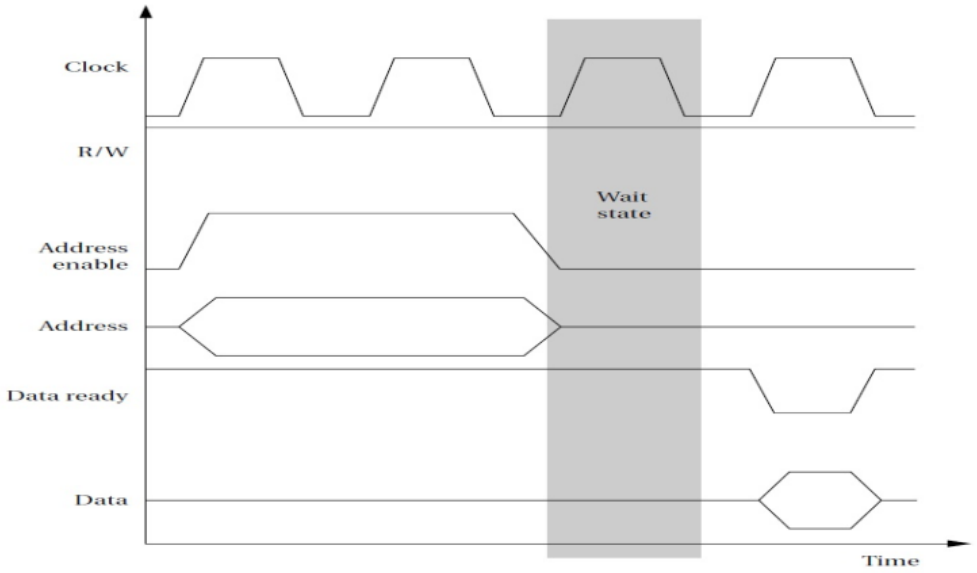
Assume both Voltage and current waveform are Symmetric periodic waveforms of 50 Hz

III.

a. An interrupt should be generated for 8 seconds. Basic clock frequency of the microcontroller system is 8 MHz with (Fosc/8). Prescaler: 1:256, Timer is using a 16bit register realization. Calculate the register contents of the timer to generate the interrupt assuming the counter is up counter (from 0 to 65535) assuming there is no overload to load the register. [4M]

b. Master and Slave cannot be interchanged in SPI compared to I2C. Justify [2M]

c. Explain briefly the below bus timing timing diagram ? [4M]


Clock
R/W
Wait state
Address enable
Address
Data ready
Data
Time

---------- All the best ----------