Part – A (12 X 0.5 = 6 Marks)

1. What is the formula to calculate the performance of the processor?

2. How many bits constitute a word?

3. What is an address?

4. The decoded instruction is stored in_____
   a) TR b) PC c) Registers d) MDR

5. What is the Arithmetic Left Shift of 110110.

6. Define clock rate.

7. What are the two modes in CPU?

8. List one function of ALU.

9. Name few classifications of computer.

10. What is DMA?

11. What are the condition codes in status bit register?

12. List out the instructions handled during interrupt handling.

Part – A (12 X 0.5 = 6 Marks)

1. The two circuits are interconnected by a circuit called as -----------
2. -------------- is set of rules that govern the behavior of various devices connected to the buses.
3. List out the two types of bus arbitration.
4. The DMA is said to steal memory cycles from the processor called ---------
   a) Burst stealing b) Cycle stealing c) Block stealing
5. --------------------------- signal indicates the master is ready for a transaction.
6. Series port transfers and receives data one bit at a time (True/False).
7. The 1's complement of 1101 is ---------
8. The array multiplication of 11 *01 is ----------.
9. The time delay for sum in a ripple carry adder is ---------.
10. The two types of integers are --------- and --------------.
11. List out one disadvantage in a carry look ahead adder.
12. The 1's complement and 2's complement for 11 are ----------- and ---------.

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Part – A (12 X 0.5 = 6 Marks)

1. Give examples for Volatile and Non-Volatile memories.
2. What is the purpose of Cache Memory?
3. Differentiate RAM and ROM.
4. _____ is the full form of SIMM.
5. _____ is the full form of DIMM.
6. Expand PROM, EPROM.
7. Give one advantage of EEPROM.
8. Expand ABR and DBR.
9. Give one example for Secondary Storage Device.
10. What is meant by Carry- Look ahead Adder?
11. Solve 1101 * 1011 by using Manual Multiplication Algorithm.
12. Find the Sum of Adding 2 numbers +7 and +4.

Part – A (12 X 0.5 = 6 Marks)

1. _____ is a mechanism that allows a device to signal the CPU that it needs attention.

2. Which of the following is NOT a standard I/O interface?

   a) PCI Bus   b) SCSI Bus   c) USB   d) SATA Bus

3. _____ bus is typically used for high-speed communication between a computer and its hard drives?

4. The _____ is a set of wires or pathways that allows data to be transmitted between components of a computer system.

5. The term I/O stands for _____ and _____.

6. SRAM and DRAM stands for------------

7. The bus that connects the CPU and memory is known as the _____ bus.

8. What is cache?

9. The primary type of semiconductor memory used for storing program instructions and data in a computer is called _____

10. Types of ROMS are _____, _____, _____ & _____

11. Replacement algorithms in cache memories determine which _____ to evict when new data needs to be cached.

12. Virtual memory is a technique that allows the computer to use _____ as an extension of physical memory.

Part – A (12 X 0.5 = 6 Marks)

1. A multicore computer system contains multiple CPUs on a single chip. True/false

2. Which of the following factors affects the performance of a computer system? a. Clock rate b. Instruction set c. Number of CPUs d. All of the above

3. The addressing mode, where you directly specify the operand value is

   _____

4. The purpose of an interrupt is to a) Speed up the processor b) Allow devices to communicate with each other c) Allow devices to signal the CPU that they need attention d) Control the flow of data to and from a device

5. The clock rate of a CPU is measured in _____.

6. RISC stands for-------------

7. Computer address bus is -a)Multidirectional b)Bidirectional c) Unidirectional d)None of the above

8. Change the given Instruction into RTN Instruction format. "ADD A,B"

9. The method of accessing the I/O devices by repeatedly checking the status flags is a) Program controlled I/O b) Interrupt driven I/O c) DMA d) None

10. A CISC instruction set typically has fewer, simpler instructions than a RISC instruction set. (True/False)

11. In queue insertion operation is called as---------

12. Mov B,A is -------------addressing modes.