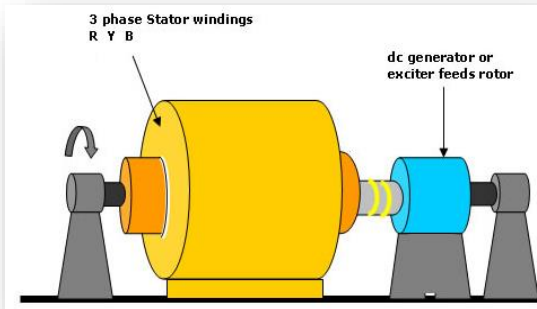


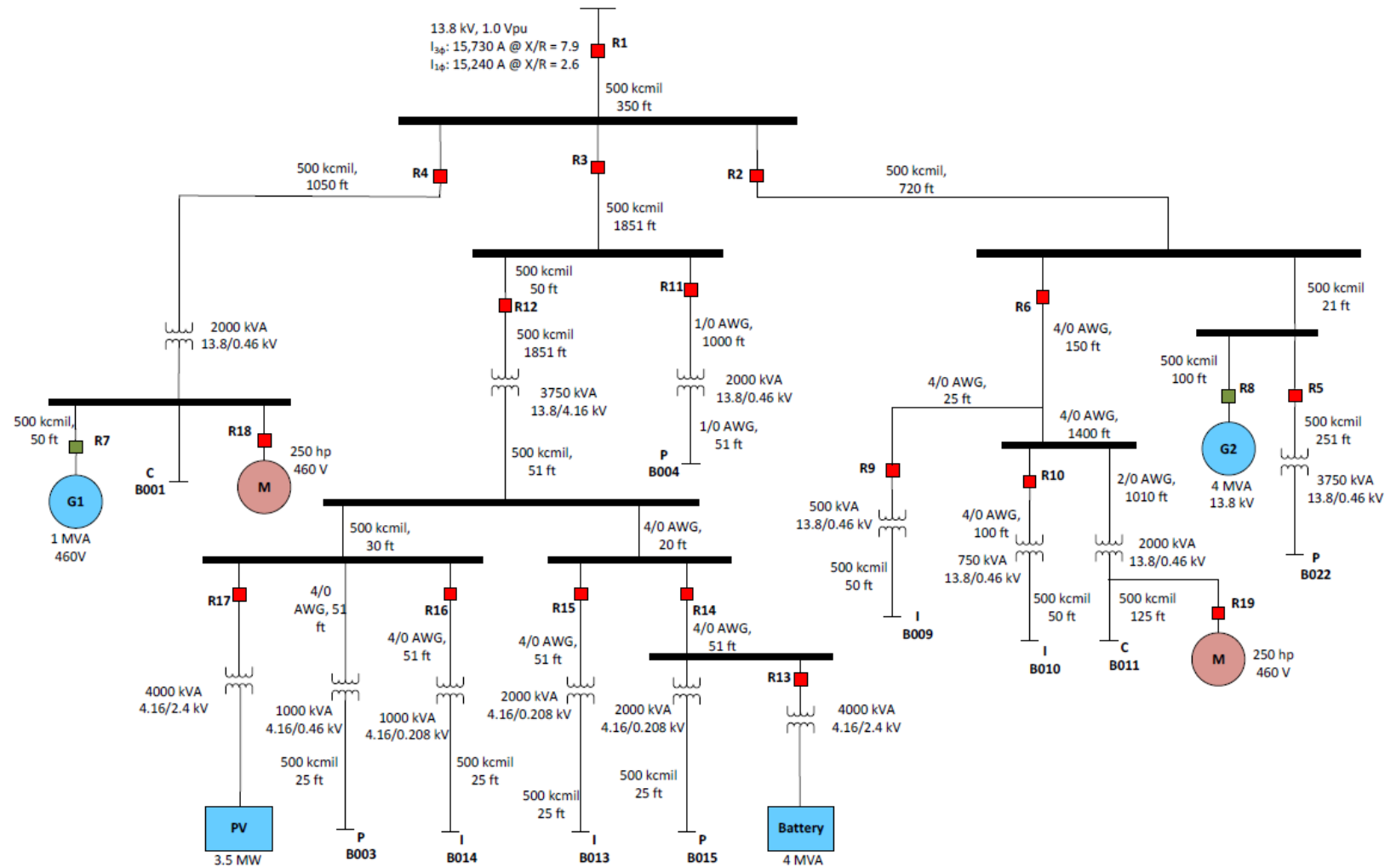
Preparing MIT Lincoln Lab Microgrid Model for Real-time Speedgoat Benchmarking Preparation



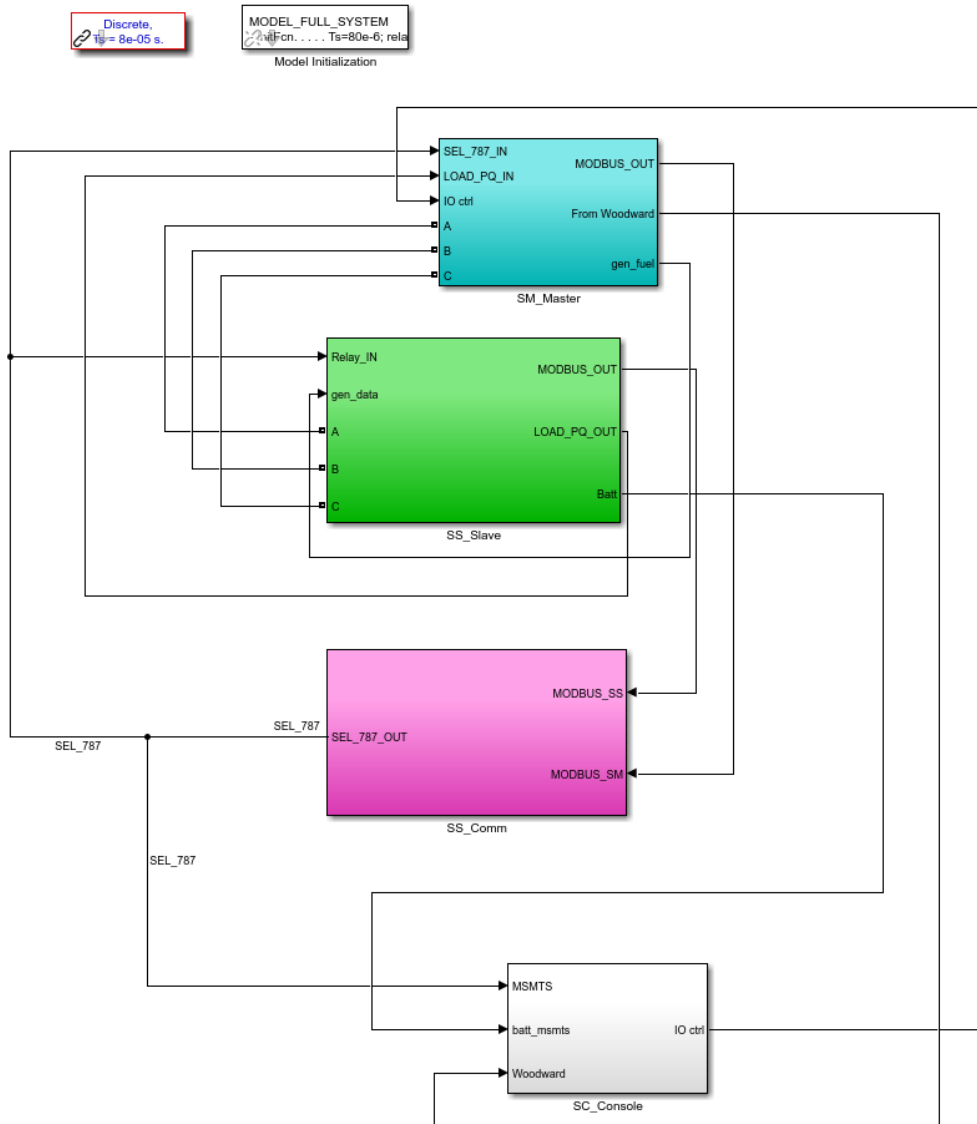
Jonathan LeSage, PhD

Application Engineer – Energy and Automation

MIT Lincoln Lab Microgrid Model

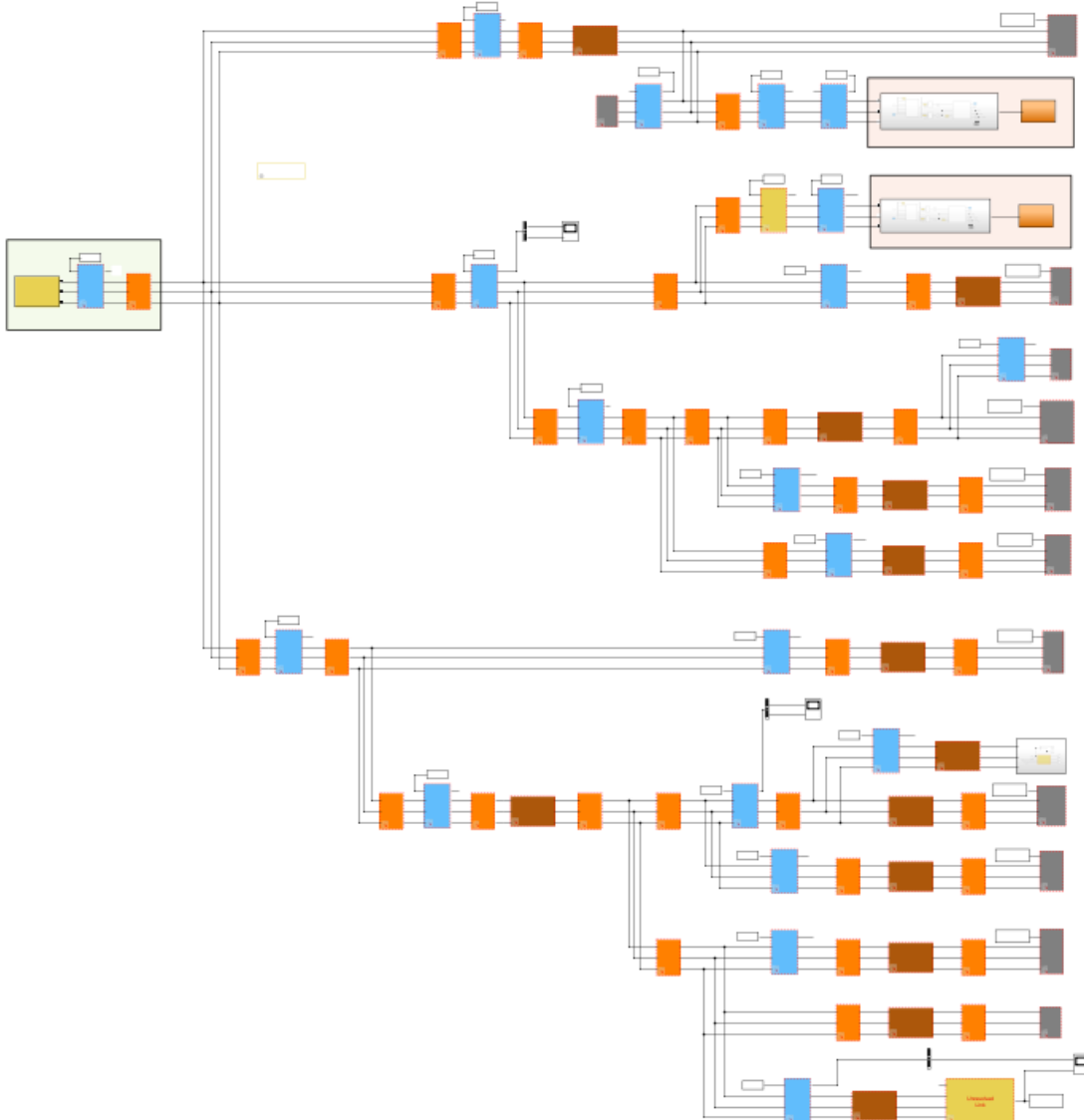


MIT Lincoln Lab Microgrid Model

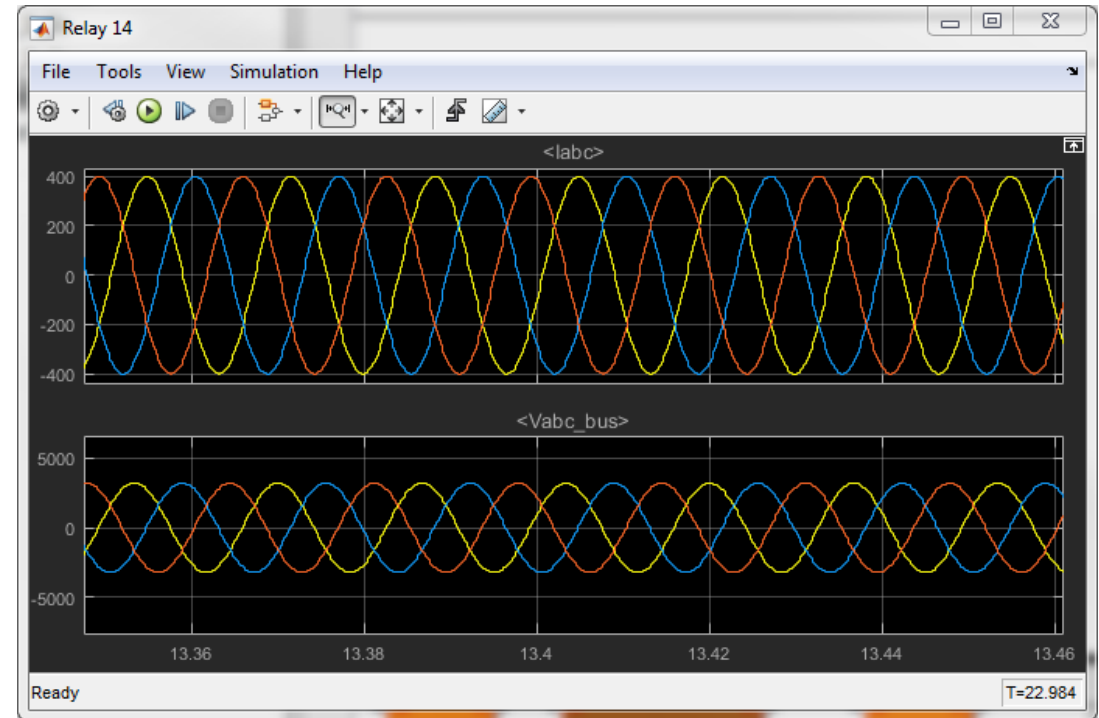


- Developed for 2015 Microgrid Symposium
 - Collaboration with Eaton and Schneider Electric
 - Real-time platform by Opal-RT
- Hardware-in-the-Loop Interfaces
 - Digital and Analog I/O (Generator controllers)
 - MODBUS TCP (Microgrid Controller)
- Simulation Details
 - 80 us (12.5 kHz)
 - No power electronics, high rates for fault transients
- Initial Model Review
 - Opal-RT blocks
 - Using pre-2014a SPS blocks (limitations)
 - No desktop only simulation

Desktop Simulation of MIT Lincoln Lab Microgrid



- Re-created Desktop Only Simulation
 - Use MIT LL simulated generator controls
 - Removed Opal-RT/Hardware Interfaces



Additional Modifications to Improve Simulation Performance

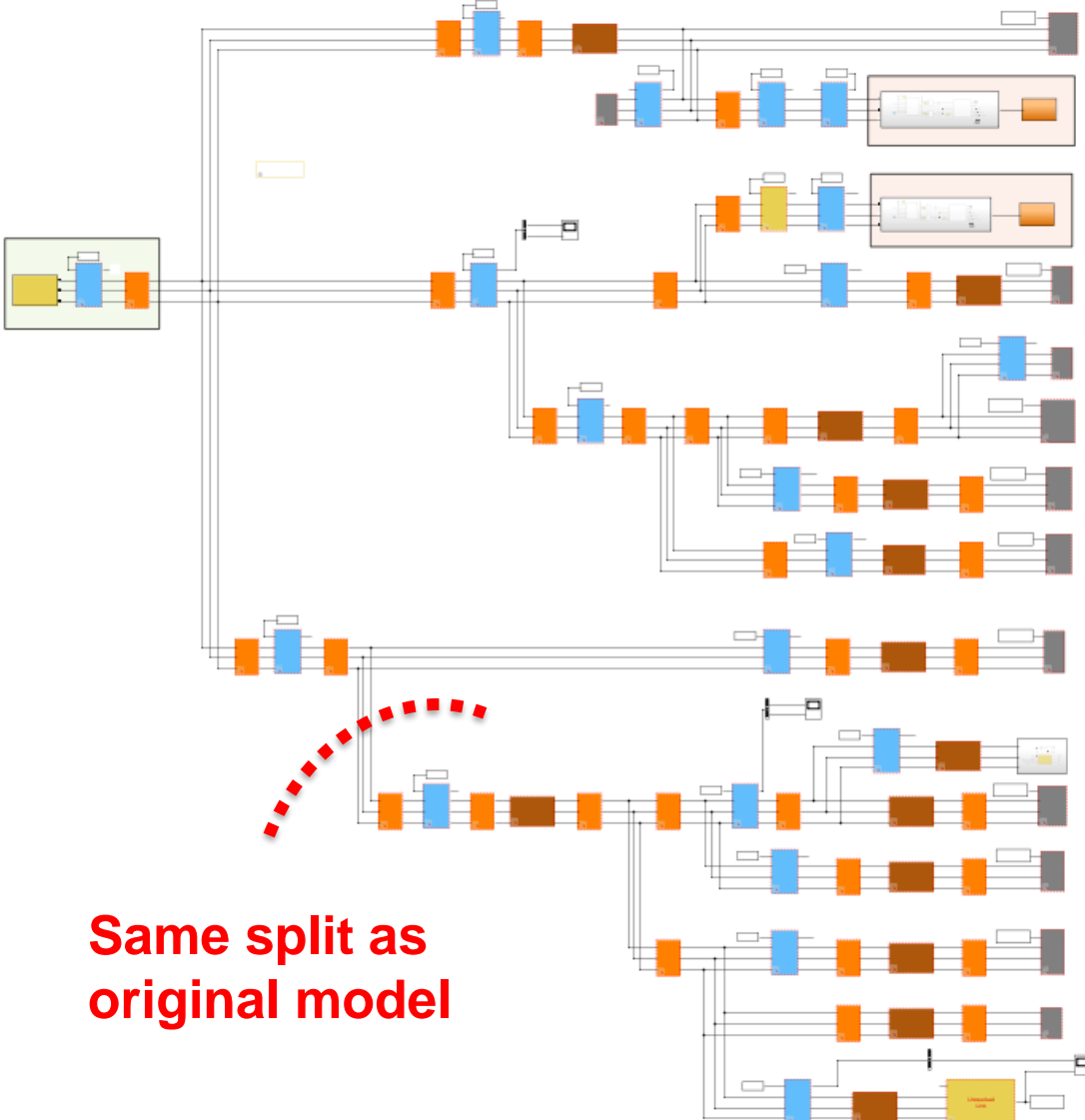
- Removed all “continuous” state blocks -> allows pure “discrete” fixed-step solver
- Selected new solver Tustin/Backward Euler (TBE)
- Upgraded old SPS blocks to R2016b -> improved computational performance

Details:

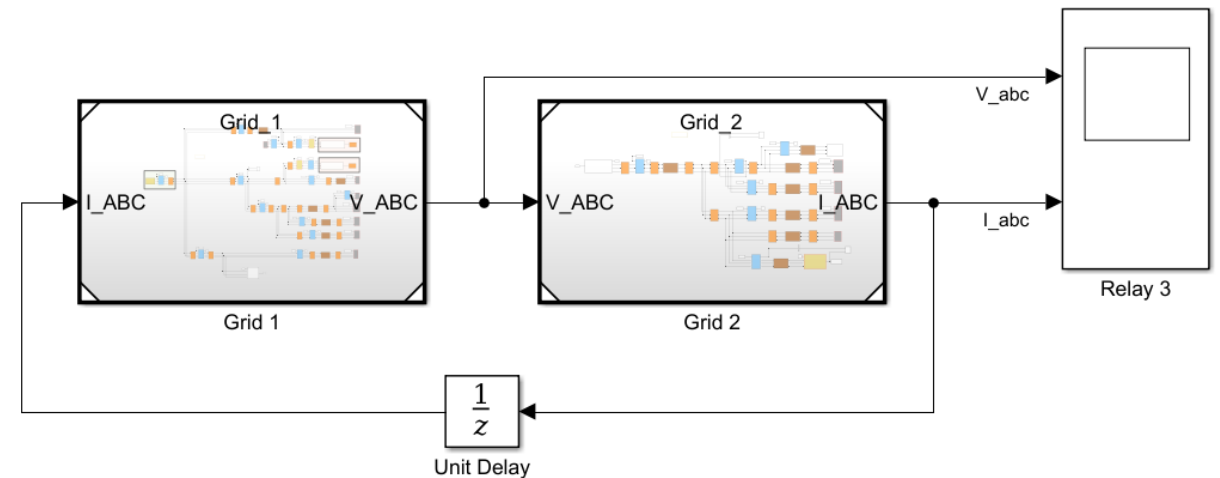
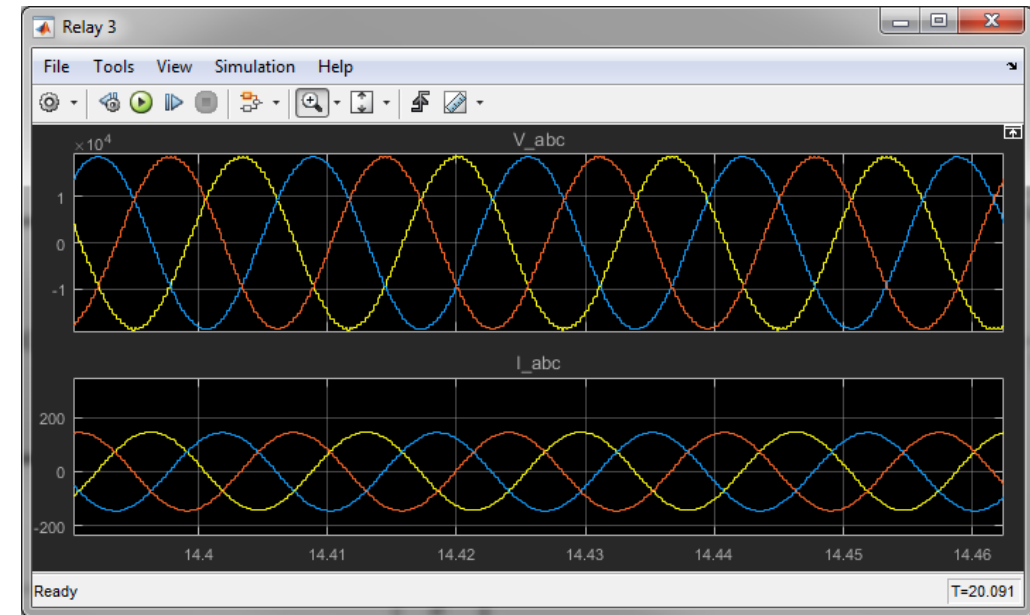
- Engine Delay in GOVERNOR block changed from **Transport Delay** to **Discrete Delay** to avoid continuous states.
- Generator blocks -> Discrete solver model was set to **Forward Euler**. This method can be unstable at larger time steps. Switched to **Trapezoidal non iterative**
- Replaced **Memory** blocks (more for Continuous time applications) with a **First-order Discrete Transfer function** for filtering/breaking algebraic loops. This prevents taking “Fixed-in-minor” time steps associated with continuous states.
- Replaced **Fourier** block in Load blocks with the latest version (has no continuous states and can be purely discrete).
- Delay length in RELAY block was changed from “ $\text{lower}((3/60)/T_s)$ ” to “ $\text{floor}((3/60)/T_s)$ ”.

Desktop Simulation with Split Network

V, I at Split

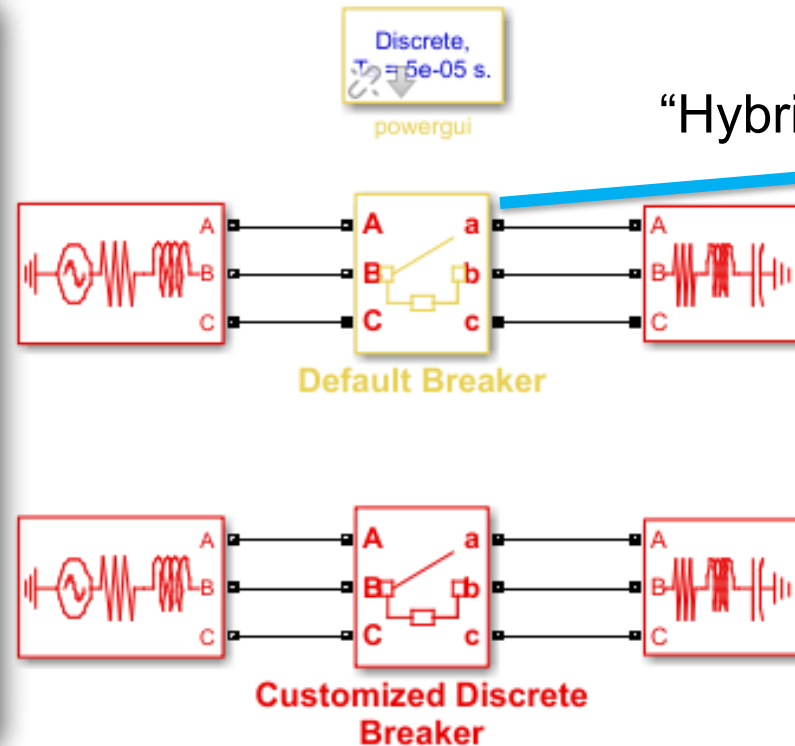
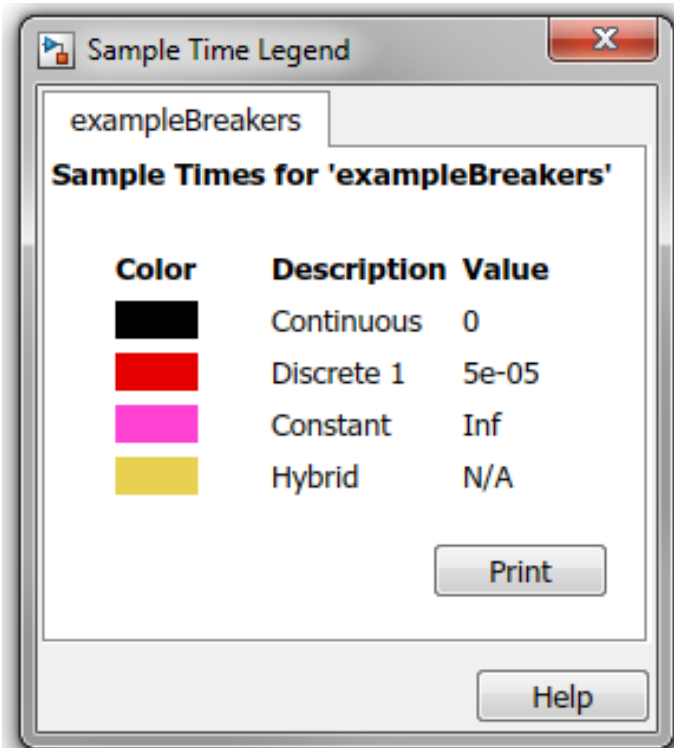


Same split as original model

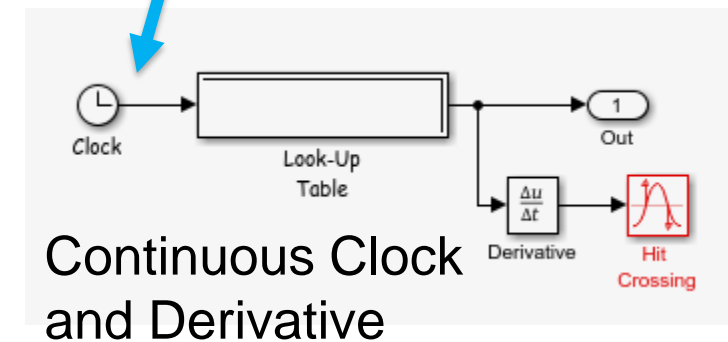
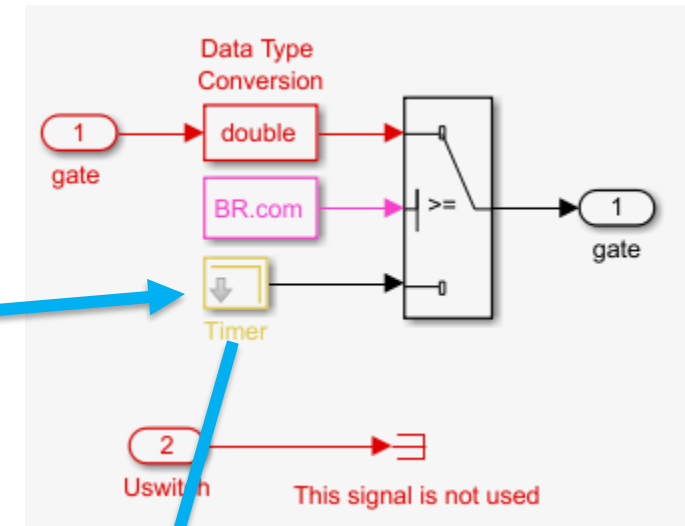


Pure Discrete Breaker Customization

Existing SPS Breaker has Continuous States for Clock



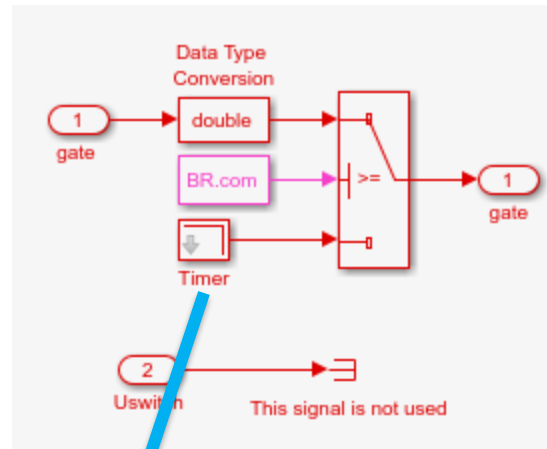
“Hybrid” Timer



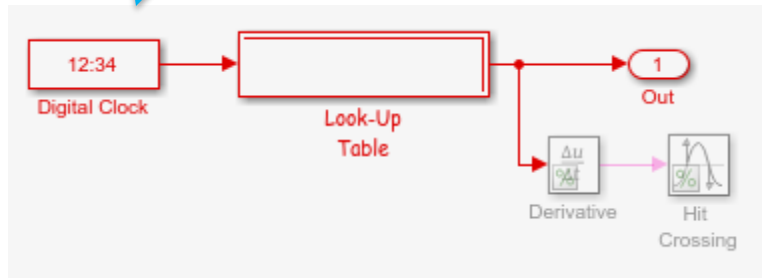
Continuous Clock and Derivative

Pure Discrete Breaker Customization

Existing SPS Breaker has Continuous States for Clock

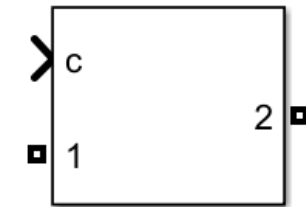


Discrete Clock

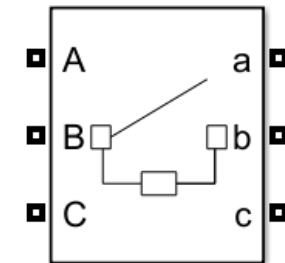


No Hit Crossing needed for minor solver steps

Replaced all Breakers with Discrete Breaker



Breaker (custom)



Three-Phase Breaker (custom)