National Institute of Technology, Tiruchirappalli

Department of Computer Science and Engineering

CYCLE TEST - 2

Digital System Design

Course/ Branch	: B.Tech/ CSE	Course Code : CSPC33	
Duration	: 1 Hour	Max Marks : 20	10/12/002

Answer All Questions

1. Convert JK flipflop to T flipflop. Draw necessary truth tables excitation tables and diagrams. (3)
2. With diagrams and truth tables, explain NOR latch in detail. (3)
3. Differentiate latch and flip-flop. (2)
4. Design a counter using JK-flipflop which counts the following sequence.
   0, 7, 6, 2, 3, 4, 1,5, 0, 7, … (5)
5. Design a 4-bit bi-directional shift register with direction control (C) bit. (Hint: If C=0, do left shift, else right shift) (5)
6. Differentiate Synchronous and asynchronous counters. (2)

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