

National Institute of Technology, Tiruchirappalli

Department of Computer Science and Engineering

CSPC33 Digital System Design /Cycle Test 1

Course/ Branch/Sem

: B.Tech/ CSE/III

Date: 20/09/2022

Duration

: I Hour

Max Marks: 20

B - Section

106121002

Answer All Questions

- Write down the boolean expression of a 4-to-1 multiplexer and design only using the NAND gates.
- 2. Minimize the expression $AB + A\overline{C} + BC AB + A\overline{C}$. Use Boolean rules. (3)
- 3. Implement $F(A, B, C, D) = \sum m(0, 1, 5, 6, 8, 10, 12, 15)$ using 8:1 multiplexer. (2)
- Design a combinational circuit whose input is a four-bit number and whose output is the 2's
 complement of the input number. Write down the truth table, simplify the boolean expression
 and draw the circuit diagram.
- 5. Minimize the boolean function using K-map

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$$
 (3)

6. Design a 4-to-16 decoder, using 2 to 4 decoders.

(3)

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