

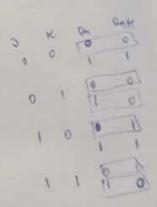
National Institute of Technology, Tiruchirappalli Department of Computer Science and Engineering

CYCLE TEST - 2

Digital System Design

Course/ Branch	: B.Tech/ CSE	Course Code: CSPC33	106121002
Duration	: 1 Hour	Max Marks : 20	100 12007
	Answer All Qu	estions	
1. Convert JK fl	ipflop to T flipflop. Draw ne	cessary truth tables excitation table	es and
diagrams.			(3)
2. With diagrams and truth tables, explain NOR latch in detail.			(3)
Differentiate latch and flip-flop.			(2)
 Design a cour 	nter using JK-flipflop which	counts the following sequence.	
0, 7, 6	5, 2, 3, 4, 1, 5, 0, 7,		(5)
5. Design a 4-bi	it bi-directional shift register	with direction control (C) bit. (Hin	t: If C=0,
do left shift,	else right shift)		(5)

6. Differentiate Synchronous and asynchronous counters.



(2)