Chapter 1

1.5

a.

performance of P1 (instructions/sec) = 2×10^9

performance of P2 (instructions/sec) = 2.5×10^9

performance of P3 (instructions/sec) = 1.8×10^9

b.

cycles(P1) =30×10^9 s

cycles(P2) =25×10^9 s

cycles(P3) =40×10^9 s

No. instructions(P1) = 20×10^9

No. instructions(P2) = 25×10^9

No. instructions(P3) = 18.18×10^9

c.

f(P1) = 5.14 GHz

f(P2) = 4.28 GHz

f(P3) = 6.75 GHz

1.7

a.

CPI(P1)=2.6

CPI(P2)=2.0

b.

clock cycles(P1)=26×10^5

clock cycles(P2)=20×10^5

1.8

a.

Compiler A CPI = 1.1

Compiler B CPI = 1.25

b.

f_B/f_A=1.37

c.

T_A/T_{new} = 1.67

T_B/T_{new} = 2.27

1.11

1.11.1

Yield(15cm)= 0.9593

Yield(20cm)= 0.9093

1.11.2

cost/die(15cm)= 0.1489

cost/die(20cm)= 0.1650

1.11.3

die area(15cm)= 1.91 cm^2

Yield(15cm)= 0.9575

die area(20cm)= 2.86 cm^2

Yield(20cm)= 0.9082

1.11.4

defects per $area_{0.92}$= 0.043 defects/cm^2

defects per $area_{0.95}$= 0.026 defects/cm^2

1.13

1.13.1

T(P1) = 1.125 s

T(P2) = 0.25 s

clock rate (P1) > clock rate(P2), performance(P1) < performance(P2)

1.13.2

9×10^8

1.13.3

MIPS(P1)=4.44×10^3

MIPS(P2)=4.0×10^3

MIPS(P1) > MIPS(P2), performance(P1) < performance(P2)

1.13.4

MFLOPS(P1)= 1.78E3

MFLOPS(P2)= 1.60E3

1.14

1.14.1

Reduction: 5.6%

1.14.2

Reduction time INT: 91%

1.14.3

NO