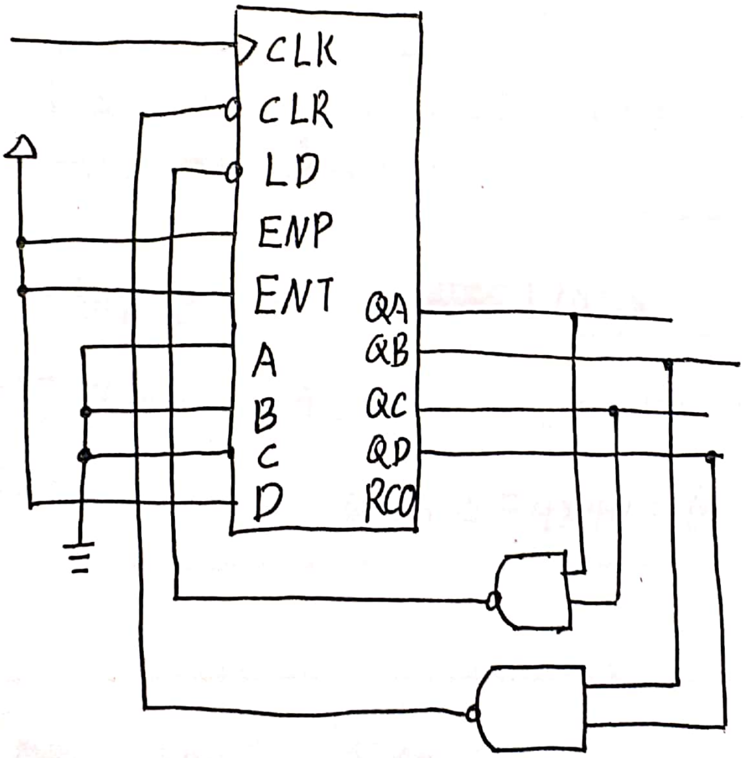
8.13

15 1111 → 7 0111 → 6 0110 → 5 0101 → 4 0100 → 3 0011 → 2 0010 → 1 0001 → 0 0000 → 8 1000 → 9 1001 → 10 1010 → 11 1011 → 12 1100 → 13 1101 → 14 1110 → 15 1111

8.14

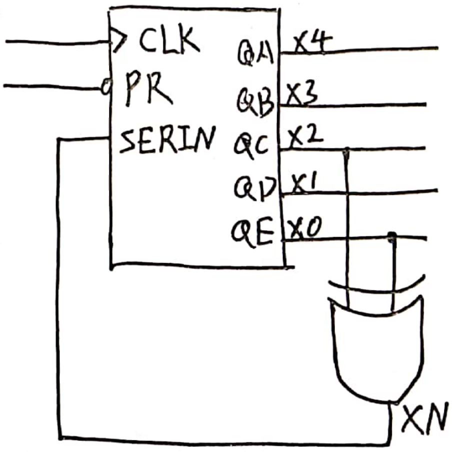


0000 → 0001 → 0010 → 0011 → 0100 → 0101

→ 1000 → 1001 → 1010 → 0000 → 0001

→ 0010 → 0011 → 0100 → 0101 → 1000

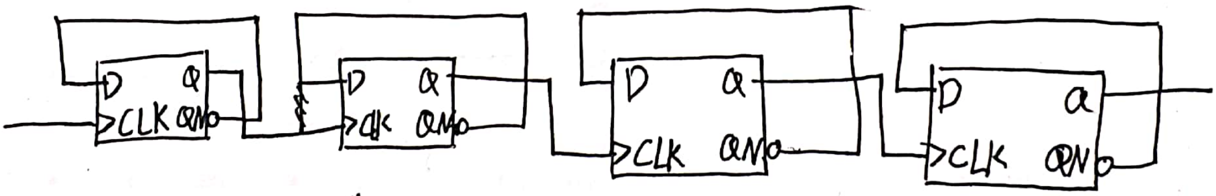
8.16



00001 → 00010 → 00100 → 01001 → 10010

→ 00101 → 01011 → 10110 → 01100 → 11001

8.28



$t_{最大延迟} = 4 \times \cancel{55}\,44 = \cancel{220ns}\ 176ns$

对于 74AHCT74，$t_{最大延迟} = 4 \times 10 = 40ns$

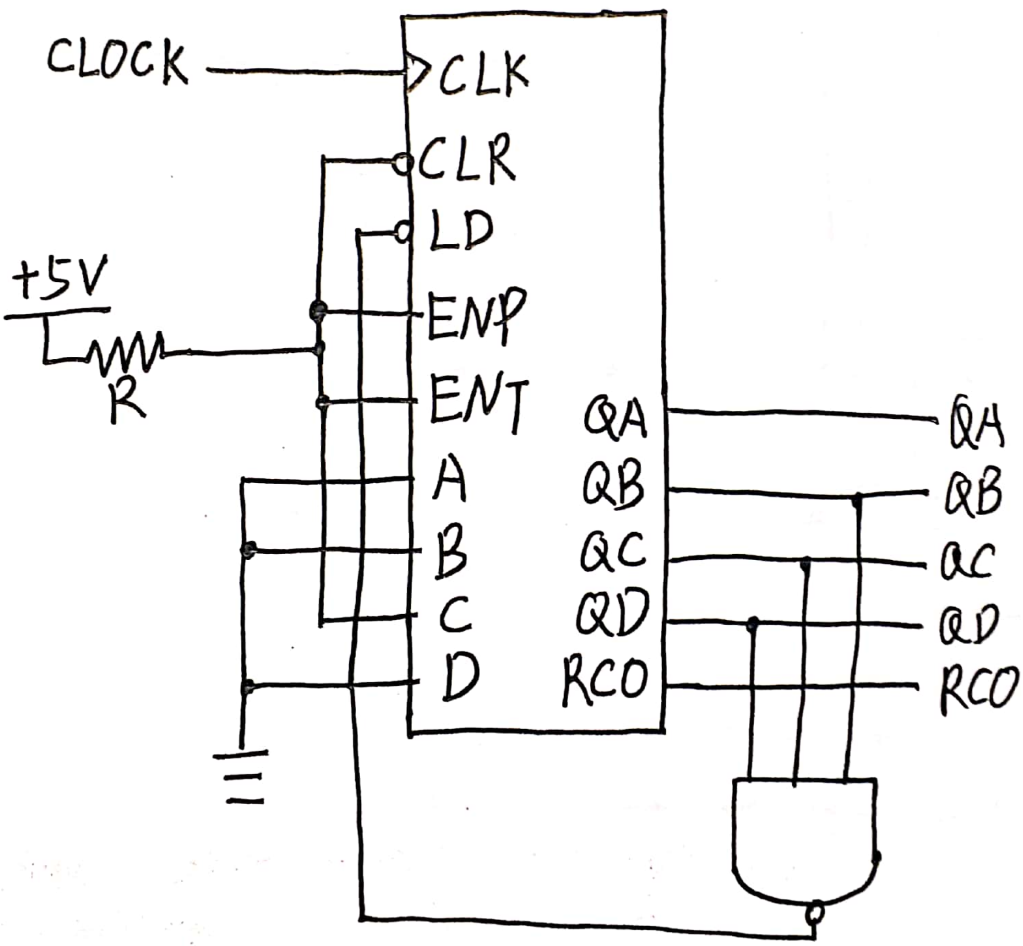
对于 74LS74，$t_{最大延迟} = 4 \times 40 = 160ns$

电路图均如上所示

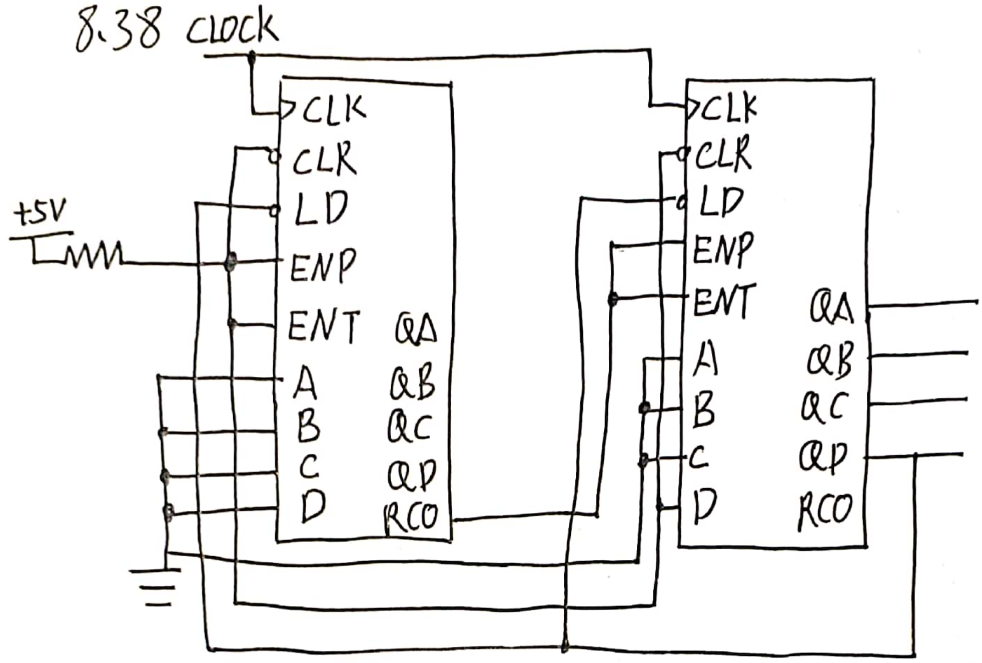
8.31. $f_{max} = \frac{1}{T_{min}} = \frac{1}{3t_{AND} + 4(t_{setup} + t_{TQ})}$

8.35 $14 = \cancel{1100_2}\ 1110_2$

$LD\_L = \overline{Q_D \cdot Q_C \cdot Q_B}$

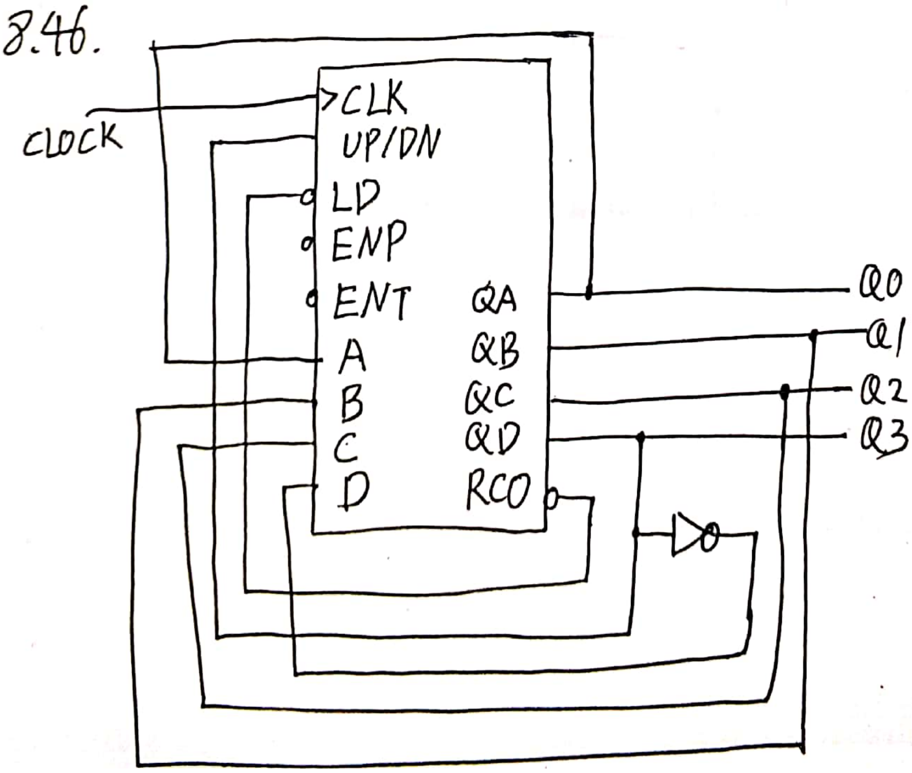


8.38

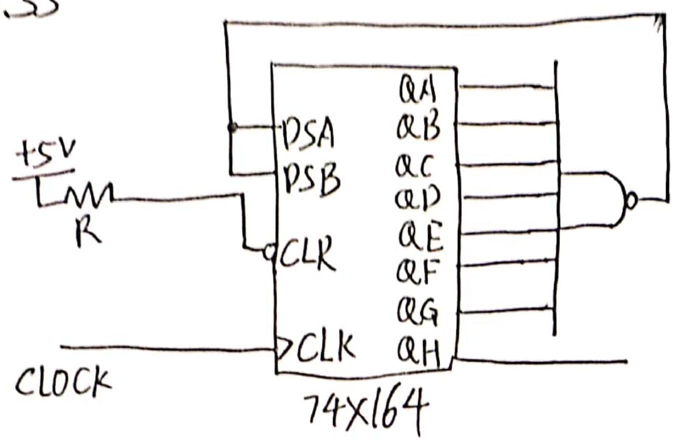


状态从 1000 0000 递增至 1111 1111，接下来是 0000 0000.
此时 LD 信号有效，下一状态为 1000 0000.

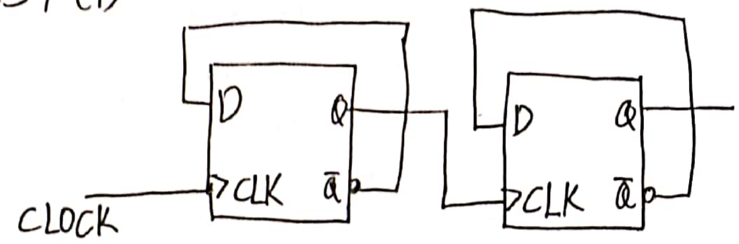
8.46.



8.55



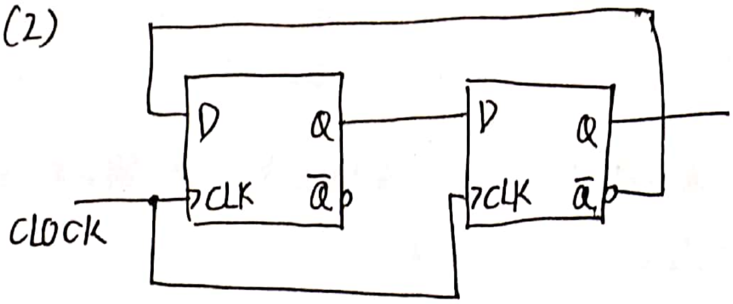
8.57 (1)



状态:

00→11→10→01

(2)



状态:

00→01→11→10

8.63 $X4 = X3 \oplus X0$

	X0	X1	X2	X3	X4
S1	1	1	1	1	0
S2	1	1	1	0	1
S3	1	1	0	1	0
S4	1	0	1	0	1
S5	0	1	0	1	1
S6	1	0	1	1	0
S7	0	1	1	0	0
S8	1	1	0	0	1
S9	1	0	0	1	0
S10	0	0	1	0	0
S11	0	1	0	0	0
S12	1	0	0	0	1
S13	0	0	0	1	1
S14	0	0	1	1	1
S15	0	1	1	1	1

8.64 如图 8.52 的 n位 LFSR计数器，反馈方程为 $Xn = X0 \oplus X1$

当 $X0X1 \cdots Xn\text{-}1$ 为 $1000\cdots0$ 时，下一状态为 $X0X1\cdots Xn\text{-}1 = 000\cdots001$

加入 n-1输入或非门与一个异或门后：

当 $X0X1 \cdots Xn\text{-}1 = 1000\cdots0$ 时，

下一状态为 $X0X1\cdots Xn\text{-}1 = 00\cdots0$

下一状态为 $X0X1\cdots Xn\text{-}1 = 00\cdots01$

对于其他状态，$X1\cdots Xn\text{-}1$ 中必存在1

此时有 $X0\oplus X1 = (X0\oplus X1)\oplus 0 = (X0\oplus X1)\oplus \overline{(X1+X2+\cdots+Xn\text{-}1)}$

不影响状态转变

所以只加入了一种状态（全零），共 2^n 种状态