3.7 4个，2个N沟道MOS晶体管，2个P沟道MOS晶体管

3.10 扇入：在特定逻辑条列中，门电路所具有的输入端的数目

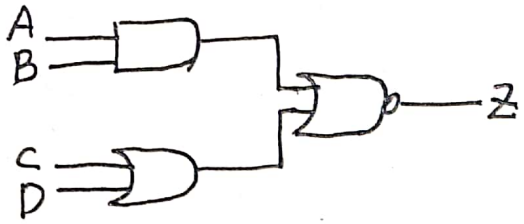
扇出：逻辑门电路在不超出其最坏情况负载规格的条件下，能够驱动的输入端个数

扇出是必须计算的，因为扇出要保证不超出最坏情况负载规格

3.11

A	B	C	D	Q_1	Q_2	Q_3	Q_4	Q_7	Q_6	Q_5	Q_8	Z
L	L	L	L	off	on	off	on	off	on	off	on	H
L	L	L	H	off	on	off	on	off	on	on	off	L
L	L	H	L	off	on	off	on	on	off	off	on	L
L	L	H	H	off	on	off	on	on	off	on	off	L
L	H	L	L	off	on	on	off	off	on	off	on	H
L	H	L	H	off	on	on	off	off	on	on	off	L
L	H	H	L	off	on	on	off	on	off	off	on	L
L	H	H	H	off	on	on	off	on	off	on	off	L
H	L	L	L	on	off	off	on	off	on	off	on	H
H	L	L	H	on	off	off	on	off	on	on	off	L
H	L	H	L	on	off	off	on	on	off	off	on	L
H	L	H	H	on	off	off	on	on	off	on	off	L
H	H	L	L	on	off	on	off	off	on	off	on	L
H	H	L	H	on	off	on	off	off	on	on	off	L
H	H	H	L	on	off	on	off	on	off	of	on	L
H	H	H	H	on	off	on	off	on	off	on	off	L

$Z = \overline{(A \wedge B) \vee (C \vee D)}$



3.20 $V_{IH\,min} = 3.15V$ $V_{IL\,max} = 1.35V$, $Min = 4.5V$, 假设输出与电阻性负载相连

当 $V_{CC} = Min$, $V_{IN} = V_{IH}$, $I_{OL} = 4mA$ 时, $V_{OL\,max} = 0.33V$

当 $V_{CC} = Min$, $V_{IN} = V_{IL}$, $I_{OH} = -4mA$ 时, $V_{OH\,min} = 3.84V$

∴低态直流噪声容限为 $1.35 - 0.33 = 1.02V$

高态直流噪声容限为 $3.84 - 3.15 = 0.69V$

3.22 $V_{IH\,min} = 3.15V$

$V_{IL\,max} = 1.35V$

$I_{IH\,max} = 1\mu A$, 所需假设: $V_{CC} = 5.5V$, $V_I = 5.5V$

$I_{IL\,max} = -1\mu A$, 所需假设: $V_{CC} = 5.5V$, $V_I = 0V$

$V_{OH\,min} = 3.84V$ 所需假设: $V_{CC} = 4.5V$, $V_{IN} = V_{IL}$, $I_{OH} = -4mA$

$V_{OL\,max} = 0.33V$ 所需假设: $V_{CC} = 4.5V$, $V_{IN} = V_{IH}$, $I_{OH} = 4mA$

$I_{OH\,max} = -4mA$ 所需假设: $V_{CC} = 4.5V$, $V_{IN} = V_{IL}$, TTL负载

$I_{OL\,max} = 4mA$ 所需假设: $V_{CC} = 4.5V$, $V_{IN} = V_{IH}$, TTL负载

3.31 不能在接触CMOS器件前与朋友握手

握手可能产生静电，之后触摸CMOS器件，静电会击穿和损坏MOS晶体管

3.32 转换时间受负载电容影响更大

3.36 $\Delta P_D = (C_{PD} + C_L) \cdot (5^2 - 2.5^2) \cdot f$

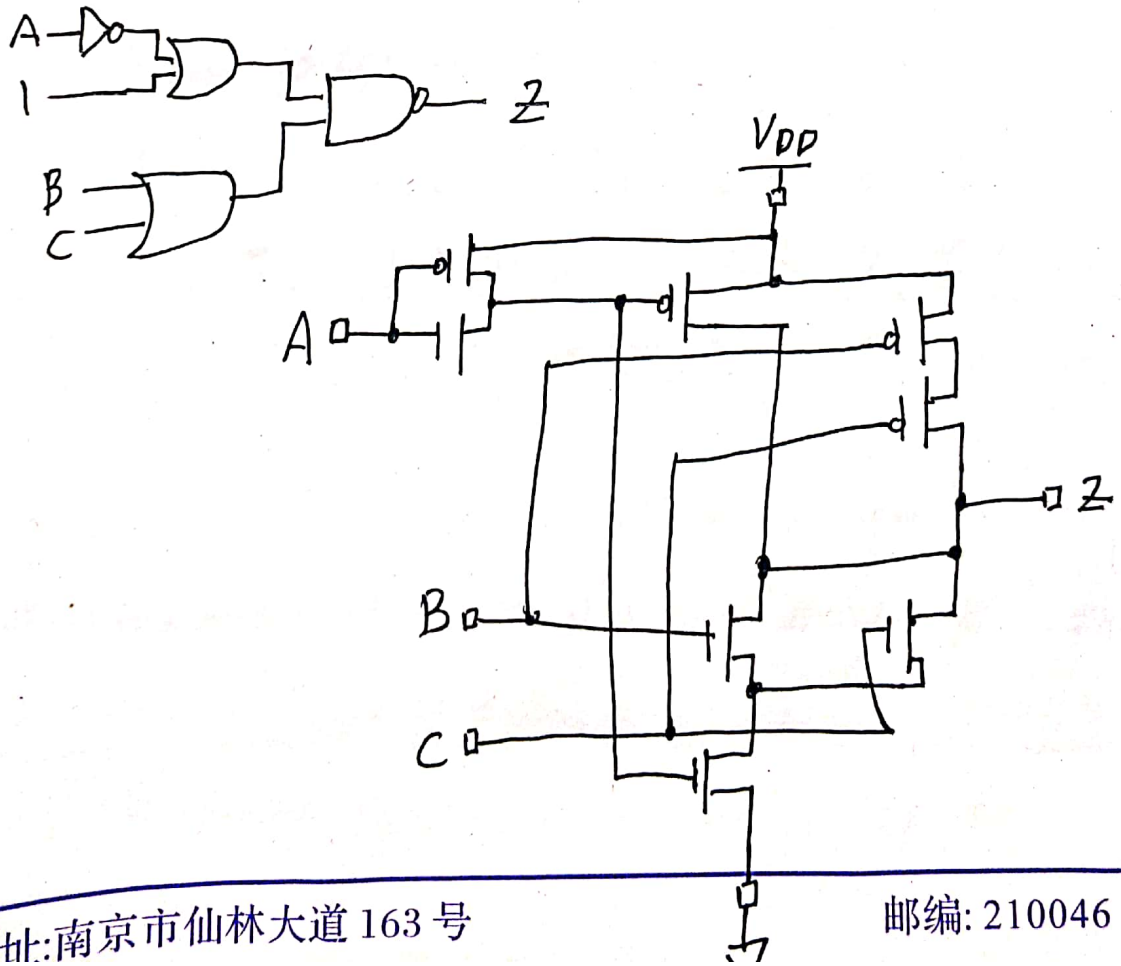
$= 18.75 (C_{PD} + C_L) \cdot f$

3.37. 滞后约为 $1.7 - 1.2 = 0.5V$

3.60 ~~$Z = \overline{\overline{A} \vee (B \wedge C)} = A \wedge (\overline{B} \vee \overline{C})$~~

$Z = \overline{\overline{A} \wedge (B \vee C)} = A \vee (\overline{B \vee C})$

考虑使用或与非门来实现



3.68 CMOS门输出为高电平时：

$$V_{OUT} = 5 - (5-2) \times \frac{200}{100+900} \approx 4.45V$$

CMOS晶体管门输出为低电平时：

$$V_{OUT} = 2 \times \frac{100}{100+900} = 0.2V$$

由高电平到低电平时：

$$V_{OUT} = 4.25 \times e^{-\frac{t}{9\times10^{-9}}} + 0.2 \quad V$$

放电时，R_L与R_n并联，$R = \frac{100\times900}{100+900} = 90\Omega$（所以$R_nC_L$为$9\times10^{-9}$秒）

$$t = -9\times10^{-9} \times \ln\frac{V_{OUT}-0.2}{4.25}$$

$$t_{3.5} = 2.278\,ns$$

$$t_{1.5} = 10.661\,ns$$

$$\Delta t = t_{1.5} - t_{3.5} = 8.383\,ns$$

3.6.1节的结果为8.5ns，二者相差不大

解释：直流负载对转换时间影响不大

3.79 最低有效位转换频率为 16MHz

最高有效位转换频率为 $\frac{16M}{2^7}=\frac{1}{2^3}MHz$

8个输出位的动态功耗，需要考虑每位的转换频率

$$f=(1+\frac{1}{2}+\frac{1}{2^2}+\cdots+\frac{1}{2^7})16MHz$$

$$=\frac{2^7+2^6+\cdots+2^0}{2^7}\cdot 16MHz$$

$$=\frac{2^8-1}{2^7}\cdot 16MHz=\frac{255}{8}MHz$$